Data Sheet | July 1999 | File Number 4321.4

10-Bit, 125/60MSPS, Dual High Speed CMOS D/A Converter

The HI5728 is a 10-bit, dual 125MSPS D/A converter which is implemented in an advanced CMOS process. It is designed for high speed applications where integration, bandwidth and accuracy are essential. Operating from a single +5V or +3V supply, the converter provides 20.48mA of full scale output current and includes an input data register. Low glitch energy and excellent frequency domain performance are achieved using a segmented architecture. A 60MSPS version and an 8-bit (HI5628) version are also available. Comparable single DAC solutions are the HI5760 (10-bit) and the HI5660 (8-bit). This DAC is a member of the CommLink™ family of communication devices.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.	MAX CLOCK SPEED
HI5728IN	-40 to 85	48 Ld LQFP	Q48.7x7A	125MHz
HI5728/6IN	-40 to 85	48 Ld LQFP	Q48.7x7A	60MHz
HI5728EVAL1	25	Evaluation Platform		125MHz

Features

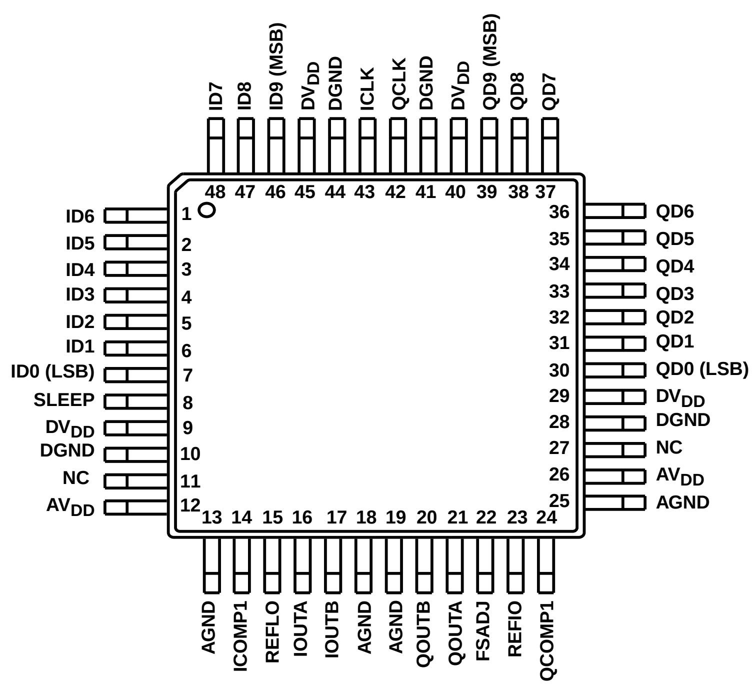
- Throughput Rate 125MSPS
- Low Power . . . . 330mW at 5V, 54mW at 3V
- Integral Linearity Error . . . . ±1 LSB
- Differential Linearity . . . . ±0.5 LSB
- Gain Matching (Typ) 0.5%
- SFDR at 5MHz Output 68dBc
- Single Power Supply from +5V to +3V
- CMOS Compatible Inputs
- Excellent Spurious Free Dynamic Range
- Internal Voltage Reference
- Dual 10-Bit D/A Converters on a Monolithic Chip

Applications

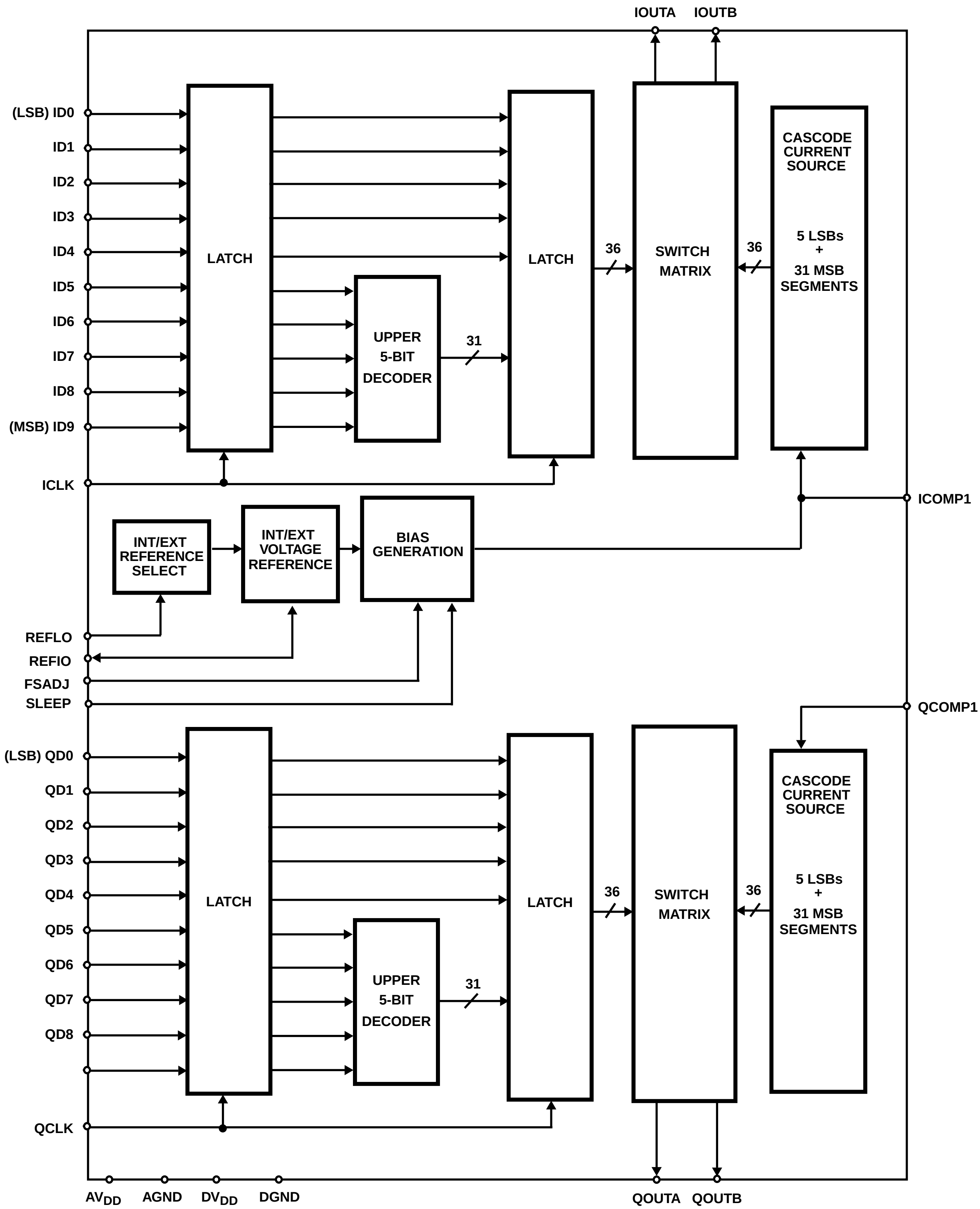
- Wireless Local Loop
- Direct Digital Frequency Synthesis
- Wireless Communications
- Signal Reconstruction
- Arbitrary Waveform Generators
- Test Equipment/Instrumentation
- High Resolution Imaging Systems

Pinout

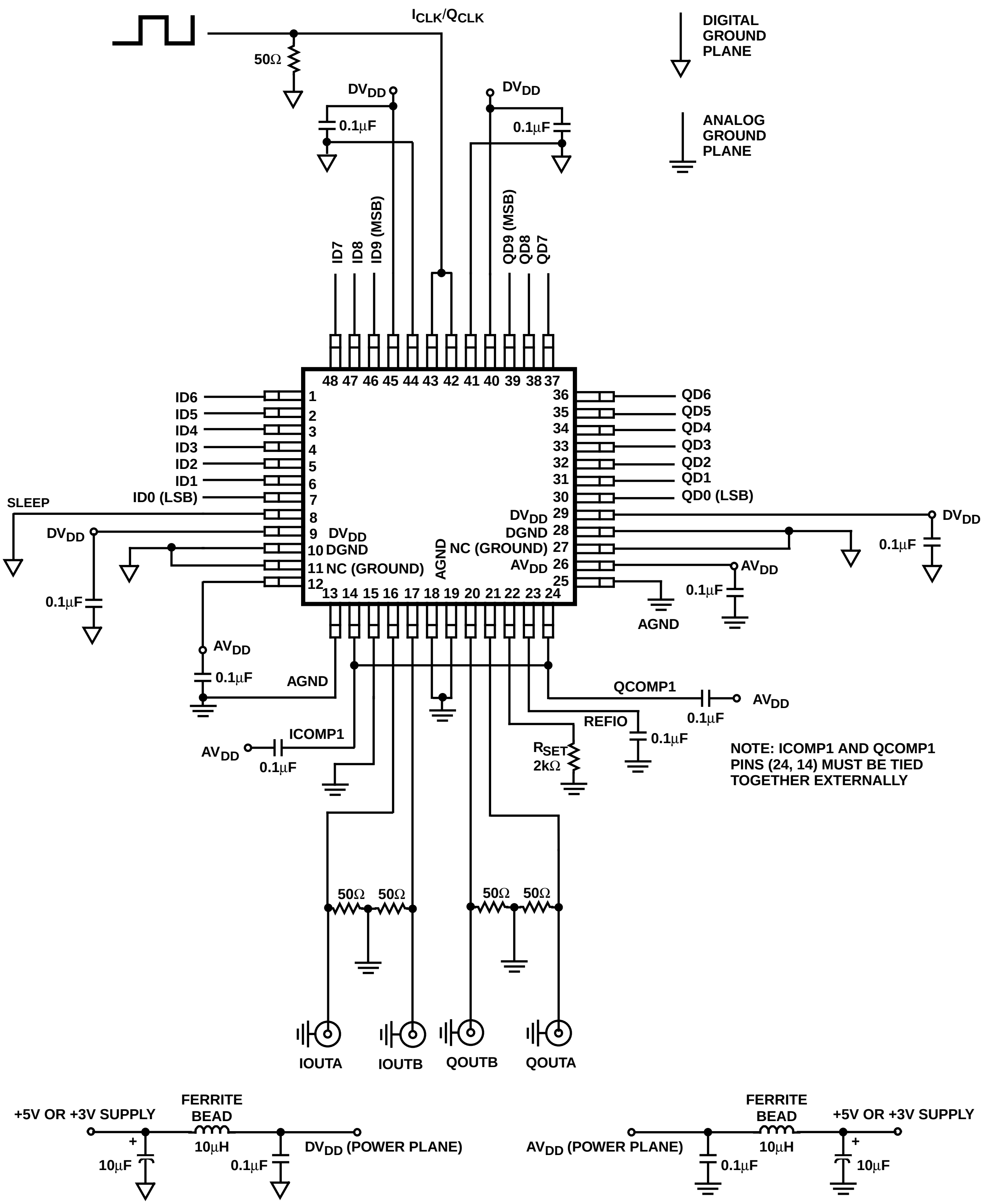
HI5728
(LQFP)
TOP VIEW



Functional Block Diagram



Typical Applications Circuit



Pin Descriptions

PIN NO.	PIN NAME	PIN DESCRIPTION
39-30	QD9 (MSB) Through QD0 (LSB)	Digital Data Bit 9, the Most Significant Bit through Digital Data Bit 0, the Least Significant Bit, of the Q channel.
1-6, 48-46	ID9 (MSB) Through ID0 (LSB)	Digital Data Bit 9, the Most Significant Bit through Digital Data Bit 0, the Least Significant Bit, of the I channel.
8	SLEEP	Control Pin for Power-Down mode. Sleep Mode is active high; Connect to ground for Normal Mode. Sleep pin has internal 20µA active pull-down current.
15	REFLO	Connect to analog ground to enable internal 1.2V reference or connect to AV_{DD} to disable.
23	REFIO	Reference voltage input if internal reference is disabled and reference voltage output if internal reference is enabled. Use 0.1µF cap to ground when internal reference is enabled.
22	FSADJ	Full Scale Current Adjust. Use a resistor to ground to adjust full scale output current. Full Scale Output Current Per Channel = 32 x I_{FSADJ}.
14, 24	ICOMP1, QCOMP1	Reduces noise. Connect each to AV_{DD} with 0.1µF capacitor near each pin. The ICOMP1 and QCOMP1 pins MUST be tied together externally.
13, 18, 19, 25	AGND	Analog Ground Connections.
17	IOUTB	The complimentary current output of the I channel. Bits set to all 0s gives full scale current.
16	IOUTA	Current output of the I channel. Bits set to all 1s gives full scale current.
20	QOUTB	The complimentary current output of the Q channel. Bits set to all 0s gives full scale current.
21	QOUTA	Current output of the Q channel. Bits set to all 1s gives full scale current.
11, 27	NC	No Connect. Recommended: connect to ground.
12, 26	AV_{DD}	Analog Supply (+2.7V to +5.5V).
10, 28, 41, 44	DGND	Digital Ground.
9, 29, 40, 45	DV_{DD}	Supply voltage for digital circuitry (+2.7V to +5.5V).
43	ICLK	Clock input for I channel. Positive edge of clock latches data.
42	QCLK	Clock input for Q channel. Positive edge of clock latches data.

Absolute Maximum Ratings

Digital Supply Voltage DV_{DD} to DCOM . . . . +5.5V
Analog Supply Voltage AV_{DD} to ACOM . . . . +5.5V
Grounds, ACOM TO DCOM . . . . -0.3V to +0.3V
Digital Input Voltages (D9-D0, CLK, SLEEP) . . . . DV_{DD} +0.3V
Internal Reference Output Current . . . . ±50µA
Reference Input Voltage Range . . . . AV_{DD} +0.3V
Analog Output Current (I_{OUT}) 24mA

Operating Conditions

Temperature Range . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
TQFP Package	75

Maximum Power Dissipation
TQFP Package 930mW
Maximum Junction Temperature . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$AV_{DD} = DV_{DD} = +5V$, V_{REF} = Internal 1.2V, IOUTFS = 20mA, $T_A = 25^oC$ for All Typical Values. Data given is per channel except for 'Power Supply Characteristics.'

PARAMETER	TEST CONDITIONS	HI5728IN $T_A = -40^oC$ TO 85^oC MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE (Per Channel)					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	"Best Fit" Straight Line (Note 7)	-1	±0.5	+1	LSB
Differential Linearity Error, DNL	(Note 7)	-0.5	±0.25	+0.5	LSB
Offset Error, I_{OS}	(Note 7)	-0.025		+0.025	% FSR
Offset Drift Coefficient	(Note 7)	-	0.1	-	ppm FSR/°C
Full Scale Gain Error, FSE	With External Reference (Notes 2, 7)	-10	±2	+10	% FSR
	With Internal Reference (Notes 2, 7)	-10	±1	+10	% FSR
Full Scale Gain Drift	With External Reference (Note 7)	-	±50	-	ppm FSR/°C
	With Internal Reference (Note 7)	-	±100	-	ppm FSR/°C
Gain Matching Between Channels		-0.5	0.1	0.5	dB
I/Q Channel Isolation	F_{OUT} = 10MHz	-	80	-	dB
Output Voltage Compliance Range	(Note 3)	-0.3	-	1.25	V
Full Scale Output Current, I_{FS}		2	-	20	mA
DYNAMIC CHARACTERISTICS (Per Channel)					
Maximum Clock Rate, f_{CLK}	(Note 3)	125	-	-	MHz
Output Settling Time, (t_{SETT})	0.1% (±1 LSB, equivalent to 9 Bits) (Note 7)	-	20	-	ns
	0.05% (±1/2 LSB, equivalent to 10 Bits) (Note 7)	-	35	-	ns
Singlet Glitch Area (Peak Glitch)	$R_L = 25\Omega$ (Note 7)	-	35	-	pV•s
Output Rise Time	Full Scale Step	-	1.5	-	ns
Output Fall Time	Full Scale Step	-	1.5	-	ns
Output Capacitance		-	10	-	pF
Output Noise	IOUTFS = 20mA	-	50	-	$pA/\sqrt{Hz}$
	IOUTFS = 2mA	-	30	-	$pA/\sqrt{Hz}$

Electrical Specifications $AV_{DD} = DV_{DD} = +5V$, V_{REF} = Internal 1.2V, IOUTFS = 20mA, $T_A = 25^oC$ for All Typical Values. Data given is per channel except for 'Power Supply Characteristics.' **(Continued)**

PARAMETER	TEST CONDITIONS	HI5728IN $T_A = -40^oC$ TO 85^oC MIN	TYP	MAX	UNITS
AC CHARACTERISTICS (Per Channel) - HI5728IN - 125MHz					
Spurious Free Dynamic Range, SFDR Within a Window	f_{CLK} = 125MSPS, f_{OUT} = 32.9MHz, 10MHz Span (Notes 4, 7)	-	75	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 5.04MHz, 4MHz Span (Notes 4, 7)	-	76	-	dBc
	f_{CLK} = 60MSPS, f_{OUT} = 10.1MHz, 10MHz Span (Notes 4, 7)	-	75	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 5.02MHz, 2MHz Span (Notes 4, 7)	-	76	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 1.00MHz, 2MHz Span (Notes 4, 7)	-	78	-	dBc
Total Harmonic Distortion (THD) to Nyquist	f_{CLK} = 100MSPS, f_{OUT} = 2.00MHz (Notes 4, 7)	-	71	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 2.00MHz (Notes 4, 7)	-	71	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 1.00MHz (Notes 4, 7)	-	76	-	dBc
Spurious Free Dynamic Range, SFDR to Nyquist	f_{CLK} = 125MSPS, f_{OUT} = 32.9MHz, 62.5MHz Span (Notes 4, 7)	-	54	-	dBc
	f_{CLK} = 125MSPS, f_{OUT} = 10.1MHz, 62.5MHz Span (Notes 4, 7)	-	64	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 40.4MHz, 50MHz Span (Notes 4, 7)	-	52	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 20.2MHz, 50MHz Span (Notes 4, 7)	-	60	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 5.04MHz, 50MHz Span (Notes 4, 7)	-	68	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 2.51MHz, 50MHz Span (Notes 4, 7)	-	74	-	dBc
	f_{CLK} = 60MSPS, f_{OUT} = 10.1MHz, 30MHz Span (Notes 4, 7)	-	63	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 20.2MHz, 25MHz Span (Notes 4, 7)	-	55	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 5.02MHz, 25MHz Span (Notes 4, 7)	-	68	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 2.51MHz, 25MHz Span (Notes 4, 7)	-	73	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 1.00MHz, 25MHz Span (Notes 4, 7)	-	73	-	dBc
AC CHARACTERISTICS (Per Channel) - HI5728/6IN - 60MHz					
Spurious Free Dynamic Range, SFDR Within a Window	f_{CLK} = 60MSPS, f_{OUT} = 10.1MHz, 10MHz Span (Notes 4, 7)	-	75	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 5.02MHz, 2MHz Span (Notes 4, 7)	-	76	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 1.00MHz, 2MHz Span (Notes 4, 7)	-	78	-	dBc
Total Harmonic Distortion (THD) to Nyquist	f_{CLK} = 50MSPS, f_{OUT} = 2.00MHz (Notes 4, 7)	-	71	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 1.00MHz (Notes 4, 7)	-	76	-	dBc
Spurious Free Dynamic Range, SFDR to Nyquist	f_{CLK} = 60MSPS, f_{OUT} = 20.2MHz, 30MHz Span (Notes 4, 7)	-	56	-	dBc
	f_{CLK} = 60MSPS, f_{OUT} = 10.1MHz, 30MHz Span (Notes 4, 7)	-	63	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 20.2MHz, 25MHz Span (Notes 4, 7)	-	55	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 5.02MHz, 25MHz Span (Notes 4, 7)	-	68	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 2.51MHz, 25MHz Span (Notes 4, 7)	-	73	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 1.00MHz, 25MHz Span (Notes 4, 7)	-	73	-	dBc
	f_{CLK} = 25MSPS, f_{OUT} = 5.02MHz, 25MHz Span (Notes 4, 7)	-	71	-	dBc
VOLTAGE REFERENCE					
Internal Reference Voltage, V_{FSADJ}	Voltage at Pin 22 with Internal Reference	1.04	1.16	1.28	V
Internal Reference Voltage Drift		-	±60	-	ppm/^oC
Internal Reference Output Current Sink/Source Capability		-	0.1	-	µA
Reference Input Impedance		-	1	-	MΩ
Reference Input Multiplying Bandwidth	(Note 7)	-	1.4	-	MHz
DIGITAL INPUTS D9-D0, CLK (Per Channel)					
Input Logic High Voltage with 5V Supply, V_{IH}	(Note 3)	3.5	5	-	V

Electrical Specifications $AV_{DD} = DV_{DD} = +5V$, V_{REF} = Internal 1.2V, IOUTFS = 20mA, $T_A = 25^oC$ for All Typical Values. Data given is per channel except for 'Power Supply Characteristics.' **(Continued)**

PARAMETER	TEST CONDITIONS	HI5728IN $T_A = -40^oC$ TO 85^oC			UNITS
		MIN	TYP	MAX	
Input Logic High Voltage with 3V Supply, V_{IH}	(Note 3)s	2.1	3	-	V
Input Logic Low Voltage with 5V Supply, V_{IL}	(Note 3)	-	0	1.3	V
Input Logic Low Voltage with 3V Supply, V_{IL}	(Note 3)	-	0	0.9	V
Input Logic Current, I_{IH}		-10	-	+10	µA
Input Logic Current, I_{IL}		-10	-	+10	µA
Digital Input Capacitance, C_{IN}		-	5	-	pF
TIMING CHARACTERISTICS (Per Channel)					
Data Setup Time, t_{SU}	See Figure 41 (Note 3)	3	-	-	ns
Data Hold Time, t_{HLD}	See Figure 41 (Note 3)	3	-	-	ns
Propagation Delay Time, t_{PD}	See Figure 41	-	1	-	ns
CLK Pulse Width, t_{PW1}, t_{PW2}	See Figure 41 (Note 3)	4	-	-	ns
POWER SUPPLY CHARACTERISTICS					
AVDD Power Supply	(Notes 8, 9)	2.7	5.0	5.5	V
DVDD Power Supply	(Notes 8, 9)	2.7	5.0	5.5	V
Analog Supply Current (I_{AVDD})	(5V or 3V, IOUTFS = 20mA)	-	46	60	mA
	(5V or 3V, IOUTFS = 2mA)	-	8	-	mA
Digital Supply Current (I_{DVDD})	(5V, IOUTFS = Don't Care) (Note 5)	-	6	10	mA
	(3V, IOUTFS = Don't Care) (Note 5)	-	3	-	mA
Supply Current (I_{AVDD}) Sleep Mode	(5V or 3V, IOUTFS = Don't Care)	-	3.2	6	mA
Power Dissipation	(5V, IOUTFS = 20mA) (Note 6)	-	330	-	mW
	(5V, IOUTFS = 2mA) (Note 6)	-	140	-	mW
	(3V, IOUTFS = 20mA) (Note 6)	-	170	-	mW
	(3V, IOUTFS = 2mA) (Note 6)	-	54	-	mW
	(5V, IOUTFS = 20mA) (Note 10)	-	300	-	mW
	(3.3V, IOUTFS = 20mA) (Note 10)	-	150	-	mW
	(3V, IOUTFS = 20mA) (Note 10)	-	135	-	mW
Power Supply Rejection	Single Supply (Note 7)	-0.2	-	+0.2	% FSR/V

NOTES:

2. Gain Error measured as the error in the ratio between the full scale output current and the current through R_{SET} (typically 625µA). Ideally the ratio should be 32.
3. Parameter guaranteed by design or characterization and not production tested.
4. Spectral measurements made with differential coupled transformer and 100% amplitude.
5. Measured with the clock at 50MSPS and the output frequency at 1MHz, both channels.
6. Measured with the clock at 100MSPS and the output frequency at 40MHz, both channels.
7. See 'Definition of Specifications'.
8. For operation below 3V, it is recommended that the output current be reduced to 12mA or less to maintain optimum performance. DV_{DD} and AV_{DD} do not have to be equal.
9. For operation above 125MHz, it is recommended that the power supply be 3.3V or greater. The part is functional with the clock above 125MSPS and the power supply below 3.3V, but performance is degraded.
10. Measured with the clock at 60MSPS and the output frequency at 10MHz, both channels.

Typical Performance Curves, 5 Volt Power Supply

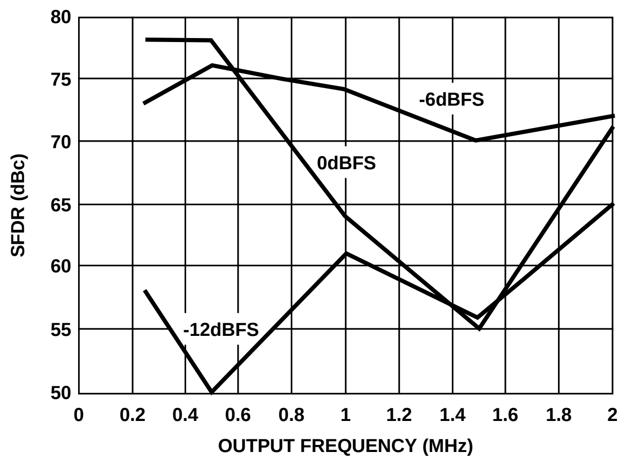


FIGURE 1. SFDR vs f_{OUT}, CLOCK = 5MSPS

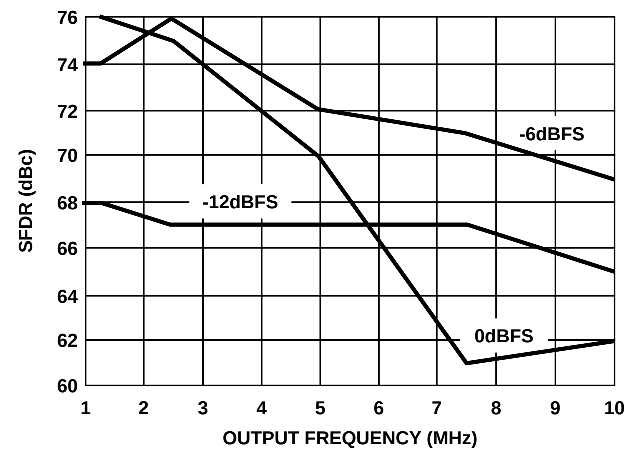


FIGURE 2. SFDR vs f_{OUT}, CLOCK = 25MSPS

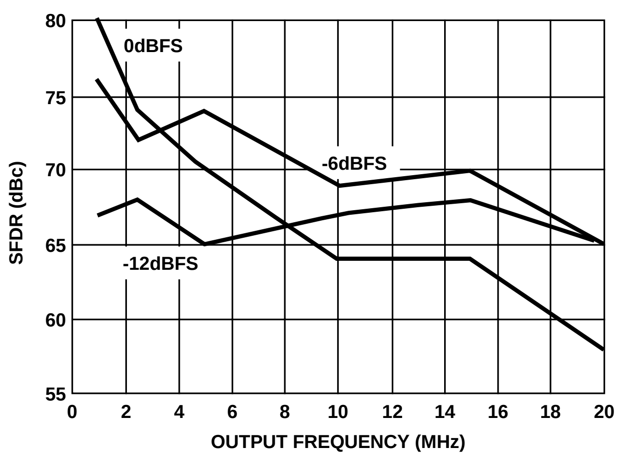


FIGURE 3. SFDR vs f_{OUT}, CLOCK = 50MSPS

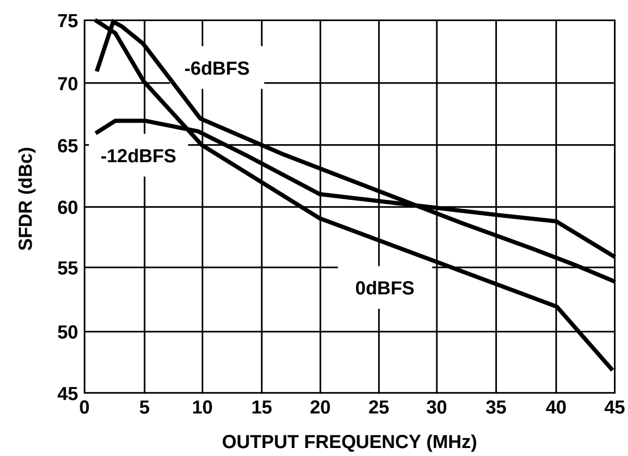


FIGURE 4. SFDR vs f_{OUT}, CLOCK =100MSPS

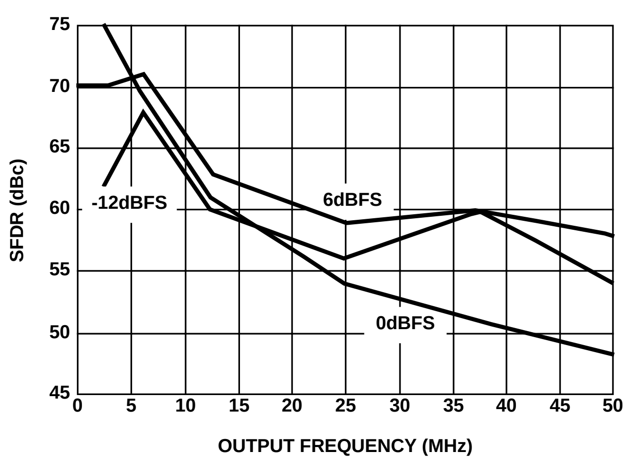


FIGURE 5. SFDR vs f_{OUT}, CLOCK = 125MSPS

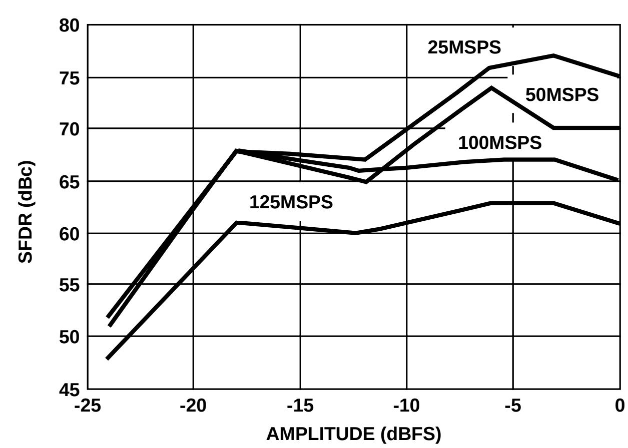


FIGURE 6. SFDR vs AMPLITUDE, f_{CLK}/f_{OUT} = 10

Typical Performance Curves, 5 Volt Power Supply (Continued)

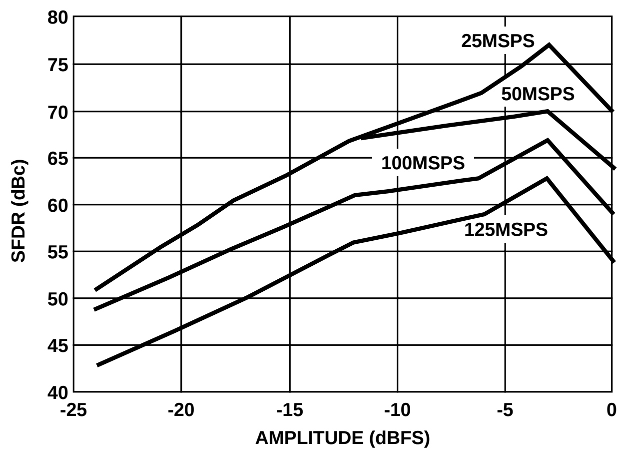


FIGURE 7. SFDR vs AMPLITUDE, $f_{CLK}/f_{OUT} = 5$

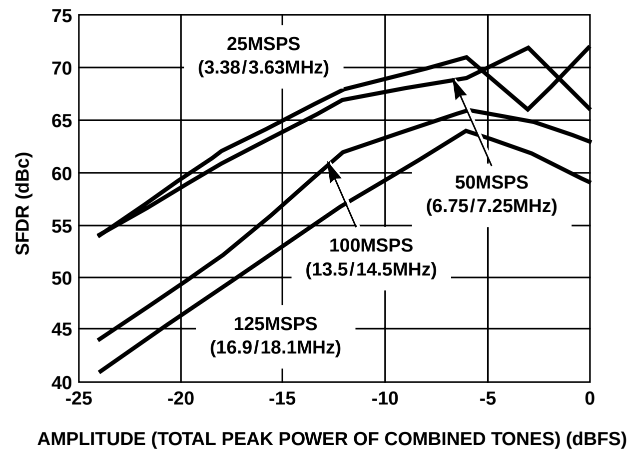


FIGURE 8. SFDR vs AMPLITUDE OF TWO TONES, $f_{CLK}/f_{OUT} = 7$

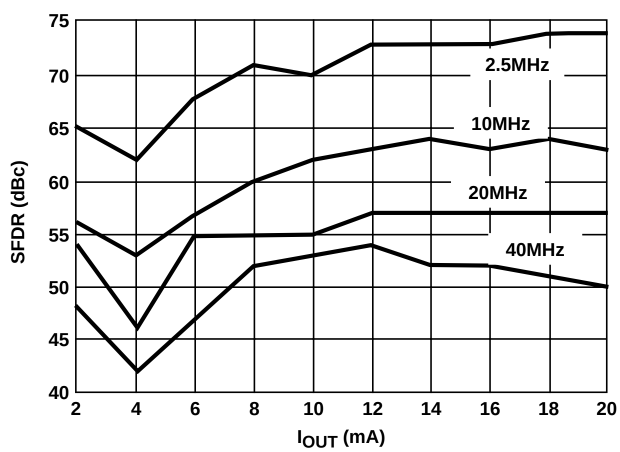


FIGURE 9. SFDR vs I_{OUT}, CLOCK = 100MSPS

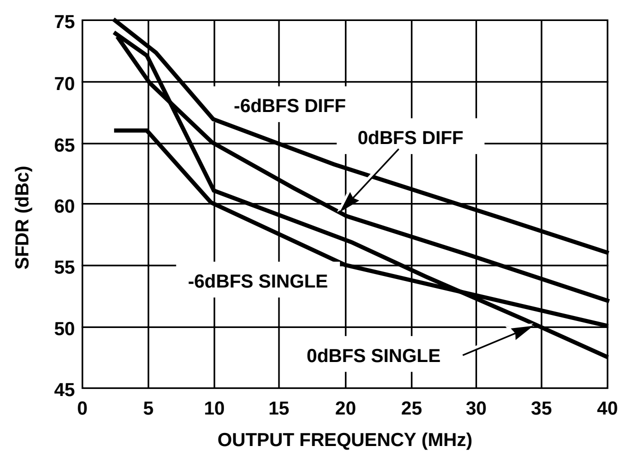


FIGURE 10. DIFFERENTIAL vs SINGLE-ENDED, CLOCK = 100MSPS

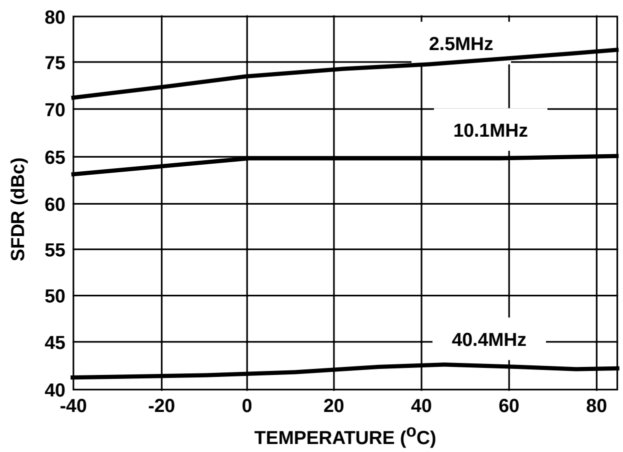


FIGURE 11. SFDR vs TEMPERATURE, CLOCK = 100MSPS

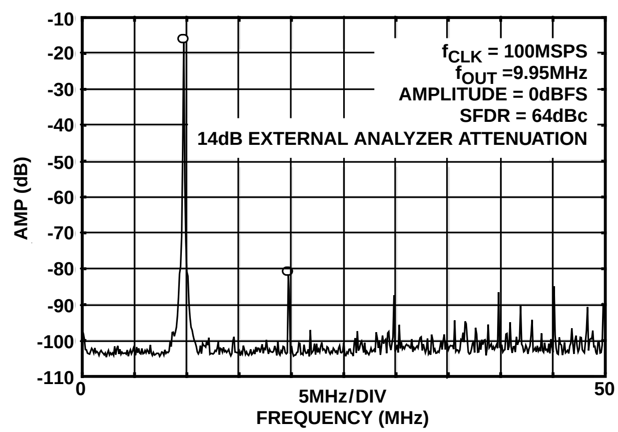


FIGURE 12. SINGLE TONE SFDR

Typical Performance Curves, 5 Volt Power Supply (Continued)

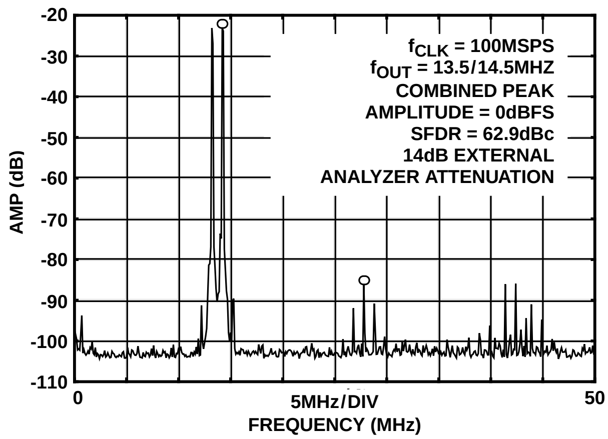


FIGURE 13. TWO TONE, CLOCK = 100MSPS

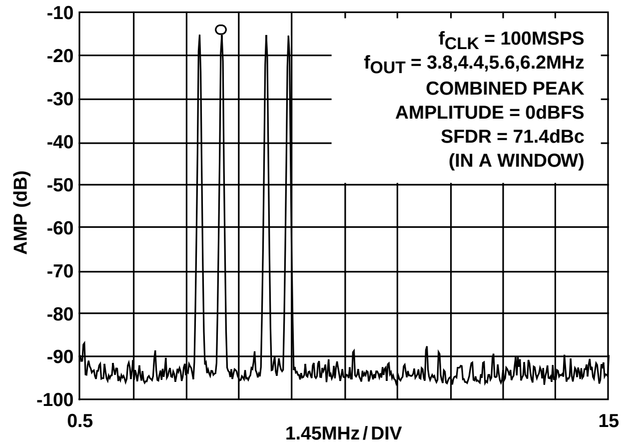


FIGURE 14. FOUR-TONE, CLOCK = 100MSPS

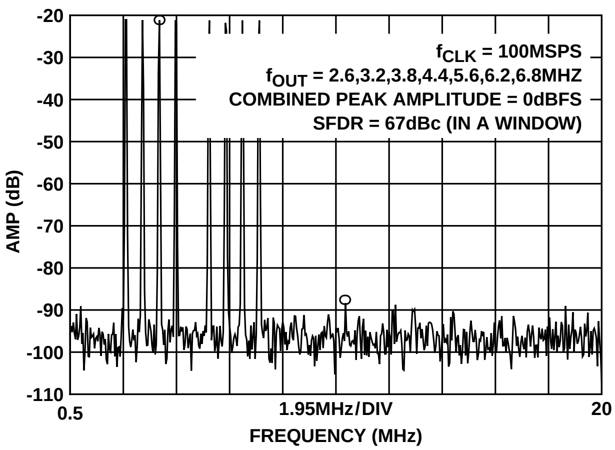


FIGURE 15. EIGHT-TONE, CLOCK = 100MSPS

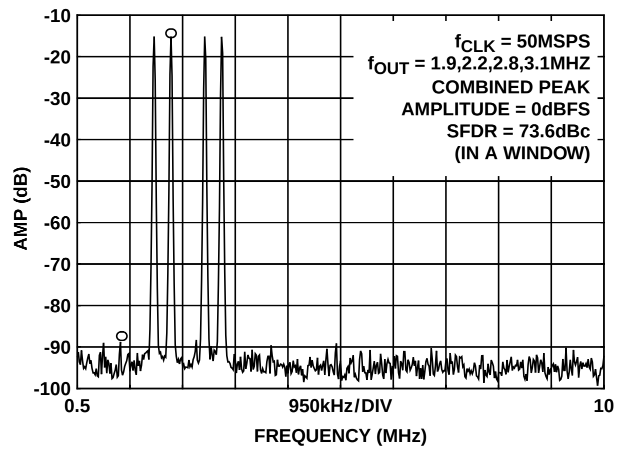


FIGURE 16. FOUR-TONE, CLOCK = 50MSPS

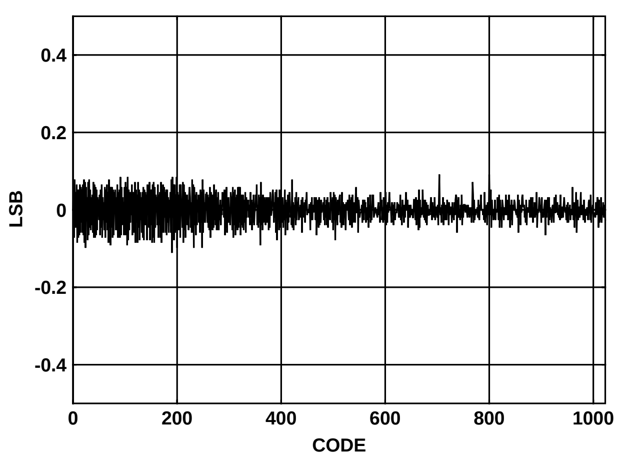


FIGURE 17. DIFFERENTIAL NONLINEARITY

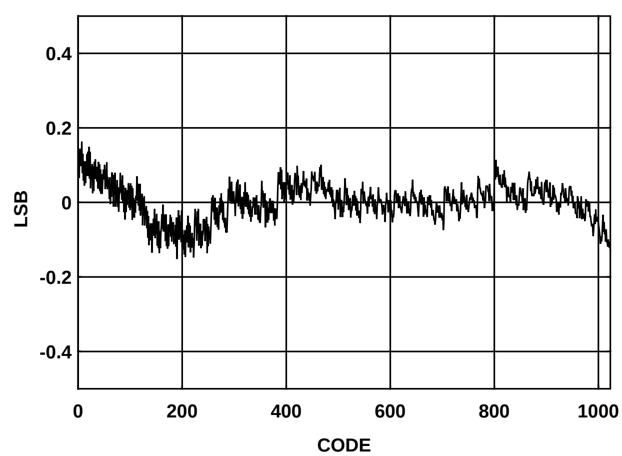


FIGURE 18. INTEGRAL NONLINEARITY

Typical Performance Curves, 5 Volt Power Supply (Continued)

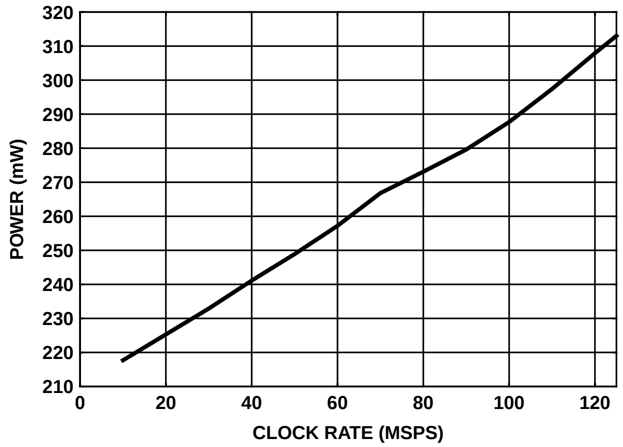


FIGURE 19. POWER vs CLOCK RATE, f_{CLK}/f_{OUT} = 10, I_{OUT} = 20mA

Typical Performance Curves, 3V Power Supply

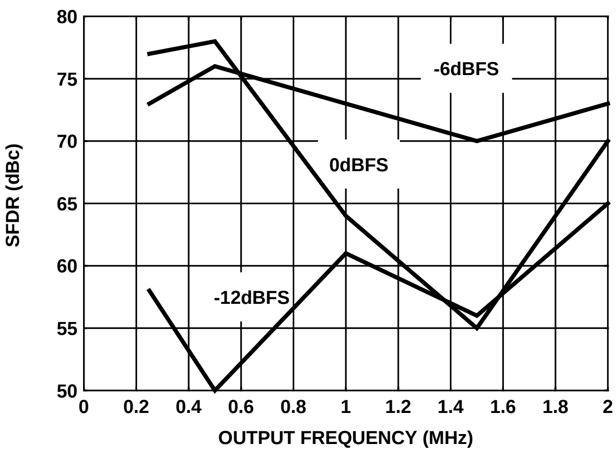


FIGURE 20. SFDR vs f_{OUT}, CLOCK = 5MSPS

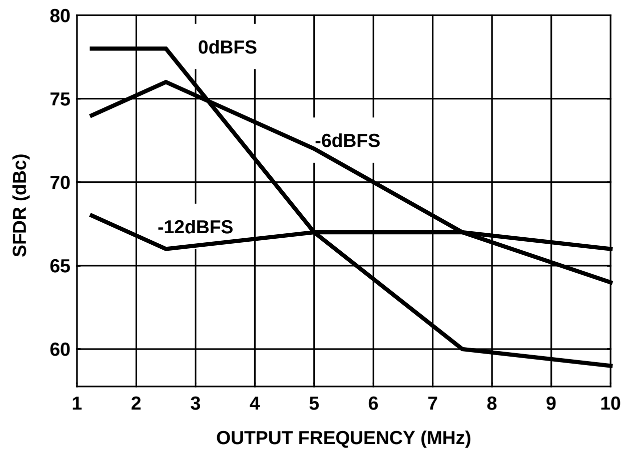


FIGURE 21. SFDR vs f_{OUT}, CLOCK = 25MSPS

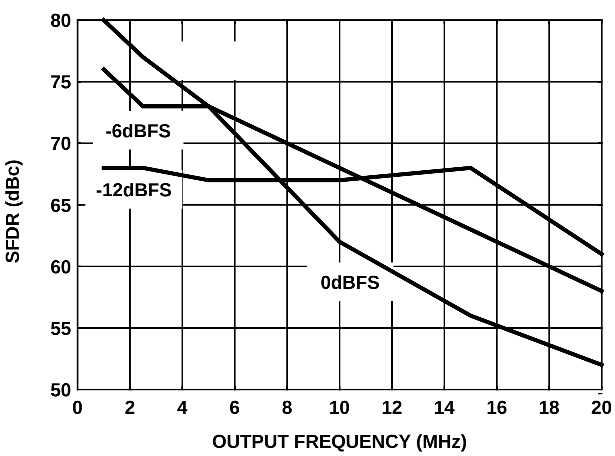


FIGURE 22. SFDR vs f_{OUT}, CLOCK = 50MSPS

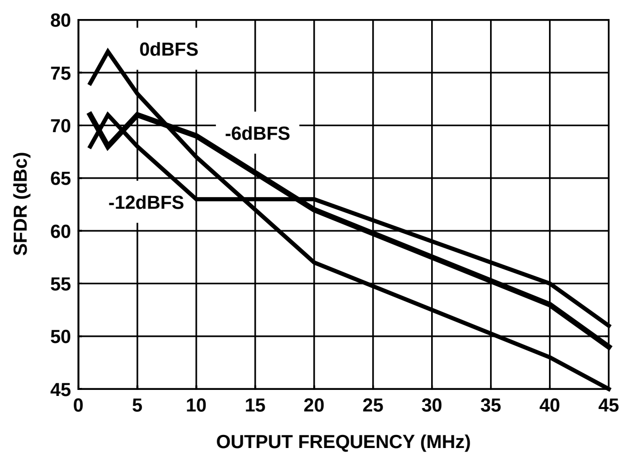


FIGURE 23. SFDR vs f_{OUT}, CLOCK = 100MSPS

Typical Performance Curves, 3V Power Supply (Continued)

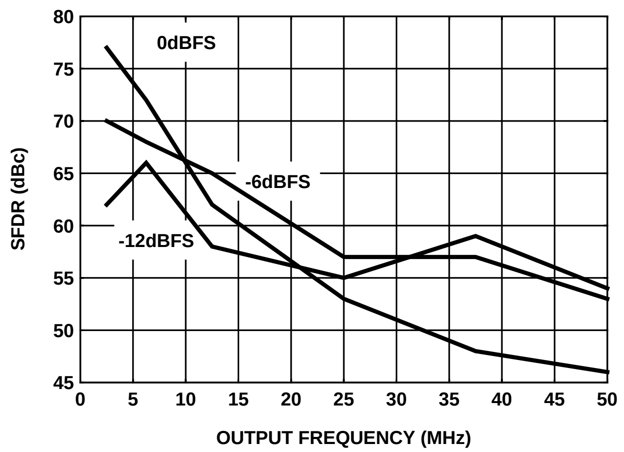


FIGURE 24. SFDR vs f_{OUT}, CLOCK = 125MSPS

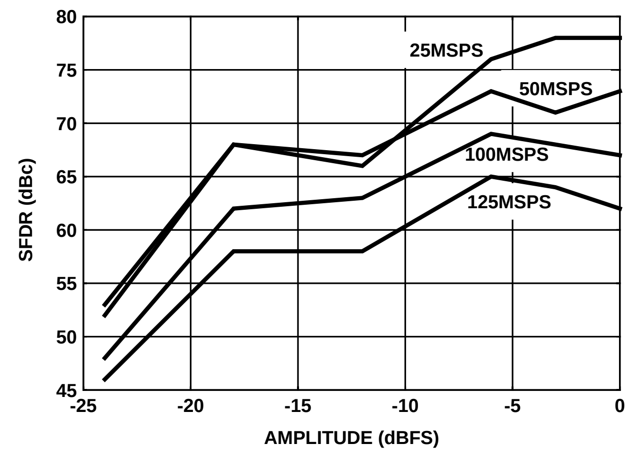


FIGURE 25. SFDR vs AMPLITUDE, f_{CLK}/f_{OUT} = 10

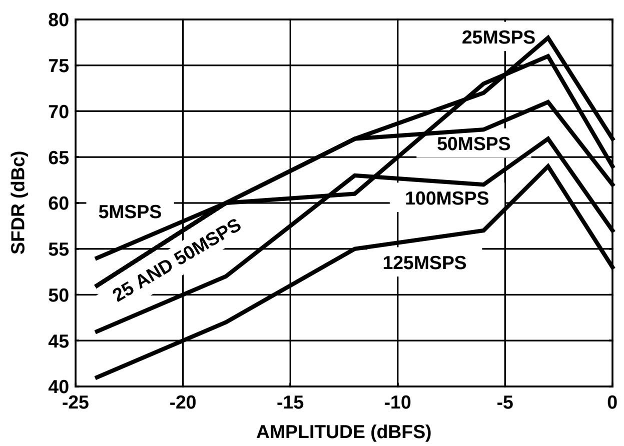


FIGURE 26. SFDR vs AMPLITUDE, f_{CLK}/f_{OUT} = 5

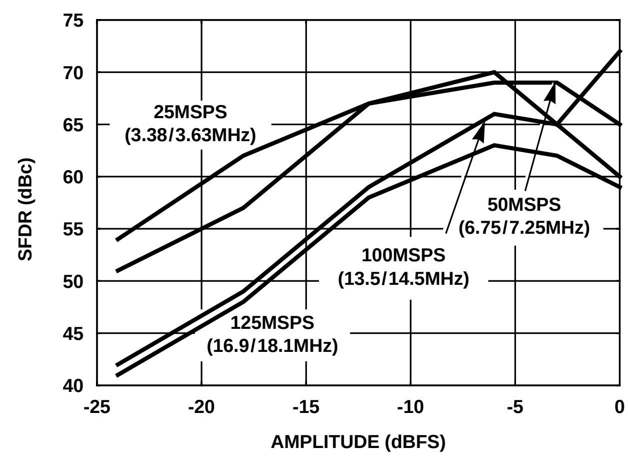


FIGURE 27. SFDR vs AMPLITUDE OF TWO TONES, f_{CLK}/f_{OUT} = 7

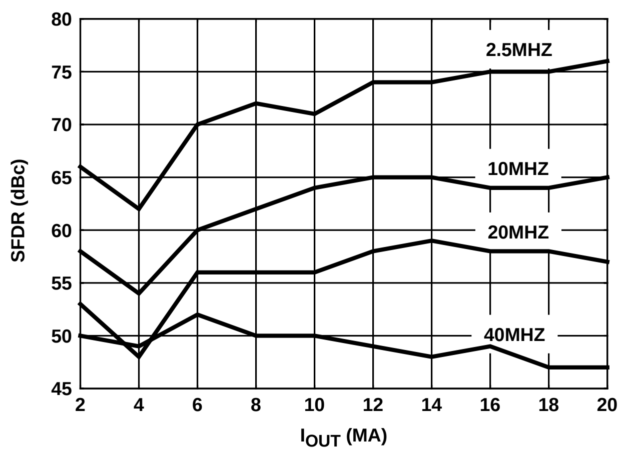


FIGURE 28. SFDR vs I_{OUT}, CLOCK = 100MSPS

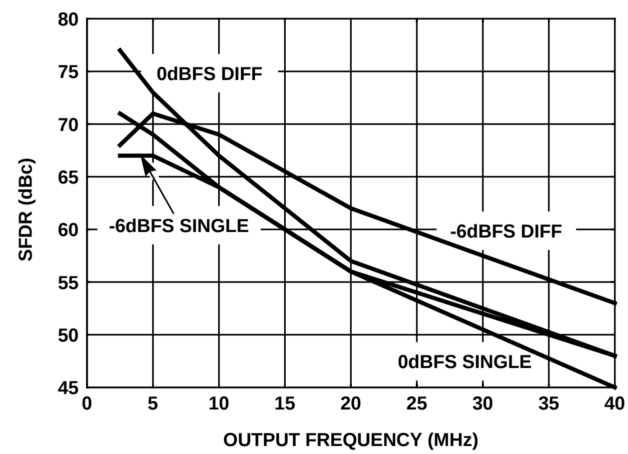


FIGURE 29. DIFFERENTIAL vs SINGLE-ENDED, CLOCK = 100MSPS

Typical Performance Curves, 3V Power Supply (Continued)

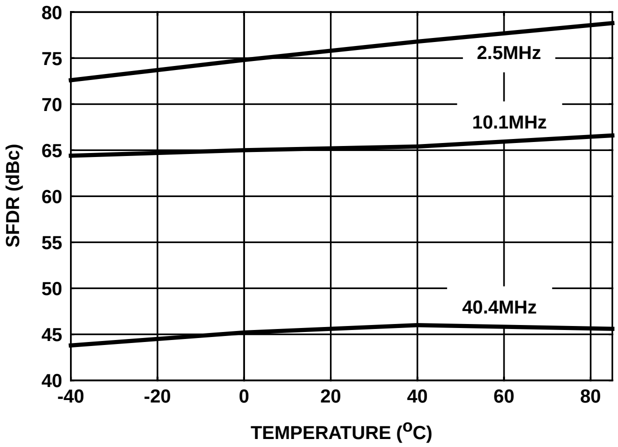


FIGURE 30. SFDR vs TEMPERATURE, CLOCK = 100MSPS

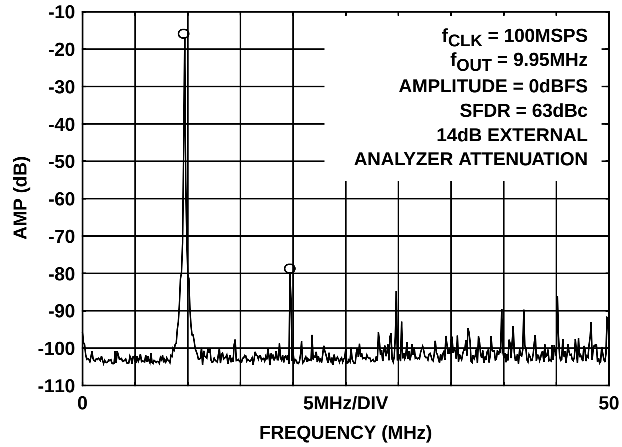


FIGURE 31. SINGLE TONE SFDR

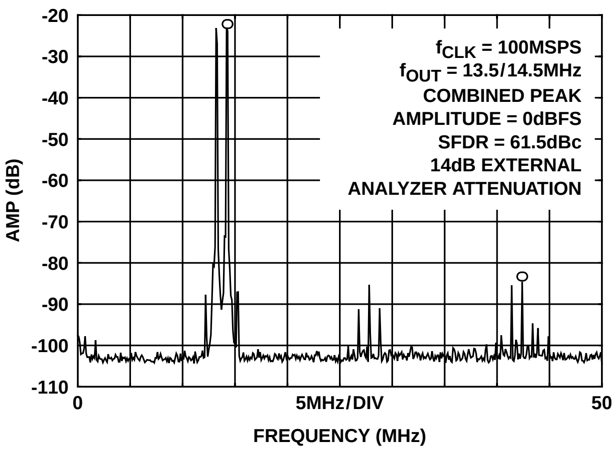


FIGURE 32. TWO-TONE, CLOCK = 100MSPS

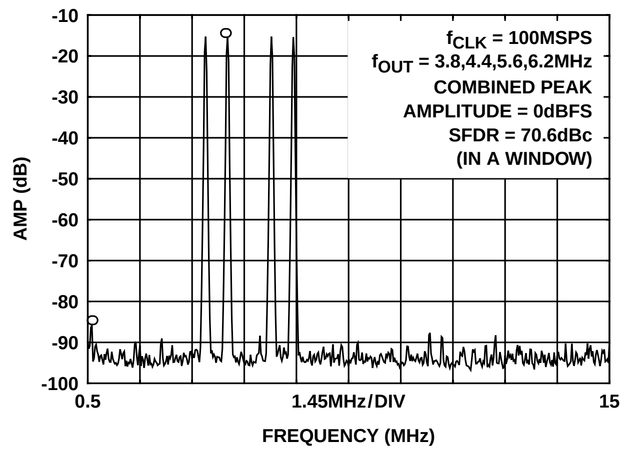


FIGURE 33. FOUR-TONE, CLOCK = 100MSPS

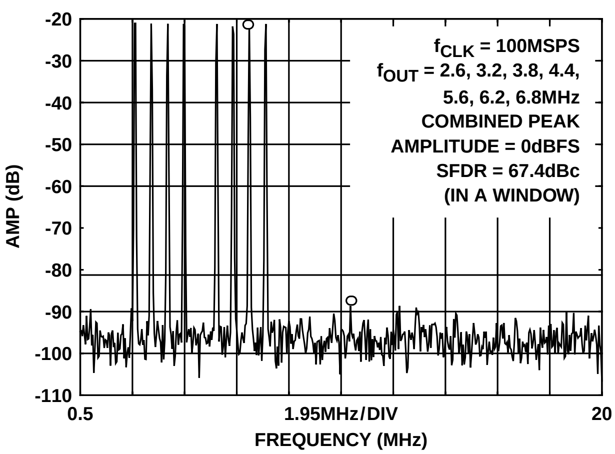


FIGURE 34. EIGHT-TONE, CLOCK = 100MSPS

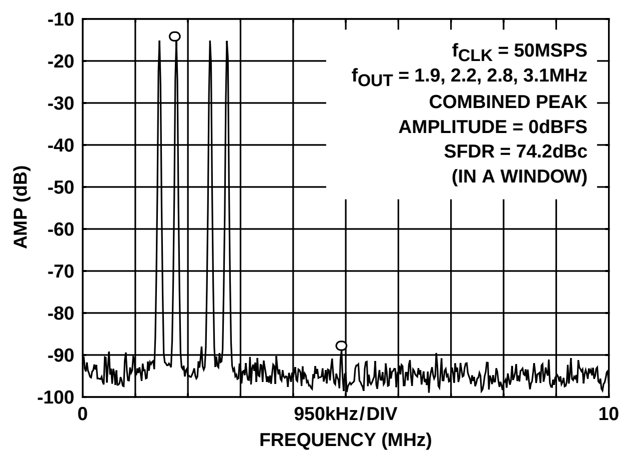


FIGURE 35. FOUR-TONE, CLOCK = 50MSPS

Typical Performance Curves, 3V Power Supply (Continued)

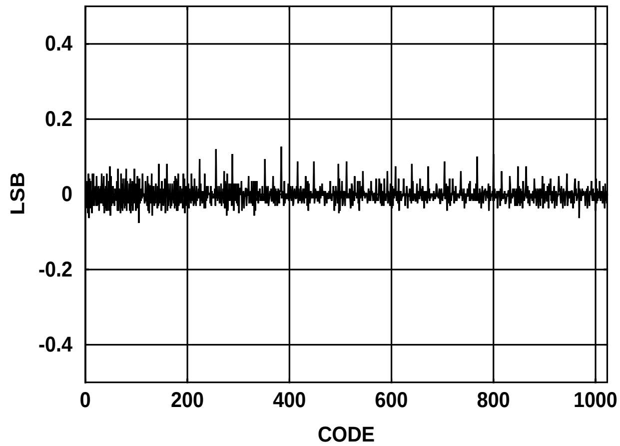


FIGURE 36. DIFFERENTIAL NONLINEARITY

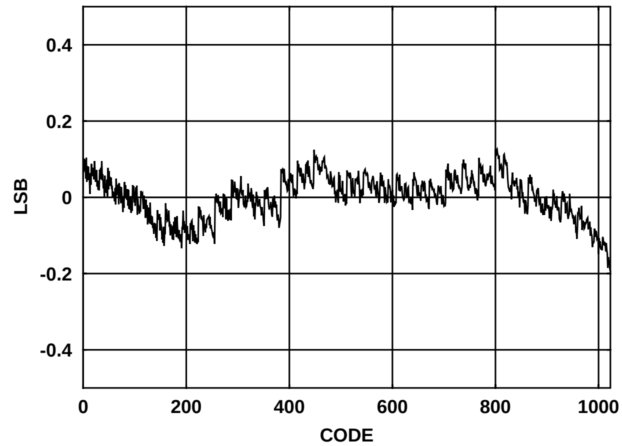


FIGURE 37. INTEGRAL NONLINEARITY

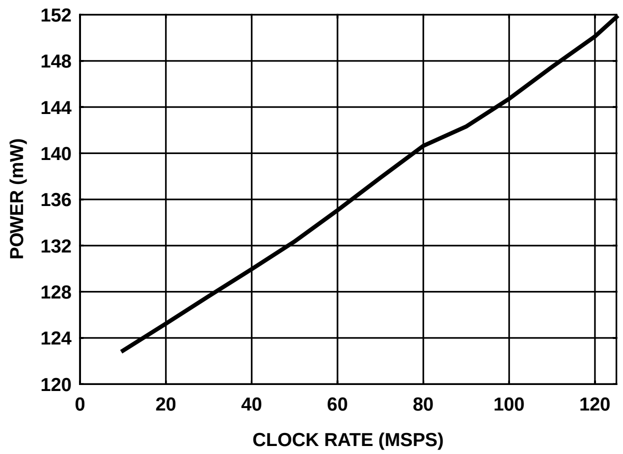


FIGURE 38. POWER vs CLOCK RATE, f_{CLK}/f_{OUT} = 10, I_{OUT} = 20mA

Timing Diagrams

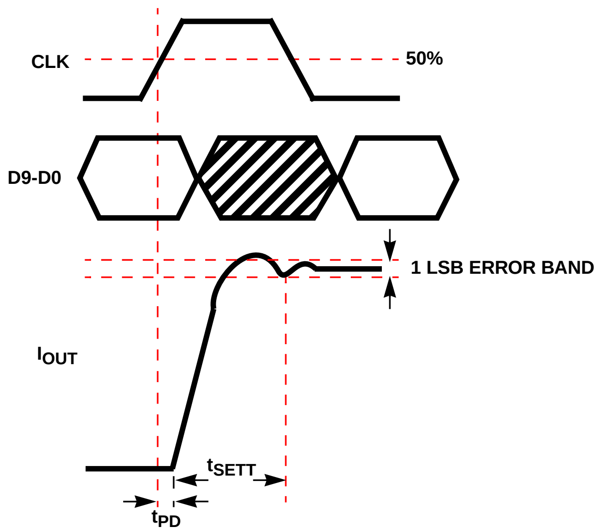


FIGURE 39. OUTPUT SETTLING TIME DIAGRAM

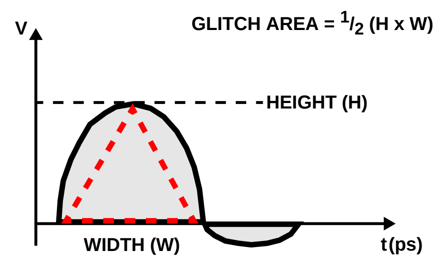


FIGURE 40. PEAK GLITCH AREA (SINGLET) MEASUREMENT METHOD

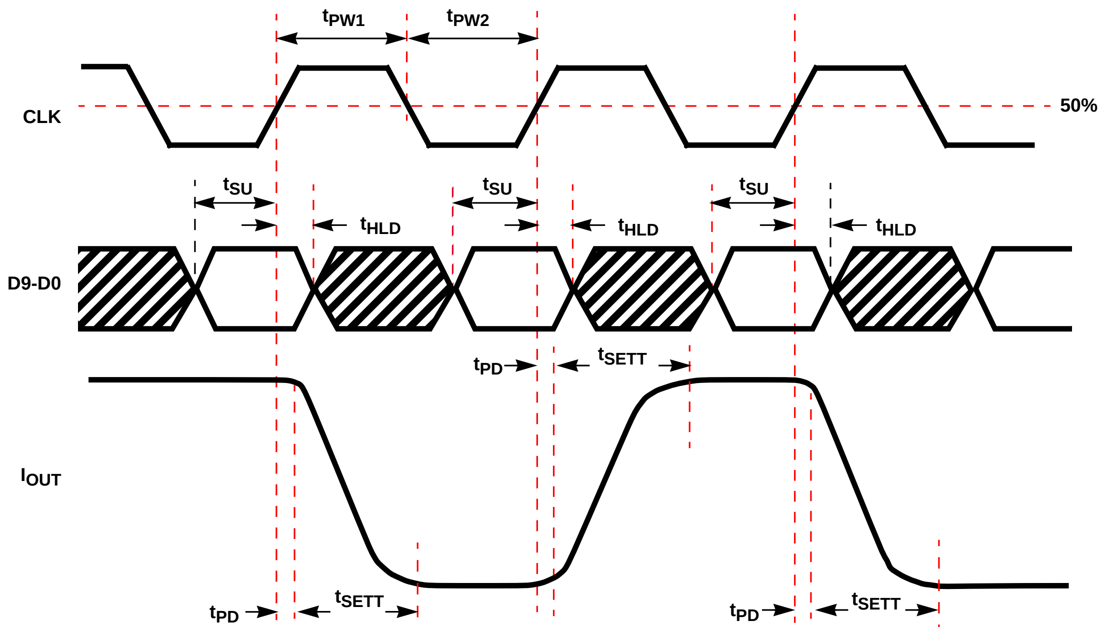


FIGURE 41. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

Definition of Specifications

Integral Linearity Error, INL, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Differential Linearity Error, DNL, is the measure of the step size output deviation from code to code. Ideally the step size should be 1 LSB. A DNL specification of 1 LSB or less guarantees monotonicity.

Output Settling Time, is the time required for the output voltage to settle to within a specified error band measured from the beginning of the output transition. The measurement was done by switching from code 0 to 256, or quarter scale. Termination impedance was 25Ω due to the parallel resistance of the output 50Ω and the oscilloscope's 50Ω input. This also aids the ability to resolve the specified error band without overdriving the oscilloscope.

Singlet Glitch Area, is the switching transient appearing on the output during a code transition. It is measured as the area under the overshoot portion of the curve and is expressed as a Volt-Time specification. This is tested under the same conditions as 'Output Settling Time.'

Full Scale Gain Error, is the error from an ideal ratio of 32 between the output current and the full scale adjust current (through R_{SET}).

Full Scale Gain Drift, is measured by setting the data inputs to all ones and measuring the output voltage through a known resistance as the temperature is varied from T_{MIN} to T_{MAX}. It is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm of FSR (full scale range) per ^oC.

Total Harmonic Distortion, THD, is the ratio of the DAC output fundamental to the RMS sum of the first five harmonics.

Spurious Free Dynamic Range, SFDR, is the amplitude difference from the fundamental to the largest harmonically or non-harmonically related spur within the specified window.

Output Voltage Compliance Range, is the voltage limit imposed on the output. The output impedance load should be chosen such that the voltage developed does not violate the compliance range.

Offset Error, is measured by setting the data inputs to all zeros and measuring the output voltage through a known resistance. Offset error is defined as the maximum *deviation* of the output current from a value of 0mA.

Offset Drift, is measured by setting the data inputs to all zeros and measuring the output voltage through a known resistance as the temperature is varied from T_{MIN} to T_{MAX}. It is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm of FSR (Full Scale Range) per ^oC.

Power Supply Rejection, is measured using a single power supply. Its nominal +5V is varied ±10% and the change in the DAC full scale output is noted.

Reference Input Multiplying Bandwidth, is defined as the 3dB bandwidth of the voltage reference input. It is measured by using a sinusoidal waveform as the external reference with the digital inputs set to all 1s. The frequency is increased until the amplitude of the output waveform is 0.707 of its original value.

Internal Reference Voltage Drift, is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm per ^oC.

Detailed Description

The HI5728 is a dual, 10-bit, current out, CMOS, digital to analog converter. Its maximum update rate is 125MSPS and can be powered by either single or dual power supplies in the recommended range of +3V to +5V. It consumes less than 330mW of power when using a +5V supply with the data switching at 100MSPS. The architecture is based on a segmented current source arrangement that reduces glitch by reducing the amount of current switching at any one time. The five MSBs are represented by 31 major current sources of equivalent current. The five LSBs are comprised of binary weighted current sources. Consider an input waveform to the converter which is ramped through all the codes from 0 to 1023. The five LSB current sources would begin to count up. When they reached the all high state (decimal value of 31) and needed to count to the next code, they would all turn off and the first major current source would turn on. To continue counting upward, the 5 LSBs would count up another 31 codes, and then the next major current source would turn on and the five LSBs would all turn off. The process of the single, equivalent, major current source turning on and the five LSBs turning off each time the converter reaches another 31 codes greatly reduces the glitch at any one switching point. In previous architectures that contained all binary weighted current sources or a binary weighted resistor ladder, the converter might have a substantially larger amount of current turning on and off at certain, worst-case transition points such as mid-scale and quarter scale transitions. By greatly reducing the amount of current switching at certain 'major' transitions, the overall glitch of the converter is dramatically reduced, improving settling times and transient problems.

Digital Inputs And Termination

The HI5728 digital inputs are guaranteed to CMOS levels. However, TTL compatibility can be achieved by lowering the supply voltage to 3V due to the digital threshold of the input buffer being approximately half of the supply voltage. The internal register is updated on the rising edge of the clock. To minimize reflections, proper termination should be implemented. If the lines driving the clock(s) and digital inputs are 50Ω lines, then 50Ω termination resistors should be placed as close to the converter inputs as possible.

Ground Plane(s)

If separate digital and analog ground planes are used, then all of the digital functions of the device and their corresponding components should be over the digital ground plane and terminated to the digital ground plane. The same is true for the analog components and the analog ground plane. Refer to the Application Note on the HI5728 Evaluation Board for further discussion of the ground plane(s) upon availability.

Noise Reduction

To minimize power supply noise, 0.1μF capacitors should be placed as close as possible to the converter's power supply pins, AV_{DD} and DV_{DD}. Also, should the layout be designed using separate digital and analog ground planes, these capacitors should be terminated to the digital ground for DV_{DD} and to the analog ground for AV_{DD}. Additional filtering of the power supplies on the board is recommended. See the Application Note on the HI5728 Evaluation Board for more information upon availability.

Voltage Reference

The internal voltage reference of the device has a nominal value of +1.2V with a ±60 ppm/^oC drift coefficient over the full temperature range of the converter. It is recommended that a 0.1µF capacitor be placed as close as possible to the REFIO pin, connected to the analog ground. The REFLO pin (15) selects the reference. The internal reference can be selected if pin 15 is tied low (ground). If an external reference is desired, then pin 15 should be tied high (to the analog supply voltage) and the external reference driven into REFIO, pin 23. The full scale output current of the converter is a function of the voltage reference used and the value of R_{SET}. I_{OUT} should be within the 2mA to 20mA range, through operation below 2mA is possible, with performance degradation.

If the internal reference is used, V_{FSADJ} will equal approximately 1.16V (pin 22). If an external reference is used, V_{FSADJ} will equal the external reference. The calculation for I_{OUT}(Full Scale) is:

I_{OUT} (Full Scale) = (V_{FSADJ}/R_{SET})x 32.

If the full scale output current is set to 20mA by using the internal voltage reference (1.16V) and a 1.86kΩ R_{SET} resistor, then the input coding to output current will resemble the following:

TABLE 1. INPUT CODING vs OUTPUT CURRENT (Per DAC)

INPUT CODE (D9-D0)	IOUTA (mA)	IOUTB (mA)
11111 11111	20	0
10000 00000	10	10
00000 00000	0	20

Outputs

IOUTA and IOUTB (or QOUTA and QOUTB) are complementary current outputs. The sum of the two currents is always equal to the full scale output current minus one LSB. If single ended use is desired, a load resistor can be used to convert the output current to a voltage. It is recommended that the unused output be either grounded or equally terminated. The voltage developed at the output must not violate the output voltage compliance range of -0.3V to 1.25V. R_{LOAD} should be chosen so that the desired output voltage is produced in conjunction with the output full scale current, which is described above in the ‘Reference’ section. If a known line impedance is to be driven, then the output load resistor should be chosen to match this impedance. The output voltage equation is:

$V_{OUT} = I_{OUT}$ X R_{LOAD}.

These outputs can be used in a differential-to-single-ended arrangement to achieve better harmonic rejection. The SFDR measurements in this data sheet were performed with a 1:1 transformer on the output of the DAC (see Figure 1). With the center tap grounded, the output swing of pins 16 and 17 will be biased at zero volts. It is important to note here that the negative voltage output compliance range limit is -300mV, imposing a maximum of 600mV_{P-P} amplitude with this configuration. The loading as shown in Figure 1 will result in a 500mV signal at the output of the transformer if the full scale output current of the DAC is set to 20mA.

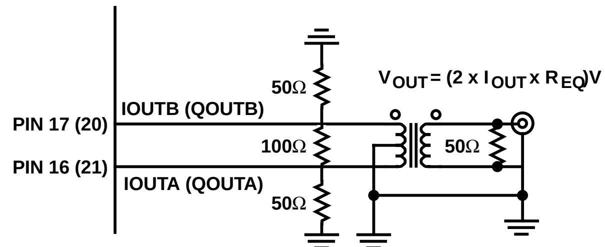


FIGURE 42.

$V_{OUT} = 2 \times I_{OUT} \times R_{EQ}$,where R_{EQ} is ~12.5Ω.

Allowing the center tap to float will result in identical transformer output, however the output pins of the DAC will have positive DC offset. The 50Ω load on the output of the transformer represents the spectrum analyzer’s input impedance.