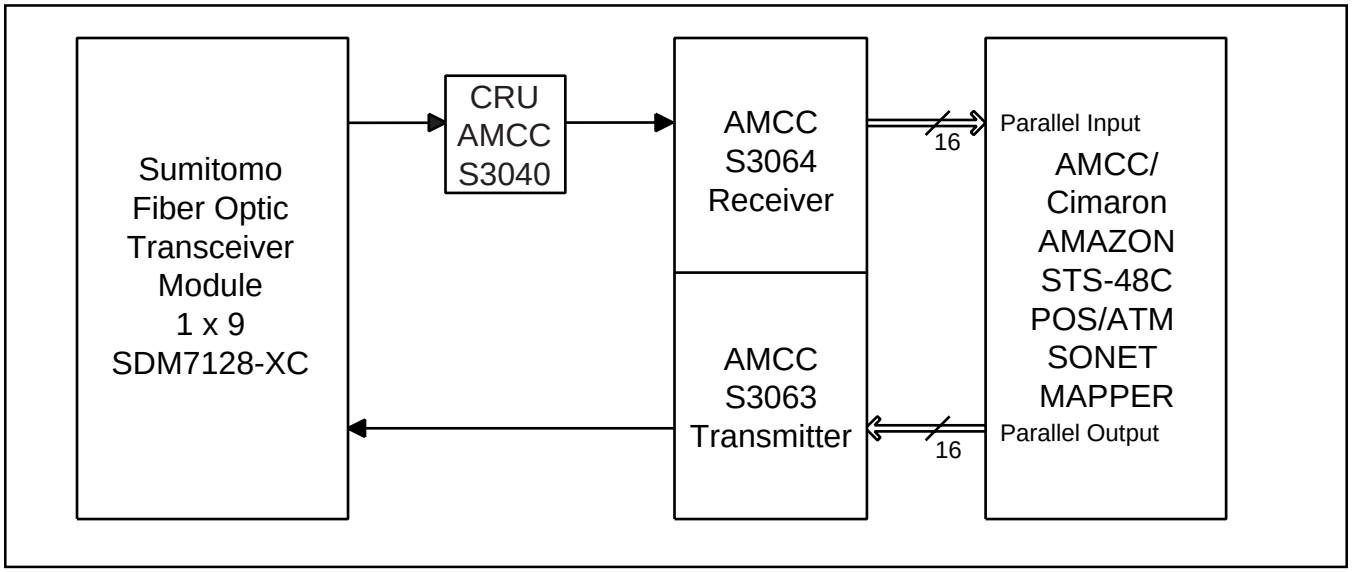
AMCC S3063 TRANSMITTER, S3064 RECEIVER, S3040 CDR, SUMITOMO SDM7128-XC FIBER OPTIC TRANSCEIVER AND AMCC/CIMARON AMAZON S4801 POS/ATM SONET MAPPER

INTRODUCTION

The AMCC S3063 transmitter and S3064 receiver chips are fully integrated serialization/deserialization SONET STS-48/OC-48 (2.488 Gbps) interface devices. These devices are suitable for SONET based ATM applications, and can be used in conjunction with AMCC's S3040 Clock Recovery Unit (CRU). The AMCC S3063 and S3064 chips provide the first stage of the digital processing of a receive and a transmit SONET STS-48 bit-serial stream. In the receive path it converts a bit-serial data stream into a 16-bit parallel data format, and in the transmit path it converts 16-bit parallel data into bit-serial data. Figure 1 shows a typical application block diagram with an AMCC/ Cimaron AMAZON. Figure 2 shows more specifically the design details. Combining these devices provides a Physical Media Dependent (PMD) layer for SONET/SDH data transfer.

Figure 1. Typical Network Application Block Diagram

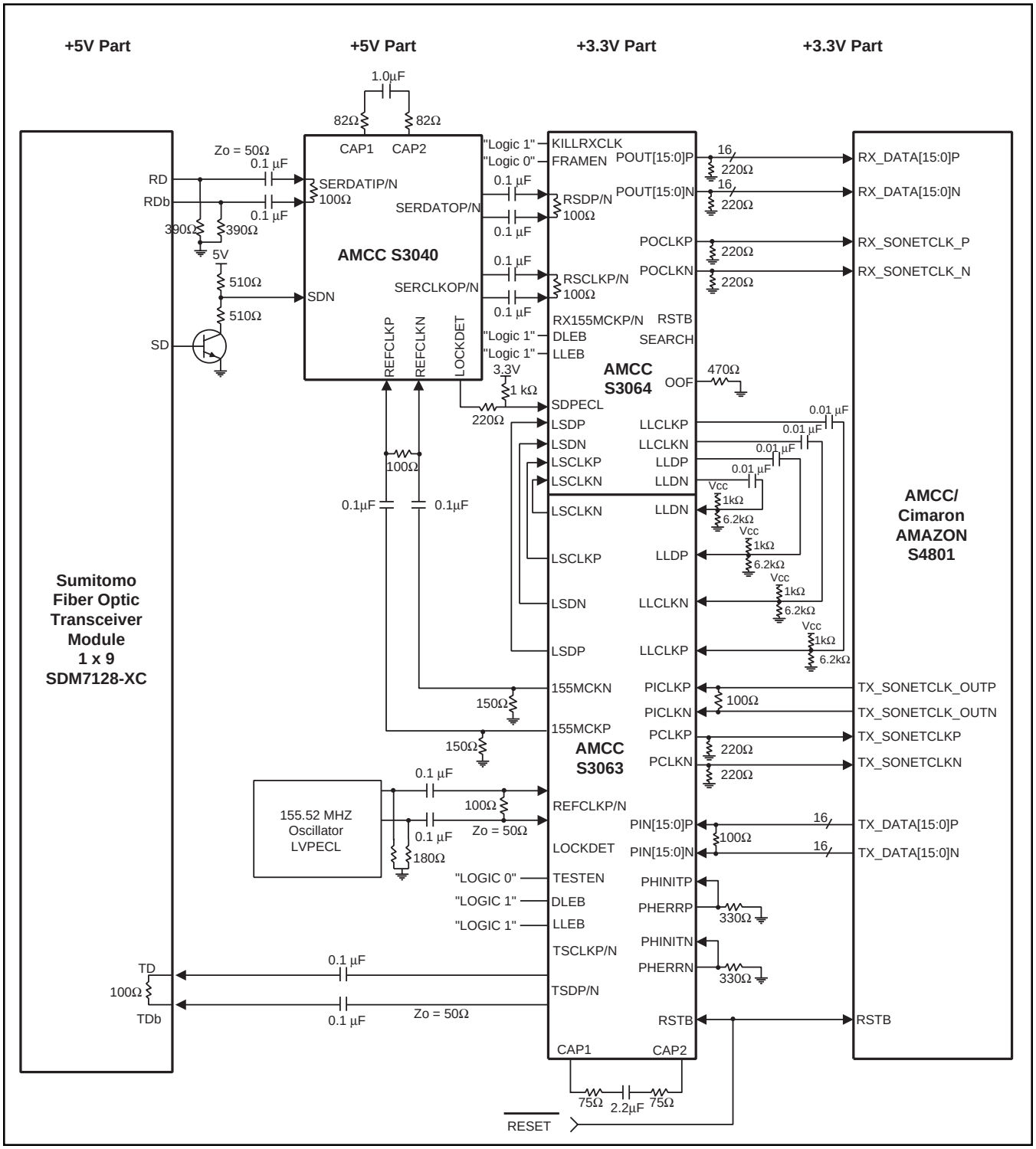


Signal Connect Description

Figure 1 shows the block diagram of this solution.

1. The Sumitomo fiber optic transceiver interfaces to the AMCC S3040 CRU chip via a bit-serial data stream.
2. After the clock is recovered from the bit-serial data stream the CRU chip transmits the recovered clock and re-timed data to the AMCC S3064 receiver.
3. The AMCC S3064 receiver transmits the bit-serial data converted into 16-bit parallel data to the AMCC/ Cimaron AMAZON.
4. The AMCC/Cimaron AMAZON transmits 16-bit parallel data to the AMCC S3063.
5. The AMCC S3063 transmits the bit-serial data to the Sumitomo fiber optic transceiver.

Figure 2. S3063 Transmitter, S3064 Receiver, S3040 CDR, Sumitomo SDM7128-XC Fiber Optic Transceiver and AMCC/Cimaron AMAZON S4801 POS/ATM SONET Mapper Block Diagram



Parts List

The following is a parts list that is a recommendation to the designer to implement the circuit in Figures 1 and 2.

QTY	Part # or Equivalent	Description
2		Resistor, 75 Ω, 10%, 1/8W, 805 or 603 package size
2		Resistor, 82 Ω, 10%, 1/8W, 805 or 603 package size
19		Resistor, 100 Ω, 10%, 1/8W, 805 or 603 package size
2		Resistor, 150 Ω, 10%, 1/8W, 805 or 603 package size
2		Resistor, 180 Ω, 10%, 1/8W, 805 or 603 package size
37		Resistor, 220 Ω, 10%, 1/8W, 805 or 603 package size
2		Resistor, 330 Ω, 10%, 1/8W, 805 or 603 package size
2		Resistor, 390 Ω, 10%, 1/8W, 805 or 603 package size
1		Resistor, 470 Ω, 10%, 1/8W, 805 or 603 package size
2		Resistor, 510 Ω, 10%, 1/8W, 805 or 603 package size
5		Resistor, 1 kΩ, 10%, 1/8W, 805 or 603 package size
4		Resistor, 6.2 kΩ, 10%, 1/8W, 805 or 603 package size
4		Capacitor, 0.01 µF, 10%, X7R, 16V, Surface Mount package
12		Capacitor, 0.1 µF, 10%, X7R, 16V, Surface Mount package
1		Capacitor, 1.0 µF, 10%, X7R, 16V, Surface Mount package
1		Capacitor, 2.2 µF, 10%, X7R, 16V, Surface Mount package
1	S3063	SONET/SDH/ATM OC-48 Transmitter
1	S3064	SONET/SDH/ATM OC-48 Receiver
1	S3040	SONET/SDH Clock Recovery Unit
1	S4801 AMAZON	AMCC/Cimaron OC-48 POS/ATM/SONET Mapper
1	SDM7128-XC	Sumitomo 5V Fiber Optic 1 x 9 Transceiver
1		LVPECL Oscillator, +3.3V at 155.52 MHz
1	MMBT3904LTI	NPN Transistor, 2N3904

Theory Of Operation

1. The S3040 extracts the clock and re-times the data from the received differential PECL serial data input (SERDATIP/N) coming from the fiber optic receiver when the signal detect (SDN) is a PECL Low level. When signal detect (SDN) is at a PECL High level, the Phase Lock Loop (PLL) will be forced to lock to the PECL Reference Clock (REFCLKP/N). When the transmit PLL is locked to the reference clock input the lock detect (LOCKDET) TTL output goes High.
2. The S3064 receives the OC-48 (2.488 Gbit/s) scrambled NRZ data signals on the serial data stream (RSDP/N) LVPECL inputs. These inputs are clocked into the S3064 by the Receive Serial Clock (RSCLKP/N) LVPECL inputs. This clock is used by the receive section as the master clock to perform framing and deserialization functions.
3. When FRAMEN is disabled [FRAMEN = 0] and OOF is connected to ground, the Frame Pulse (FP) output is always inactive. The AMAZON device should be in default mode [RX_FRMR_INH = 0]. In this mode, the parallel input data is not assumed to be byte aligned. The AMAZON device will align to the incoming data.
4. The serial-bit data stream is then converted into a 16-bit parallel data format for output onto the differential parallel output data bus (POUTP/N[15:0]). The differential 16-bit parallel data is clocked out of the S3064 and into the AMCC/Cimaron AMAZON S4801 with the differential Parallel Output Clock (POCLK).
5. The 16-bit parallel data is output from the AMCC/Cimaron AMAZON S4801 into the S3063 differential parallel data input bus (PIN[15:0]) and is sampled by the Parallel Input Clock (PICLK) of the S3063. This clock is generated by the S3063 Parallel Clock (PCLK) which is fed into the AMCC/Cimaron AMAZON S4801 as the transmit clock (TX_SONETCLK) and then back into the PICLK input of the S3063.
6. The 16-bit parallel data is then converted to bit-serial data and output through the Transmit Serial Data (TSDP/N) connections to the Sumitomo fiber optic transmitter (SDM7128-XC).
7. If the incoming serial-bit data stream is lost (when SDN is High) the lock detect circuit internal to the S3040 substitutes the external reference clock for the missing data stream clocking signal. This substitution of reference timing source is helpful to supply a continuous timing signal for the upstream devices and system operation even though valid received data does not exist. This switch over is a smooth transition with no noticeable phase shift.

Terminations

The following is a list of terminations that need to be added for this particular design.

1. The 100 Ω line to line termination resistor should be as close to the termination points as possible.
2. The 330 Ω and 390 Ω pull down resistors should be as close to the sources as possible.
3. The high frequency traces should be designed as 50 Ω transmission lines with the termination as depicted in Figure 2.
4. All the termination resistors should be placed at the end of the transmission line, and the power supply decoupling should be placed as close as possible to the devices.
5. The PECL and LVPECL (differential pairs) traces should have equal length, (allows both signals to arrive at the destination at the same time) and be run in parallel and in close proximity of one another. This allows the same noise to couple onto both of the lines and become common mode noise which is ignored by differential inputs.

Conclusion

The Sumitomo fiber optic transceiver, AMCC's S3063/S3064/S3040 and the AMCC/Cimaron AMAZON S4801 solution combine to make a complete OC-48 Physical Media Dependent (PMD) layer for SONET/SDH data transfer.

Disclaimer

The circuit presented in this application note is based on data sheet information as well as standard implementation of termination schemes. It has not been built and tested in the lab environment.

Applied Micro Circuits Corporation • 6290 Sequence Dr., San Diego, CA 92121

Phone: (858) 450-9333 • (800) 755-2622 • Fax: (858) 450-9885

http://www.amcc.com