PRELIMINARY

W127/W127-A

Spread Spectrum 3 DIMM System Frequency Synthesizer w/AGP

Features

- **Maximized EMI suppression using Cypress's Spread Spectrum technology**
- **I^2C interface**
- **Four copies of CPU Output**
- **Six copies of PCI Output**
- **Two copies of AGP Output**
- **One copy of 48-MHz USB Output**
- **One copy of 24-MHz SIO Output**
- **Twelve copies of SDRAM Output**
- **One buffered copy of 14.318-MHz reference input**
- **Mode input pin selects optional power management input control pins (reconfigures pins 29, 30, 31, and 32)**
- **Smooth frequency transition upon frequency reselection**
- **Available in 48-pin SSOP (300 mils)**
- **Standard W127 device supports up to 112-MHz operations. High-performance option W127-A supports up to 124-MHz.**

Key Specifications

Supply Voltages: ..... V_{DDQ3} = 3.3V, V_{DDQ2} = 3.3V or 2.5V

CPU Cycle to Cycle Jitter: ..... 250 ps

CPU to AGP Skew: ..... 0±500 ps

AGP to PCI Skew: ..... 1.5 ns (AGP Leads)

CPU Output Edge Rate: ..... ≥1 V/ns

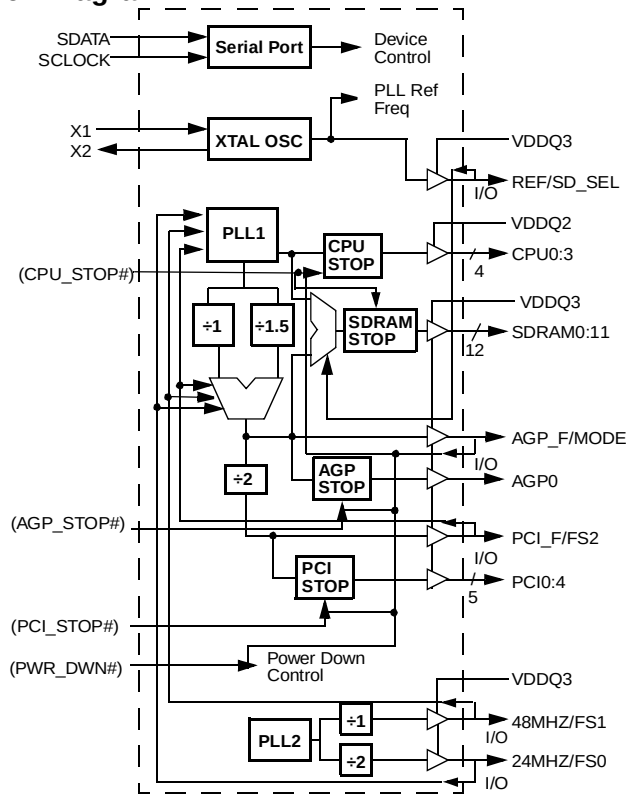
SDRAM Output Edge Rate: ..... ≥1.5 V/ns

Note: All skews are optimized @V_{DDQ2} = V_{DDQ3} = 3.3V±5%. Skews are not guaranteed for V_{DDQ2} = 2.5V.

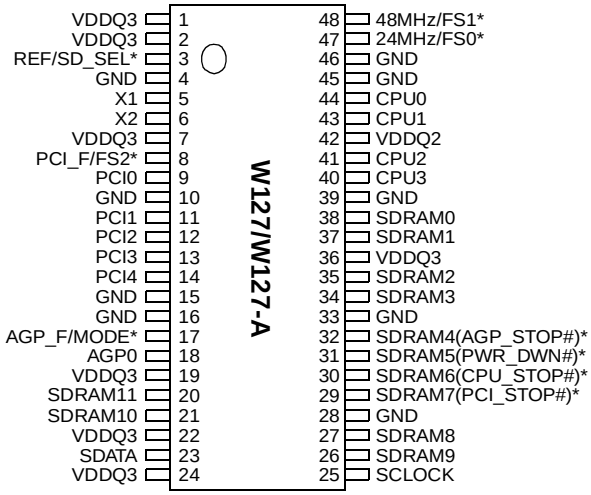
Table 1. Pin Selectable Frequency[1]

Input Address			CPU (MHz)	AGP (MHz)	PCI (MHz)
FS2	FS1	FS0			
0	0	0	68.5	68.5	34.25
0	0	1	112	74.6	37.3
0	1	0	95.25	63.5	31.75
0	1	1	100	66.6	33.3
1	0	0	83.3	55.53	27.77
1	0	1	75.0	75	37.5
1	1	0	124	82.6	41.3
1	1	1	66.6	66.6	33.3

Block Diagram



Pin Configuration[2]



Notes:

1. Configuration "110" is supported by W127-A only (see shaded row of *Table 1*).
2. Signal names with "*" denote pins have internal 250K pull-up resistor, though not relied upon for pulling to V_{DDQ3}. Signal names with parenthesis denote function is selectable by MODE pin strapping.

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:3	44, 43, 41, 40	O	***CPU Clock Outputs 0 through 3:*** These four CPU clock outputs are controlled by the CPU_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ2.
PCI_F/FS2	8	I/O	***Free-running PCI Clock Output and Frequency Selection Bit 2:*** As an output, this pin works in conjunction with PCI0:4. Output voltage swing is controlled by voltage applied to VDDQ3. When an input, this pin functions as part of the frequency selection address. The value of FS0:2 determines the power-up default frequency of device output clocks as per *Table 1*, “Pin Selectable Frequency” on page 1.
PCI0:4	9, 11, 12, 13, 14	O	***PCI Clock Outputs 0 through 4:*** Output voltage swing is controlled by voltage applied to VDDQ3. Outputs are held LOW if PCI_STOP# is set LOW.
SDRAM0:3 SDRAM8:11	38, 37, 35, 34, 27, 26, 21, 20	O	***SDRAM Clock Outputs:*** These eight SDRAM clock outputs run synchronous to the CPU clock outputs or AGP clock output as selected using SD_SEL per *Table 2*.
SDRAM4:7	32, 31, 30, 29	I/O	***SDRAM Clock Outputs:*** These four SDRAM clock outputs run synchronous to the CPU clock outputs or AGP clock output as selected using SD_SEL per *Table 2*. If programmed as inputs, (refer to MODE pin description), these pins are used for STOP_ CPU, AGP, PCI, and power-down control.
48MHZ/FS1	48	I/O	***48-MHz Output and Frequency Selection Bit 1:*** Fixed clock output that defaults to 48 MHz following device power-up. When an input, this pin functions as part of the frequency selection address. The value of FS0:2 determines the power-up default frequency of device output clocks as per *Table 1*, “Pin Selectable Frequency” on page 1.
24MHZ/FS0	47	I/O	***24-MHz Output and Frequency Selection Bit 0:*** Fixed clock output that defaults to 24 MHz following device power-up. When an input, this pin functions as part of the frequency selection address. The value of FS0:2 determines the power-up default frequency of device output clocks as per *Table 1*, “Pin Selectable Frequency” on page 1.
AGP_F/MODE	17	I/O	***Free-running AGP Output and Mode Control Input:*** As an output, this pin works in conjunction with AGP0 and is a free running clock. When an input, it determines the functions for pin 29, 30, 31, and 32. See *Table 3*.
AGP0	18	O	***AGP Output:*** This output is controlled by the AGP_STOP# pin.
REF/SD_SEL	3	I/O	***Fixed 14.318-MHz and SDRAM Output Selection:*** As an output, this pin is used for various system applications. Output voltage swing is controlled by voltage applied to VDDQ3. When an input, this pin selects the SDRAM to run synchronous to either CPU or AGP. See *Table 2*.
X1	5	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
X2	6	I	***Crystal Connection:*** An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
SDATA	23	I	***Serial Data Input:*** Data input for Serial Data Interface. Refer to Serial Data Interface section that follows.
SCLOCK	25	I	***Serial Clock Input:*** Clock input for Serial Data Interface. Refer to Serial Data Interface section that follows.
VDDQ3	1, 2, 7, 19, 22, 24, 36	P	***Power Connection:*** Connected to 3.3V supply.
VDDQ2	42	P	***Power Connection:*** Power Supply for CPU0:3 clock outputs. (3.3V Supply)
GND	4, 10, 15, 16, 28, 33, 39, 45, 46	G	***Ground Connection:*** Connect all ground pins to the common system ground plane.

W127/W127-A Pin Selection Tables

Table 2. SD_SEL Function

SD_SEL	SDRAM0:11
1	Running @ CPU Frequency
0	Running @ AGP Frequency

Table 3. Mode Function

Pin Function				
Mode	**Pin 29**	**Pin 30**	**Pin 31**	**Pin 32**
1	SDRAM7	SDRAM6	SDRAM5	SDRAM4
0	PCI_STOP#	CPU_STOP#	PWR_DWN#	AGP_STOP#

Table 4. Power Management Pin Function

SIGNAL	=0	=1
CPU_STOP#	CPU0:3 & SDRAM0:11 = LOW	Active
PCI_STOP#	PCI0:4 = LOW	Active
AGP_STOP#	AGP0 = LOW	Active
PWR_DWN#	All Clock Outputs LOW	Active

Overview

The W127/W127-A was designed specifically to provide all clock signals required for a motherboard designed with the Via MVP3 chipset using either a Pentium® or K6 microprocessor. Although it can be used with split voltages (3.3/2.5), the skew specifications are guaranteed only for single 3.3V supply. The primary distinguishing feature of the W127/W127-A is the 95.25-MHz CPU frequency option, which supports the K6 333-MHz CPU.

Twelve SDRAM outputs are provided for support of up to 3 SDRAM DIMM modules. Unused clock outputs can be disabled through the I^2C interface to reduce system power consumption and more importantly reduce EMI emissions.

Functional Description

I/O Pin Operation

Pins 3, 8, 17, 47, and 48 are dual-purpose I/O pins. Upon power-up these pins act as logic inputs, allowing the determination of assigned device functions. A short time after power-up, the logic state of each pin is latched and the pins then become clock outputs. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10-kΩ “strapping” resistor is connected between each I/O pin and ground or V_{DDQ3}. Connection to ground sets a latch to “0,” connection to V_{DDQ3} sets a latch to “1.” *Figure 1* and *Figure 2* show two suggested methods for strapping resistor connection.

Upon W127/W127-A power-up, the first 2 ms of operation is used for input logic selection. During this period, the 24-MHz, 48-MHz, REF, PCI_F and AGP_F clock output buffers are three-stated, allowing the output strapping resistor on each I/O pin to pull the pin and its associated capacitive clock load to either a logic HIGH or logic LOW state. At the end of the 2-ms period, the established logic 0 or 1 condition of each I/O pin is latched. Next the output buffers are enabled, converting all I/O pins into operating clock outputs. The 2-ms timer starts when V_{DDQ3} reaches 2.0V. The input bits can only be reset by turning V_{DDQ3} off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of the clock output is 40Ω (nominal), which is minimally affected by the 10-kΩ strap to ground or V_{DDQ3}. As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or V_{DDQ3} should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

When the clock outputs are enabled following the 2-ms input period, target (normal) output frequency is delivered, assuming that V_{DDQ3} has stabilized. If V_{DDQ3} has not yet reached full value, output frequency initially may be below target but will increase to target once V_{DDQ3} voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.

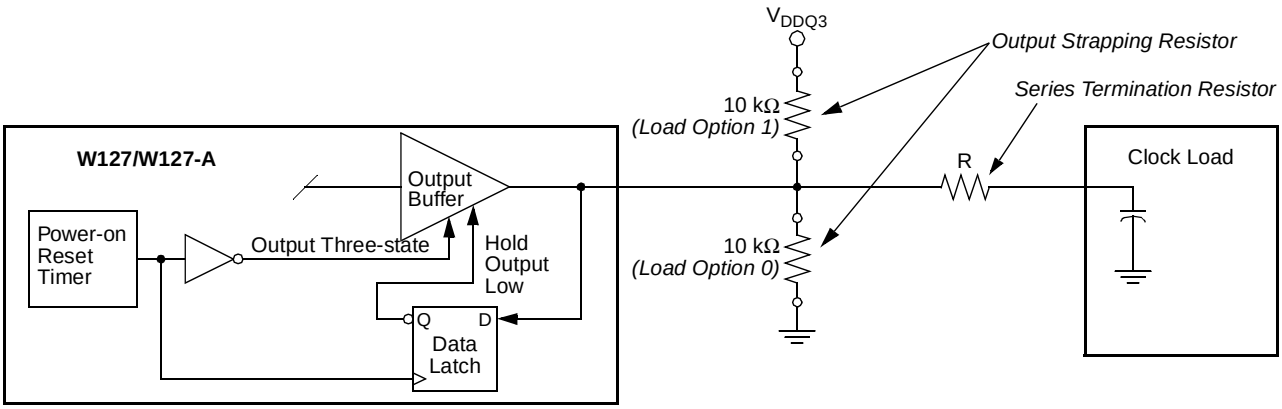


Figure 1. Input Logic Selection Through Resistor Load Option

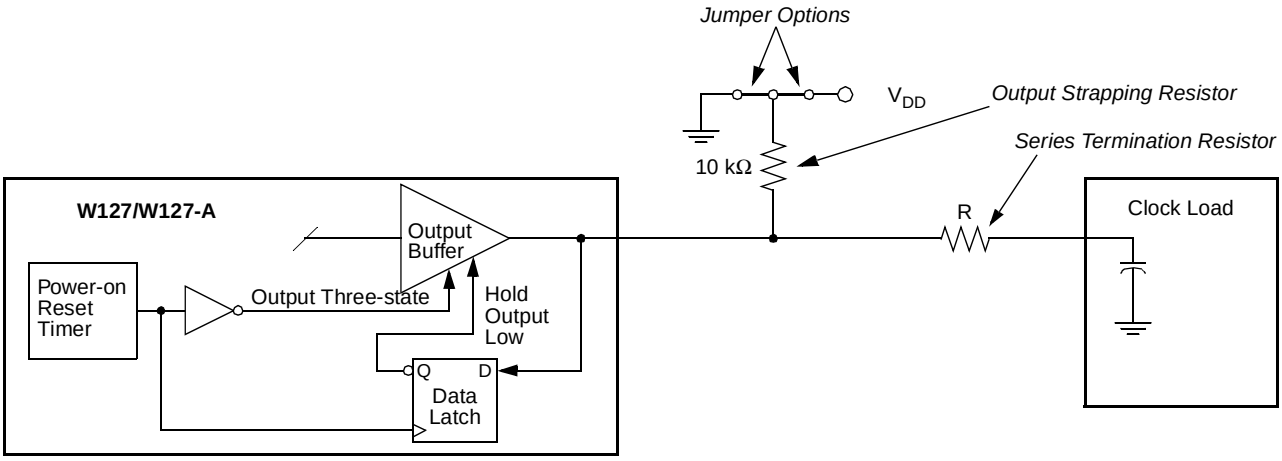


Figure 2. Input Logic Selection Through Jumper Option

CPU/PCI Frequency Selection

CPU output frequency is selected with I/O pins 8, 47, and 48. Refer to *Table 1* for CPU/PCI frequency programming information. Alternatively, frequency selections are available through the serial data interface. Refer to *Table 8*, “Additional Frequency Selections through Serial Data Interface Data Bytes,” on page 9.

Output Buffer Configuration

Clock Outputs

All clock outputs are designed to drive serially terminated clock lines. The W127/W127-A outputs are CMOS-type, which provide rail-to-rail output swing.

Crystal Oscillator

The W127/W127-A requires one input reference clock to synthesize all output frequencies. The reference clock can be either an externally generated clock signal or the clock generated by the internal crystal oscillator. When using an external clock signal, pin X1 is used as the clock input and pin X2 is left open. The input threshold voltage of pin X1 is (V_{DDQ3})/2.

The internal crystal oscillator is used in conjunction with a quartz crystal connected to device pins X1 and X2. This forms a parallel resonant crystal oscillator circuit. The W127/W127-A incorporates the necessary feedback resistor and crystal load capacitors. Including typical stray circuit capacitance, the total load presented to the crystal is approximately 20 pF. For optimum frequency accuracy without the addition of external capacitors, a parallel-resonant mode crystal specifying a load of 20 pF should be used. This will typically yield reference frequency accuracies within ±100 ppm. To achieve similar accuracies with a crystal calling for a greater load, external capacitors must be added such that the total load (internal, external, and parasitic capacitors) equals that called for by the crystal.

Spread Spectrum Generator

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 3*.

As shown in *Figure 3*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is:

$$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$$

Where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 4*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is ±0.5% of the center frequency. *Figure 4* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Spread Spectrum clocking is activated or deactivated by selecting the appropriate values for bits 1–0 in data byte 0 of the I^2C data stream. Refer to *Table 7* for more details.

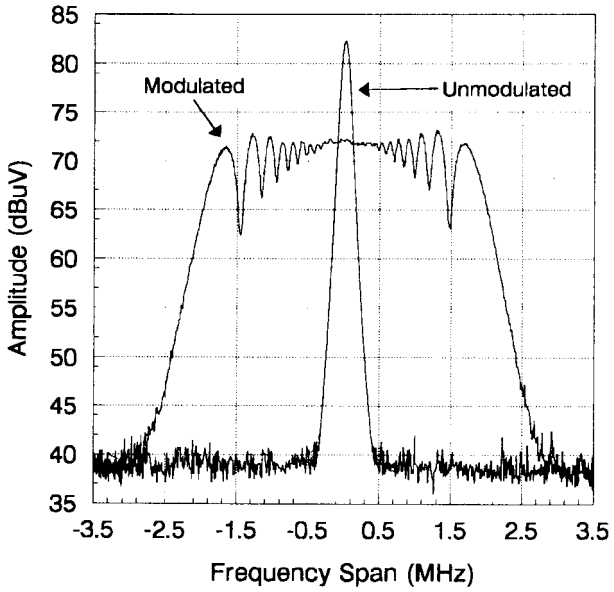


Figure 3. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

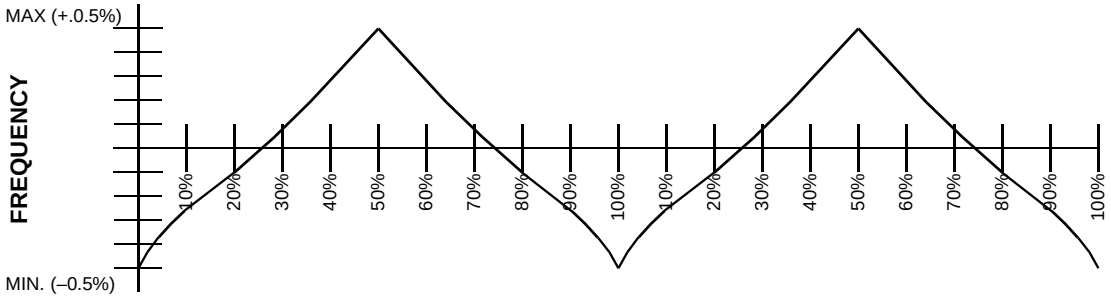


Figure 4. Typical Modulation Profile

Serial Data Interface

The W127/W127-A features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the W127/W127-A initializes with default register settings, therefore the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. *Table 5* summarizes the control functions of the serial data interface.

Operation

Data is written to the W127/W127-A in ten bytes of eight bits each. Bytes are written in the order shown in *Table 6*.

Table 5. Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held LOW.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused SDRAM DIMM socket or PCI slot.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections. Frequency is changed in a smooth and controlled fashion.	For alternate CPU devices and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Output Three-state	Puts all clock outputs into a high-impedance state.	Production PCB testing.
(Reserved)	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Table 6. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the W127/W127-A to accept the bits in Data Bytes 0–6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the W127/W127-A is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the W127/W127-A, therefore bit values are ignored ("don't care"). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the W127/W127-A, therefore bit values are ignored ("don't care"). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to *Table 7*	The data bits in these bytes set internal W127/W127-A registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to *Table 7*, Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3		
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

Writing Data Bytes

Each bit in the data bytes controls a particular device function except for the “reserved” bits, which must be written as a logic 0. Bits are written MSB (most significant bit) first, which is bit 7. *Table 7* gives the bit formats for registers located in Data Bytes 0–6.

Table 8 details additional frequency selections that are available through the serial data interface.

Table 9 details the select functions for Byte 0, bits 1 and 0.

Table 7. Data Bytes 0–6 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 0						
7	--	--	(Reserved)	--	--	0
6	--	--	SEL_2	Refer to *Table 8*		0
5	--	--	SEL_1	Refer to *Table 8*		0
4	--	--	SEL_0	Refer to *Table 8*		0
3	8, 47, 48	FS0:2	BYT0 /FS#	Frequency Controlled by external pins FS0:2	Frequency Controlled by SEL_0:2, above	0
2			(Reserved)	--	--	0
1–0	--	--	Bit 1 Bit 0 Function (See *Table 9* for function details) 0 0 Normal Operation 0 1 (Reserved) 1 0 Spread Spectrum On 1 1 All Outputs Three-stated			00
Data Byte 1						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	40	CPU3	Clock Output Disable	Low	Active	1
2	41	CPU2	Clock Output Disable	Low	Active	1
1	43	CPU1	Clock Output Disable	Low	Active	1
0	44	CPU0	Clock Output Disable	Low	Active	1
Data Byte 2						
7	--	--	(Reserved)	--	--	0
6	8	PCI_F	Clock Output Disable	Low	Active	1
5	--	--	(Reserved)	--	--	0
4	14	PCI4	Clock Output Disable	Low	Active	1
3	13	PCI3	Clock Output Disable	Low	Active	1
2	12	PCI2	Clock Output Disable	Low	Active	1
1	11	PCI1	Clock Output Disable	Low	Active	1
0	9	PCI0	Clock Output Disable	Low	Active	1

Table 7. Data Bytes 0–6 Serial Configuration Map (continued)

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 3						
7	29	SDRAM7	Clock Output Disable	Low	Active	1
6	30	SDRAM6	Clock Output Disable	Low	Active	1
5	31	SDRAM5	Clock Output Disable	Low	Active	1
4	32	SDRAM4	Clock Output Disable	Low	Active	1
3	34	SDRAM3	Clock Output Disable	Low	Active	1
2	35	SDRAM2	Clock Output Disable	Low	Active	1
1	37	SDRAM1	Clock Output Disable	Low	Active	1
0	38	SDRAM0	Clock Output Disable	Low	Active	1
Data Byte 4						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	17	AGP_F	Clock Output Disable	Low	Active	1
4	18	AGP0	Clock Output Disable	Low	Active	1
3	20	SDRAM11	Clock Output Disable	Low	Active	1
2	21	SDRAM10	Clock Output Disable	Low	Active	1
1	26	SDRAM9	Clock Output Disable	Low	Active	1
0	27	SDRAM8	Clock Output Disable	Low	Active	1
Data Byte 5						
7	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	--	--	(Reserved)	--	--	0
0	3	REF	Clock Output Disable	Low	Active	1
Data Byte 6						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	--	--	(Reserved)	--	--	0
0	--	--	(Reserved)	--	--	0

Table 8. Additional Frequency Selections through Serial Data Interface Data Bytes[3]

Input Conditions			Output Frequency		
Data Byte 0, Bit 3 = 1					
Bit 6 SEL_2	Bit 5 SEL_1	Bit 4 SEL_0	CPU Clocks (MHz)	AGP	PCI Clocks (MHz)
0	0	0	68.5	68.5	34.25
0	0	1	112	74.6	37.3
0	1	0	95.25	63.5	31.75
0	1	1	100	66.6	33.3
1	0	0	83.3	55.53	27.77
1	0	1	75.0	75	37.5
1	1	0	124	82.6	41.3
1	1	1	66.6	66.6	33.3

Table 9. Select Function for Data Byte 0, Bits 0:1

Function	Input Conditions		Output Conditions			
	Data Byte 0		CPU0:3, SRAM0:11	PCI_F, PCI0:4	REF	48/24MHZ
	Bit 1	Bit 0				
Normal Operation	0	0	Note 4	Note 4	14.318 MHz	48/24 MHz
Spread Spectrum	1	0	±0.5%	±0.5%	14.318 MHz	48/24 MHz
Three-state	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Notes:
3. Configuration “110” is supported by W127-A only (see shaded row of *Table 8*).
4. CPU, SDRAM, and PCI frequency selections are listed in *Table 1* and *Table 8*.

How To Use the Serial Data Interface

Electrical Requirements

Figure 5 illustrates electrical characteristics for the serial interface bus used with the W127/W127-A. Devices send data over the bus with an open drain logic output that can (a) pull the bus line LOW, or (b) let the bus default to logic 1. The pull-up resistors on the bus (both clock and data lines) establish a default logic 1. All bus devices generally have logic inputs to receive data.

Although the W127/W127-A is a receive-only device (no data write-back capability), it does transmit an “acknowledge” data pulse after each byte is received. Thus, the SDATA line can both transmit and receive data.

The pull-up resistor should be sized to meet the rise and fall times specified in AC parameters, taking into consideration total bus line capacitance.

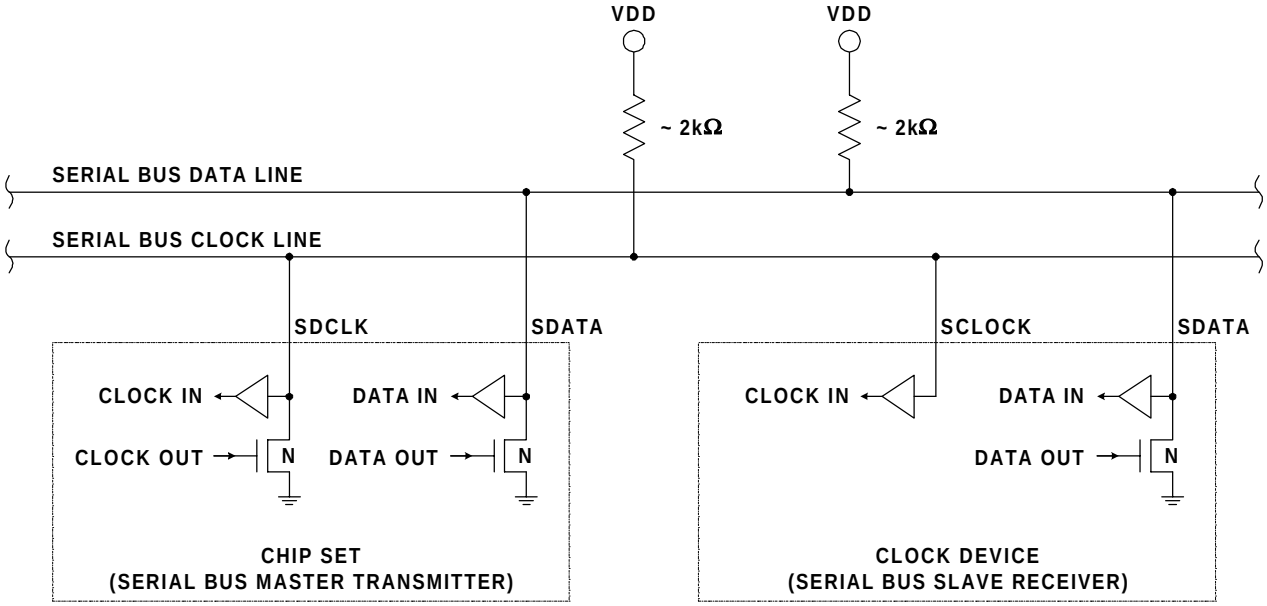


Figure 5. Serial Interface Bus Electrical Characteristics

Signaling Requirements

As shown in *Figure 6*, valid data bits are defined as stable logic 0 or 1 condition on the data line during a clock HIGH (logic 1) pulse. A transitioning data line during a clock HIGH pulse may be interpreted as a start or stop pulse (it will be interpreted as a start or stop pulse if the start/stop timing parameters are met).

A write sequence is initiated by a “start bit” as shown in *Figure 7*. A “stop bit” signifies that a transmission has ended.

As stated previously, the W127/W127-A sends an “acknowledge” pulse after receiving eight data bits in each byte as shown in *Figure 8*.

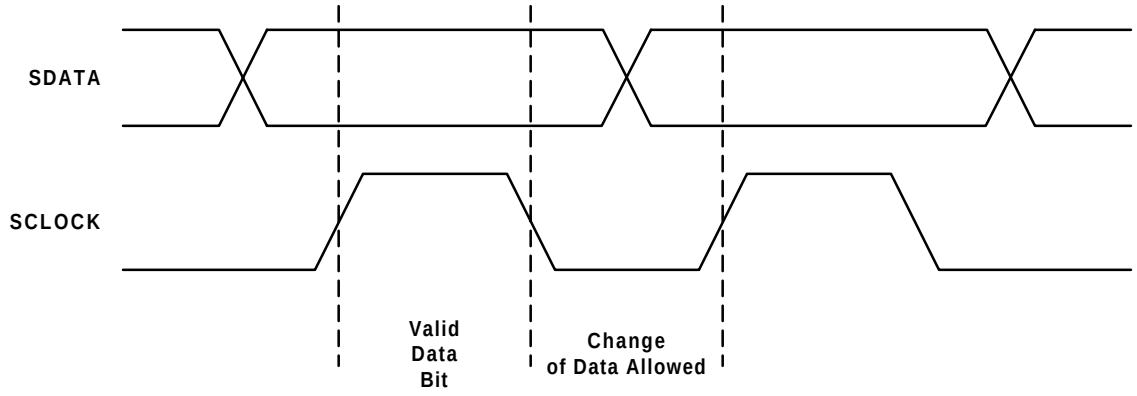


Figure 6. Serial Data Bus Valid Data Bit

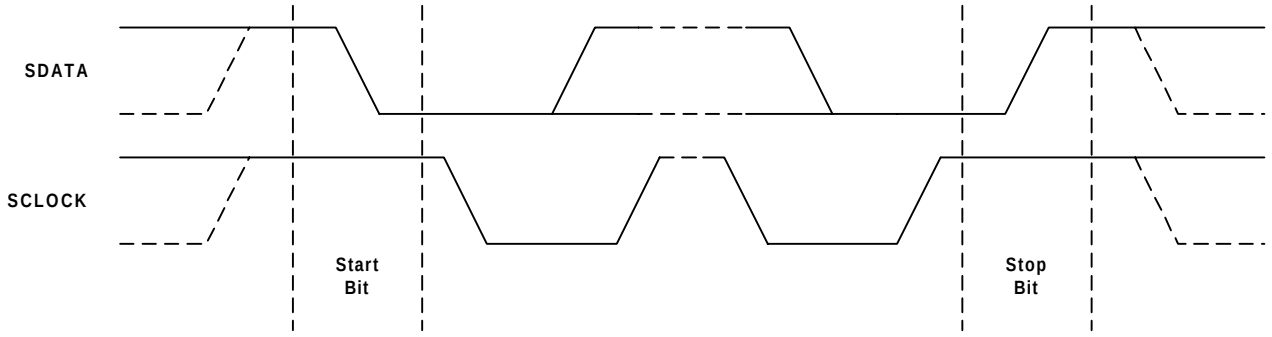


Figure 7. Serial Data Bus Start and Stop Bit

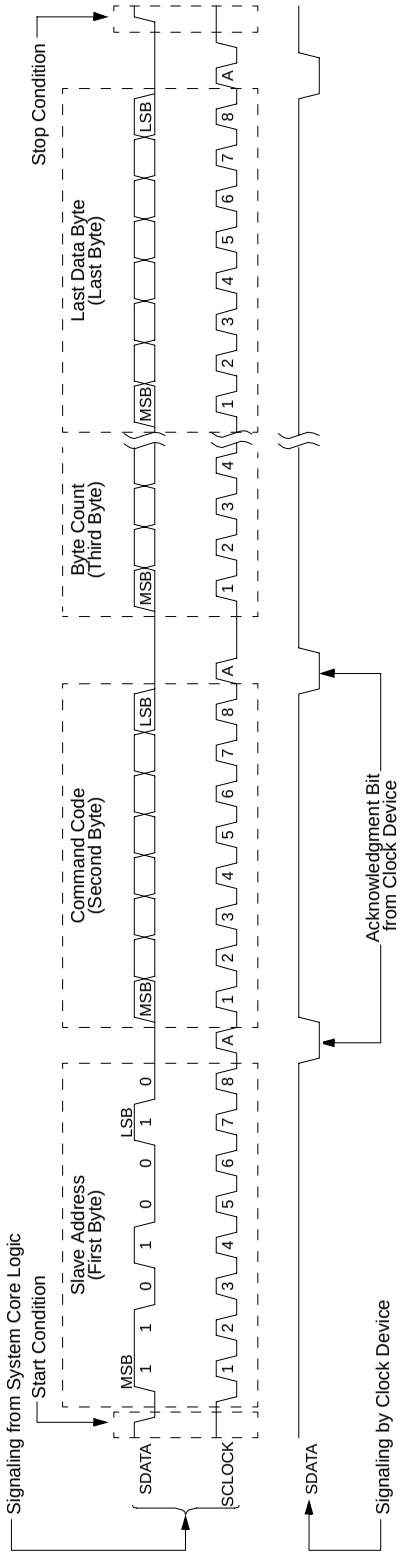


Figure 8. Serial Data Bus Write Sequence

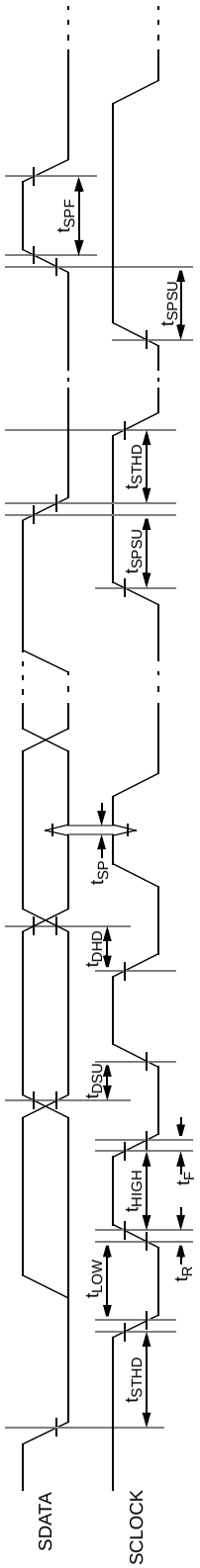


Figure 9. Serial Data Bus Timing Diagram

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DDQ3}, V_{IN}	Voltage on any Pin with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C
ESD_{PROT}	Input ESD Protection	2 (min.)	kV

3.3V DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DDQ3} = V_{DDQ2} = 3.3V±5% (3.135–3.465V)

Parameter	Description		Test Condition	Min.	Typ.	Max.	Unit
Supply Current							
I_{DD}	Combined 3.3V Supply Current		CPU0:3 = 66.6 MHz Outputs Loaded[5]		290		mA
Logic Inputs							
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.0			V
I_{IL}	Input Low Current[6]					20	µA
I_{IH}	Input High Current					5	µA
Clock Outputs							
V_{OL}	Output Low Voltage		I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage		I_{OH} = –1 mA	3.1			V
I_{OL}	Output Low Current	CPU0:3	V_{OL} = 1.5V	55	75	105	mA
		SDRAM0:11, AGP_F, AGP0		80	110	155	
		PCI_F, PCI0:4		55	75	105	
		REF		60	75	90	
		48/24MHz		55	75	105	
I_{OH}	Output High Current	CPU0:3	V_{OH} = 1.5V	55	85	125	mA
		SDRAM0:11, AGP_F, AGP0		80	120	175	
		PCI_F, PCI0:4		55	85	125	
		REF		60	85	110	
		48/24MHz		55	85	125	
Crystal Oscillator							
V_{TH}	X1 Input Threshold Voltage[7]				1.65		V
C_{LOAD}	Load Capacitance, Imposed on External Crystal[8]				20		pF
$C_{IN,X1}$	X1 Input Capacitance[9]		Pin X2 unconnected		30		pF

Notes:

5. All clock outputs loaded with maximum lump capacitance test load specified in AC Electrical Characteristics section.
6. W127/127-A logic inputs have internal pull-up devices (not full CMOS level).
7. X1 input threshold voltage (typical) is $V_{DD}/2$.
8. The W127/W127-A contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 20 pF; this includes typical stray capacitance of short PCB traces to crystal.
9. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

3.3V DC Electrical Characteristics (continued) T_A = 0°C to +70°C, V_{DDQ3} = V_{DDQ2} = 3.3V±5% (3.135–3.465V)

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH
Serial Input Port						
V_{IL}	Input Low Voltage	V_{DDQ3} = 3.3V			$0.3V_{DDQ3}$	V
V_{IH}	Input High Voltage	V_{DDQ3} = 3.3V	$0.7V_{DDQ3}$			V
I_{IL}	Input Low Current				10	µA
I_{IH}	Input High Current				10	µA
I_{OL}	Sink Current into SDATA or SCLOCK, Open Drain N-Channel Device On	$I_{OL} = 0.3(V_{DDQ3})$	6			mA
C_{IN}	Input Capacitance of SDATA and SCLOCK				10	pF
C_{SDATA}	Total Capacitance of SDATA Bus				400	pF
C_{SCLOCK}	Total Capacitance of SCLOCK Bus				400	pF

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5% (3.35–3.465V), f_{XTL} = 14.31818 MHz
Spread Spectrum function turned off

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

CPU AGP Clock Outputs, CPU0:3, AGP_F, AGP0 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6 MHz			Unit
			Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V	15			ns
f	Frequency, Actual	Determined by PLL divider ratio		66.6		MHz
t_H	High Time	Duration of clock cycle above 2.4V	5.2			ns
t_L	Low Time	Duration of clock cycle below 0.4V	5			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			250	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	10	15	20	Ω

AC Electrical Characteristics (continued)

SDRAM Clock Outputs, SDRAM0:11 (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6 MHz			Unit
			Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V	15			ns
f	Frequency, Actual	Determined by PLL divider ratio		66.6		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V		100		ps
t_{SK}	CPU to SDRAM Clock Skew	Covers all CPU/SDRAM outputs. Measured on rising edge at 1.5V.			500	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	10	15	20	Ω

PCI Clock Outputs, PCI_F and PCI0:4 (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6 MHz			Unit
			Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V	30			ns
f	Frequency, Actual	Determined by PLL divider ratio		33.3		MHz
t_H	High Time	Duration of clock cycle above 2.4V	12			ns
t_L	Low Time	Duration of clock cycle below 0.4V	12			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			250	ps
t_O	AGP to PCI Clock Skew	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.	1		3	ns
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20		Ω

AC Electrical Characteristics (continued)

REF Clock Output (Lump Capacitance Test Load = 45 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator		14.31818		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	40		60	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			1.5	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		30		Ω

48-/24-MHZ Clock Outputs (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Determined by PLL divider ratio (see m/n below)		48.008/24.004		MHz
f_D	Deviation from 48 MHz	(48.008 – 48)/48		+167		ppm
m/n	PLL Ratio	(14.31818 MHz x 57/17 = 48.008 MHz)		57/17, 54/34		
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		30	0	Ω

Serial Input Port

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
f_{SCLOCK}	SCLOCK Frequency	Normal Mode	0		100	kHz
t_{STHD}	Start Hold Time		4.0			µs
t_{LOW}	SCLOCK Low Time		4.7			µs
t_{HIGH}	SCLOCK High Time		4.0			µs
t_{DSU}	Data Set-up Time		250			ns
t_{DHD}	Data Hold Time	(Transmitter should provide a 300-ns hold time to ensure proper timing at the receiver.)	0			ns
t_R	Rise Time, SDATA and SCLOCK	From $0.3V_{DD}$ to $0.7V_{DD}$			1000	ns
t_F	Fall Time, SDATA and SCLOCK	From $0.7V_{DD}$ to $0.3V_{DD}$			300	ns
t_{STSU}	Stop Set-up Time		4.0			µs
t_{SPF}	Bus Free Time between Stop and Start Condition		4.7			µs
t_{SP}	Allowable Noise Spike Pulse Width				50	ns

Ordering Information

Ordering Code	Package Name	Package Type
W127	H	48-pin SSOP (300 mils)
W127-A		

Document #: 38-00893

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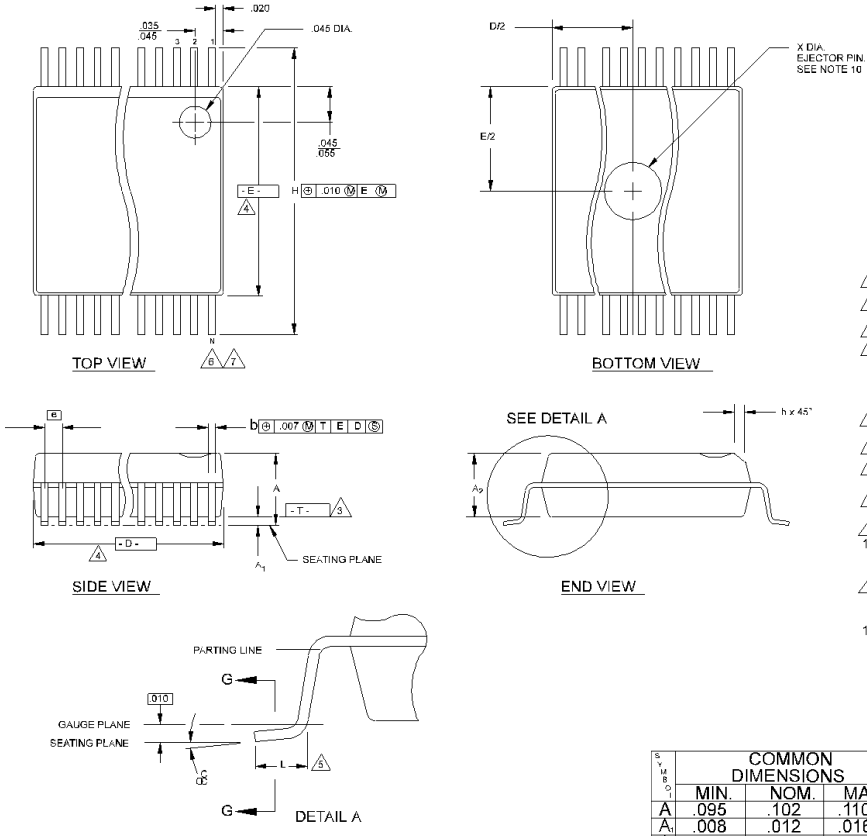
Package Diagram

48-Pin Small Shrink Outline Package (SSOP, 300 mils)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. CONTROLLING DIMENSION: INCHES.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015"/.025".

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE 4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	.095	.102	.110		AA	.620	.625	.630	48
A_1	.008	.012	.016		AB	.720	.725	.730	56
A_2	.088	.090	.092						
b	.008	.010	.0135						
b_1	.008	.010	.012						
c	.005	-	.010						
c_1	.005	.006	.0085						
D	SEE VARIATIONS			4					
E	.292	.296	.299						
e	.025 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			6					
X	.085	.093	.100	10					
α	0°	5°	8°						

THIS TABLE IN INCHES

Summary of nominal dimensions in inches:

Body Width: 0.296
Lead Pitch: 0.025
Body Length: 0.625
Body Height: 0.102

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE 4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	2.41	2.59	2.79		AA	15.75	15.88	16.00	48
A_1	0.20	0.31	0.41		AB	18.29	18.42	18.54	56
A_2	2.24	2.29	2.34						
b	0.203	0.254	0.343						
b_1	0.203	0.254	0.305						
c	0.127	-	0.254						
c_1	0.127	0.152	0.216						
D	SEE VARIATIONS			4					
E	7.42	7.52	7.59						
e	0.635 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			6					
X	2.16	2.36	2.54	10					
α	0°	5°	8°						

THIS TABLE IN MILLIMETERS

Addendum: W127/W127-A Replaces W48S87-27A

The W127/W127-A is a pin-compatible replacement for the W48S87-27A with the following output frequency modifications (Refer to *Table 1*):

1. The 90-MHz CPU operation is changed to 95.25-MHz to support the K6 333-MHz chipset.
2. The 60-MHz CPU operation is changed to 124-MHz to support new motherboard designs.

Revision History

Document Title: W127/W127-A Document Number: 38-00893				
REV.	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
0.4	--	--	?	1. Revision Control established
0.90	--	--	?	1. Distinguished between standard W127 device and high-performance W127-A option (see *Table 1*)
**			IKA	1. Converted to Cypress template, entered into DCON system