National Semiconductor

MILITARY DATA SHEET

MN100336-X REV 2A0

Original Creation Date: 10/30/95
Last Update Date: 10/21/96
Last Major Revision Date: 10/16/96

4-STAGE COUNTER/SHIFT REGISTER

General Description

The F100336 operates as either a modulo-16 up/down counter or as a 4-bit bidirectional shift register. Three Select (Sn) inputs determine the mode of operation, as shown in the Function Select table. Two Count Enable ($\overline{CEP}$, $\overline{CET}$) inputs are provided for ease of cascading in multistage counters. One Count Enable ($\overline{CET}$) input also doubles as a Serial Data (Do) Input for shift-up operation. For shift-down operation D3 is the Serial Data input. In counting operations the Terminal Count ($\overline{TC}$) output goes LOW when the counter reaches 15 in the count/up mode or 0 (zero) in the count/down mode. In the shift modes, the $\overline{TC}$ output repeats the Q3 output. The dual nature of this $\overline{TC}$/Q3 output and Do/$\overline{CET}$ input means that one interconnection from one stage to the next higher stage serves as the link for multistage counting or shift-up operation. The individual Preset (Pn) inputs are used to enter data in parallel or to preset the counter in programmable counter applications. A HIGH signal on the Master Reset (MR) input overrides all other inputs and asynchronously clears the flip-flops. In addition, a synchronous clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops. All inputs have 50K ohm pull-down resistors.

Industry Part Number

100336

Prime Die

F336

NS Part Numbers

100336DMQB
100336FMQB
100336J-QMLV
100336W-QMLV

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 40% power reduction of the 100136
- 2000V ESD protection
- Pin/Function compatible with 100136
- Voltage compensated operating range= -4.2V to -5.7V
- Available to industrial grade temperatue range
- Available to MIL-STD-883

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature (Tstg)	−65C to +150C
Maximum Junction Temperature (Tj)	
Ceramic	+175C
Plastic	+150C
Vee Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	Vee to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (Tc)	
Commercial	0 C to +85 C
Industrial	−40 C to +85C
Military	−55C to +125C
Supply Voltage (Vee)	−5.7V to −4.2V

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vee Range: -4.2V to -5.7V, Tc= -55C to +125C, VCC=VCCA=GND

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	Input HIGH Current	VEE=-5.7V, VM=-0.87V	1, 3	INPUTS		240	uA	1, 2
			1, 3	INPUTS		340	uA	3
IIL	Input Low Current	VEE=-4.2V, VM=-1.83V	1, 3	INPUTS	0.5		uA	1, 2, 3
VOH	Output HIGH Voltage	VEE=-4.2V/-5.7V, VIH=-0.87V, VIL=-1.83V, LOADING: 50 Ohms to -2.0V	1, 3	OUTPUTS	-1025	-870	mV	1, 2
			1, 3	OUTPUTS	-1085	-870	mV	3
VOL	Output LOW Voltage	Vee=-4.2V/-5.7V, VIH=-0.87, VIL=-1.83V, LOADING: 50 Ohms to -2.0V	1, 3	OUTPUTS	-1830	-1620	mV	1, 2
			1, 3	OUTPUTS	-1830	-1555	mV	3
VOHC	Output HIGH Voltage Corner Point High	Vee=-4.2V/-5.7V, VIH=-1.165V, VIL=-1.475V, Loading: 50 Ohms to-2.0V	1, 3	OUTPUTS	-1035		mV	1, 2
			1, 3	OUTPUTS	-1085		mV	3
VOLC	Output LOW Voltage Corner Point High	Vee=-4.2V/-5.7V, VIH=-1.165V, VIL=-1.475V, Loading: 50 Ohms to-2.0V	1, 3	OUTPUTS		-1610	mV	1, 2
			1, 3	OUTPUTS		-1555	mV	3
VIH	Input HIGH Voltage		1, 3, 7	INPUTS	-1165	-870	mV	1, 2, 3
VIL	Input LOW Voltage		1, 3, 7	INPUTS	-1830	-1475	mV	1, 2, 3
IEE	Power Supply Current	VEE=-4.2/-4.8V/-5.7V	1, 3	VEE	-185	-70	mA	1, 2, 3

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: VEE Range: -4.2V to -5.7V, VCC=VCCA=GND, Loading:50 Ohms to -2.0V

tpLH/tpHL(1)	Propagation Delay	VEE=-4.2/-5.7V	2, 4	CP to Qn/$\overline{Qn}$	0.4	2.2	ns	9
			2, 4	CP to Qn/$\overline{Qn}$	0.4	2.5	ns	10
			2, 4	CP to Qn/$\overline{Qn}$	0.4	2.3	ns	11
tPLH/tPHL(2)	Propagation Delay	VEE=-4.2/-5.7V (SHIFT MODE)	2, 4	CP to $\overline{TC}$	1.7	3.8	ns	9
			2, 4	CP to $\overline{TC}$	1.7	4.2	ns	10
			2, 4	CP to $\overline{TC}$	1.3	3.9	ns	11

Electrical Characteristics

AC PARAMETERS (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: VEE Range: -4.2V to -5.7V, VCC=VCCA=GND, Loading:50 Ohms to -2.0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPLH/tPHL(3)	Propagation Delay	VEE=-4.2/-5.7V (COUNT MODE)	2, 4	CP TO $\overline{TC}$	1.5	4.6	ns	9
			2, 4	CP TO $\overline{TC}$	1.6	5.2	ns	10
			2, 4	CP TO $\overline{TC}$	1.2	4.6	ns	11
tPLH/tPHL(4)	Propagation Delay	VEE=-4.2/-5.7V	2, 4	MR to Qn/$\overline{Qn}$	0.8	2.8	ns	9
			2, 4	MR to Qn/$\overline{Qn}$	0.9	3.2	ns	10
			2, 4	MR to Qn/$\overline{Qn}$	0.6	2.9	ns	11
tPLH/tPHL(5)	Propagation Delay	VEE=-4.2/-5.7V (COUNT MODE)	2, 4	MR to $\overline{TC}$	2.7	5.2	ns	9
			2, 4	MR to $\overline{TC}$	2.9	5.9	ns	10
			2, 4	MR to $\overline{TC}$	2.3	5.2	ns	11
tPHL	Propagation Delay	VEE=-4.2/-5.7V (SHIFT MODE)	2, 4	MR to $\overline{TC}$	2.2	4.1	ns	9
			2, 4	MR to $\overline{TC}$	2.4	4.7	ns	10
			2, 4	MR to $\overline{TC}$	2.1	4.3	ns	11
tPLH/tPHL(6)	Propagation Delay	VEE=-4.2/-5.7V	2, 4	D0/$\overline{CET}$ to $\overline{TC}$	1.0	3.2	ns	9
			2, 4	D0/$\overline{CET}$ to $\overline{TC}$	1.3	4.1	ns	10
			2, 4	D0/$\overline{CET}$ to $\overline{TC}$	0.7	3.2	ns	11
tPLH/tPHL(7)	Propagation Delay	VEE=-4.2/-5.7V	2, 4	Sn to $\overline{TC}$	1.5	4.2	ns	9
			2, 4	Sn to $\overline{TC}$	1.7	4.9	ns	10
			2, 4	Sn to $\overline{TC}$	1.3	4.1	ns	11
tTLH/tTHL	Transistion Time	VEE=-4.2/-5.7V	6	Qn/$\overline{Qn}$	0.2	1.8	ns	9
			6	Qn/$\overline{Qn}$	0.2	2.0	ns	10
			6	Qn/$\overline{Qn}$	0.2	1.9	ns	11

Electrical Characteristics

AC PARAMETERS (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: VEE Range: -4.2V to -5.7V, VCC=VCCA=GND, Loading:50 Ohms to -2.0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tS(1)	Setup Time	VEE=-4.2/-5.7V	6	D3 to CP	1.4		ns	9, 10, 11
tS(2)	Setup Time	VEE=-4.2/-5.7V	6	Pn to CP	1.7		ns	9, 10, 11
tS(3)	Setup Time	VEE=-4.2/-5.7V	6	D0/$\overline{\text{CET}}$ to CP	1.8		ns	9, 10, 11
tS(4)	Setup Time	VEE=-4.2/-5.7V	6	$\overline{\text{CEP}}$ to CP	1.8		ns	9, 10, 11
tS(5)	Setup Time	VEE=-4.2/-5.7V	6	Sn to CP	3.3		ns	9, 10, 11
tS(6)	Setup Time	VEE=-4.2/-5.7V	6	MR to CP	2.6		ns	9, 10, 11
tH(1)	Hold Time	VEE=-4.2/-5.7V	6	D3 to CP	0.9		ns	9, 10, 11
tH(2)	Hold Time	VEE=-4.2/-5.7V	6	Pn to CP	1.0		ns	9, 10, 11
tH(3)	Hold Time	VEE=-4.2/-5.7V	6	D0/$\overline{\text{CET}}$ to CP	0.7		ns	9, 10, 11
tH(4)	Hold Time	VEE=-4.2/-5.7V	6	$\overline{\text{CEP}}$ to CP	0.6		ns	9, 10, 11
tH(5)	Hold Time	VEE=-4.2/-5.7V	6	Sn to CP	0.0		ns	9, 10, 11
tPW(1)	Pulse Width	VEE= -4.2/-5.7V	6	CP	1.6		ns	9, 10, 11
tPW(2)	Pulse Width	VEE= -4.2/-5.7V	6	MR	2.0		ns	9, 10, 11
fSHIFT/fCOUNT	Shift Frequency	VEE= -4.2/-5.7V	6	CP	325		MHz	9, 10, 11

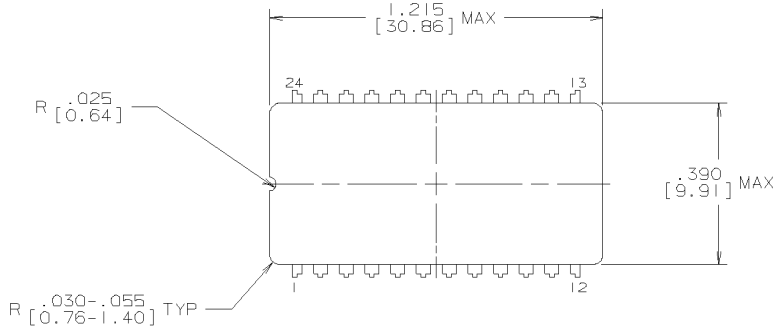
Note 1: Screen tested 100% on each device at -55 C, +25 C and +125 C temp., subgroups 1, 2, 3, 7 & 8.
Note 2: For QB devices, screen tested 100% on each device at +25C temperature only, subgroup A9. For QMLV devices, screen tested 100% on each device at +25C, +125C & -55C temperature, subgroups A9, 10 & 11.
Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, +125 C & -55 C temp., subgroups A1, 2, 3, 7 & 8.
Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, subgroup A9, and at +125 C & -55 C temp., subgroups A10 & 11.
Note 5: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C temp. only, subgroup A9.
Note 6: Not tested at +25 C, +125 C & -55 C temp. (DESIGN CHARACTERIZATION DATA).
Note 7: Guaranteed by applying specified input condition and testing VOH/VOL.

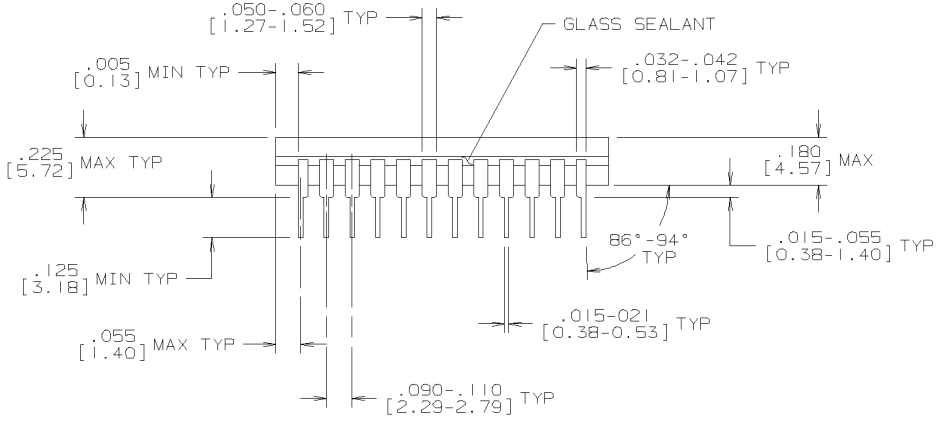
Graphics and Diagrams

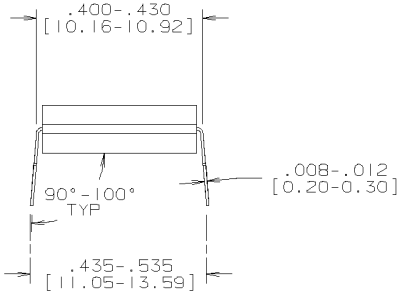
GRAPHICS#	DESCRIPTION
J24ERJ	CERDIP(J), 24LD .400 CENTERS (P/P DWG)
P000070A	CERDIP (J), 24LD .400 CENTERS (PIN OUT)
P000071A	CERPAC, QUAD, 24 LEAD (PIN OUT)
W24BRE	CERPAC, QUAD, 24 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
J	REVISE AND REDRAW	09044	03/05/92	DEG/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES/5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. LEAD THICKNESS MAY BE INCREASED BY .003 [0.08] MAXIMUM AFTER LEAD FINISH APPLIED.
3. BUMPERS ARE AVAILABLE ON CERTAIN PRODUCTS. BUMPERS WILL ADD .040 [1.02] MAX TO THE LENGTH OF THE PACKAGE.
4. NO JEDEC REGISTRATION AS OF 2/17/92.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN D.E.GRADY	03/05/92
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J),
24 LEAD,
.400 CENTERS

PROJECTION
INCH
MM

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-J24E	J

FORMERLY: N/A

SHEET 1 OF 1