Beckman® Series 7521M CMOS, 12-BIT MULTIPLYING D/A CONVERTERS

Effective date: October, 1977

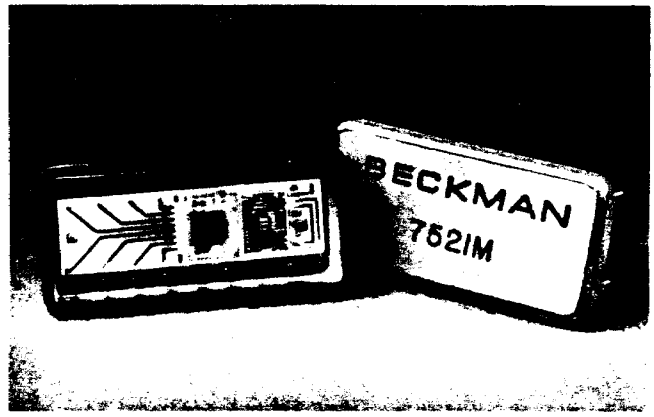
Series 7521M are 12-bit multiplying D/A converters designed for military, aerospace and other applications demanding high performance over environmental extremes of temperature, shock, vibration and humidity. They are hermetically sealed in a standard 18-pin metal dual in-line package and provide true 12-bit accuracy over the full −55°C to +125°C temperature range.

Series 7521M are compatible with TTL and CMOS logic, and with the addition of external amplifiers enable unipolar or bipolar operation. The converters operate from +5 to +15 volt power supplies, and consume only 20 mW of power.

Series 7521M features:

- 12-bit accuracy and resolution for uncompromised −55°C to +125°C operation.
- Guaranteed ± ½ LSB linearity over the full temperature range.
- 1 LSB gain and offset error over the −55°C to +125°C range.
- 20mW dissipation to enable operation in low-power, portable or airborne system.
- Direct interface with TTL and CMOS logic families.
- Material, construction and workmanship to MIL-STD-883 Method 2017 level B.
- Pin-for-pin compatibility with AD7521.

The 7521M can directly replace competitive models thereby improving system performance by a factor of four, 0.012% FSR non-linearity instead of 0.05%. No other system changes are required.



Operation

Series 7521M consists of a CMOS integrated circuit, a thin film resistor network and a zener diode. The CMOS IC provides 12 parallel inputs with level shifters, two compensation transistors and 12 current steering switches. As shown in Figure 1, each 2R leg of an inverted R-2R ladder is connected to a pair of N-channel transistors. These transistors switch the binary weighted currents that flow in each 2R leg to either the $I_{OUT\ 1}$ bus (logic high input) or to the $I_{OUT\ 2}$ bus (logic low input). Normal operation maintains $I_{OUT\ 1}$ and $I_{OUT\ 2}$ at ground or virtual ground.

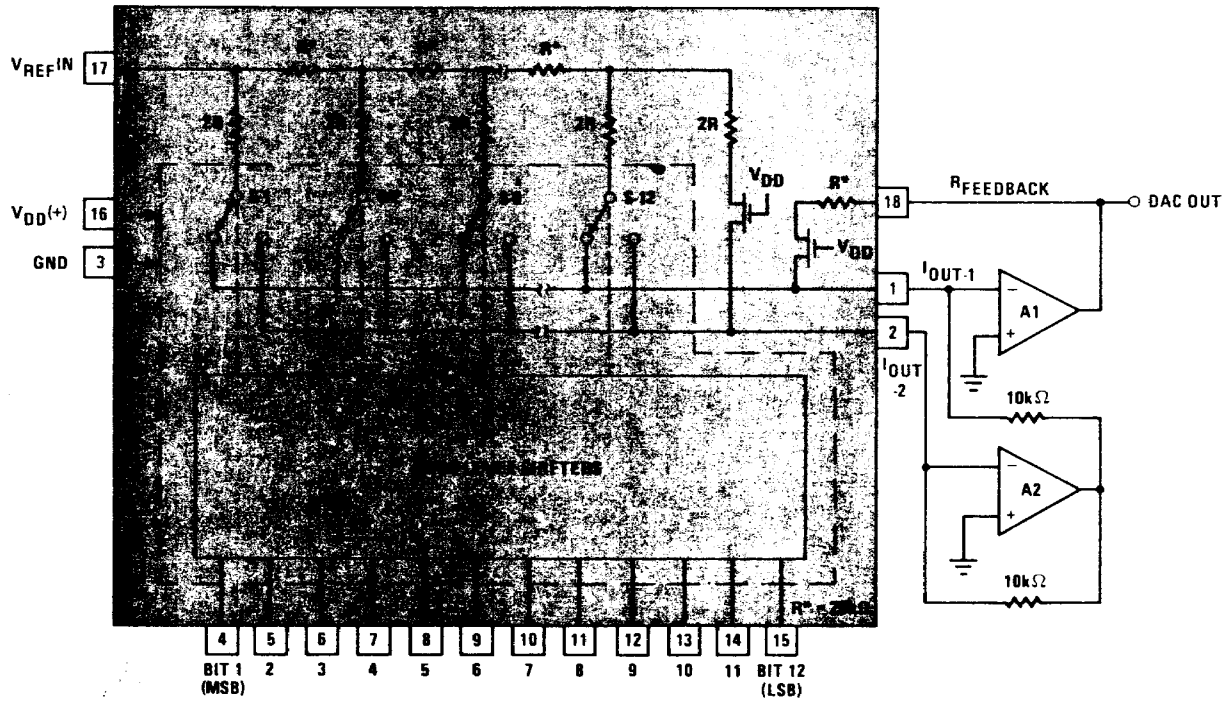


Figure 1—7521M D/A Converter Block Diagram. Bipolar operation is provided by external amplifiers A1 and A2.

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Internal Compensation

The "on" resistance of the MOS transistor switches are binary weighted with the MSB set at 25 ohms. The linearity of the DAC is dependent upon the ratio accuracies of the switch resistances and not upon their absolute values. Excellent switch ratio tolerances account for small linearity errors even over the operating temperature range of the DAC. Also, the low power density in the switching transistors eliminates transient thermal gradients normally encountered with bipolar current switches.

Feedback gain compensation for switch resistance is provided by an "on" switch in series with the internal "R" feedback resistor. This compensation transistor reduces gain drift errors to less than 2 p/10°/°C and provides outstanding power supply rejection.

A second compensation transistor (unique to Series 7521M) compensates the R-2R ladder terminating resistor, thereby eliminating the requirement for the external 10MΩ compensating resistor required by competitive models in the bipolar configuration. When replacing competitive units with the 7521M, the 10MΩ resistor can simply be removed from the board without changing the board layout.

Unipolar Operation

Figure 2 shows the circuit connection required for unipolar operation. Table I gives the input code/output relationship. Series 7521M is internally preset to an initial full scale gain accuracy of ±0.1%. The resistor R1 and R2 shown in Figure 2 are required only when system gain adjustment is required or when a more precise initial setting is required. If external gain adjustment is used, it is normally set after adjustment of the external amplifier's zero offset.

Zero Offset Adjustment—With all bits set to "0," adjust the external amplifier (A1) offset to zero. (A zero offset appearing at the summing function will produce a linearity error, therefore, the output should be adjusted to zero by a method that will set the summing junction to zero.)

Gain Adjustment—Set R1 and R2 to zero (Figure 2) and turn all bits to "1." If the output is greater than required full scale value, increase R1. If the output is less than required full scale value, increase R2.

Bipolar Operation

Figure 3 shows the circuit connections required for bipolar operation. Table II gives the input code/output relationship.

Zero Offset Adjustment—Adjust the amplifier offsets of A1 and A2 to zero.

Gain Adjustment—Set all inputs to "0." Set R1 and R2 to zero. If the output is greater than V_{REF}, increase R1 until the output equals V_{REF}. If the output is less than V_{REF}, increase R2 until it equals V_{REF}.

Absolute Maximum Ratings

VDD	±17 Volts
V_{REF}	±25 Volts
$I_{OUT\,1}$, $I_{OUT\,2}$	−100mV to VDD
Digital Input Voltage Range	VDD to GND
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Operation Cautions

Do not apply voltages higher than VDD or less than GRD potential to any other input or output terminal except V_{REF} or $R_{FEEDBACK}$.

Construction

Series 7521M D-to-A Converters utilize cermet thick film conductors fired to an alumina substrate. Interconnections between these conductors, the thin film resistor network, and the CMOS IC are made by thermal compression gold wire bonding. The completed hybrid substrate is mounted on a gold plated Kovar* header, and the circuit I/O leads are wire bonded to the terminal pins.

*Kovar is a registered trademark of Westinghouse Electric Corp.

Table I—Unipolar Code Table

MSB Digital Input LSB	Analog Output
1 1 1 . . . . . 1 1 1	$-V_{REF}(1 - 2^{-12})$
1 0 0 . . . . . 0 0 1	$-V_{REF}(\frac{1}{2} + 2^{-12})$
1 0 0 . . . . . 0 0 0	$-V_{REF/2}$
0 1 1 . . . . . 1 1 1	$-V_{REF}(\frac{1}{2} - 2^{-12})$
0 0 0 . . . . . 0 0 1	$-V_{REF}(2^{-12})$
0 0 0 . . . . . 0 0 0	0

Table II—Bipolar Code Table

MSB Digital Input LSB	Analog Output
1 1 1 . . . . . 1 1 1	$-V_{REF}(1 - 2^{-11})$
1 0 0 . . . . . 0 0 1	$-V_{REF}(2^{-11})$
1 0 0 . . . . . 0 0 0	0
0 1 1 . . . . . 1 1 1	$V_{REF}(2^{-11})$
0 0 0 . . . . . 0 0 1	$V_{REF}(1 - 2^{-11})$
0 0 0 . . . . . 0 0 0	V_{REF}

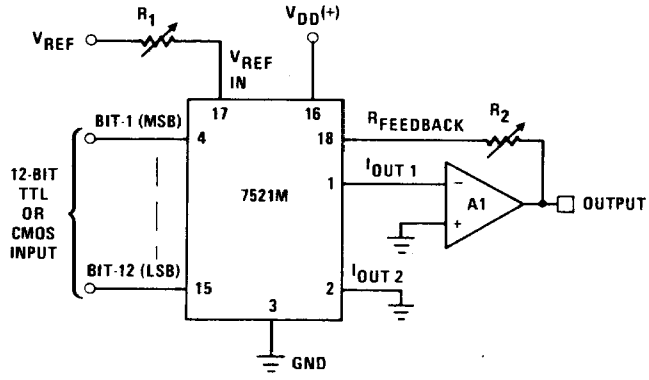

Figure 2—Unipolar Operation

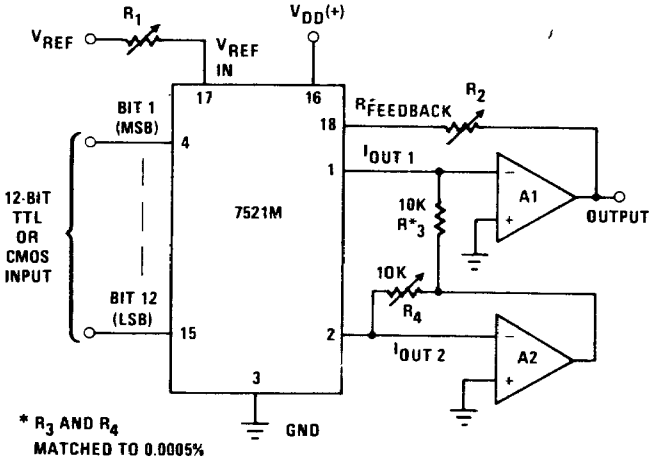

Figure 3—Bipolar Operation

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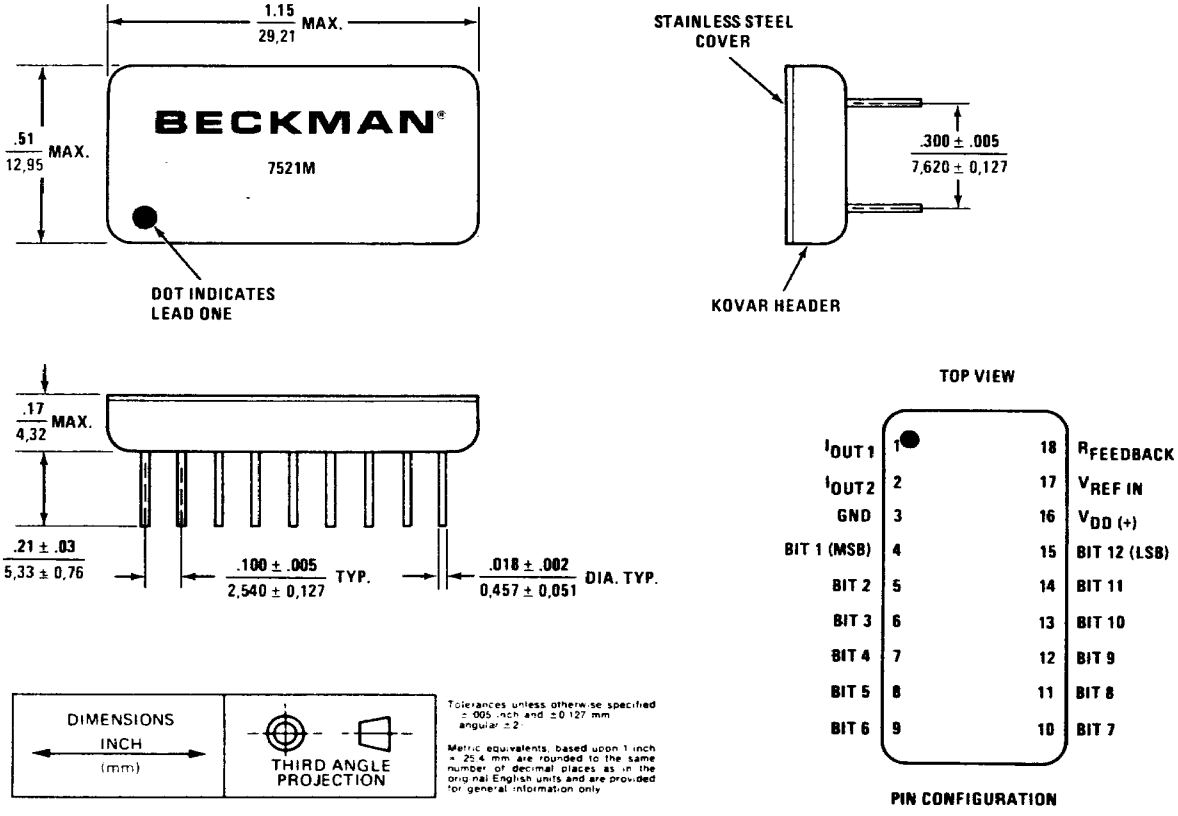
Table III—Performance Specifications

Parameters			Conditions	Minimum	Typical	Maximum	Units
Transfer Characteristics (Note 1)	Resolution					12	bits
	Nonlinearity		$-55°C \le T_C \le +125°C$			±0.012	% FSR
	Differential Nonlinearity		$-55°C \le T_C \le +125°C$		±0.012		% FSR
	Gain Error (Note 2)		$-55°C \le T_C \le +125°C$			±0.2	% FSR
	Gain Error Tempco (Note 2)		$-55°C \le T_C \le +125°C$		±1	±2	p/10⁶/°C
	Reference Feedthrough		VREF = 20V p-p; 10KHz		1	10	mV p-p
	Settling Time		To 0.01% of FSR for a FSR Step		2		μs
Reference Input	Reference Input Range					±10	V
	Input Resistance				20		kΩ
Analog Output	Output Capacitance	CO1	All Data Bits High		200		pF
		CO2	All Data Bits High		150		pF
		CO1	All Data Bits Low		125		pF
		CO2	All Data Bits Low		70		pF
	Output Leakage Current (I01, I02)		$-55°C \le T_C \le +125°C$			100	nA
Digital Input Characteristics	TTL Logic Levels	Logic "1" Voltage		3			V
		Logic "0" Voltage				0.8	V
		Input Leakage Current I_{IL}, I_{IH}	Any Input		$+10^{-5}$	+1	μA
Power Supply	IDD				1	2	mA
	VDD Rejection (DC)				10		p/10⁶/FSR/%
	Total Dissipation (Including ladder)				20		mW

Unless otherwise specified, specifications apply to VDD = +15V, VREF = ±10V. Specifications apply over a temperature range of $-55°C \le T_C \le +125°C$. Typical values shown are for $T_C = 25°C$.

Notes: 1. Full scale range (FSR) is 10V for unipolar mode and ±10V for bipolar mode.
2. Using the internal $R_{FEEDBACK}$ resistor.

Outline Drawing



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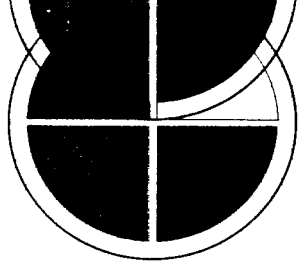

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