CRYSTAL
Semiconductor Corporation

CS5501
CS5503

Low-Cost, 16 & 20-Bit Measurement A/D Converter

Features

- Monolithic CMOS ADC with Filtering
  6-Pole, Low-Pass Gaussian Filter
- Up to 4kHz Output Word Rates
- On Chip Self-Calibration Circuitry
  - Linearity Error: ±0.0003%
  - Differential Nonlinearity:
    CS5501: 16-Bit No Missing Codes
    (DNL ±1/8LSB)
    CS5503: 20-Bit No Missing Codes
- System Calibration Capability
- Flexible Serial Communications Port
  - μC-Compatible Formats
  - 3-State Data and Clock Outputs
  - UART Format (CS5501 only)
- Pin-Selectable Unipolar/Bipolar Ranges
- Low Power Consumption: 25mW
  - 10μW Sleep Mode for Portable Applications
- Evaluation Boards Available

General Description

The CS5501 and CS5503 are low-cost CMOS A/D converters ideal for measuring low-frequency signals representing physical, chemical, and biological processes. They utilize charge-balance techniques to achieve 16-bit (CS5501) and 20-bit (CS5503) performance with up to 4kHz word rates at very low cost.

The converters continuously sample at a rate set by the user in the form of either a CMOS clock or a crystal. On-chip digital filtering processes the data and updates the output register at up to a 4kHz rate. The converters' low-pass, 6-pole Gaussian response filter is designed to allow corner frequency settings from .1Hz to 10Hz in the CS5501 and .5Hz to 10Hz in the CS5503. Thus, each converter rejects 50Hz and 60Hz line frequencies as well as any noise at spurious frequencies.

The CS5501 and CS5503 include on-chip self-calibration circuitry which can be initiated at any time or temperature to insure offset and full-scale errors of typically less than 1/2 LSB for the CS5501 and less than 4LSB for the CS5503. The devices can also be applied in system calibration schemes to null offset and gain errors in the input channel.

Each device's serial port offers two general purpose modes of operation for direct interface to shift registers or synchronous serial ports of industry-standard microcontrollers. In addition, the CS5501's serial port offers a third, UART-compatible mode of asynchronous communication.

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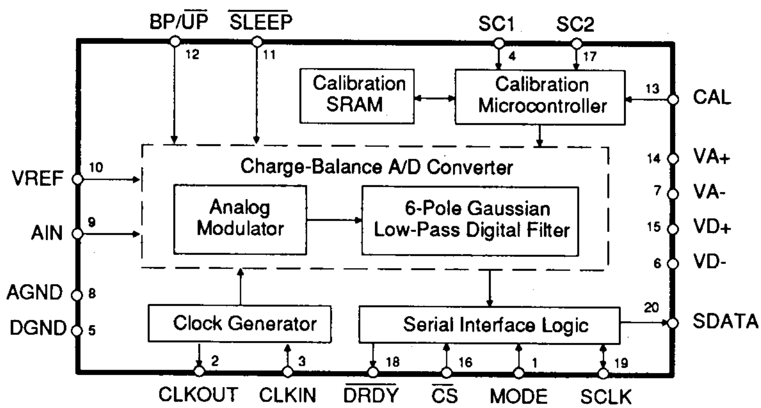

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CS5501 ANALOG CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 2.5V; CLKIN = 4.096MHz; Bipolar Mode; MODE = +5V; R_{source} = 750Ω with a 1nF to AGND at AIN (see Note 1); Digital Inputs: Logic 0 = GND; Logic 1 = VD+; unless otherwise specified.)

Parameter*		CS5501-A,B,C Min	Typ	Max	CS5501-S,T Min	Typ	Max	Units
Specified Temperature Range			-40 to +85			-55 to +125		°C
Accuracy								
Linearity Error	-A,S	-	0.0015	0.003	-	-	0.003	±%FS
	-B,T	-	0.0007	0.0015	-	0.0007	0.0015	±%FS
	-C	-	0.0003	0.0012				±%FS
Differential Nonlinearity	T_{MIN} to T_{MAX}	-	±1/8	±1/2	-	±1/8	±1/2	LSB_{16}
Full Scale Error	(Note 2)	-	±0.13	±0.5	-	±0.13	±0.5	LSB_{16}
Full Scale Drift	(Note 3)	-	±1.2	-	-	±2.3	-	LSB_{16}
Unipolar Offset	(Note 2)	-	±0.25	±1	-	±0.25	±1	LSB_{16}
Unipolar Offset Drift	(Note 3)	-	±4.2	-	-	+3.0 -25.0	-	LSB_{16}
Bipolar Offset	(Note 2)	-	±0.25	±1	-	±0.25	±1	LSB_{16}
Bipolar Offset Drift	(Note 3)	-	±2.1	-	-	+1.5 -12.5	-	LSB_{16}
Bipolar Negative Full Scale Error	(Note 2)	-	±0.5	±2	-	±0.5	±2	LSB_{16}
Bipolar Negative Full Scale Drift	(Note 3)	-	±0.6	-	-	±1.2	-	LSB_{16}
Noise (Referred to Output)		-	1/10	-	-	1/10	-	LSBrms (16)

Notes: 1. The AIN pin presents a very high input resistance at dc and a minor dynamic load which scales to the master clock frequency. Both source resistance and shunt capacitance are therefore critical in determining the CS5501's source impedance requirements. For more information refer the text section *Analog Input Impedance Considerations.*

2. Applies after calibration at the temperature of interest.
3. Total drift over the specified temperature range since calibration at power-up at 25°C (see Figure 11). This is guaranteed by design and /or characterization. Recalibration at any temperature will remove these errors.

	Unipolar Mode			Bipolar Mode		
µV	LSB's	%FS	ppm FS	LSB's	%FS	ppm FS
10	0.26	0.0004	4	0.13	0.0002	2
19	0.50	0.0008	8	0.26	0.0004	4
38	1.00	0.0015	15	0.50	0.0008	8
76	2.00	0.0030	30	1.00	0.0015	15
152	4.00	0.0061	61	2.00	0.0030	30

CS5501 Unit Conversion Factors, VREF = 2.5V

* Refer to the Specification Definitions immediately following the Pin Description Section.

CS5503 ANALOG CHARACTERISTICS

($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 2.5V; CLKIN = 4.096MHz; Bipolar Mode; MODE = +5V; R_{source} = 750Ω with a 1nF to AGND at AIN (see Note 1): unless otherwise specified.)

Parameter*		CS5503-A,B,C Min	Typ	Max	CS5503-S,T Min	Typ	Max	Units
Specified Temperature Range			-40 to +85			-55 to +125		°C
Accuracy								
Linearity Error	-AS	-	0.0015	0.003	-	-	0.003	±%FS
	-B,T	-	0.0007	0.0015	-	0.0007	TBD	±%FS
	-C	-	0.0003	0.0012				±%FS
Differential Nonlinearity (No Missing Codes)	T_{MIN} to T_{MAX}	-	20	-	-	20	-	Bits
Full Scale Error (Note 2)		-	±4	±16	-	±4	±16	LSB_{20}
Full Scale Drift (Note 3)		-	±19	-	-	±37	-	LSB_{20}
Unipolar Offset (Note 2)		-	±4	±16	-	±4	±16	LSB_{20}
Unipolar Offset Drift	(Note 3)	-	±67	-	-	+48 -400	-	LSB_{20}
Bipolar Offset (Note 2)		-	±4	±16	-	±4	±16	LSB_{20}
Bipolar Offset Drift	(Note 3)	-	±34	-	-	+24 -200	-	LSB_{20}
Bipolar Negative Full Scale Error	(Note 2)	-	±8	±32	-	±8	±32	LSB_{20}
Bipolar Negative Full Scale Drift	(Note 3)	-	±10	-	-	±20	-	LSB_{20}
Noise (Referred to Output)		-	1.6	-	-	1.6	-	LSBrms (20)

µV	Unipolar Mode LSB's	%FS	ppm Fs	Bipolar Mode LSB's	%FS	ppm FS
0.596	0.25	0.0000238	0.24	0.13	0.0000119	0.12
1.192	0.50	0.0000477	0.47	0.26	0.0000238	0.24
2.384	1.00	0.0000954	0.95	0.50	0.0000477	0.47
4.768	2.00	0.0001907	1.91	1.00	0.0000954	0.95
9.537	4.000	0.0003814	3.81	2.00	0.0001907	1.91

CS5503 Unit Conversion Factors, VREF = 2.5V

* Refer to the Specification Definitions immediately following the Pin Description Section.

ANALOG CHARACTERISTICS (Continued)

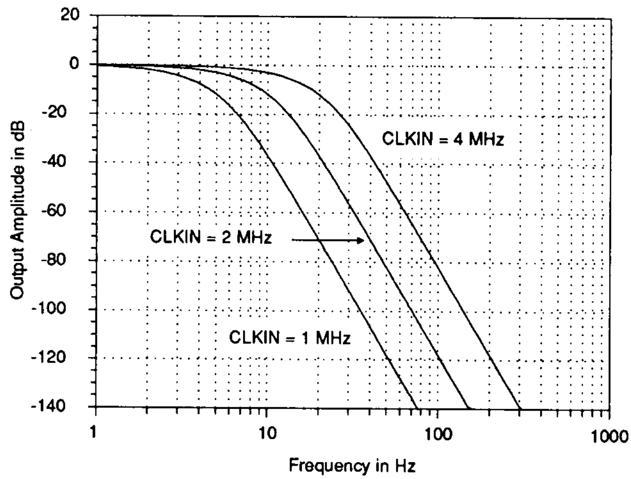
Parameter		CS5501/3-A,B,C Min	Typ	Max	CS5501/3-S,T Min	Typ	Max	Units
Power Supplies								
DC Power Supply Currents								
IA+		-	2	3.2	-	2	3.2	mA
IA-		-	2	3.2	-	2	3.2	mA
ID+		-	1	1.5	-	1	1.5	mA
ID-	(Note 4)	-	0.03	0.1	-	0.03	0.1	mA
Power Dissipation								
$\overline{\text{SLEEP}}$ High		-	25	40	-	25	40	mW
$\overline{\text{SLEEP}}$ Low	(Note 4)	-	10	20	-	10	40	µW
Power Supply Rejection								
Positive Supplies		-	70	-	-	70	-	dB
Negative Supplies	(Note 5)	-	75	-	-	75	-	dB
Analog Input								
Analog Input Range								
Unipolar			0 to +2.5			0 to +2.5		V
Bipolar			±2.5			±2.5		V
Input Capacitance		-	20	-	-	20	-	pF
System Calibration Specifications								
Positive Full Scale Calibration Range				VREF+0.1			VREF+0.1	V
Positive Full Scale Input Overrange				VREF+0.1			VREF+0.1	V
Negative Full Scale Input Overrange				-(VREF+0.1)			-(VREF+0.1)	V
Maximum Offset Calibration Range (Notes 6, 7)	Unipolar Mode			-(VREF+0.1)			-(VREF+0.1)	V
	Bipolar Mode			-40%VREF to +40%VREF			-40%VREF to +40%VREF	V
Input Span	(Note 8)	80%VREF		2VREF +0.2	80%VREF		2VREF +0.2	V

4. All outputs unloaded.
5. 0.1Hz to 10Hz. PSRR at 60 Hz will exceed 120 dB due to the benefit of the digital filter.
6. In unipolar mode the offset can have a negative value (-VREF) such that the unipolar mode can mimic bipolar mode operation.
7. The specifications for Input Overrange and for Input Span apply additional constraints on the offset calibration range.
8. For Unipolar mode, Input Span is the difference between full scale and zero scale. For Bipolar mode, Input Span is the difference between positive and negative full scale points. When using less than the maximum input span, the span range may be placed anywhere within the range of ±(VREF + 0.1).

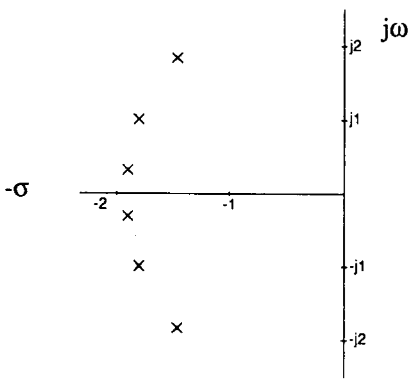
Specifications are subject to change without notice.

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Units
Sampling Frequency	f_s	CLKIN/ 256	Hz
Output Update Rate	f_{out}	CLKIN /1024	Hz
Filter Corner Frequency	f_{-3dB}	CLKIN /409,600	Hz
Settling Time to ±0.0007% FS (FS Step)	t_s	506,880/CLKIN	s



Frequency Response



$S_{1,2} = -1.4667 \pm j1.8199$

$S_{3,4} = -1.7559 \pm j1.0008$

$S_{5,6} = -1.8746 \pm j0.32276$

S-Domain Pole/Zero Plot (Continuous-Time Representation)

$$H(x) = [1 + 0.694x^2 + 0.241x^4 + 0.0557x^6 + 0.009664x^8 + 0.00134x^{10} + 0.000155x^{12}]^{-1/2}$$

where $x = f/f_{-3dB}$, f_{-3dB} = CLKIN/409,600, and f is the frequency of interest.

Continuous-Time Representation of 6-Pole Gaussian Filter

DIGITAL CHARACTERISTICS (T_A = T_{min} to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
Calibration Memory Retention Power Supply Voltage (VD+ and VA+)	V_{MR}	2.0	-	-	V
High-Level Input Voltage All Except CLKIN	V_{IH}	2.0	-	-	V
High-Level Input Voltage CLKIN	V_{IH}	3.5	-	-	V
Low-Level Input Voltage All Except CLKIN	V_{IL}	-	-	0.8	V
Low-Level Input Voltage CLKIN	V_{IL}	-	-	1.5	V
High-Level Output Voltage (Note 9)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA
3-State Leakage Current	I_{OZ}	-	-	±10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Notes: 9. I_{out} = -100 µA. This guarantees the ability to drive one TTL load. (V_{OH} = 2.4V @ I_{out} = -40 µA).

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	VA+ + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Notes 10, 11)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	VA- - 0.3	VA+ + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	VA+ + 0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 10. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pin.
11. Transient currents of up to 100mA will not cause SCR latch-up. Maximum input current for a power supply pin is ± 50 mA.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see Note 12.)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive Digital	VD+	4.5	5.0	VA+	V
Negative Digital	VD-	−4.5	−5.0	−5.5	V
Positive Analog	VA+	4.5	5.0	5.5	V
Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage	VREF	1.0	2.5	3.0	V
Analog Input Voltage: Unipolar (Note 13)	V_{AIN}	AGND	-	VREF	V
Bipolar	V_{AIN}	-VREF	-	VREF	V

Notes: 12. All voltages with respect to ground.
13. The CS5501 and CS5503 can accept input voltages up to the analog supplies (VA+ and VA-). They will accurately convert and filter signals with noise excursions up to 100mV beyond |VREF|. After filtering, the devices will output all 1's for any input above VREF and all 0's for any input below

3

SWITCHING CHARACTERISTICS (T_A = T_{min} to T_{max}; CLKIN=4.096 MHz; VA+, VD+ = 5V±10%; VA-, VD- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF; unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency: Internal Gate Oscillator: (See Table 1)	CLKIN	200	4096	5000	kHz
Externally Supplied: (Note 14) Maximum	CLKIN	-	-	5000	kHz
Minimum (Note 15)	CLKIN	200	40	-	kHz
CLKIN Duty Cycle	-	20	-	80	%
Rise Times: Any Digital Input	trise	-	-	1.0	µs
Any Digital Output (Note 16)	trise	-	20	-	ns
Fall Times: Any Digital Input	tfall	-	-	1.0	µs
Any Digital Output (Note 16)	tfall	-	20	-	ns
Set Up Times: SC1, SC2 to CAL Low (Note 17)	tscs	100	-	-	ns
$\overline{\text{SLEEP}}$ High to CLKIN High (Note 18)	tsls	1	-	-	µs
Hold Time: SC1, SC2 hold after CAL falls	tsch	100	-	-	ns

Notes: 14. CLKIN must be supplied whenever the CS5501 or CS5503 is not in $\overline{\text{SLEEP}}$ mode. If no clock is present when not in $\overline{\text{SLEEP}}$ mode, the device can draw higher current than specified and possibly become uncalibrated.
15. The CS5501/CS5503 is production tested at 4.096 MHz. It is guaranteed by characterization to operate at 200 kHz.
16. Specified using 10% and 90% points on waveform of interest.
17. Silicon prior to mid 1992 latched SC0, SC2 on the rising edge of CAL. All silicon after mid 1992 will latch SC1, SC2 on the falling edge of CAL.
18. In order to synchronize several CS5501's or CS5503's together using the $\overline{\text{SLEEP}}$ pin, this specification must be met.

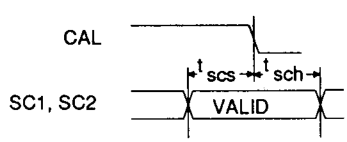
SWITCHING CHARACTERISTICS (continued) ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

Parameter		Symbol	Min	Typ	Max	Units
SSC Mode (Mode = VD+)						
Access Time	$\overline{CS}$ Low to SDATA Out	t_{csd1}	3/CLKIN	-	-	ns
SDATA Delay Time	SCLK Falling to New SDATA bit	t_{dd1}	-	25	100	ns
SCLK Delay Time (at 4.096 MHz)	SDATA MSB bit to SCLK Rising	t_{cd1}	250	380	-	ns
Serial Clock (Out)	Pulse Width High (at 4.096MHz) Pulse Width Low	t_{ph1} t_{pl1}	- -	240 730	300 790	ns ns
Output Float Delay	SCLK Rising to Hi-Z	t_{fd2}	-	1/CLKIN + 100	1/CLKIN +200	ns
Output Float Delay (Note 19)	$\overline{CS}$ High to Output Hi-Z	t_{fd1}	-	-	4/CLKIN + 200	ns
SEC Mode (Mode = DGND)						
Serial Clock (In)		f_{sclk}	dc	-	4.2	MHz
Serial Clock (In)	Pulse Width High Pulse Width Low	t_{ph2} t_{pl2}	50 180	- -	- -	ns ns
Access Time	$\overline{CS}$ Low to Data Valid (Note 20)	t_{csd2}	-	80	160	ns
Maximum Data Delay Time (Note 21)	SCLK Falling to New SDATA bit	t_{dd2}	-	75	150	ns
Output Float Delay	$\overline{CS}$ High to Output Hi-Z	t_{fd3}	-	-	250	ns
Output Float Delay	SCLK Falling to Output Hi-Z	t_{fd4}	-	100	200	ns

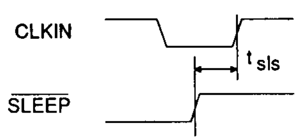
Notes: 19. If $\overline{CS}$ is returned high before all data bits are output, the SDATA and SCLK outputs will complete the current data bit and then go to high impedance.

20. If $\overline{CS}$ is activated asynchronously to $\overline{DRDY}$, $\overline{CS}$ will not be recognized if it occurs when $\overline{DRDY}$ is high for 4 clock cycles. The propagation delay time may be as great as 4 CLKIN cycles plus 160 ns. To guarantee proper clocking of SDATA when using asychronous $\overline{CS}$, SCLK(i) should not be taken high sooner than 4 CLKIN cycles plus 160ns after $\overline{CS}$ goes low.

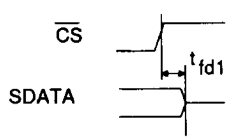
21. SDATA transitions on the falling edge of SCLK(i).



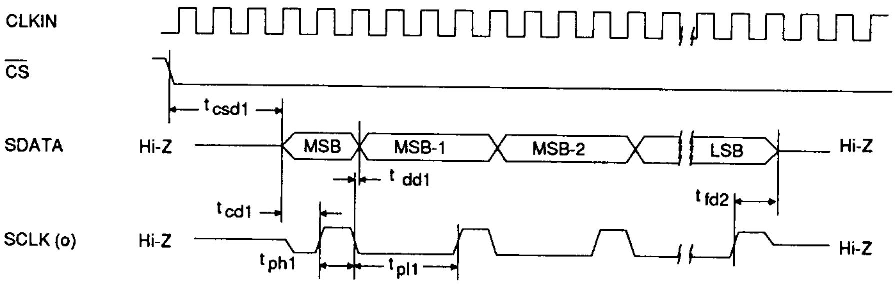
Calibration Control Timing



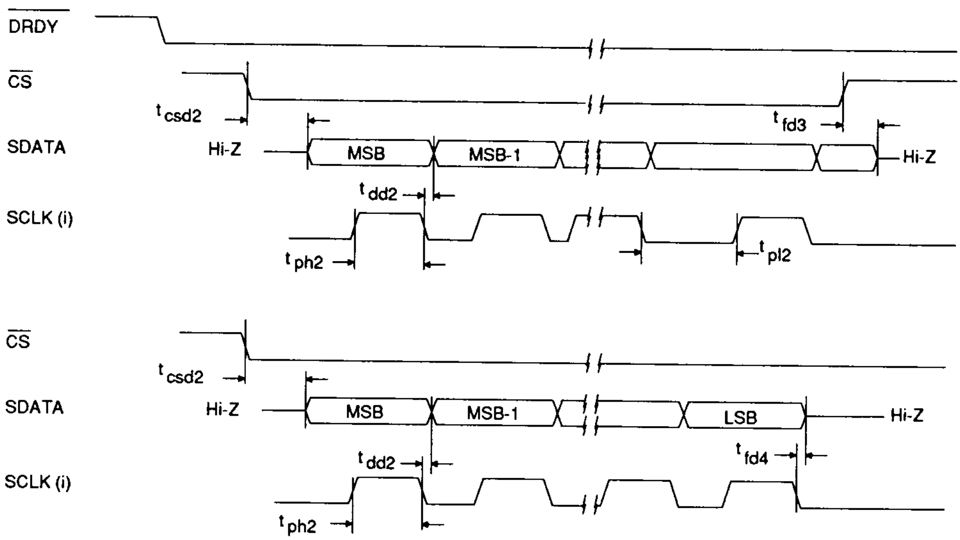
Sleep Mode Timing for Synchronization



Output Float Delay SSC Mode (Note 19)



SSC MODE Timing Relationships



SEC MODE Timing Relationships

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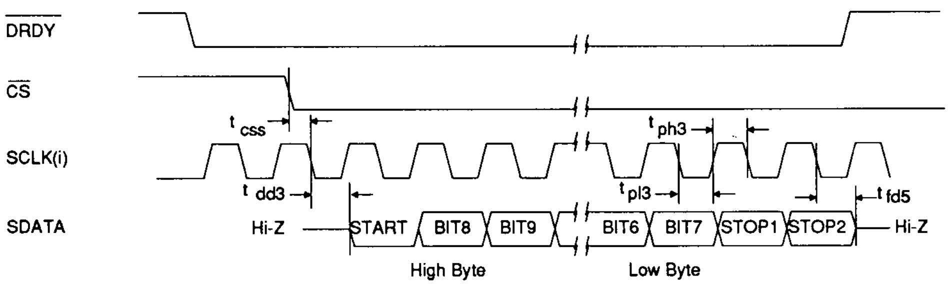
SWITCHING CHARACTERISTICS (continued) ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

Parameter		Symbol	Min	Typ	Max	Units
AC Mode (Mode = VD-) CS5501 only						
Serial Clock (In)		f_{sclk}	dc	-	4.2	MHz
Serial Clock (In)	Pulse Width High	t_{ph3}	50	-	-	ns
	Pulse Width Low	t_{pl3}	180	-	-	ns
Set-up Time	$\overline{CS}$ Low to SCLK Falling	t_{css}	-	20	40	ns
Maximum Data Delay Time	SCLK Falling to New SDATA bit	t_{dd3}	-	90	180	ns
Output Float Delay (Note 22)	$\overline{CS}$ High to Output Hi-Z	t_{fd5}	-	100	200	ns

22. If $\overline{CS}$ is returned high after an 11-bit data packet is started, the SDATA output will continue to output data until the end of the second stop bit. At that time the SDATA output will go to high impedance.



AC MODE Timing Relationships (CS5501 only)

GENERAL DESCRIPTION

The CS5501/CS5503 are monolithic CMOS A/D converters designed specifically for high resolution measurement of low-frequency signals. Each device consists of a charge-balance converter (16-Bit for the CS5501, 20-Bit for the CS5503), calibration microcontroller with on-chip SRAM, and serial communications port.

The CS5501/CS5503 A/D converters perform conversions continuously and update their output ports after every conversion (unless the serial port is active). Conversions are performed and the serial port is updated independent of external control. Both devices are capable of measuring either unipolar or bipolar input signals, and calibration cycles may be initiated at any time to ensure measurement accuracy.

The CS5501/CS5503 perform conversions at a rate determined by the master clock signal. The master clock can be set by an external clock or with a crystal connected to the pins of the on-chip gate oscillator. The master clock frequency determines:

1. The sample rate of the analog input signal.
2. The corner frequency of the on-chip digital filter.
3. The output update rate of the serial output port.

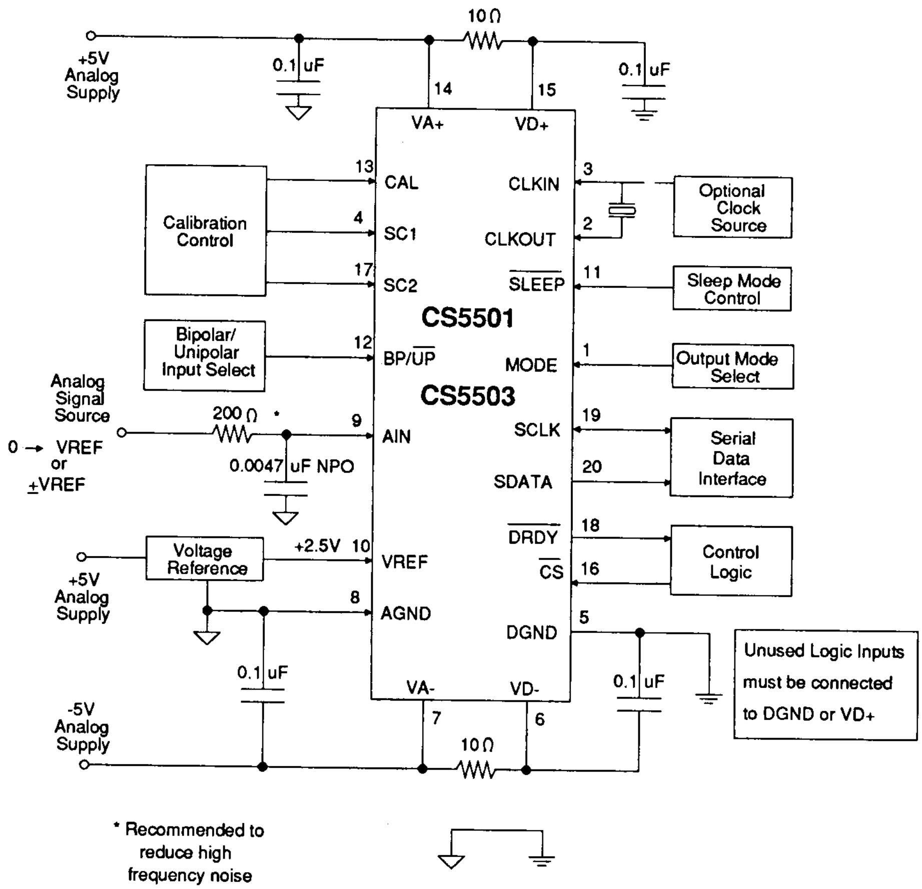


Figure 1. Typical Connection Diagram

The CS5501/CS5503 design includes several self-calibration modes and several serial port interface modes to offer users maximum system design flexiblity.

The Delta-Sigma Conversion Method

The CS5501/CS5503 A/D converters use charge-balance techniques to achieve low cost, high resolution measurements. A charge-balance A/D converter consists of two basic blocks: an analog modulator and a digital filter. An elementary example of a charge-balance A/D converter is a conventional voltage-to-frequency converter and counter. The VFC's 1-bit output conveys information in the form of frequency (or duty cycle), which is then filtered (averaged) by the counter for higher resolution.

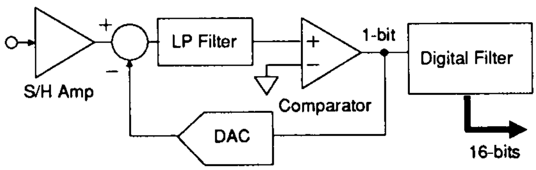


Figure 2. Charge Balance (Delta-Sigma) A/D Converter

The analog modulator of the CS5501/CS5503 is a multi-order delta-sigma modulator. The modulator consists of a 1-bit A/D converter (that is, a comparator) embedded in an analog feedback loop with high open loop gain (see Figure 2). The modulator samples and converts the input at a rate well above the bandwidth of interest. The 1-bit output of the comparator is sampled at intervals based on the clock rate of the part and this information (either a 1 or 0) is conveyed to the digital filter. The digital filter is much more sophisticated than a simple counter. The filter on the chip has a 6-pole low pass Gaussian response which rolls off at 120 dB/decade (36 dB/octave). The corner frequency of the digital filter scales with the master clock frequency. In comparison, VFC's and dual slope converters offer (sin x)/x filtering for high frequency rejection (see Figure 3 for a comparison of the characteristics of these two filter types). When operating from a 1 MHz master clock the digital filter in the CS5501/CS5503 offers better than 120 dB rejection of 50 and 60 Hz line frequencies and does not require any type of line synchronization to achieve this rejection. It should be noted that the CS5501/CS5503 will update its output port almost at 1000 times per second when operating from the 1 MHz clock. This is a much higher update rate (typically by a factor of at least 50 times) than either VFCs or dual-slope converters can offer.

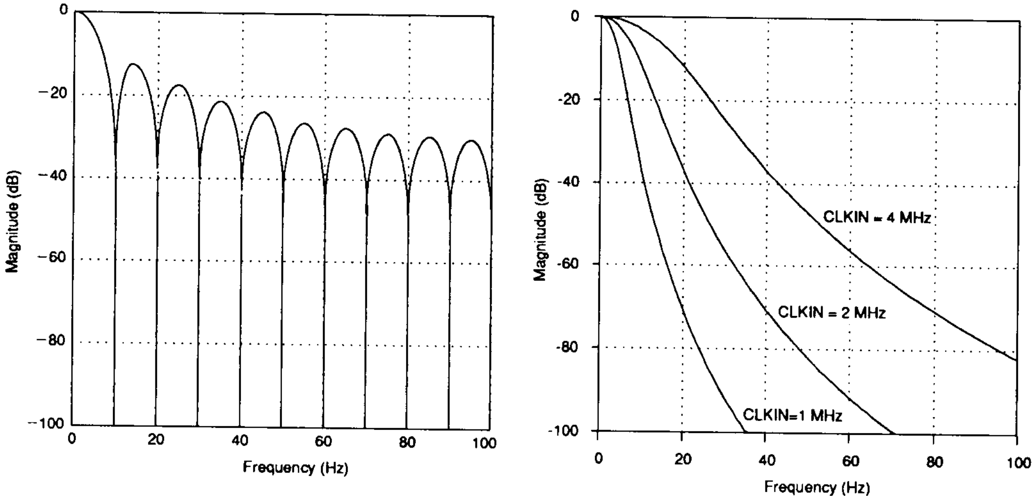
For a more detailed discussion on the delta-sigma modulator see the Application note "Delta-Sigma A/D Conversion Technique Overview" in the application note section of the data book. The application note discusses the delta-sigma modulator and some aspects of digital filtering.

OVERVIEW

As shown in the block diagram on the front page of the data sheet, the CS5501/CS5503 can be segmented into five circuit functions. The heart of the chip is the charge balance A/D converter (16-bit for the CS5501, 20-bit for the CS5503). The converter and all of the other circuit functions on the chip must be driven by a clock signal from the clock generator. The serial interface logic outputs the converted data. The calibration microcontroller along with the calibration SRAM (static RAM), supervises the device calibration. Each segment of the chip has control lines associated with it. The function of each of the pins is described in the pin description section of the data sheet.

Clock Generator

The CS5501/CS5503 both include gates which can be connected as a crystal oscillator to provide the master clock signal for the chip. Alternatively, an external (CMOS compatible) clock can be input to the CLKIN pin as the master clock for the device. Figure 4 illustrates a simple model of

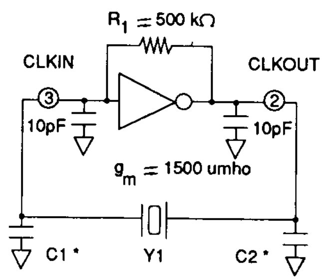


a. Averaging (Integrating) Filter Response (tavg = 100 ms)

b. 6-Pole Gaussian Filter Response

Figure 3. Filter Responses

the on-chip gate oscillator. The gate has a typical transconductance of 1500 μmho. The gate model includes 10 pf capacitors at the input and output pins. These capacitances include the typical stray capacitance of the pins of the device. The on-chip gate oscillator is designed to properly operate without additional loading capacitors when using a 4.096 MHz (or 4 MHz) crystal. If other crystal frequencies or if ceramic resonators are used, loading capacitors may be necessary for reliable operation of the oscillator. Table 1 illustrates some typical capacitor values to be used with selected resonating elements.



* See Table 1

Figure 4. On-chip Gate Oscillator Model

CLKOUT (pin 2) can be used to drive one external CMOS gate for system clock requirements. In this case, the external gate capacitance must be taken into account when choosing the value of C2.

Resonators	C1	C2
Ceramic		
200 kHz	330pF	470pF
455 kHz	100pF	100pF
1.0 MHz	50pF	50pF
2.0 MHz	20pF	20pF
Crystals		
2.000 MHz	30pF	30pF
3.579 MHz	20pF	20pF
4.096 MHz	None	None

Table 1. Resonator Loading Capacitors

Caution: A clock signal should always be present whenever the $\overline{SLEEP}$ is inactive ($\overline{SLEEP}$ = VD+). If no clock is provided to the part when not in $\overline{SLEEP}$, the part may draw excess current and possibly even lose its calibration data. This is because the device is built using dynamic logic.

Serial Interface Logic

The CS5501 serial data output can operate in any one of the following three different serial interface modes depending upon the MODE pin selection:

SSC (Synchronous Self-Clocking) mode;
MODE pin tied to VD+ (+5V).

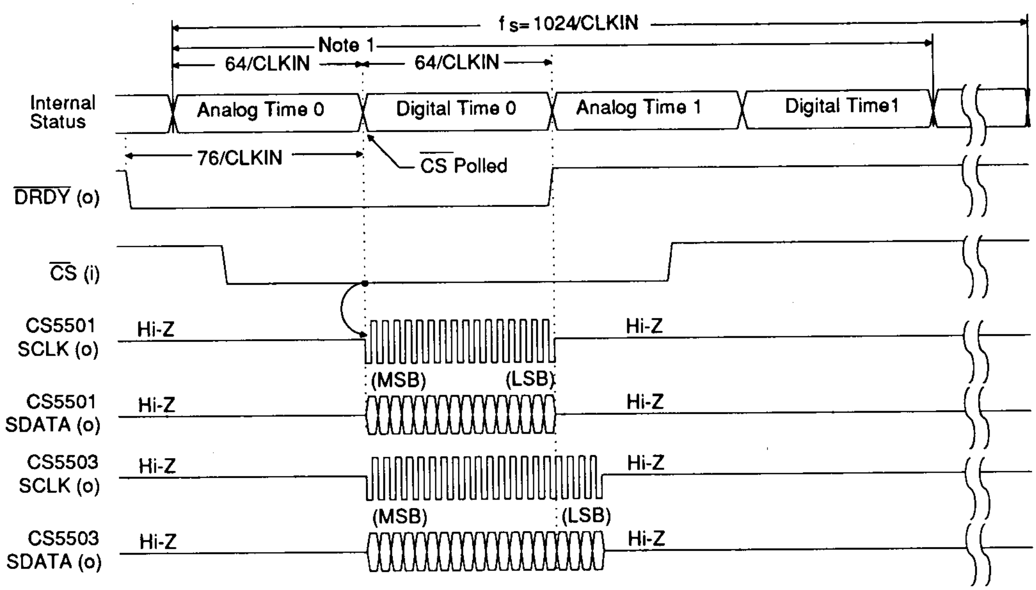
SEC (Synchronous External Clocking) mode;
MODE pin tied to DGND.

and AC (Asynchronous Communication) mode;
CS5501 only
MODE pin tied to VD- (-5V)

The CS5503 can only operate in the first two modes, SEC and SSC.

Synchronous Self-Clocking Mode

When operated in the SSC mode (MODE pin tied to VD+), the CS5501/CS5503 furnish both serial output data (SDATA) and an internally-generated serial clock (SCLK). Internal timing for the SSC mode is illustrated in Figure 5. Figure 6 shows detailed SSC mode timing for both the CS5501/CS5503. A filter cycle occurs every 1024 cycles of CLKIN. During each filter cycle, the status of $\overline{\text{CS}}$ is polled at eight specific times during the cycle. If $\overline{\text{CS}}$ is low when it is polled, the CS5501/CS5503 begin clocking the data bits out, MSB first, at a SCLK output rate of CLKIN/4. Once transmission is complete, $\overline{\text{DRDY}}$ rises and both SDATA and SCLK outputs go into a high impedance state. A filter cycle begins each time $\overline{\text{DRDY}}$ falls. If the $\overline{\text{CS}}$ line is not active, $\overline{\text{DRDY}}$ will return high 1020 clock cycles after it falls. Four clock cycles later $\overline{\text{DRDY}}$ will fall to signal that the serial port has been updated with new data and that a new filter cycle has begun.



Note: There are 16 analog and digital settling periods per filter cycle (4 are shown). Data can be output in the SSC mode in only 1 of the 8 digital time periods in each filter cycle.

Figure 5. Internal Timing

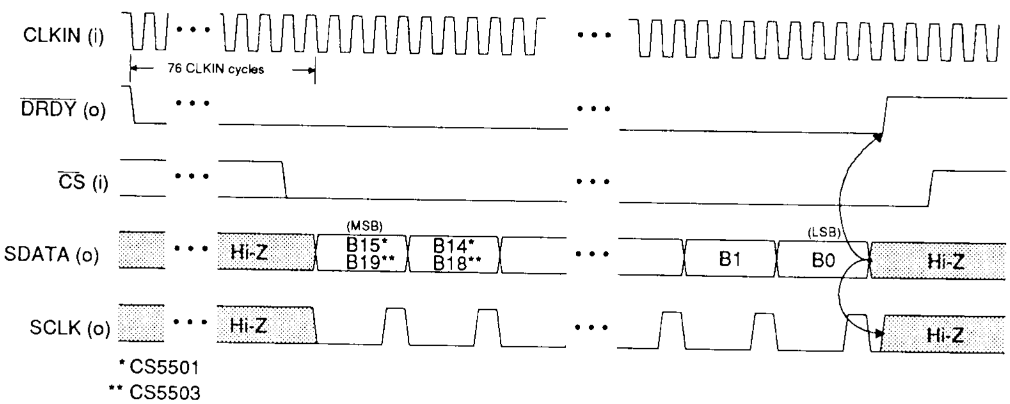


Figure 6. Synchronous Self-Clocking (SSC) Mode Timing

The first $\overline{CS}$ polling during a filter cycle occurs 76 clock cycles after $\overline{DRDY}$ falls (the rising edge of CLKIN on which $\overline{DRDY}$ falls is considered clock cycle number one). Subsequent pollings of $\overline{CS}$ occur at intervals of 128 clock cycles thereafter (76, 204, 332, etc.). The $\overline{CS}$ signal is polled at the beginning of each of eight data output windows which occur in a filter cycle. To transmit data during any one of the eight output windows, $\overline{CS}$ must be low at least three CLKIN cycles before it is polled. If $\overline{CS}$ does not meet this setup time, data will not be transmitted during the window time. Furthermore, $\overline{CS}$ is not latched internally and therefore must be held low during the entire data transmission to obtain all of the data bits.

The eighth output window time overlaps the time in which the serial output port is to be updated. If the $\overline{CS}$ is recognized as being low when it is polled for the eighth window time, data will be output as normal, but the serial port will not be updated with new data until the next serial port update time. Under these conditions, the serial port will experience an update rate of only 2 kHz (CLKIN = 4.096 MHz) instead of the normal 4 kHz serial port update rate.

Upon completion of transmission of all the data bits, the SCLK and SDATA outputs will go to a high impedance state even with $\overline{CS}$ held low. In the event that $\overline{CS}$ is taken high before all data bits are output, the SDATA and SCLK outputs will complete the current data bit output and go to a high impedance state when SCLK goes low.

Synchronous External Clocking Mode

When operated in the SEC mode (MODE pin tied to DGND), the CS5501/CS5503 outputs the data in its serial port at a rate determined by an external clock which is input into the SCLK pin. In this mode the output port will be updated every 1024 CLKIN cycles. $\overline{DRDY}$ will go low when new data is loaded into the output port. If $\overline{CS}$ is not active, $\overline{DRDY}$ will return positive 1020 CLKIN cycles later and remain so for four CLKIN cycles. If $\overline{CS}$ is taken low it will be recognized immediately unless it occurs while $\overline{DRDY}$ is high for the four clock cycles. As soon as $\overline{CS}$ is recognized, the SDATA output will come out of its high-impedance state and present the MSB data bit. The MSB data bit will remain present until a falling edge of SCLK occurs to advance the output to the MSB-1 bit. If the $\overline{CS}$ and external SCLK are operated asynchronously to CLKIN, errors can result in the output data unless certain precautions are taken. If $\overline{CS}$ is activated asynchronously, it may occur during the four clock cycles when $\overline{DRDY}$ is high and therefore not be recognized immediately. To be certain that data misread errors will not result if $\overline{CS}$ occurs at this time, the SCLK input should not transition high to latch the MSB until four CLKIN cycles plus 160 ns after CS is taken low. This insures that CS will be recognized and the MSB bit will become stable before the SCLK transitions positive to latch the MSB data bit.

When SCLK returns low the serial port will present the MSB-1 data bit on its output. Subsequent cycles of SCLK will advance the data output. When all data bits are clocked out, DRDY will then go high and the SDATA output will go into a high impedance state. If the CS input goes low and all of the data bits are not clocked out of the port, filter cycles will continue to occur but the output serial port will not be updated with new data (DRDY will remain low). If CS is taken high at any time, the SDATA output pin will go to a high impedance state. If any of the data bits in the serial port have not been clocked out, they will remain available until DRDY returns high for four clock cycles. After this DRDY will fall and the port will be updated with a new 16-bit word in the CS5501 or 20-bit word in the CS5503. It is acceptable to clock out less than all possible data bits if CS is returned high to allow the port to be updated. Figure 7 illustrates the serial port timing in the SEC mode.

Asynchronous Communication Mode (CS5501 Only)

In the CS5501, the AC mode is activated when the MODE pin is tied to VD- (-5 V). When operating in the AC mode the CS5501 is designed to provide data output in UART compatible format. The baud rate of the SDATA output will be determined by the rate of the SCLK input. The data which is output of the SDATA pin will be formated such that it will contain two 11 bit data packets. Each packet includes one start bit, eight data bits, and two stop bits. The packet which carries the most-significant-byte data will be output first, with its lsb being the first data bit output after the start bit.

In this mode, DRDY will occur every 1024 clock cycles. If the serial port is not outputting a data byte, DRDY will return high after 1020 clock cycles and remain high for 4 clock cycles. DRDY will then go low to indicate that an update to the serial output port with a new 16 bit word has occured. To initiate a transmission from the port the CS line must be taken low. Then SCLK, which is an input in this mode, must transition from a high to a low to latch the state of CS internal to the CS5501. Once CS is recognized and latched as a low, the port will begin to output data. Figure 8 details the timing for this output. CS can be returned high before the end of the 11-bit transmission and the transmission will continue until the second stop bit of the first 11-bit packet is

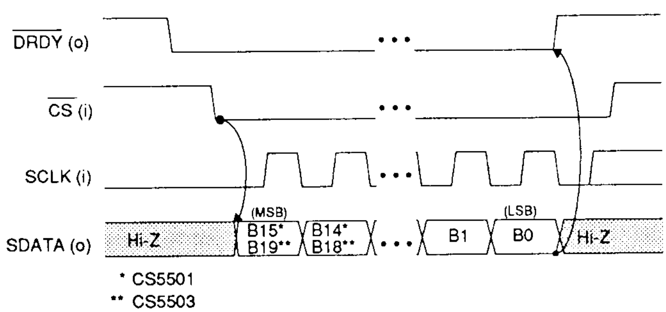


Figure 7. Synchronous External-Clocking (SEC) Mode Timing

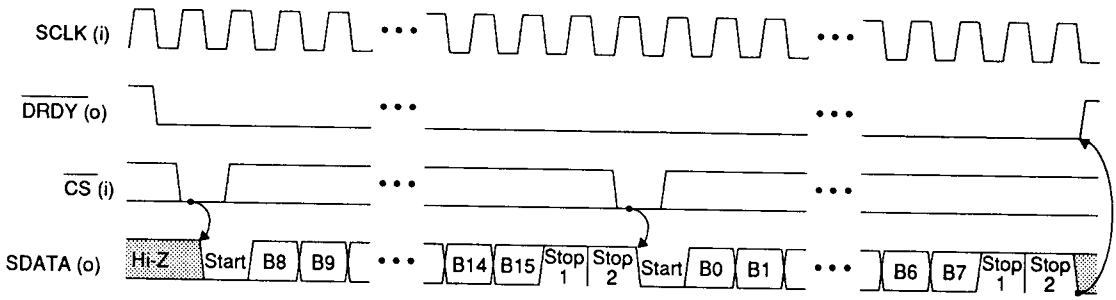


Figure 8. CS5501 Asynchrounous (UART) Mode Timing

3

output. The SDATA output will go into a high impedance state after the second stop bit is output. To obtain the second 11-bit packet CS must again be brought low before DRDY goes high or the second 11-bit data packet will be overwritten with a serial port update. For the second 11-bit packet, CS need only to go low for 50 ns; it need not be latched by a falling edge of SCLK. Alternately, the CS line can be taken low and held low until both 11-bit data packets are output. This is the preferred method of control as it will prevent losing the second 11-bit data packet if the port is updated. Some serial data rates can be quite slow compared to the rate at which the CS5501 can update its output port. A slow data rate will leave only a short period of time to start the second 11-bit packet if CS is returned high momentarily. If CS is held low continuously (CS hard-wired to DGND), the serial port will be updated only after all 22 bits have been clocked out of the port.

Upon the completion of a transmission of the two 11-bit data packets the SDATA output will go into a high impedance state. If at any time during transmission the CS is taken back high, the current 11-bit data packet will continue to be output. At the end of the second stop bit of the data packet, the SDATA output will go into a high impedance state.

Linearity Performance

The CS5501/CS5503 delta-sigma converters are like conventional charge-balance converters in that they have no source of nonmonotonicity. The devices therefore have no missing codes in their transfer functions. See Figure 9 for a plot of the excellent differential linearity achieved by the CS5501. The CS5501/CS5503 also have excellent integral linearity, which is accomplished with a well-designed charge-balance architecture. Each device also achieves low input drift through the use of chopper-stabilized techniques in its input

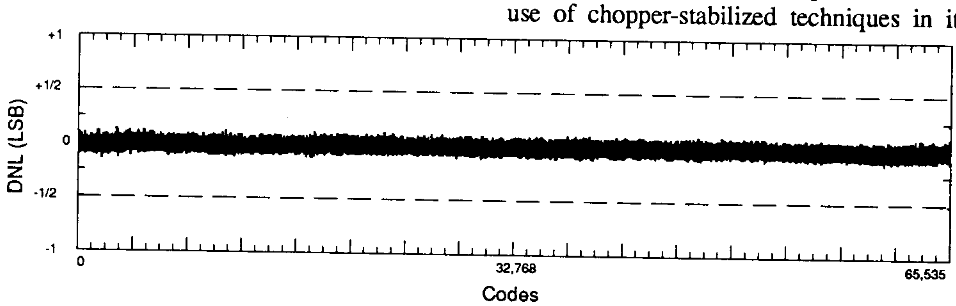


Figure 9. CS5501 Differential Nonlinearity Plot

stage. To assure that the CS5501/CS5503 achieves excellent performance over time and temperature, it uses digital calibration techniques to minimize offset and gain errors to typically within ±1/2 LSB at 16 bits in the CS5501 and ±4 LSB at 20 bits in the CS5503.

Converter Calibration

The CS5501/CS5503 offer both self-calibration and system level calibration capability. To understand the calibration features, a basic comprehension of the internal workings of the converter are helpful. As mentioned previously in this data sheet, the converter consists of two sections. First is the analog modulator which is a delta-sigma type charge-balance converter. This is followed by a digital filter. The filter circuitry is actually an arithematic logic unit (ALU) whose architecture and instructions execute the filter function. The modulator (explained in more detail in the applications note "Delta-Sigma Conversion Technique Overview") uses the VREF voltage connected to pin 10 to determine the magnitude of the voltages used in its feedback DAC. The modulator accepts an analog signal at its input and produces a data stream of 1's and 0's as its output. This data stream value can change (from 1 to 0 or vice versa) every 256 CLKIN cycles. As the input voltage increases the ratio of 1's to 0's out of the modulator increases proportionally. The 1's density of the data stream out of the modulator therefore provides a digital representation of the analog input signal where the 1's density is defined as the ratio of the number of 1's to the number of 0's out of the modulator for a given period of time. The 1's density output of the modulator is also a function of the voltage on the VREF pin. If the voltage on the VREF pin increases in value (say, due to temperature drift), and the analog input voltage into the modulator remains constant, the 1's density output of the modulator will decrease (less 1's will occur). The analog input into the modulator which is necessary to produce a given binary output code from the converter is ratiometric to the voltage on the VREF pin. This means that if VREF increases by one per cent, the analog signal on AIN must also increase by one per cent to maintain the same binary output code from the converter.

For a complete calibration to occur, the calibration microcontroller inside the device needs to record the data stream 1's density out of the modulator for two different input conditions. First, a "zero scale" point must be presented to the modulator. Then a "full scale" point must be presented to the modulator. In unipolar self-cal mode the zero scale point is AGND and the full scale point is the voltage on the VREF pin. The calibration microcontroller then remembers the 1's density out of the modulator for each of these points and calculates a slope factor (LSB/uV). This slope factor represents the gain slope for the input to output transfer function of the converter. In unipolar mode the calibration microcontroller determines the slope factor by dividing the span between the zero point and the full scale point by the total resolution of the converter (2^{16} for the CS5501, resulting in 65,536 segments or 2^{20} for the CS5503, resulting in 1,048,578 segments). In bipolar mode the calibration microcontroller divides the span between the zero point and the full scale point into 524,288 segments for the CS5503 and 32,768 segments for the CS5501. It then extends the measurement range 524,288 segments for the CS5503, 32,768 segments for the CS5501, below the zero scale point to achieve bipolar measurement capability. In either unipolar or bipolar modes the calculated slope factor is saved and later used to calculate the binary output code when an analog signal is present at the AIN pin during measurement conversions.

System calibration allows the A/D converter to compensate for system gain and offset errors (see Figure 10). System calibration performs the same slope factor calculations as self-cal but uses voltage values presented by the system to the AIN pin for the zero scale point and for the full scale point. Table 2 depicts the calibration modes available. Two system calibration modes are

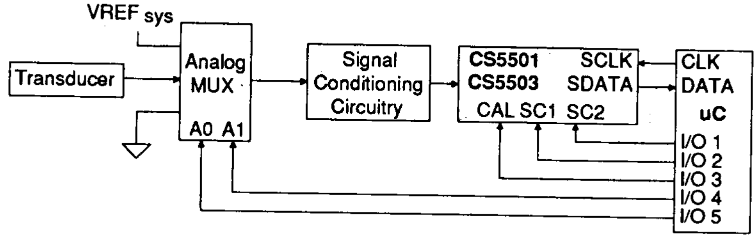


Figure 10. System Calibration

CAL	SC1	SC2	Cal Type	ZS Cal	FS Cal	Sequence	Calibration Time
↓	0	0	Self-Cal	AGND	VREF	One Step	3,145,655/fclk
↓	1	1	System Offset & System Gain	AIN	-	1st Step	1,052,599/fclk
↓	0	1		-	AIN	2nd Step	1,068,813/fclk
↓	1	0	System Offset	AIN	VREF	One Step	2,117,389/fclk

* $\overline{\text{DRDY}}$ remains high throughout the calibration sequence. In Self-Cal mode (SC1 and SC2 low) $\overline{\text{DRDY}}$ falls once the CS5501 or CS5503 has settled to the analog input. In all other modes $\overline{\text{DRDY}}$ falls immediately after the calibration term has been determined.

Table 2. Calibration Control

listed. The first mode offers system level calibration for system offset and for system gain. This is a two-step calibration. The zero scale point (system offset) must be presented to the converter first. The voltage that represents zero scale point must be input to the converter before the calibration step is initiated and must remain stable until the step is complete. The $\overline{\text{DRDY}}$ output from the converter will signal when the step is complete by going low. After the zero scale point is calibrated, the voltage representing the full scale point is input to the converter and the second calibration step is initiated. Again the voltage must remain stable thoughout the calibration step.

This two-step calibration mode offers another calibration feature. After a two-step calibration sequence (system offset and system gain) has been properly performed, additional offset calibrations can be performed by themselves to reposition the gain slope (the slope factor is not changed) to adjust its zero reference point to the new system zero reference value.

A second system calibration mode is available which uses an input voltage for the zero scale calibration point, but uses the VREF voltage as the full scale calibration point.

Whenever a system calibration mode is used, there are limits to the amount of offset and to the amount of span which can be accomodated. The range of input span which can be accomodated in either unipolar or bipolar mode is restricted to not less than 80% of the voltage on VREF and not more than 200% of (VREF + 0.1) V. The amount of offset which can be calibrated depends upon whether unipolar or bipolar mode is being used. In unipolar mode the system calibration modes can handle offsets as positive as 20% of VREF (this is restricted by the minimum span requirement of 80% VREF) or as negative as -(VREF + 0.1) V. This capability enables the unipolar mode of the CS5501/CS5503 to be calibrated to mimic bipolar mode operation.

In the bipolar mode the system offset calibration range is restricted to a maximum of ±40% of VREF. It should be noted that the span restrictions limit the amount of offset which can be calibrated. The span range of the converter in bipolar mode extends an equidistance (+ and -)

from the voltage used for the zero scale point. When the zero scale point is calibrated it must not cause either of the two endpoints of the bipolar transfer function to exceed the positive or the negative input overrange points (+(VREF + 0.1) V or - (VREF + 0.1) V). If the span range is set to a minimum (80% VREF) the offset voltage can move ±40% VREF without causing the end points of the transfer function to exceed the overrange points. Alternatively, if the span range is set to 200% of VREF, the input offset cannot move more than +0.1 or - 0.1 V before an endpoint of the transfer function exceeds the input overrange limit.

Initiating Calibration

Table 2 illustrates the calibration modes available in the CS5501/CS5503. Not shown in the table is the function of the BP/$\overline{\text{UP}}$ pin which determines whether the converter is calibrated to measure bipolar or unipolar signals. A calibration step is initiated by bringing the CAL pin (13) high for at least 4 CLKIN cycles to reset the part and then bringing CAL low. The states of SC1 (pin 4) and SC2 (pin 17) along with the BP/$\overline{\text{UP}}$ (pin 12) will determine the type of calibration to be performed. The SC1 and SC2 inputs are latched when CAL goes low. The BP/$\overline{\text{UP}}$ input is not latched and therefore must remain in a fixed state thoughout the calibration and measurement cycles. Any time the state of the BP/$\overline{\text{UP}}$ pin is changed, a new calibration cycle must be performed to enable the CS5501/CS5503 to properly function in the new mode.

When a calibration step is initiated, the $\overline{\text{DRDY}}$ signal will go high and remain high until the step is finished. Table 2 illustrates the number of clock cycles each calibration requires. Once a calibration step is initiated it must finish before a new calibration step can be executed. In the two step system calibration mode, the offset calibration step must be initiated before initiating the gain calibration step.

When a self-cal is completed $\overline{\text{DRDY}}$ falls and the output port is updated with a data word that represents the analog input signal at the AIN pin. When a system calibration step is completed, $\overline{\text{DRDY}}$ will fall and the output port will be updated with the appropriate data value (zero scale point, or full scale point). In the system calibration mode, the digital filter must settle before the output code will represent the value of the analog input signal.

Tables 3 and 4 indicate the output code size and output coding of the CS5501/CS5503 in its various modes. The calibration equations which represent the CS5501/CS5503 transfer function are shown in Figure 11.

Underrange And Overrange Considerations

The input signal range of the CS5501/CS5503 will be determined by the mode in which the part is calibrated. Table 4 indicates the input signal range in the various modes of operation. If the input signal exceeds the full scale point the converter will output all ones. If the signal is less than the zero scale point (in unipolar) or more

DOUT = Slope (AIN - Unipolar Offset) + 0.5 LSB

a. Unipolar Calibration

CS5501

DOUT = Slope (AIN - Bipolar Offset) + 2^{15} + 0.5 LSB_{16}

CS5503

DOUT = Slope(AIN - Bipolar Offset) + 2^{19} + 0.5 LSB_{20}

b. Bipolar Calibration

Figure 11. Calibration Equations

Cal Mode	Zero Scale	Gain Factor	1LSB			
			Unipolar		Bipolar	
			CS5501	CS5503	CS5501	CS5503
Self-Cal	AGND	VREF	$\frac{VREF}{65,536}$	$\frac{VREF}{1,048,526}$	$\frac{2VREF}{65,536}$	$\frac{2VREF}{1,048,526}$
System Cal	SOFF	SGAIN	$\frac{SGAIN - SOFF}{65,536}$	$\frac{SGAIN - SOFF}{1,048,526}$	$\frac{2(SGAIN - SOFF)}{65,536}$	$\frac{2(SGAIN - SOFF)}{1,048,526}$

Table 3. Output Code Size After Calibration

Input Voltage, Unipolar Mode		Output Codes (Hex)		Input Voltage, Bipolar Mode	
System-Cal	Self-Cal	CS5501	CS5503	Self-Cal	System Cal
>(SGAIN - 1.5 LSB)	>(VREF - 1.5 LSB)	FFFF	FFFFF	>(VREF - 1.5 LSB)	>(SGAIN - 1.5 LSB)
SGAIN - 1.5 LSB	VREF - 1.5 LSB	FFFF FFFE	FFFFF FFFFE	VREF - 1.5 LSB	SGAIN - 1.5 LSB
(SGAIN - SOFF)/2 - 0.5 LSB	VREF/2 - 0.5 LSB	8000 7FFF	80000 7FFFF	AGND - 0.5 LSB	SOFF -0.5 LSB
SOFF + 0.5 LSB	AGND + 0.5 LSB	0001 0000	00001 00000	-VREF+ 0.5 LSB	-SGAIN + 2SOFF + 0.5 LSB
<(SOFF + 0.5 LSB)	<(AGND+0.5 LSB)	0000	00000	<(-VREF+0.5 LSB)	<(-SGAIN+2SOFF+0.5 LSB)

Table 4. Output Coding

negative in magnitude than minus the full scale point (in bipolar) it will output all zeroes.

Note that the modulator-filter combination in the chip CS5501/CS5503 is designed to accurately convert and filter input signals with noise excursions which extend up to 100 mV below the analog value which produces all zeros out or above the analog value which produces all ones out. Overrange noise excursions greater than 100 mV may increase output noise.

All pins of the CS5501/CS5503 include diodes which clamp the input signals to within the positive and negative supplies. If a signal on any pin (including AIN) exceeds the supply voltage (either + or -) a clamp diode will be forward-biased. Under these fault conditions the CS5501/CS5503 might be damaged. Under normal operating conditions (with the power supplies established), the device will survive transient currents through the clamp diodes up to 100 mA and continuous currents up to 10 mA. The drive current into the AIN pin should be limited to a safe value if an overvoltage condition is likely to occur. See the application note "Buffer Amplifiers for the CS501X Series of A/D Converters" for further discussion on the clamp diode input structure and on current limiting circuits.

System Synchronization

If more than one CS5501/CS5503 is included in a system which is operating from a common clock, all of the devices can be synchronized to sample and output at exactly the same time. This can be accomplished in either of two ways. First, a single CAL signal can be issued to all the

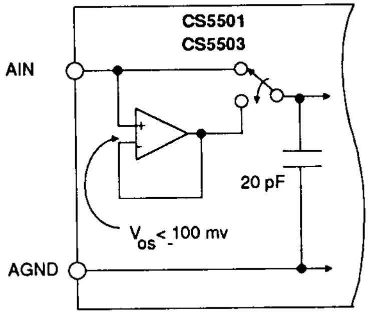


Figure 12. Analog Input Model

CS5501/CS5503's in the system. To insure synchronization on the same clock signal the CAL signal should go low on the falling edge of CLKIN. Or second, a common SLEEP control signal can be issued. If the SLEEP signal goes positive with the appropriate set up time to CLKIN, all parts will be synchronized on the same clock cycle.

Analog Input Impedance Considerations

The analog input of the CS5501/CS5503 can be modeled as illustrated in Figure 12. A 20 pF capacitor is used to dynamically sample the input signal. Every 64 CLKIN cycles the switch alternately connects the capacitor to the output of the buffer and then directly to the AIN pin. Whenever the sample capacitor is switched from the output of the buffer to the AIN pin, a small packet of charge (a dynamic demand of current) will be required from the input source to settle the voltage on the sample capacitor to its final value. The voltage at the output of the buffer may differ up to 100 mV from the actual input voltage due to the offset voltage of the buffer. Timing allows 64 cycles of master clock (CLKIN) for the voltage on the sample capacitor to settle to its final value. The equation which defines settling time is:

$$Vo = Vin\ [1 - e^{-t/RC}]$$

Where Vo is the final settled value, Vin is the value of the input signal, R is the value of the input source resistance, C is the 20 pF sample capacitor plus the value of any stray or additional capacitance at the input pin. The value of t is equal to 64/CLKIN.

From this basic equation the following equation can be developed which indicates the maximum acceptable sourc resistance (R_{SMAX}) for an error of Ve:

$$R_{Smax} = \frac{64}{CLKIN(20pF + Cstr)\ln\left[\frac{100\ mV}{Ve}\right]}$$

This equation assumes that the offset voltage of the buffer is 100 mV, which is the worst case. The value of Ve is the maximum error voltage which is acceptable.

For a maximum error voltage (Ve) of 10 µV in the CS5501 (1/4LSB at 16-bits) and 600 nV in the CS5503 (1/4LSB at 20-bits), the above equation indicates that when operating from a 4.096 MHz CLKIN, source resistances up to 75 kΩ in the CS5501 or 60 kΩ in the CS5503 are acceptable in the absence of stray capacitance ($C_{str} = 0$). If higher input source resistances are desired the master clock rate can be reduced to yield a longer settling time for the 64 cycle period.

An RC filter may be added in front of the CS5503 to reduce high frequency noise (see Figure 1). With an external capacitor added (from AIN to AGND) the following equation will specify the maximum allowable source resistance:

$$R_{Smax} = \frac{64}{CLKIN(20pF + Cext)\ln\left[\frac{\frac{20pF(100\ mV)}{(20pF + Cext)}}{Ve}\right]}$$

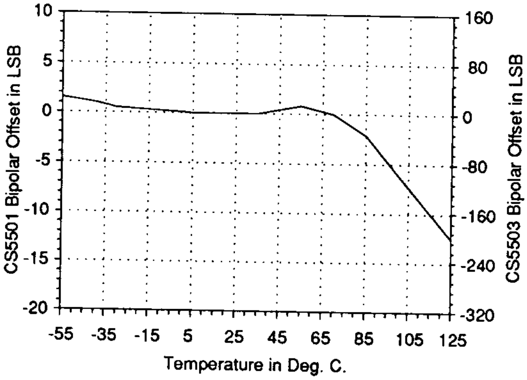


Figure 13. Typical Self-Cal Bipolar Offset vs. Temperature After Calibration at 25 °C

Analog Input Drift Considerations

The CS5501/CS5503 analog input uses chopper-stabilization techniques to minimize input offset drift. Charge injection in the analog switches and leakage currents at the sampling node are the primary sources of offset voltage drift in the converter. Figure 13 indicates the typical offset drift due to temperature changes experienced after calibration at 25 °C. Drift is relatively flat up to about 75 °C. Above 75 °C leakage current becomes the dominant source of offset drift. Leakage currents approximately double with each 10 °C of temperature increase. Therefore the offset drift due to leakage current increases as the temperature increases. The value of the voltage on the sample capacitor is updated at a rate determined by the master clock, therefore the amount of offset drift which occurs will be proportional to the elapsed time between samples. In conclusion, the offset drift increases with temperature and is inversely proportional to the CLKIN rate. To minimize offset drift with increased temperature, higher CLKIN rates are desireable. At temperatures above 100 °C, a CLKIN rate above 1 MHz is recommended. The effects of offset drift due to temperature changes can be eliminated by recalibrating the CS5501/CS5503 whenever the temperature has changed.

Gain drift within the converter depends predominately upon the temperature tracking of internal capacitors. Gain drift is not affected by leakage currents, therefore gain drift is significantly less than comparable offset errors due to temperature increases. The typical gain drift over the specified temperature range is less than 2.5 LSBs for the CS5501 and less than 40 LSBs for the CS5503 .

Measurement errors due to offset drift or gain drift can be eliminated at any time by recalibrating the converter. Using the system calibration mode can also minimize offset and gain errors in the signal conditioning circuitry. The CS5501/CS5503 can be recalibrated at any temperature to remove the effects of these errors.

Linearity and differential non linearity are not significantly affected by temperature changes.

Filtering

At the system level, the digital filter in the CS5501/CS5503 can be modeled exactly like an analog filter with a few minor differences. Digital filtering resides *behind* the A/D conversion and can thus reject noise injected during the conversion process (i.e. power supply ripple, voltage reference noise, or noise in the ADC itself). Analog filtering cannot.

Also, since digital filtering resides behind the A/D converter, noise riding unfiltered on a near-full-scale input could potentially overrange the ADC. In contrast, analog filtering removes the noise before it ever reaches the converter. To address this issue, the CS5501/CS5503 each contain an analog modulator and digital filter which reserve headroom such that the device can process signals with 100mV "excursions" above full-scale and still output accurately converted and filtered data. Filtered input signals above full-scale still result in an output of all ones.

The digital filter's corner frequency occurs at CLKIN/409,600, where CLKIN is the master clock frequency. With a 4.096MHz clock, the filter corner is at 10Hz and the output register is updated at a 4kHz rate. CLKIN frequency can be reduced with a proportional reduction in the filter corner frequency and in the update rate to the output register. A plot of the filter response is shown in the specification tables section of this data sheet.

Both the CS5501/CS5503 employ internal digital filtering which creates a 6-pole Gaussian relationship. With the corner frequency set at 10Hz for minimized settling time, the CS5501/CS5503 offer approximately 55dB rejection at 60Hz to signals coming into either the AIN or VREF pins. With a 5Hz cut-off, 60Hz rejection increases to more than 90dB.

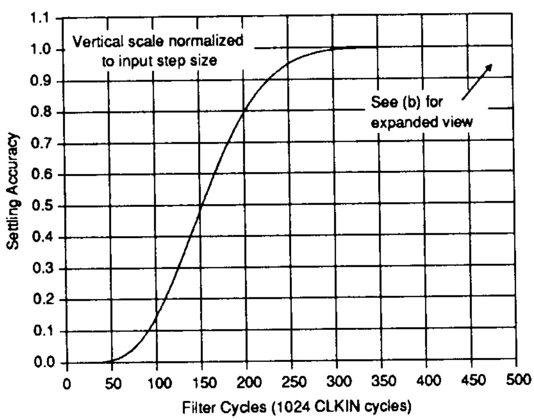
The digital filter (rather than the analog modulator) dominates the converters' settling for step-function inputs. Figure 14 illustrates the settling characteristics of the filter. The vertical axis is normalized to the input step size. The horizontal axis is in filter cycles. With a full scale input step (2.5 V in unipolar mode) the output will exhibit an overshoot of about 0.25 LSB_{16} in the CS5501 and 4 LSB_{20} in the CS5503.

Anti-Alias Considerations

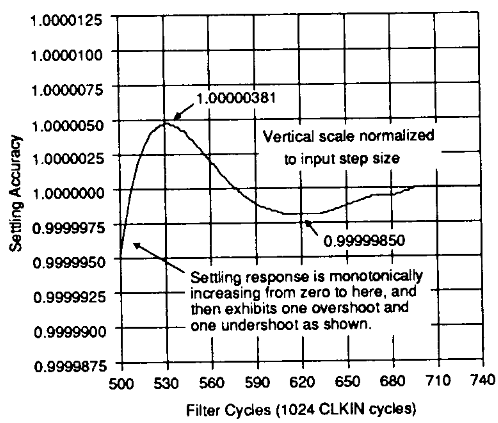
The digital filter in the CS5501/CS5503 does not provide rejection around integer multiples of the oversampling rate [(N*CLKIN)/256, where N = 1,2,3,...]. That is, with a 4.096 MHz master clock the noise on the analog input signal within the narrow ±10 Hz bands around the 16 kHz, 32 kHz, 48 kHz, etc., passes unfiltered to the digital output. Most broadband noise will be very well filtered because the CS5501/CS5503 use a very high oversampling ratio of 800 (16 kHz: 2x10 Hz). Broadband noise is reduced by:

$$e_{out} = e_{in}\sqrt{2f_{-3dB}/f_s}$$
$$e_{out} = 0.035\ e_{in}$$

where e_{in} and e_{out} are rms noise terms referred to the input. Since f_{-3dB} equals CLKIN/409,600 and f_s equals CLKIN/256, the digital filter reduces white, broadband noise by 96.5% independent of the CLKIN frequency. For example, a typical operational amplifier's 50µV rms noise would be reduced to 1.75µV rms (0.035 LSB's rms at the 16-bit level in the CS5501 and 0.4 LSB's rms at the 20-bit level in the CS5503).



(a) Settling Time Due to Input Step Change



(b) Expanded Version of (a)

Figure 14. Output Settling

Bits of Output Accuracy	Filter Cycles	CLKIN Cycles
9	340	348,160
10	356	364,544
11	389	398,336
12	435	445,440
13	459	470,016
14	475	486,400
15	486	497,664
16	495	506,880
17	500	512,000
18	504	516,096
19	506	518,144
20	507	519,168

Table 5. Settling Time of the 6 Pole Low Pass Filter in the CS5501 to 1/2 LSB Accuracy with a Full Scale Step Input

Simple high frequency analog filtering in the signal conditioning circuitry can aid in removing energy at multiples of the sampling rate.

Post Filtering

Post filtering is useful to enhance the noise performance of the CS5503. With a constant input voltage the output codes from the CS5503 will exhibit some variation due to noise. The CS5503 has typically 1.6 LSB_{20} rms noise in its output codes. Additional variation in the output codes can arise due to noise from the input signal source and from the voltage reference. Post filtering (digital averaging) will be necessary to achieve less than 1 LSB p-p noise at the 20-bit level. The CS5503 has peak noise less than the 18-bit level without additional filtering if care is exercised in the design of the voltage reference and the input signal condition circuitry. Noise in the bandwidth from dc to 10 Hz on both the AIN and VREF inputs should be minimized to ensure maximum performance. As the amount of noise will be highly system dependent, a specific recommendation for post filtering for all applications cannot be stated. The following guidelines are helpful. Realize that the digital filter in the CS5503, like any other low pass filter, acts as an information storage unit. The filter retains past information for a period of time even after the input signal has changed. The implication of this is that immediately sequential 20-bit updates to the serial port contain highly correlated information. To most efficiently post filter the CS5503 output data, uncorrelated samples should be used. Samples which have sufficiently reduced correlation can be obtained if the CS5503 is allowed to execute 200 filter cycles between each subsequent data word collected for post filtering.

The character of the noise in the data will influence the post filtering requirements. As a general rule, averaging N uncorrelated data samples will reduce noise by $1/\sqrt{N}$. While this rule assumes that the noise is white (which is true for the CS5503 but not true for all real system signals between dc and 10Hz), it does offer a starting point for developing a post filtering algorithm for removing the noise from the data. The algorithm will have to be empirically tested to see if it meets the system requirements. It is recommended that any testing include input signals across the entire input span of the converter as the signal level will affect the amount of noise from the reference input which is transferred to the output data.

Voltage Reference

The voltage reference applied to the VREF input pin defines the analog input range of the CS5501/CS5503. The preferred reference is 2.5V, but the device can typically accept references from 1V to 3V. Input signals which exceed 2.6V (+ or -) can cause some linearity degradation. Figure 15 illustrates the voltage reference connections to the CS5501/CS5503.

The circuitry inside the VREF pin is identical to that as seen at the AIN pin. The sample capacitor (see Figure 13) requires packets of charge from the external reference just as the AIN pin does. Therefore the same settling time requirements apply. Most reference IC's can handle this dynamic load requirement without inducing er-

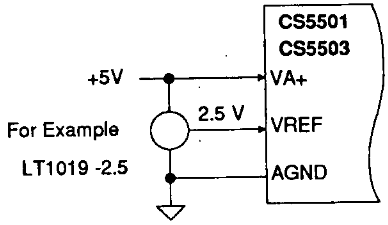


Figure 15. Voltage Reference Connections

rors. They exhibit sufficiently low output impedance and wide enough bandwidth to settle to within the necessary accuracy in the requisite 64 CLKIN cycles.

Noise from the reference is filtered by the digital filter, but the reference should be chosen to minimize noise below 10 Hz. The CS5501/CS5503 typically exhibit 0.1 LSB rms and 1.6 LSB rms noise respectively. This specification assumes a clean reference voltage. Many monolithic band-gap references are available which can supply 2.5 V for use with the CS5501/CS5503. Many of these devices are not specified for noise, especially in the 0.1 to 10 Hz bandwidth. Some of these devices may exhibit noise characteristics which degrade the performance of the CS5501/CS5503.

Power Supplies And Grounding

The CS5501/CS5503 use the analog ground connection, AGND, as a measurement reference node. It carries no power supply current. The AGND pin should be used as the reference node for both the analog input signal and for the reference voltage which is input into the VREF pin.

The analog and digital supply inputs are pinned out separately to minimize coupling between the analog and digital sections of the chip. To achieve maximum performance, all four supplies for the CS5501/CS5503 should be decoupled to their respective grounds using 0.1 µF capacitors. This is illustrated in the System Connection Diagram, Figure 1, at the beginning of this data sheet.

As CMOS devices, the CS5501/CS5503 require that the positive analog supply voltage always be greater than or equal to the positive digital supply voltage. If the voltage on the positive digital supply should ever become greater than the voltage on the positive analog supply, diode junctions in the CMOS structure which are normally reverse-biased will become forward-biased. This may cause the part to draw high currents and experience permanent damage. The connections shown in Figure 1 eliminate this possibility.

To ensure reliable operation, be certain that power is applied to the part before signals at AIN, VREF, or the logic input pins are present. If current is supplied into any pin before the chip is powered-up, latch-up may result. As a system, it is desirable to power the CS5501/CS5503, the voltage reference, and the analog signal conditioning circuitry from the same primary source. If separate supplies are used, it is recommended that the CS5501/CS5503 be powered up first. If a common power source is used for the analog signal conditioning circuitry as well as the A/D converter, this power source should be applied before application of power to the digital logic supply.

The CS5501/CS5503 exhibit good power supply rejection for frequencies within the passband (dc to 10 Hz). Any small offset or gain error caused by long term drift of the power supplies can be removed by recalibration. Above 10 Hz the digital filter will provide additional rejection. When the benefits of the digital filter are added to the regular power supply rejection the effects of line frequency variations (60 Hz) on the power supplies will be reduced greater than 120 dB. If the supply voltages for the CS5501/CS5503 are generated with a dc-dc converter the operating frequency of the dc-dc converter should not operate at the sampling frequency of the CS5501/CS5503 or at integer multiples thereof.

At these frequencies the digital filter will not aid in power supply rejection. See *Anti-Alias Considerations* section of this data sheet.

The recommended system connection diagram for the CS5501/CS5503 is illustrated in Figure 1. Note that any digital logic inputs which are to be unused should be tied to either DGND or the VD+ as appropriate. They should not be left floating; nor should they be tied to some other logic supply voltage in the system.

Power-Up and Initialization

Upon power-up, a calibration cycle must be initiated at the CAL pin to insure a consistent starting condition and to initially calibrate the device. The CAL pin must be strobed high for a minimum of 4 clock cycles. The falling edge will initiate a calibration cycle. A simple power-on reset circuit can be built using a resistor and capacitor (see Figure 16). The resistor and capacitor values should allow for clock or oscillator startup time, and the voltage reference stabilization time.

Due to the devices' low power dissipation and low temperature drift, no warm-up time is required to accommodate any self-heating effects.

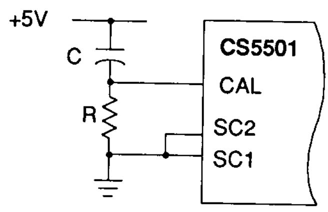


Figure 16. Power-On Reset Circuitry (Self-Calibration Only)

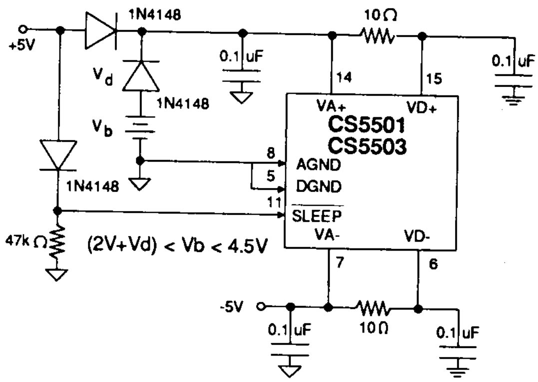


Figure 17. Example Calibration Memory Battery Back-Up Circuit

Sleep Mode

The CS5501/CS5503 include a sleep mode ($\overline{\text{SLEEP}}$ = DGND) which shuts down the internal analog and digital circuitry reducing power consumption to less than 10 µW. All calibration coefficients are retained in memory such that no time is required after "awakening" for recalibration. Still, the CS5501/CS5503 will require time for the digital filter to settle before an accurate reading will occur after a rising edge on $\overline{\text{SLEEP}}$ occurs.

Battery Backed-Up Calibrations

The CS5501/CS5503 use SRAM to store calibration information. The contents of the SRAM will be lost whenever power is removed from the chip. Figure 17 shows a battery back-up scheme that can be used to retain the calibration memory during system down time and/or protect it against intermittent power loss. Note that upon loss of power, the $\overline{\text{SLEEP}}$ input goes low, reducing power consumption to just 10 µW. Lithium cells of 3.6 V are available which average 1750 mA-hours before they drop below the typical 2 V memory-retention specification of the CS5501/CS5503.

When $\overline{\text{SLEEP}}$ is active ($\overline{\text{SLEEP}}$ = DGND), both VD+ and VA+ must remain powered to no less than 2 V to retain calibration memory. The VD- and VA- voltages can be reduced to 0 V but must not be allowed to go above ground potential. The negative supply must exhibit low source impedance in the powered-down state as the current into the VA+ pin flows out the VA- pin. (AGND is only a reference node. No power supply current flows in or out of AGND.) Care should be taken to ensure that logic inputs are maintained at either VD+ ar DGND potential when $\overline{\text{SLEEP}}$ is low.

Note that battery life could be shortened if the +5 V supply drops slowly during power-down. As the supply drops below the battery voltage but not yet below the logic threshold of the $\overline{\text{SLEEP}}$ pin, the battery will be supplying the CS5501/CS5503 at full power (typically 3 mA). Faster transitions at $\overline{\text{SLEEP}}$ can be triggered using a resistive divider or a simple resistor network to generate the $\overline{\text{SLEEP}}$ input from the +5 V supply.

Output Loading Considerations

To maximize performance of the CS5501/CS5503, the output drive currents from the digital output lines should be minimized. It is recommended that CMOS logic gates (4000B, 74HC, etc.) be used to provide minimum loading. If it is necessary to drive an opto-isolator the outputs of the CS5501/CS5503 should be buffered. An easy means of driving the LED of an opto-isolator is to use a 2N7000 or 2N7002 low cost FET.

PIN DESCRIPTIONS

SERIAL INTERFACE MODE SELECT	MODE	1	20	SDATA	SERIAL DATA OUTPUT
CLOCK OUT	CLKOUT	2	19	SCLK	SERIAL CLOCK INPUT/OUTPUT
CLOCK IN	CLKIN	3	18	$\overline{\text{DRDY}}$	DATA READY
SYSTEM CALIBRATION 1	SC1	4	17	SC2	SYSTEM CALIBRATION 2
DIGITAL GROUND	DGND	5	16	$\overline{\text{CS}}$	CHIP SELECT
NEGATIVE DIGITAL POWER	VD-	6	15	VD+	POSITIVE DIGITAL POWER
NEGATIVE ANALOG POWER	VA-	7	14	VA+	POSITIVE ANALOG POWER
ANALOG GROUND	AGND	8	13	CAL	CALIBRATE
ANALOG IN	AIN	9	12	BP/$\overline{\text{UP}}$	BIPOLAR/UNIPOLAR SELECT
VOLTAGE REFERENCE	VREF	10	11	$\overline{\text{SLEEP}}$	SLEEP

* Pinout applies to both DIP and SOIC packages

3

Clock Generator

CLKIN; CLKOUT -Clock In; Clock Out, Pins 3 and 2.

A gate inside the CS5501/CS5503 is connected to these pins and can be used with a crystal or ceramic resonator to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock can be input to the CLKIN pin as the master clock for the device. When not in SLEEP mode, a master clock (CLKIN) should be present at all times.

Serial Output I/O

MODE -Serial Interface Mode Select, Pin 1.

Selects the operating mode of the serial port. If tied to VD- (-5V), the CS5501 will operate in the UART-compatible AC mode for Asynchronous Communication. The SCLK pin will operate as an *input* to set the data rate, and data will transmit *formatted* with one start and two stop bits. If MODE is tied to DGND, the CS5501/CS5503 will operate in the SEC (Synchronous External-Clocking) mode, with the SCLK pin operating as an *input* and the output appearing MSB-first. If MODE is tied to VD+ (+5V), the CS5501/CS5503 will operate in its SSC (Synchronous Self-Clocking) mode, with SCLK providing a serial clock *output* of CLKIN/4 (25% duty-cycle).

$\overline{\text{DRDY}}$ -Data Ready, Pin 18.

$\overline{\text{DRDY}}$ goes low every 1024 cycles of CLKIN to indicate that new data has been placed in the output port. $\overline{\text{DRDY}}$ goes high when all the serial port data is clocked out, when the serial port is being updated with new data, when a calibration is in progress, or when $\overline{\text{SLEEP}}$ is low.

$\overline{\text{CS}}$ -Chip Select, Pin 16.

An input which can be enabled by an external device to gain control over the serial port of the CS5501/CS5503.

SDATA -Serial Data Output, Pin 20.

Data from the serial port will be output from this pin at a rate determined by SCLK and in a format determined by the MODE pin. It furnishes a high impedance output state when not transmitting data.

SCLK -Serial Clock Input/Output, Pin 19.

A clock signal at this pin determines the output rate of the data from the SDATA pin. The MODE pin determines whether the SCLK signal is an input or output. SCLK may provide a high impedance output when data is not being output from the SDATA pin.

Calibration Control Inputs

SC1; SC2 -System Calibration 1 and 2, Pins 4 and 17.

Control inputs to the CS5501/CS5503's calibration microcontroller for calibration. The state of SC1 and SC2 determine which of the calibration modes is selected for operation (see Table 2).

BP/$\overline{UP}$ -Bipolar/Unipolar Select, Pin 12.

Determines whether the CS5501/CS5503 will be calibrated to measure bipolar (BP/$\overline{UP}$ = VD+) or unipolar (BP/$\overline{UP}$ = DGND) input signals. Recalibration is necessary whenever the state of BP/$\overline{UP}$ is changed.

CAL -Calibrate, Pin 13.

If brought high for 4 clock cycles or more, the CS5501/CS5503 will reset and upon returning low a full calibration cycle will begin. The state of SC1, SC2, and BP/$\overline{UP}$ when CAL is brought low determines the type and length of calibration cycle initiated (see Table 2). Also, a single CAL signal can be used to strobe the CAL pins high on several CS5501/CS5503's to synchronize their operation. Any spurious glitch on this pin may inadvertently place the chip in Calibration mode.

Other Control Input

$\overline{SLEEP}$ -Sleep, Pin 11.

When brought low, the CS5501/CS5503 will enter a low-power state. When brought high again, the CS5501/CS5503 will resume operation without the need to recalibrate. After $\overline{SLEEP}$ goes high again, the device's output will settle to within +0.0007% of the analog input value within $1.3/f_{-3dB}$, where f_{-3dB} is the passband frequency. The $\overline{SLEEP}$ input can also be used to synchronize sampling and the output updates of several CS5501/CS5503's.

Analog Inputs

VREF -Voltage Reference, Pin 10.

Analog reference voltage input.

AIN -Analog Input, Pin 9.

Power Supply Connections

VD+ -Positive Digital Power, Pin 15.
Positive digital supply voltage. Nominally +5 volts.

VD- -Negative Digital Power, Pin 6.
Negative digital supply voltage. Nominally -5 volts.

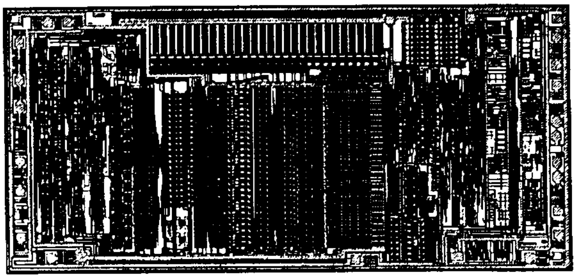
DGND -Digital Ground, Pin 5.
Digital ground.

VA+ -Positive Analog Power, Pin 14.
Positive analog supply voltage. Nominally +5 volts.

VA- -Negative Analog Power, Pin 7.
Negative analog supply voltage. Nominally -5 volts.

AGND -Analog Ground, Pin 8.
Analog ground.

DIE INFORMATION



CS5501-YU
CS5503-YU

Crystal Semiconductor Procedure 42AA00007 outlines the General Requirements for Die Sales. The document includes information on wafer fabrication, manufacturing flow, screening and inspection procedures, packing, shipping, and change notification.

Assembly Information

1. Die size shall be 0.149" by 0.303" (± 0.002")

2. The die are suited for die attach through either eutectic or adhesive means. When eutectic die attach is used, Crystal Semiconductor recommends either a 99.9% Au or 98% Au/2% Si preform of the appropriate size. The backside of the die should be electrically connected to VA+.

3. Die thickness shall be 0.0175" ±0.0035". If tighter tolerances are required, contact the factory.

4. The maximum number of die per waffle pack carrier is 28.

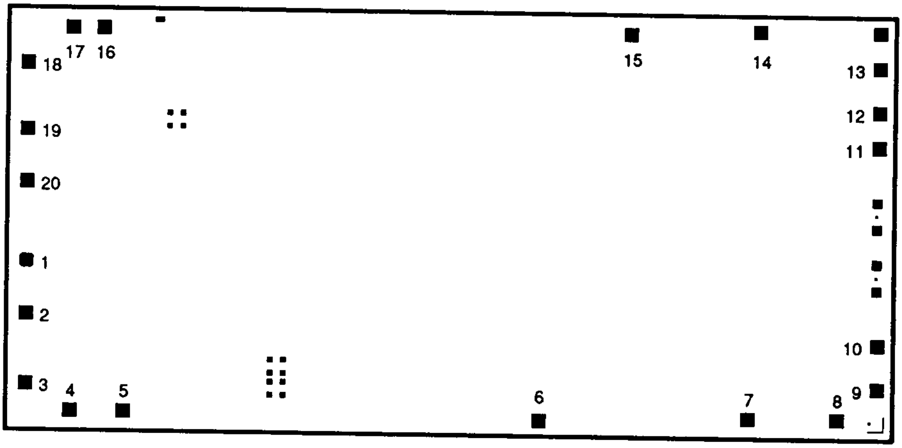
5. The cavity dimensions for each die within the waffle pack are .180" by .330" (Waffle Pack Type H20-179329).

6. The die require no particular bonding sequence.

7. Each pin of the CS5501 and CS5503 has ESD and latch-up protection circuitry. Still, Crystal Semiconductor strongly recommends proper handling procedures and in-circuit application.

8. Technical constraints limit the viability of accurate performance measurements of precision analog IC's at wafer probe. Although high yield to the limits listed in the specification tables is anticipated, no guarantee is given for unpackaged die product.

CS5501-YU, CS5503-YU Bonding Diagram



1	-	MODE	11	-	$\overline{\text{SLEEP}}$
2	-	CLKOUT	12	-	BP/$\overline{\text{UP}}$
3	-	CLKIN	13	-	CAL
4	-	SC1	14	-	VA+
5	-	DGND	15	-	VD+
6	-	VD-	16	-	$\overline{\text{CS}}$
7	-	VA-	17	-	SC2
8	-	AGND	18	-	$\overline{\text{DRDY}}$
9	-	AIN	19	-	SCLK
10	-	VREF	20	-	SDATA

SPECIFICATION DEFINITIONS

Linearity Error

The deviation of a code from a straight line which connects the two endpoints of the A/D Converter transfer function. One endpoint is located 1/2 LSB below the first code transition and the other endpoint is located 1/2 LSB beyond the code transition to all ones. Units in percent of full-scale.

Differential Linearity

The deviation of a code's width from the ideal width. Units in LSB's.

Full-Scale Error

The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSBs.

Unipolar Offset

The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/$\overline{UP}$ low). Units in LSBs.

Bipolar Offset

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSBs.

Bipolar Negative Full-Scale Error

The deviation of the first code transition from the ideal when in bipolar mode (BP/$\overline{UP}$ high). The Ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSBs.

Positive Full-Scale Input Overrange

The absolute maximum positive voltage allowed for either accurate system calibration or accurate conversions. Units in volts.

Negative Full-Scale Input Overrange

The absolute maximum negative voltage allowed for either accurate system calibration or accurate conversions. Units in volts.

Offset Calibration Range

The CS5501/CS5503 calibrate their offset to the voltage applied to the AIN pin when in system calibration mode. The first code transition defines Unipolar Offset when BP/$\overline{UP}$ is low and the mid-scale transition defines Bipolar Offset when BP/$\overline{UP}$ is high. The Offset Calibration Range specification indicates the range of voltages applied to AIN that the CS5501 or CS5503 can accept and still calibrate offset accurately. Units in volts.

Input Span

The voltages applied to the AIN pin in system-calibration schemes define the CS5501/CS5503 analog input range. The Input Span specification indicates the minimum and maximum input spans from zero-scale to full-scale in unipolar, or from positive full scale to negative full scale in bipolar, that the CS5501/CS5503 can accept and still calibrate gain accurately. Units in volts.

Ordering Guide

Model Number	No. of Bits	Linearity Error (Max)	Temperature Range	Package
CS5501-AS	16	0.003%	-40 to +85°C	20 Lead SOIC
CS5501-BS	16	0.0015%	-40 to +85°C	20 Lead SOIC
CS5501-AP	16	0.003%	-40 to +85°C	20 Pin Plastic DIP
CS5501-BP	16	0.0015%	-40 to +85°C	20 Pin Plastic DIP
CS5501-CP	16	0.0012%	-40 to +85°C	20 Pin Plastic DIP
CS5501-SD	16	0.003%	-55 to +125°C	20 Pin Cerdip
CS5501-TD	16	0.0015%	-55 to +125°C	20 Pin Cerdip
CS5501-YU	16			Unpackaged Die
CDB5501	Evaluation Board			
CS5503-AS	20	0.003%	-40 to +85°C	20 Lead SOIC
CS5503-BS	20	0.0015%	-40 to +85°C	20 Lead SOIC
CS5503-AP	20	0.003%	-40 to +85°C	20 Pin Plastic DIP
CS5503-BP	20	0.0015%	-40 to +85°C	20 Pin Plastic DIP
CS5503-CP	20	0.0012%	-40 to +85°C	20 Pin Plastic DIP
CS5503-SD	20	0.003%	-55 to +125°C	20 Pin Cerdip
CS5503-TD	20	0.0015%	-55 to +125°C	20 Pin Cerdip
CS5503-YU	20			Unpackaged Die
CDB5503	Evaluation Board			

APPENDIX A: APPLICATIONS

Parallel Interface

Figures A1 and A2 show two serial-to-parallel conversion circuits for interfacing the CS5501 in its SSC mode to 16- and 8-bit systems respectively. Each circuit includes an optional 74HCT74 flip-flop to latch $\overline{DRDY}$ and generate a level-sensitive interrupt.

Both circuits require that the parallel read process be synchronized to the CS5501's operation. That is, the system must not try to enable the registers' parallel output while they are accepting serial data from the CS5501. The CS5501's $\overline{DRDY}$ falls just prior to serial data transmission and returns high as the last bit shifts out. Therefore, the $\overline{DRDY}$ pin can be polled for a *rising* transition directly, or it can be latched as a level-sensitive interrupt.

With the $\overline{CS}$ input tied low the CS5501 will shift out every available sample (4kHz word rate with a 4MHz master clock). Lower output rates (and interrupt rates) can be generated by dividing down the $\overline{DRDY}$ output and applying it to $\overline{CS}$.

Totally asynchronous interfaces can be created using a *Shift Data* control signal from the system which enables the CS5501's $\overline{CS}$ input and/or the shift registers' S1 inputs. The $\overline{DRDY}$ output can then be used to disable serial data transmission once an output word has been fully registered.

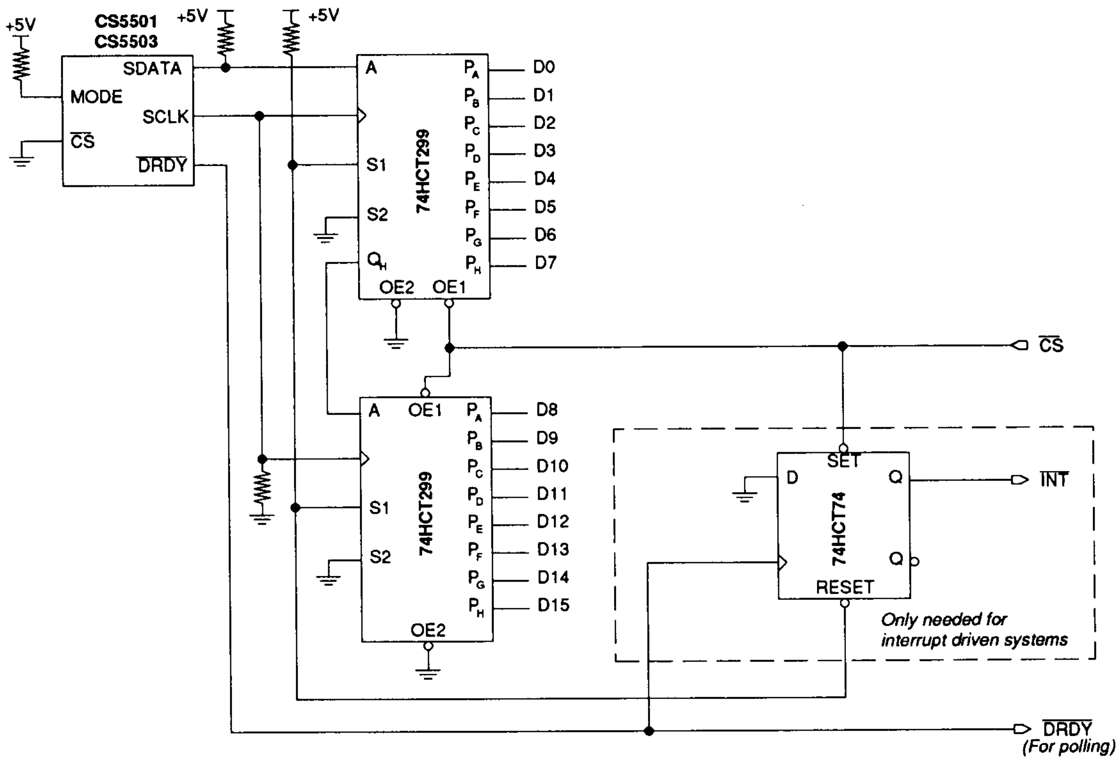


Figure A1. 16-bit Parallel Interface

In such asynchronous configurations the CS5501 is operated much like a successive-approximation converter with a *Convert* signal and a subsequent read cycle.

If it is required to latch the 16-bit data, then 2 74HC595 8-bit "shift register with latch" parts may be used instead of 74HC299's.

Serial Interfaces

Figures A3 to A8 offer both the hardware and software interfaces to several industry-standard microcontrollers using the CS5501's SEC and AC output modes. In each instance a system initialization routine is provided which configures the controller's I/O ports to accept the CS5501's serial data and clock outputs and/or generate its own serial clock. The routine also sets the CS5501 into a known state.

For each interface, a second subroutine is also provided which will collect one complete 16-bit output word from the CS5501. Figure A5 illustrates the detailed timing throughout the subroutine for one particular interface - the COPS family interface of Figure A4.

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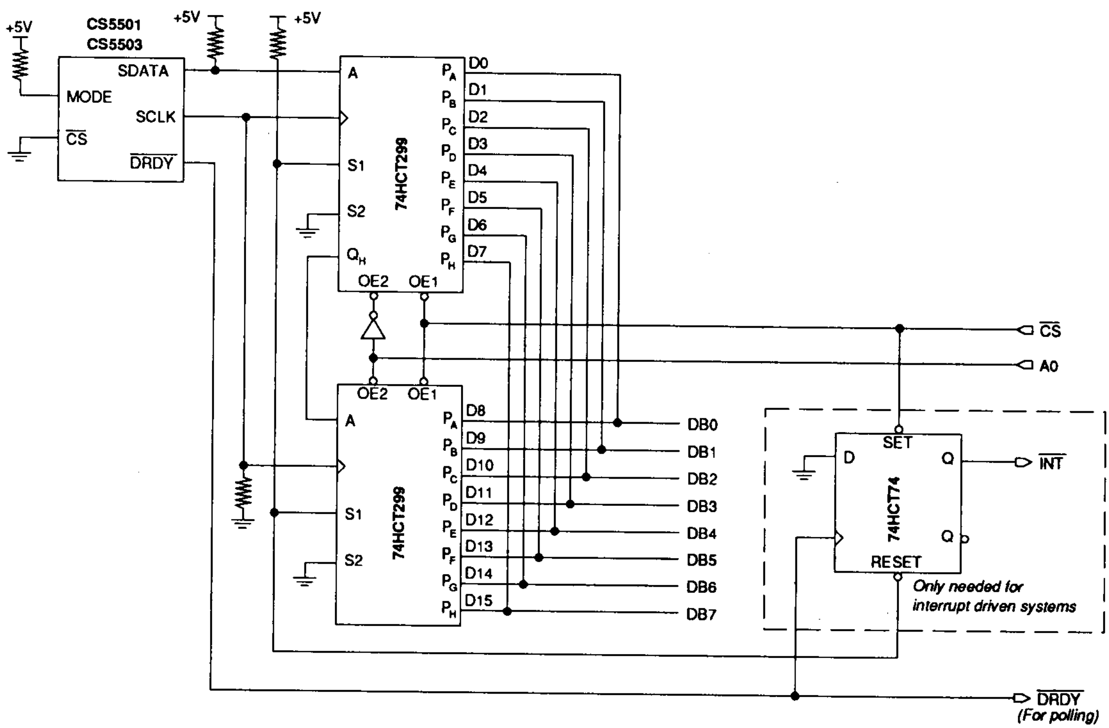

Figure A2. 8-Bit Parallel Interface

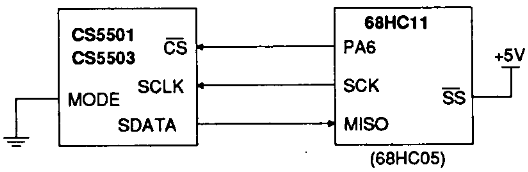

Figure A3. 68HC11/CS5501 Serial Interface

Notes:

1. CS5501 in *Synchronous External Clocking* mode.
2. Using 68HC11's SPI port. (Can use SCI and CS5501's Asynchronous mode.)
3. Maximum bit rate is 1.05 Mbps.

Assumptions:

1. PA6 used as CS.
2. 68HC11 in single-chip mode.
3. Receive data via polling.
4. Normal equates for peripheral registers.
5. Data returned in register D.

Initial Code:

```
SPINIT: PSHA                    ; Store temporary copy of A
        LDAA  #%x1xxxxxx        ; Bit 6 = 1, all others are don't cares
        STAA  PORTA             ; CS = 1, inactive; deselect CS5501
        LDAA  #$10              ;
        STAA  SPCR              ; Disable serial port
        LDAA  #%xx0110xx        ; SS-input, SCK-output,
                                ;  MOSI-output, MISO-input
        STAA  DDRD              ; Data direction register for port D
        LDAA  #$50              ; Enable serial port, CMOS outputs,
        STAA  SPCR              ;  master, highest clock rate (int. clk/2
        LDAA  SPSR              ;
        LDAA  SPDR              ; Bogus read to clr port and SPIF flag
        PULA                    ; Restore A
        RTS                     ;
```

Code to get word of data:

```
SP_IN:  LDAA  #%x0xxxxxx        ;
        STAA  PORTA             ; CS = 0, active; select CS5501
        STAA  SPDR              ; Put data in serial port to start clk
WAIT1:  LDAA  SPSR              ; Get port status
        BPL   WAIT1             ; If SPIF (MSB) 0, no data yet, wait
        LDAA  SPDR              ; Put most significant byte in A
        STAA  SPDR              ; Start serial port for second byte
WAIT2:  LDAB  SPSR              ; Get port status
        BPL   WAIT2             ; If SPIF (MSB) 0, no data yet, wait
        LDAB  #%x1xxxxxx        ;
        STAB  PORTA             ; CS = 1, inactive; deselect CS5501
        LDAB  SPDR              ; Put least significant byte in B
        RTS                     ;
```

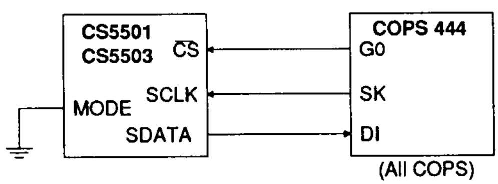

Figure A4. COPS/CS5501 Interface

Notes:

1. CS5501 in *Synchronous External Clocking* mode.
2. COPS 444 max baud = 62.5 kbps. (Others = 500 kbps)
3. See timing diagram for detailed timing.

Assumptions:

1. G0 used as CS.
2. Register 0 (upper four nibbles) used to store 16-bit word.

Initial Code:

```
SPINIT:  OGI   15        ; CS = 1, inactive; deselect CS5501
         RC              ; Reset carry, used in next
         XAS             ;  instruction to turn SK off
```

Code to get word of data:

```
SP_IN:   LBI   0,12      ; Point to start of data
                         ;  storage location
         SC              ; Set carry - enables SK in
                         ;  XAS instruction
         OGI   14        ; CS = 0, active; select CS5501
         LEI   0         ; Shift register mode, S0 = 0
         XAS             ; Start clocking serial port
         NOP             ;
         NOP             ; Wait for (first) M.S. nibble
GETNIB:  NOP             ;
         XAS             ; Get nibble of data from SIO
         XIS             ; Put nibble in memory, inc. pointer,
         JP    GETNIB    ;  if overflow, jump around this inst.
         RC              ; Reset carry - disables SK in XAS
                         ;  instruction
         XAS             ; Bogus read - stops SK
         OGI   15        ; CS = 1, inactive; deselect CS5501
         RET             ;
```

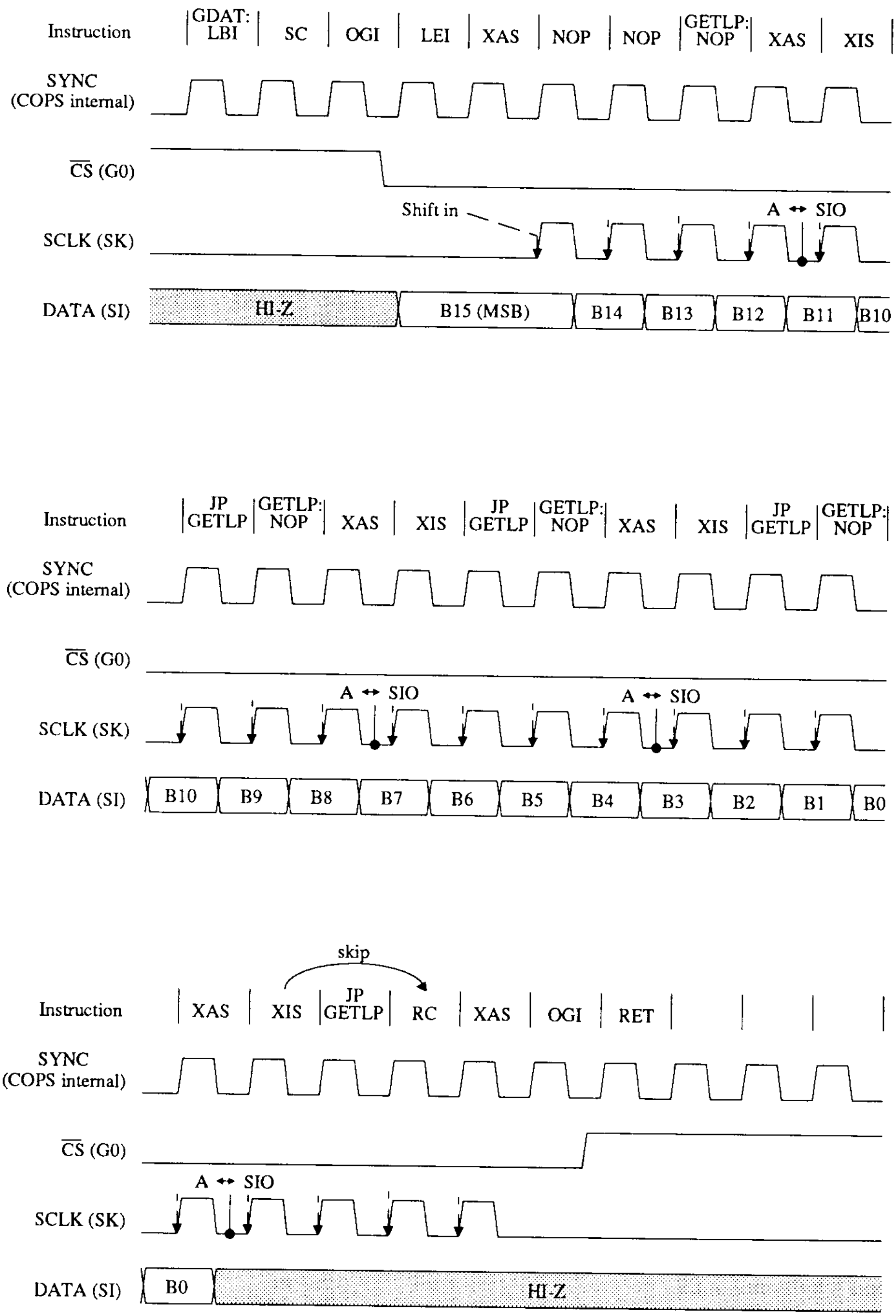

Figure A5. Serial Timing Example - COPS

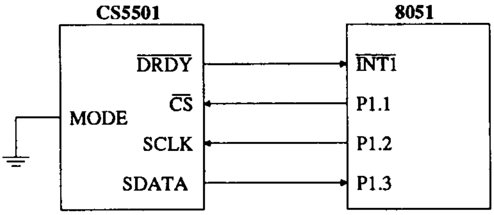

Figure A6. MCS51 (8051) /CS5501 Serial Interface

Notes:

1. CS5501 in *Synchronous External Clocking* mode.
2. Interrupt driven I/O on 8051 (For polling, connect DRDY to another port pin).

Assumptions:

1. INT1 external interrupt used.
2. Register bank 1, R6, R7 used to store data word, R7 MSbyte.
3. EA enabled elsewhere.

Initial Code:

```
CS       EQU   P1.1
SCLK     EQU   P1.2
DATA     EQU   P1.3
SPINIT:  CLR   EX1              ; Disable INT1
         SETB  IT1              ; Set INT1 for falling edge triggered
         SETB  DATA             ; Set DATA to be input pin
         SETB  CS               ; CS = 1; deselect CS5501
         CLR   SCLK             ; SCLK low
         SETB  EX1              ; Enable INT1 interrupt
```

Code to get word of data:

```
         ORG 0003H
         LJMP  GETWD            ; Interrupt vector
GETWD:   PUSH  PSW              ; Save temp. copy
         PUSH  A                ; Save temp. copy
         MOV   PSW,#08          ; Set register bank 1 active
         MOV   R6,#8            ; number of bits in a byte
         CLR   CS               ; CS = 0; select CS5501
MSBYTE:  SETB  SCLK             ; Toggle SCLK high
         MOV   C,DATA           ; Put bit of data into carry bit
         CLR   SCLK             ; Toggle SCLK low; next data bit
         RLC   A                ; Shift DATA bit into A register
         DJNZ  R6,MSBYTE        ; Dec. R6, if not 0, get another bit
         MOV   R7,A             ; Put MSbyte into R7
         MOV   R6,#8            ; Reset R6 to number of bits in byte
LSBYTE:  SETB  SCLK             ; Toggle SCLK high
         MOV   C,DATA           ; Put bit of data into carry bit
         CLR   SCLK             ; Toggle SCLK low; next data bit
         RLC   A                ; Shift DATA bit into A register
         DJNZ  R6,LSBYTE        ; Dec. R6, if not 0, get another bit
         MOV   R6,A             ; Put LSbyte into R6
         SETB  CS               ; CS = 1; deselect CS5501
         POP   A                ; Restore original value
         POP   PSW              ; Restore original value
         RETI
```

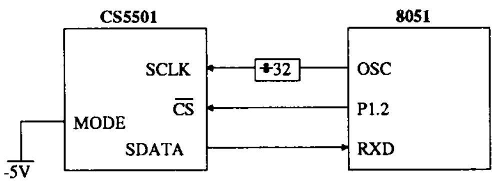

Figure A7. MCS51 (8051) /CS5501 UART Interface

Notes:

1. CS5501 in Asynchronous (UART-like) mode.
2. 8051 in mode 2, with OSC = 12 MHz, max baud = 375 kbps.

Assumptions:

1. P1.2 (port 1, bit 2) used as $\overline{CS}$.
2. Using serial port mode 2, Baud rate = OSC/32.

(Assumptions cont.)

3. Word received put in A (ACC) and B registers, A = MSbyte.
4. No error checking done.
5. Equates used for peripheral names.

Initial Code:

```
SPINIT:  SETB  SMOD             ; Set SMOD = 1, baud = OSC/32
         SETB  P1.2             ; CS = 1, inactive
         MOV   SCON,#10010000B    ; Enable serial port mode 2,
                                ;  receiver enabled, transmitter disabled
         CLR   ES               ; Disable serial port interrupts (polling)
         RET                    ;
```

Code to get word of data:

```
SP_IN:   CLR   P1.2             ; CS = 0, active; select CS5501
         JNB   RI,$             ; Wait for first byte
         CLR   RI               ;
         MOV   A,SBUF           ; Put most significant byte in A
         JNB   RI,$             ; wait for second byte
         CLR   RI               ;
         MOV   B,SBUF           ; Put least significant byte in B
         SETB  P1.2             ; CS = 1, inactive; deselect CS5501
         RET                    ;
```

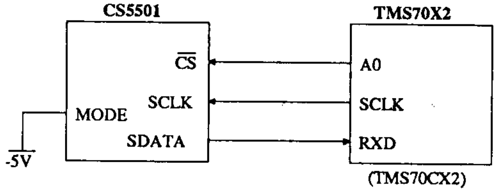

Figure A8. TMS70X2/CS5501 Serial Interface

Notes:

1. CS5501 in Asynchronous (UART-like) mode.
2. TMS70X2 in Isosynchronous mode.
3. TMS70X2 with 8 MHz master clock has max baud =1.0 Mbps.

Assumptions:

1. A0 used as $\overline{CS}$.
2. Receive data via polling.
3. Word received put in A and B upon return, A = MS byte.
4. No error checking done.
5. Normal equates for peripheral registers.

Initial Code:

```
SPINIT: DINT                        ;
        MOVP %1,ADDR                ; A port is output
        MOVP %1,APORT               ; A0 = 1, (CS is inactive)
        MOVP %0,P17                 ;
        MOVP %>10,SCTLO             ; Resets port errors
        MOVP %?x1x01101,SMODE       ; Set port for Isosync,
        MOVP %?00x1110x,SCTLO       ;     8 bits, no parity
        MOVP %07,T3DATA             ; Max baud rate
        MOVP %?01000000,SCTL1       ; No multiprocessor;
                                    ;     prescale = 4
        MOVP %0,IOCNT1              ; Disable INT4 - will poll port
        PUSH A                      ; Store original
        MOVP RXBUF,A                ; Bogus read to clr receiver port flag
        POP  A                      ; Restore original
        EINT                        ;
        RET                         ;
```

Code to get word of data:

```
SP_IN:  MOVP  %0,APORT              ; CS active, select CS5501
WAIT1   BTJZP %2,SSTAT,WAIT1        ; Wait to receive first byte
        MOVP  RXBUF,A               ; Put most significant byte in reg. A
WAIT2   BTJZP %2,SSTAT,WAIT2        ; Wait to receive second byte
        MOVP  RXBUF,B               ; Put least significant byte in reg. B
        MOVP  %1,APORT              ; CS inactive, deselect CS5501
        RET                         ;
```