



# 256Kx8 Monolithic SRAM

## FEATURES

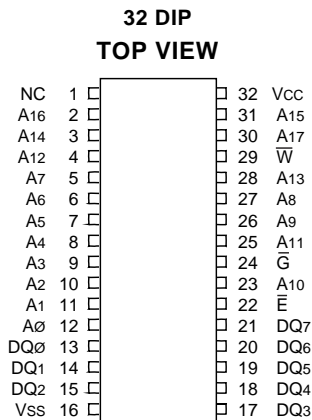
- 256Kx8 CMOS Static
- Random Access Memory
  - Access Times of 70, 85, 100ns
  - Data Retention Function (LP Versions)
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- JEDEC Approved Pinout
  - 32 pin Ceramic DIP, 0.6 mils wide (Package 9)
- Single +5V ( $\pm 10\%$ ) Supply Operation

The EDI88257C is a 2 Megabit 256Kx8 bit Monolithic CMOS Static RAM.

The 32 pin DIP pinout adheres to the JEDEC standard for the two megabit device, and is a pin replacement for the 256Kx8 module, EDI88257C. The device is upgradeable to the 512Kx8 SRAM, the EDI88512C. Pin 1 becomes the higher order address.

A Low Power version, EDI88257LP, offers a data retention function for battery back-up operation. Military product is available compliant to Appendix A of MIL-PRF-38535.

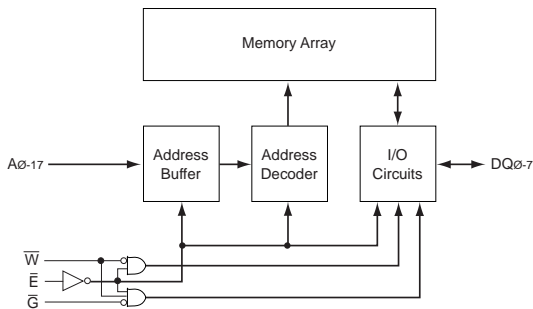
FIG. 1 PIN CONFIGURATION



## PIN DESCRIPTION

A0-17	Address Inputs
$\bar{W}$	Write Enable
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
DQ0-7	Data Inputs/Outputs
Vcc	Power (+5V $\pm 10\%$ )
Vss	Ground
NC	Not Connected

## BLOCK DIAGRAM





## ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on any pin relative to Vss	-0.5 to 7.0	V
<b>Operating Temperature TA (Ambient)</b>		
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Ceramic	-65 to +150	°C
Power Dissipation	1	W
Output Current	20	mA
Junction Temperature, Tj	175	°C

### NOTE:

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE

Parameter	Symbol	Condition	Max	Unit
Address Lines	C <sub>I</sub>	V <sub>IN</sub> = V <sub>CC</sub> or V <sub>SS</sub> , f = 1.0MHz	30	pF
Data Lines	C <sub>D/Q</sub>	V <sub>OUT</sub> = V <sub>CC</sub> or V <sub>SS</sub> , f = 1.0MHz	14	pF

These parameters are sampled, not 100% tested.

## DC CHARACTERISTICS

(V<sub>CC</sub> = 5V, T<sub>A</sub> = +25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = 0V to V <sub>CC</sub>	—	—	±10	µA	
Output Leakage Current	I <sub>LO</sub>	V <sub>I/O</sub> = 0V to V <sub>CC</sub>	—	—	±10	µA	
Operating Power Supply Current	I <sub>CC1</sub>	$\bar{W}, \bar{E} = V_{IL}, I_{I/O} = 0mA, \text{Min Cycle (70-100ns)}$	—	45	75	mA	
Standby (TTL) Power Supply Current	I <sub>CC2</sub>	$\bar{E} \geq V_{IH}, V_{IN} \leq V_{IL}, V_{IN} \geq V_{IH}$	—	3	10	mA	
Full Standby Power Supply Current	I <sub>CC3</sub>	$\bar{E} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V \text{ or } V_{IN} \leq 0.2V$	C	—	—	5	mA
			LP	—	—	1	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1mA	—	—	0.4	V	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA	2.4	—	—	V	

## TRUTH TABLE

$\bar{G}$	$\bar{E}$	$\bar{W}$	Mode	Output	Power
X	H	X	Standby	High Z	I <sub>CC2</sub> , I <sub>CC3</sub>
H	L	H	Output Deselect	High Z	I <sub>CC1</sub>
L	L	H	Read	Data Out	I <sub>CC1</sub>
X	L	L	Write	Data In	I <sub>CC1</sub>

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Supply Voltage	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> + 0.5	V
Input Low Voltage	V <sub>IL</sub>	-0.3	—	+0.8	V

## AC TEST CONDITIONS

Figure 1

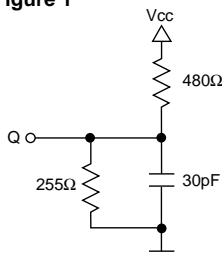
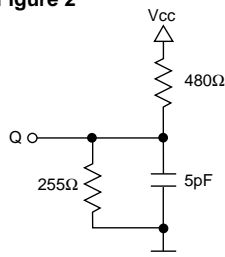


Figure 2



Input Pulse Levels	V <sub>SS</sub> to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t<sub>EH0Z</sub>, t<sub>GH0Z</sub> and t<sub>wLOZ</sub>, C<sub>L</sub> = 5pF Figure 2)



**AC CHARACTERISTICS – READ CYCLE**

(V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tAVAV	tRC	70		85		100		ns
Address Access Time	tAVQV	tAA		70		85		100	ns
Chip Select Access Time	tELQV	tACS		70		85		100	ns
Chip Select to Output in Low Z (1)	tELQX	tCLZ	10		10		10		ns
Chip Disable to Output in High Z (1)	tEHQZ	tCHZ		25		30		30	ns
Output Hold from Address Change	tAVQX	tOH	10		10		10		ns
Output Enable to Output Valid	tGLQV	tOE		35		45		50	ns
Output Enable to Output in Low Z (1)	tGLQX	tOLZ	5		5		5		ns
Output Disable to Output in High Z (1)	tGHQZ	tOHZ	0	25	0	30	0	30	ns

1. This parameter is guaranteed by design but not tested.

**AC CHARACTERISTICS – WRITE CYCLE**

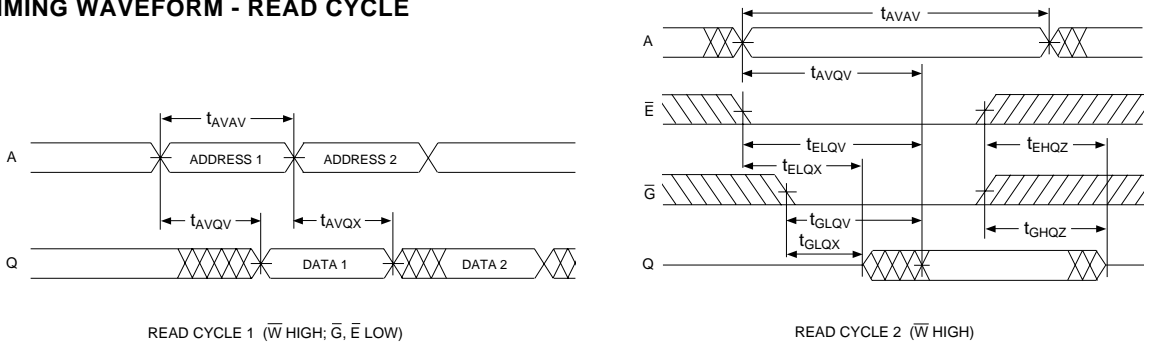
(V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	70		85		100		ns
Chip Select to End of Write	tELWH	tCW	60		70		80		ns
	tELEH	tCW	60		70		80		ns
Address Setup Time	tAVWL	tAS	0		0		0		ns
	tAVEL	tAS	0		0		0		ns
Address Valid to End of Write	tAVWH	tAW	65		70		80		ns
	tAVEH	tAW	65		70		80		ns
Write Pulse Width	tWLWH	tWP	50		55		60		ns
	tWLEH	tWP	50		55		60		ns
Write Recovery Time	tWHAX	tWR	0		0		0		ns
	tEHAX	tWR	0		0		0		ns
Data Hold Time	tWHDX	tDH	0		0		0		ns
	tEHDX	tDH	0		0		0		ns
Write to Output in High Z (1)	tWLQZ	tWHZ	0	25	0	30	0	30	ns
Data to Write Time	tDVWH	tDW	40		40		40		ns
	tDVEH	tDW	30		35		40		ns
Output Active from End of Write (1)	tWHQX	tWLZ	5		5		5		ns

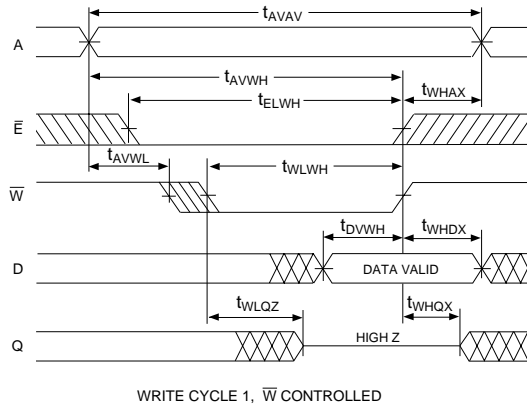
1. This parameter is guaranteed by design but not tested.



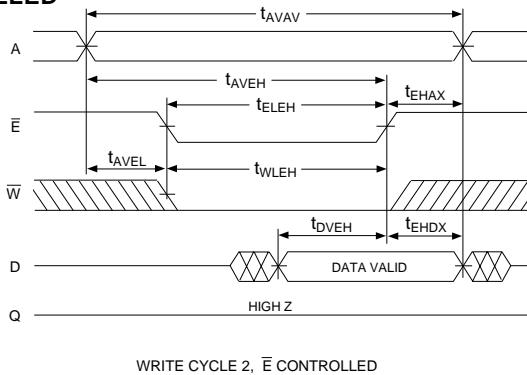
**FIG. 2**  
**TIMING WAVEFORM - READ CYCLE**



**FIG. 3**  
**WRITE CYCLE -  $\bar{W}$  CONTROLLED**



**FIG. 4**  
**WRITE CYCLE -  $\bar{E}$  CONTROLLED**

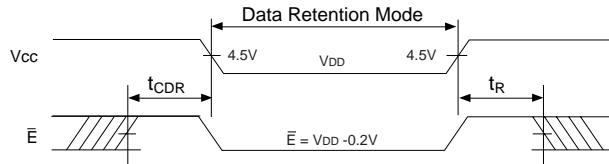




**DATA RETENTION CHARACTERISTICS (EDI88257LP ONLY)**  
(TA = -55°C to +125°C)

Characteristic Low Power Version only	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V <sub>DD</sub>	V <sub>DD</sub> = 2.0V	2	–	–	V
Data Retention Quiescent Current	I <sub>CCDR</sub>	$\bar{E} \geq V_{DD} - 0.2V$	–	–	185	μA
Chip Disable to Data Retention Time	T <sub>CDR</sub>	V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V	0	–	–	ns
Operation Recovery Time	T <sub>R</sub>	or V <sub>IN</sub> ≤ 0.2V	T <sub>AVAV</sub>	–	–	ns

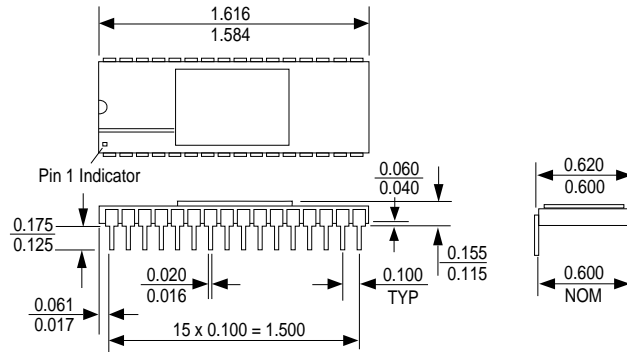
**FIG. 5**  
**DATA RETENTION -  $\bar{E}$  CONTROLLED**



DATA RETENTION,  $\bar{E}$  CONTROLLED



PACKAGE 9: 32 PIN SIDEBRAZED CERAMIC DIP (600mils wide)



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

