MT9071

Quad T1/E1/J1 Transceiver

Preliminary Information

Features

- 4 T1/E1/J1 framers and longhaul/shorthaul LIUs
- LIU sensitivity is 36dB in T1 and 40dB in E1
- Internal reference switching PLL with holdover capability
- One timeslot assignable HDLC per framer
- Comprehensive alarm detection, performance monitoring and error insertion functions
- 2.048Mbit/s or 8.192Mbit/s ST-BUS interface
- 3.3V operation with 5V tolerant inputs
- Intel or Motorola non-multiplexed 16-bit microprocessor port
- JTAG boundary scan

Applications

- T1/E1 add/drop multiplexers
- Access networks
- Primary rate ISDN nodes
- Digital Cross-connect Systems (DCS)

Ordering Information

MT9071AB   128 Pin LQFP
MT9071AV   256 Pin LBGA
-40 to +85°C

Description

The MT9071 is a multiport T1/E1/J1 transceiver that integrates four feature rich T1/E1/J1 framers, four longhaul / shorthaul LIUs and four HDLCs. The internal PLL can use any of the LIUs or an external signal as its source of network timing; the timing source can be changed without loss of synchronization.

The MT9071 is software selectable between T1, E1 or J1 modes and meets the latest relevant recommendations and standards from Telcordia, ANSI, ETSI and the ITU. An extensive suite of features makes the MT9071 very flexible and suitable for a wide variety of applications around the globe.
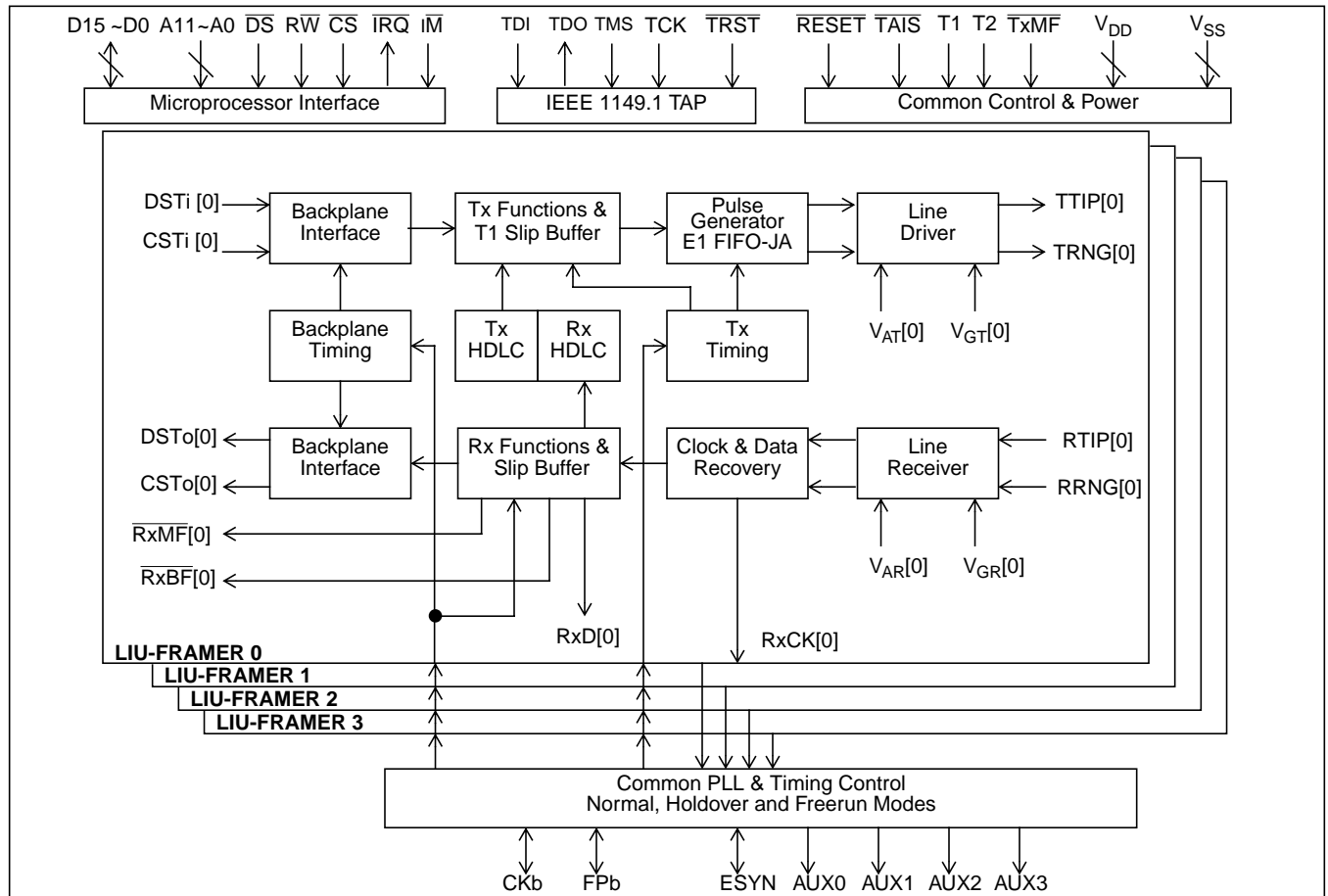

Figure 1 - MT9071 Functional Block

MT9071 Detailed Feature Summary

Standards Compliance and Support

<u>T1/J1 Mode</u>

ANSI:
T1.102, T1.231
T1.403, T1.408

AT&T:
TR 62411, PUB43801

Telcordia:
GR-303-CORE

ITU-T:
G.802

TTC:
JT-G703, JT-G704
JT-G706

<u>E1 Mode</u>

ETSI:
TBR4, TBR13, ETS 300 166
ETS 300 233, ETS 300 324 (V5.1)
ETS 300 347 (V5.2)

ITU-T:
G.703, G.704, G.706, G.711, G.732
G.775, G.796, G.823, I.431
G.964 (5.1), G.965 (V5.2)

Line Interface Unit (LIU)

- Automatically adapts to long or short loop lengths
- T1 and E1 modes use the same 1:2.42 transmit and 1:1 receive transformers
- Programmable pulse shapes and pulse amplitudes
- Automatic or manual receiver equalization
- LIU output is disabled at power-up until enabled by software
- Input pin to force transmission of AIS

<u>T1/J1 Mode</u>

- Reliably recovers signals with cable attenuation up to 36dB @ 772 kHz

- Transmit pulse meets T1.403 and T1.102 pulse templates

- Receiver tolerates jitter as required by AT&T TR62411

- Transmit Pre-equalization and Line Build Out options:

    0-133 feet
    133-266 feet
    266-399 feet
    399-533 feet
    533-655 feet
    -7.5dB
    -15dB
    -22.5dB

<u>E1 Mode</u>

- Reliably recovers signals with cable attenuation up to 40 dB @ 1024 kHz

- Transmit pulse meets G.703 pulse template

- Receiver tolerates jitter as required by ETSI TBR4 and G.823

Line Codes

T1/J1 Mode

- AMI
- Optional B8ZS
- Pulse density enforcement
- Forced ones stuffing (bit 7 of a DS0)
- GTE zero suppression code
- Bell zero suppression code
- DDS zero suppression code

E1 Mode

- AMI
- Optional HDB3

Phase Lock Loop

- Accepts two references
- Limits change in output phase while switching between references (Maximum Time Interval Error)
- Optionally limits the rate of change of output phase (phase slope)
- Meets the jitter transfer requirements of AT&T TR62411
- Meets the jitter transfer requirements of ETSI TBR4
- Meets requirements of Telecordia GR-1244-CORE Stratum 4E
- Attenuates jitter and wander from 1.9Hz
- Intrinsic jitter less than 0.02UI
- Operates in the following modes:
    Free Run
    Line Synchronization
    System Bus Synchronization
    External Synchronization
    Holdover

Access and Control

- A 16-bit parallel Motorola or Intel non-multiplexed microprocessor interface is used to access the control and status registers.

Backplane Interfaces
- 2.048Mbit/s or 8.192Mbit/s ST-BUS
- CSTo/CSTi pins can be used to access the receive/transmit signaling data
- RxD pin can be used to access the entire B8ZS/HDB3 decoded receive stream without the slip buffer

T1/J1 Mode

- PCM24 channels 1-24 are mapped to ST-BUS channels 0-23 respectively

- The framing-bit is mapped to ST-BUS channel 31

E1 Mode

- PCM30 timeslots 0-31 are mapped to ST-BUS channels 0-31 respectively

Data Link

<u>T1/J1 Mode</u>

- Three methods are provided to access the datalink:
  1. RxD pin supports receive datalink
  2. Bit Oriented Messages are supported via internal registers
  3. An internal HDLC can be assigned to transmit/receive over the FDL in ESF mode

<u>E1 Mode</u>

- Two methods are provided to access the datalink:
  1. RxD pin supports receive datalink over the Sa4~Sa8 bits
  2. An internal HDLC can be assigned to transmit/receive data via the Sa4~Sa8 bits
- In transparent mode, if the Sa4 bit is used for an intermediate datalink, the CRC-4 remainder can be updated to reflect changes to the Sa4 bit

One Embedded Floating HDLC per Framer

- Flag generation and Frame Check Sequence (FCS) generation and detection, zero insertion and deletion
- Continuous flags, or continuous 1s are transmitted between frames
- Transmit frame-abort
- Invalid frame handling:
    Frames yielding an incorrect FCS are tagged as bad packets
    Frames with fewer than 25 bits are ignored
    Frames with fewer than 32 bits between flags are tagged as bad packets
    Frames interrupted by a Frame-Abort sequence remain in the FIFO and an interrupt is generated
- Access is provided to the receive FCS
- FCS generation can be inhibited for terminal adaptation
- Recognizes single byte, dual byte and all call addresses
- Independent, 32 byte deep transmit and receive FIFOs
- Receive FIFO maskable interrupts for nearly full and overflow conditions
- Transmit FIFO maskable interrupts for nearly empty and underflow conditions
- Maskable interrupts for transmit end-of–packet and receive end-of-packet
- Maskable interrupts for receive bad-frame (includes frame abort)
- Transmit-to-receive and receive-to-transmit loopbacks are provided
- Transmit and receive bit rates and enables are independent
- Frame aborts can be sent under software control and they are automatically transmitted in the event of a transmit FIFO underrun

<u>T1/J1 Mode</u>

- Assignable to the ESF Facility Data Link or any other channel
- Operates at 4 kbit/s (FDL), 56 kbit/s or 64 kbit/s

<u>E1 Mode</u>

- Assignable to timeslot-0, bits Sa4~Sa8 or any other timeslot
- Operates at 4, 8, 12, 16 or 20 kbit/s (Sa bits) or 64 kbit/s

Common Channel Signaling Timeslot Assigner

- Selected 64 Kbit/s CCS channels (for V5.2 and GR-303) can be routed to/from an external multichannel HDLC, using the CSTi/o pins

Access and Monitoring for National (Sa) Bits (E1 mode only)

In addition to the datalink functions, the Sa bits can be accessed using:
- Single byte register
- Five byte transmit and receive national bit buffers
- A maskable interrupt is generated on the change of state of any Sa bit

Slip Buffers

T1/J1 Mode

Transmit Slip Buffer

- Two-frame slip buffer capable of performing a controlled slip. Intended for rate conversion in the transmit direction

- Programmable delay

- Transmit slips are independent of receive slips

- Indication of slip

- Indication of slip direction

Receive Slip Buffer

- Two-frame slip buffer capable of performing a controlled slip
- Wander tolerance of 142 UI (92 µs) peak
- Indication of slip
- Indication of slip direction

E1 Mode

Receive Slip Buffer

- Two-frame slip buffer capable of performing a controlled slip
- Wander tolerance of 208 UI peak-to-peak
- Indication of slip
- Indication of slip direction

Framing Algorithm

T1/J1 Mode

- Synchronizes with D4 or ESF protocols
- Supports T1DM synchronization with the D4 pattern and timeslot 24 T1DM Sychronization bytes
- Framing circuit is off-line
- Transparent transmit and receive mode
- In D4 mode Fs bits can be optionally cross checked with the Ft bits
- The start of the ESF multiframe can be determined by the following methods:
- Free-run
- Software reset
- Synchronized to the incoming multiframe
- An automatic reframe is initiated if the framing bit error density exceeds the programmed threshold
- In transparent mode no reframing is forced by the device
- Software can force a reframe at any time
- In ESF mode the CRC-6 bits can be optionally confirmed before forcing a new frame alignment
- During a reframe the signaling bits are frozen, and error counting for Ft, Fs, ESF framing pattern and CRC-6 bits is suspended
- If J1 CRC-6 is selected the Fs bits are included in the CRC-6 calculation
- J1-CRC-6 and J1-Yellow Alarm can be independently selected
- Supports Robbed Bit Signaling
- Optional forced ones insertion

E1 Mode

- Three distinct and independent E1 framing algorithms
  1. Basic frame alignment
  2. Signalling multiframe alignment
  3. CRC-4 multiframe alignment
- Transparent receive mode
- Transparent transmit mode
- Optional automatic interworking between interfaces with and without CRC-4 processing capabilities is supported
- An automatic reframe is forced if 3 consecutive frame alignment patterns or three consecutive non-frame alignment bits are received in error
- In receive transparent mode no reframing is forced by the device
- Software can force a reframe at any time
- Software can force a multiframe reframe at any time
- E-bits can optionally be set to zero or one until CRC synchronization is achieved
- Optional automatic RAI
- Supports CAS multiframing
- Optional automatic Y-bit to indicate CAS multiframe alignment

Channel Associated Signaling

- ABCD or AB bits can be automatically inserted and extracted
- Transmit ABCD or AB bits can be passed via the microport or via the CSTi pin
- Receive ABCD or AB bits are accessible via the microport or via the CSTo pin
- Unused nibble positions in the CSTi/CSTo bandwidth are tri-stated
- An interrupt is provided in the event of changes in any of the signaling bits
- Receive signaling bits are frozen if digital loss of signal or loss of multiframe alignment is declared

T1/J1 Mode

- Signaling bits can be debounced by 6 ms
- Robbed bit or clear channel signaling are selected on a channel by channel basis
- Signaling interrupt period can be selected: 1, 4 or 8 msec

E1 Mode

- Signaling bits can be debounced by 14 ms
- Signaling interrupt period can be selected 1, 4 or 8 msec

Alarms

T1/J1 Mode

Yellow Alarm
D4 mode, two types:

- Bit position 2 is zero for virtually every DS0 over 48ms
- Two consecutive ones in the S-bit position of the twelfth frame

ESF mode, two types:

1. Reception of 0000000011111111 in eight or more codewords out of ten (T1)
2. Reception of 1111111111111111 in eight or more codewords out of ten (J1)

T1DM mode:

- Bit 2 of the T1DM synchronization byte is 0

Alarm Indication Signal (AIS)

- Declared if fewer than six zeros are detected during a 3 ms interval

Loss Of Signal (LOS)

- Loss Of Signal is declared if 192 or 32 consecutive zeros are received

E1 Mode

Remote Alarm Indication (RAI)

- Bit 3 of the receive NFAS

Alarm Indication Signal (AIS)
- Unframed all ones signal for at least a double frame or two double frames

Timeslot 16 Alarm Indication Signal

- All ones signal in timeslot 16

Loss Of Signal (LOS)

- Loss Of Signal is declared if 192 or 32 consecutive zeros are received

Remote Signaling Multiframe Alarm

- Y-bit of the multiframe alignment signal

Maskable Interrupts

T1/J1 Mode Interrupts

- Framing bit error counter overflow
- CRC-6 error counter overflow
- Out of frame alignment counter overflow
- Change of frame alignment counter overflow
- Bipolar violation counter overflow
- PRBS error counter overflow
- PRBS multiframe counter overflow
- Multiframes out of alignment counter overflow
- Change of state of terminal frame synchronization
- Change of state of multiframe synchronization
- Receive framing bit error
- Change of receive frame alignment after a reframe
- Reception of a severely errored frame
- Reception of AIS
- Receive CRC-6 error
- Reception of digital LOS
- D4 yellow alarm detected
- D4 yellow alarm detected for 48ms
- Secondary D4 yellow alarm received
- ESF yellow alarm received
- T1DM yellow alarm received
- Receive bipolar violation
- Receive PRBS error
- Pulse density violation
- Loop code enable detected
- Loop code disable detected
- Receive new bit oriented message (debounced)
- Bit oriented message match detected
- Signaling (AB or ABCD) bit change

E1 Mode Interrupts

- Receive FEBE and RAI
- Receive slip
- Receive Y-bit
- Receive V3 auxiliary pattern (0101010…)
- Receive change of state of RAI
- Receive change of state of AIS
- Receive change of state of AIS in timeslot 16
- Change of state of reception of digital LOS
- Remote CRC-4 and RAI for 10ms
- Remote CRC-4 and RAI for 450ms
- Reception of consecutive errored FASs
- Remote CRC-4 multiframe generator/detector failure
- Change of state of CRC-4 multiframe synchronization
- Change of state of signaling multiframe synchronization
- Change of state of basic frame alignment
- Loss of frame sync counter overflow
- FAS error counter overflow
- FAS error indication
- FAS bit error counter overflow
- FAS bit error indication
- CRC-4 error counter overflow
- Receive CRC-4 error
- Receive bipolar violation error counter overflow
- Receive bipolar violation
- Receive E-bit counter overflow
- Receive E-bit error
- PRBS multiframe counter overflow
- Jitter attenuator empty/full
- PRBS error counter overflow

HDLC Interrupts

- Go ahead pattern received
- End of packet received
- End of packet transmitted
- End of packet read from receive FIFO
- Transmit FIFO low (16 bytes)
- Frame abort received
- Transmit FIFO underrun
- Receive FIFO full (above 16 byte threshold
- Receive FIFO overflow

Maskable Interrupts (continued)

- One second timer
- Two second timer
- Excessive zero counter overflow
- Excessive zero event
- Transmit slip
- Receive slip

- Receive PRBS error
- Sa5 bit set
- Sa6 bit set
- Eighth consecutive identical Sa6 nibble
- Sa6 nibble change
- Sa nibble change
- Sa5 bit change
- Sa bit change
- Signaling (CAS) bit change
- Two millisecond timer
- Ten millisecond timer
- One hundred millisecond timer
- One second timer

Performance Monitoring

Error Counters

- All counters can be cleared or preset by writing to the appropriate locations
- Maskable occurrence interrupt
- Maskable overflow interrupt
- Counters can be latched on one second intervals

T1/J1 Mode

- CRC-6 Multiframe Counter (8-bit)
- PRBS Error Counter (8-bit)
- Multiframes Out of Sync Counter (16-bit)
- Framing Bit Error Counter (16-bit)
- Bipolar Violation Counter (16-bit)
- CRC-6 Error Counter (16-bit)
- Out of Frame Alignment Counter (8-bit)
- Change of Frame Alignment Counter (8-bit)
- Excessive Zeros Counter (8-bit)

E1 Mode

- PRBS Error Counter (8-bit)
- CRC-4 Multiframe Counter (8-bit)
- Loss of Basic Frame Sync (16-bit)
- E-bit Error Counter (16-bit)
- Bipolar Violation Counter (16-bit)
- CRC-4 Error Counter (16-bit)
- FAS Bit Error Counter (8-bit)
- FAS Error Counter (8-bit)

Error Insertion

Loopbacks

- Digital loopback
- Remote loopback
- ST-BUS loopback
- Payload loopback
- Local timeslot loopback

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T1/J1 Mode

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- Bipolar Violations
- CRC-6 errors
- Ft errors
- Fs errors
- Payload errors
- Loss of Signal error


- Remote timeslot loopback
- Metallic loopback

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E1 Mode

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- E-bit
- Bipolar Violations
- CRC-4 Errors
- FAS Errors
- NFAS Errors
- Payload Errors
- Loss of Signal Error

Per Timeslot Control

The following features can be controlled on a per timeslot basis:

- Clear Channel Capability (only used in T1/J1)
- Choice of sourcing transmit signaling bits from microport or CSTi pin
- Remote timeslot loopback
- Local timeslot loopback
- PRBS insertion and reception
- Digital milliwatt pattern insertion
- Per channel inversion for transmit and receive
- Transmit and receive idle code
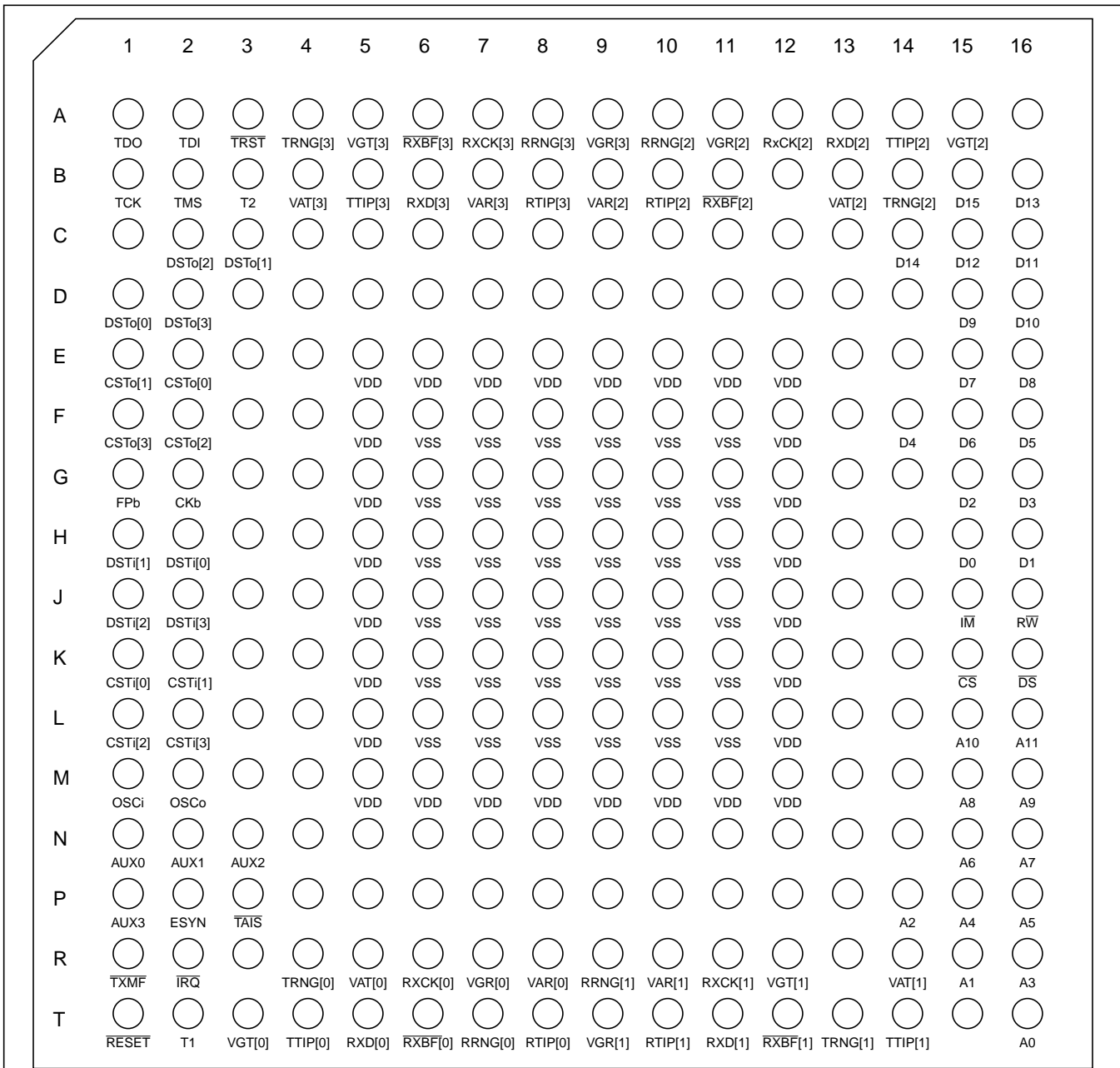
Figure 2 - 256 Pin LBGA Package

Notes:
1. LBGA is a 256 Pin LBGA 1.00mm Pitch 17mm X 17mm Package and 16 X 16 Matrix and 15mm X 15mm footprint.
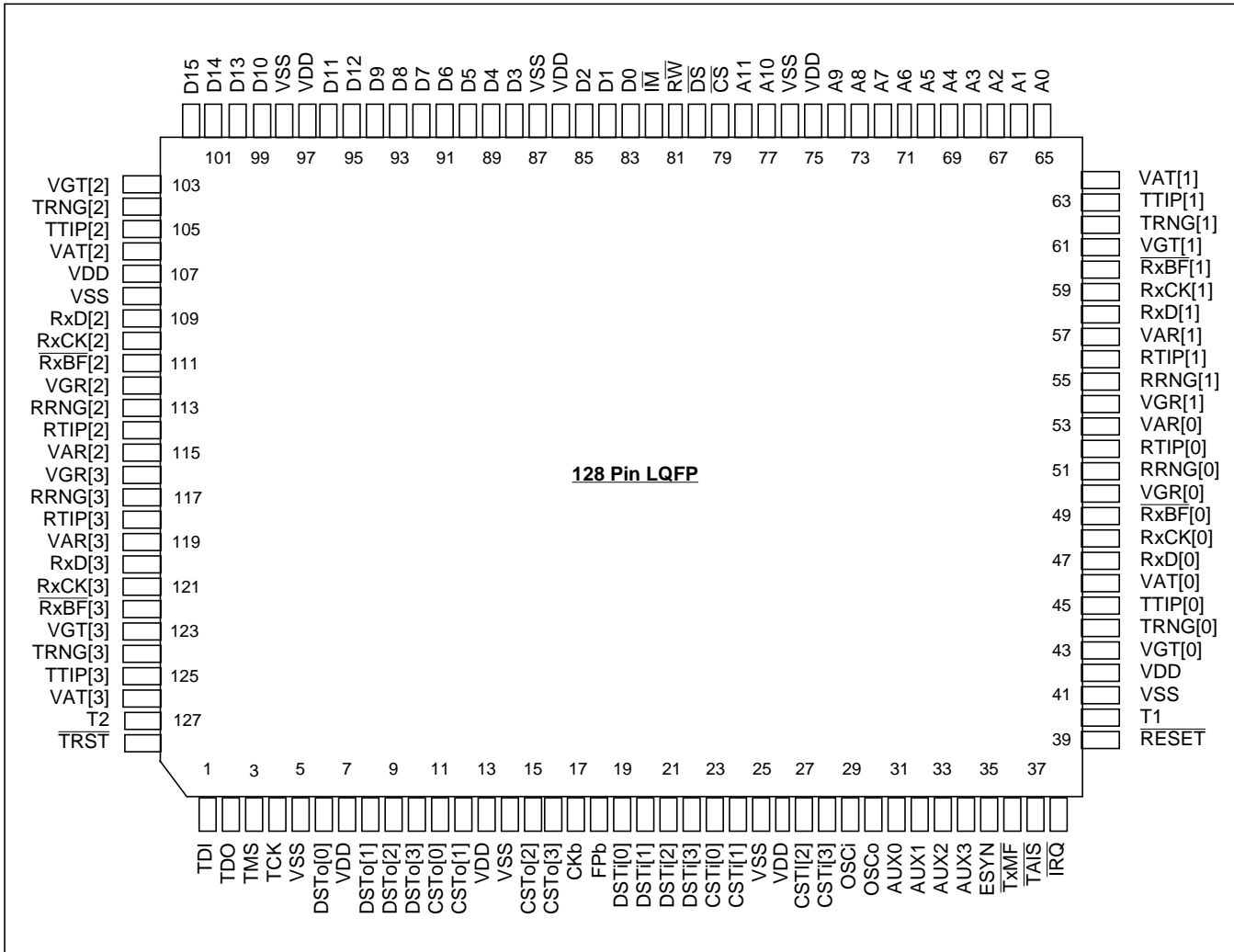2. Name below circle indicates BGA ball name.

Figure 3 - 128 Pin LQFP Package

Pin Description

LBGA Pin	LQFP Pin	Name	Description (see notes 1, 2, 3 and 4)
			DS0/PCM30 Interface
T4 T14 A14 B5	45 63 105 125	TTIP[0] TTIP[1] TTIP[2] TTIP[3]	**Transmit Tip (analog output).** This output along with the TRNG output pin are the differential output pair which are connected to the transmit line signal through a transformer. See Figure 29 - 100 ohm T1 & 120 ohm E1 Analog Line Interface and Figure 30 - 75 ohm E1 Analog Line Interface.
R4 T13 B14 A4	44 62 104 124	TRNG[0] TRNG[1] TRNG[2] TRNG[3]	**Transmit Ring (analog output).** See the TTIP pin description.
T8 T10 B10 B8	52 56 114 118	RTIP[0] RTIP[1] RTIP[2] RTIP[3]	**Receive Tip (analog input).** This input along with the RRNG input pin are the differential input pair which are connected to the receive line signal through a transformer. See Figure 29 - 100 ohm T1 & 120 ohm E1 Analog Line Interface and Figure 30 - 75 ohm E1 Analog Line Interface.
T7 R9 A10 A8	51 55 113 117	RRNG[0] RRNG[1] RRNG[2] RRNG[3]	**Receive Ring (analog input).** See the RTIP pin description.

Pin Description (continued)

LBGA Pin	LQFP Pin	Name	Description (see notes 1, 2, 3 and 4)
			ST-BUS Backplane Interface
G2	17	CKb	**System Clock (CMOS compatible input/output).** This is the sync source for the backplane and transmit link clock. In Line Sync Mode this is an output, in Backplane Sync Mode this is an input. In 2.048Mb/s Backplane Mode, this clock is 4.096MHz, in 8.192Mb/s mode this clock is 16.384MHz. See Figure 39 - ST-BUS 2.048Mb/s Timing and Figure 41 - ST-BUS 8.192Mb/s Timing.
G1	18	FPb	**Frame Pulse (CMOS compatible input/output).** This is the backplane 8kHz frame synchronization signal for the DSTi, DSTo, CSTi and CSTo data streams. In Line Sync Mode this is an output, in Backplane Sync Mode this is an input. See Figure 39 - ST-BUS 2.048Mb/s Timing and Figure 41 - ST-BUS 8.192Mb/s Timing.
H2 H1 J1 J2	19 20 21 22	DSTi[0] DSTi[1] DSTi[2] DSTi[3]	**Data ST-BUS (CMOS compatible input).** In 2.048Mb/s backplane mode, this input accepts a 2.048Mb/s serial stream which contains up to 32 8-bit timeslots. In T1/J1 mode, 24 of these timeslots map to the T1 link payload data. In E1 mode, 30 of these timeslots map to the E1 link payload data. In 8.192Mb/s backplane mode, DSTi[0] accepts a single 8.192Mb/s serial stream which contains 128 8-bit timeslots accommodating all four tranceivers. DSTi[1:3] are not used. See Figure 39 - ST-BUS 2.048Mb/s Timing and Figure 41 - ST-BUS 8.192Mb/s Timing.
D1 C3 C2 D2	6 8 9 10	DSTo[0] DSTo[1] DSTo[2] DSTo[3]	**Data ST-BUS (CMOS compatible output).** In 2.048Mb/s backplane mode, this output delivers a 2.048Mb/s serial stream which contains up to 32 8-bit timeslots. In T1/J1 mode, 24 of these timeslots map to the T1 link payload data. In E1 mode, 30 of these timeslots map to the E1 link payload data. In 8.192Mb/s backplane mode, DSTo[0] outputs a single 8.192Mb/s serial stream which contains 128 8-bit timeslots accommodating all four tranceivers. DSTo[1:3] are high impedance. See Figure 39 - ST-BUS 2.048Mb/s Timing and Figure 41 - ST-BUS 8.192Mb/s Timing.
K1 K2 L1 L2	23 24 25 26	CSTi[0] CSTi[1] CSTi[2] CSTi[3]	**Control ST-BUS (CMOS compatible input).** In 2.048Mb/s backplane mode, this input accepts a 2.048Mb/s serial stream which contains up to 32 8-bit timeslots. In T1/J1 mode, 24 of these timeslots map to the T1 link CAS ABCD bits. In E1 mode, selected timeslots map to either the E1 link CAS bits or the E1 link CCS bits. In 8.192Mb/s backplane mode, CSTi[0] accepts a single 8.192Mb/s serial stream which contains 128 8-bit timeslots accommodating all four tranceivers. CSTi[1:3] are not used. See Figure 39 - ST-BUS 2.048Mb/s Timing and Figure 41 - ST-BUS 8.192Mb/s Timing.

Pin Description (continued)

LBGA Pin	LQFP Pin	Name	Description (see notes 1, 2, 3 and 4)
E2 E1 F2 F1	11 12 15 16	CSTo[0] CSTo[1] CSTo[2] CSTo[3]	**Control ST-BUS (CMOS compatible output).** In 2.048Mb/s backplane mode, this output delivers a 2.048Mb/s serial stream which contains up to 32 8-bit timeslots. In T1/J1 mode, 24 of these timeslots map to the T1 link CAS ABCD bits. In E1 mode, selected timeslots map to either the E1 link CAS bits or the E1 link CCS bits. In 8.192Mb/s backplane mode, CSTo[0] outputs a single 8.192Mb/s serial stream which contains 128 8-bit timeslots accommodating all four tranceivers. CSTo[1:3] are high impedance. See Figure 39 - ST-BUS 2.048Mb/s Timing and Figure 41 - ST-BUS 8.192Mb/s Timing.
		Receive Data Outputs Before Buffering	
T5 T11 A13 B6	47 58 109 120	RxD[0] RxD[1] RxD[2] RxD[3]	**Receive Data (CMOS compatible output).** Provides a serial output stream which contains all timeslots of the received data after decoding. This data does not pass through the elastic buffer and is clocked out with the falling edge of RxCK. In T1 and J1 mode, the data rate is 1.544Mb/s and the decoding is B8ZS. In E1 mode, the data rate is 2.048Mb/s and the decoding is HDB3. See Figure 49 - Receive Data (Slip Buffer Bypass) Timing.
R6 R11 A12 A7	48 59 110 121	RxCK[0] RxCK[1] RxCK[2] RxCK[3]	**Receive Clock (CMOS compatible output).** This output clock is extracted from the receive signal at the RTIP and RRNG inputs and is used internally to clock in the receive data. In T1 and J1 modes, the clock rate is 1.544MHz. In E1 mode, the clock rate is 2.048MHz. See Figure 50 - Receive Data (Slip Buffer Bypass) Functional Timing.
T6 T12 B11 A6	49 60 111 122	$\overline{\text{RxBF}}$[0] $\overline{\text{RxBF}}$[1] $\overline{\text{RxBF}}$[2] $\overline{\text{RxBF}}$[3]	**Receive Basic Frame Pulse (CMOS compatible output).** Provides an 8kHz basic frame pulse which is synchronized to the received data (RxD) after decoding. This frame pulse does not pass through the elastic buffer and is clocked out with the falling edge of RxCK. See Figure 49 - Receive Data (Slip Buffer Bypass) Timing.
		Control and Timing	
R1	36	TxMF	**Transmit Multiframe Boundary (CMOS compatible input).** This input is applicable in E1 mode only. The frame pulse applied to this pin sets the transmitted CAS multiframe boundary or the transmitted CRC-4 multiframe boundary. The falling edge of this frame pulse identifies basic frame 0 (the start of bit cell 7 of timeslot 0) on the ST-BUS data stream (DSTi) of the 16 frame multiframe. The device will generate its own multiframe boundary if this pin is held high, and is pulled high in most applications. This input is common for all four transceivers, and is enabled on a per transceiver basis with control register bit MFBE detailed in Table 83 - E1 Interrupts and I/O Control - R/W Address Y02. Operation is identical in 2.048Mb/s and 8.192Mb/s modes. See Figure 43 - Transmit Multiframe (CRC-4 or CAS) Timing.
P3	37	$\overline{\text{TAIS}}$	**Transmit Alarm Indication Signal (CMOS compatible input).** When zero, all four transceivers of the MT9071 transmit an all ones signal (AIS) at the TTIP and TRNG output pins. When one, all four transceivers of the MT9071 transmit data normally. This input is typically set to zero during initial power up, then set to one.
T1	39	RESET	**Reset (CMOS compatible input).** When zero, all four transceivers of the MT9071 are in a reset condition where all registers are set to their default values. When one, all four transceivers of the MT9071 operate normally where all registers may be programmed by the external processor. A valid reset condition requires this input to be held low for a minimum of 100ns. This input is should be set to zero during initial power up, then set to one.

Pin Description (continued)

LBGA Pin	LQFP Pin	Name	Description (see notes 1, 2, 3 and 4)
M1	29	OSCi	**Oscillator Master Clock (CMOS compatible input).** For crystal operation, a 20MHz crystal is connected from this pin to OSCo. For clock oscillator operation, this pin is connected to a clock source. See Figure 22 - Crystal Oscillator Circuit and Figure 21 - Clock Oscillator Circuit.
M2	30	OSCo	**Oscillator Master Clock (CMOS compatible output).** For crystal operation, a 20MHz crystal is connected from this pin to OSCi. For clock oscillator operation, this pin is left unconnected. See the OSCi pin description.
P2	35	ESYN	**External Sync Clock (CMOS compatible input/output).** In T1 and J1 modes, the clock rate is 1.544MHz. In E1 mode, the clock rate is 2.048MHz. In Line Sync Mode this is an input which may be used as the synchronization source for the device. In Backplane Sync Mode this is an output which is synchronized to one of the four incoming links.
N1 N2 N3 P1	31 32 33 34	AUX0 AUX1 AUX2 AUX3	**Auxiliary Signals 0-3 (CMOS compatible output).** A programmable output signal. See Section 3.6 Auxiliary Output Signals.
		Micro Port Interface	
K15	79	$\overline{CS}$	**Chip Select (CMOS compatible input).** A zero enables the read and write functions of the MT9071 parallel processor interface; all bidirectional data bus lines (D0-D15) will operate normally. A one disables the read and write functions of the parallel processor interface; all bidirectional data bus lines (D0-D15) will be in a high impedance state.
K16	80	$\overline{DS}$	**Data Strobe (CMOS compatible input).** Data Strobe for Motorola mode ($\overline{IM}$=0). The MT9071 reads data from the address bus (A0-A11) on the falling edge of $\overline{DS}$; writes data to the bidirectional data bus (D0-D15) on the falling edge of $\overline{DS}$ (processor read); reads data from the bidirectional data bus (D0-D15) on the falling edge of $\overline{DS}$ (processor write). $\overline{DS}$ may be connected to $\overline{CS}$.
		$(\overline{RD})$	**Read:** Read for Intel type mode ($I\overline{M}$=1). The MT9071 reads data from the address bus (A0-A11) on the falling edge of $\overline{RD}$; writes data to the bidirectional data bus (D0-D15) on the falling edge of $\overline{RD}$ (processor read).
J16	81	$R\overline{W}$	**Read/Write (CMOS compatible input).** Read and Write for Motorola mode ($I\overline{M}$=0). A zero sets the MT9071 bidirectional data bus lines (D0-D15) as inputs for a processor write. A one sets the MT9071 bidirectional data bus lines as outputs for a processor read.
		$(\overline{WR})$	**Write:** Write for Intel type mode ($I\overline{M}$=1). The MT9071 reads data from the address bus (A0-A11) on the falling edge of $\overline{WR}$; reads data from the bidirectional data bus (D0-D15) on the falling edge of $\overline{WR}$ (processor write).
J15	82	$I\overline{M}$	**Intel / Motorola (CMOS compatible input).** High configures the processor interface for Intel type of parallel non-multiplexed processors where RD and WR pins are used. Low configures the processor interface for Motorola type of parallel non-multiplexed processors where R/W and DS pins are used.
R2	38	$\overline{IRQ}$	**Interrupt Request (open drain output).** When zero, one or more of the four transceivers in the MT9071 has generated an interrupt request. When one, the MT9071 has not generated an interrupt request. $\overline{IRQ}$ is an open drain output that should be connected to V_{DD} through a pull-up resistor. $\overline{CS}$ can be either high or low for this output pin to function.

Pin Description (continued)

LBGA Pin	LQFP Pin	Name	Description (see notes 1, 2, 3 and 4)
T16 R15 P14 R16 P15 P16 N15 N16 M15 M16 L15 L16	65 66 67 68 69 70 71 72 73 74 77 78	A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11	**Address 0 to 11 (CMOS compatible input).** These 12 signals form the input address bus for the non-multiplexed parallel processor interface. Bits A7 to A0 select specific registers within the transceivers, bits A10 to A8 determine which of the four transceivers is selected for read and write operations (bit A10 should be kept at zero), bit A11 selects all four transceivers for a simultaneous write operation. A11 is the most significant bit.
H15 H16 G15 G16 F14 F16 F15 E15 E16 D15 D16 C16 C15 B16 C14 B15	83 84 85 88 89 90 91 92 93 94 95 96 99 100 101 102	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	**Data 0 to 15 (CMOS compatible input/output).** These 16 signals form the bidirectional data bus for the non-multiplexed parallel processor interface. D15 is the most significant bit.
		Test Pins	
T2	40	T1	**Test Pin 1 (CMOS compatible input with pull-down).** For factory test purposes. Connect to ground for normal operation.
B3	127	T2	**Test Pin 2 (CMOS compatible input with pull-down).** No Connection, for factory test purposes. Internally pulled down to V_{SS}.
A2	1	TDI	**Test Data Input (CMOS compatible input with pull-up).** One of five signals (TDI, TDO, TMS, TCK & $\overline{TRST}$) making up the Test Access Port (TAP) of the IEEE 1149.1-1990 Standard Test Port and Boundary-Scan Architecture. The TAP provides access to test support functions built into the MT9071. The TAP is also referred to as a JTAG (Joint Test Action Group) port. Serial input data applied to this pin is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. The received input data is sampled at the rising edge of TCK pulses. Internally pulled up to V_{DD}. See Section 8.0 JTAG Operation.
A1	2	TDO	**Test Data Output (CMOS compatible output and high impedance).** Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out towards the TDO. The data out of the TDO is clocked on the falling edge of the TCK pulses. When no data is shifted through the boundary scan cells, the TDO driver is set to a high impedance state. See the pin description for TDI and Section 8.0 JTAG Operation.

Pin Description (continued)

LBGA Pin	LQFP Pin	Name	Description (see notes 1, 2, 3 and 4)
B2	3	TMS	**Test Mode Select Input (CMOS compatible input with pull-up).** The logic signals received at the TMS input are interpreted by the TAP Controller to control the test operations. The TMS signals are sampled at the rising edge of the TCK pulse. Internally pulled up to V_{DD}. See the pin description for TDI and Section 8.0 JTAG Operation.
B1	4	TCK	**Test Clock Input (CMOS compatible input with pull-up).** TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clocks and thus remains independent. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic. Internally pulled up to V_{DD}. See the pin description for TDI and Section 8.0 JTAG Operation.
A3	128	$\overline{TRST}$	**Test Reset (CMOS compatible input with pull-up).** When zero, the JTAG scan structure is reset. When one, the JTAG scan structure operates normally. Internally pulled up to V_{DD}. A valid device reset condition requires this input to be held low for a minimum of 100ns. This input is should be set to zero during initial power up, then set to one if the JTAG port is to be used, otherwise, it may be permanently set to zero. See the pin description for TDI and Section 8.0 JTAG Operation.

Pin Description

LBGA Pin	LQFP Pin	Name	Description (see notes 1, 2, 3 and 4)
			Power Supplies
F6 - F11, G6 - G11, H6 - H11, J6 - J11, K6 - K11, L6 - L11	5 14 25 41 76 87 98 108	V_{SS}	**Digital Ground.** $0V_{DC}$. Common ground for all digital sections in the device.
E5 - E12, F5, F12, G5, G12, H5, H12, J5, J12, K5, K12, L5, L12, M5 - M12	7 13 26 42 75 86 97 107	V_{DD}	**Digital Supply Voltage.** +3.3V_{DC} nominal. Common supply for all digital sections in the device.
R5 R14 B13 B4	46 64 106 126	$V_{AT}[0]$ $V_{AT}[1]$ $V_{AT}[2]$ $V_{AT}[3]$	**Transmitter Analog Supply Voltage.** +3.3V_{DC} nominal. Unique supply for each analog transmitter in the device. Connect to V_{DD} power plane.
T3 R12 A15 A5	43 61 103 123	$V_{GT}[0]$ $V_{GT}[1]$ $V_{GT}[2]$ $V_{GT}[3]$	**Transmitter Analog Ground.** $0V_{DC}$. Unique ground for each analog transmitter in the device. Connect to V_{SS} ground plane.

Pin Description (continued)

LBGA Pin	LQFP Pin	Name	Description (see notes 1, 2, 3 and 4)
R8 R10 B9 B7	53 57 115 119	$V_{AR}[0]$ $V_{AR}[1]$ $V_{AR}[2]$ $V_{AR}[3]$	**Receiver Analog Supply Voltage.** +3.3V_{DC} nominal. Unique supply for each analog receiver in the device. Connect to V_{DD} power plane.
R7 T9 A11 A9	50 54 112 116	$V_{GR}[0]$ $V_{GR}[1]$ $V_{GR}[2]$ $V_{GR}[3]$	**Receiver Analog Ground.** 0V_{DC}. Unique ground for each analog receiver in the device. Connect to V_{SS} ground plane.

Notes:
1. All unused inputs should be tied high or low.
2. See AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels for input and output voltage thresholds.
3. The number enclosed in parentheses following the pin name identifies the transceiver as follows:
    [0] - transceiver 0, [1] - transceiver 1, [2] - transceiver 2, [3] - transceiver 3
4. The "Y" character in the register address symbolizes the upper 4 address bits ($A_{11}A_{10}A_9A_8$) which identify the particular transceiver addressed within the MT9071 as follows:
    [0] 0000 - transceiver 0, [1] 0001 - transceiver 1, [2] 0010 - transceiver 2, [3] 0011 - transceiver 3.
    [8] 1000 - write for all 4 transceivers.
    [9] 1001 - global registers (read and/or write) for all four transceivers

1.0   Device Overview

The MT9071 is a four port (quad) long/short haul T1/E1/J1 transceiver with an integrated reference switching PLL. Each of the four transceivers has one embedded HDLC (High-level Data Link Controller) that can be assigned to the maintenance channel or to any other channel.

1.1   Standards Compliance

In T1 mode the MT9071 meets or supports the latest recommendations including AT&T PUB43801, TR-62411; ANSI T1.102, T1.403 and T1.408; ITU-T G.802. It also supports Telcordia GR-303-CORE. In T1 ESF mode the CRC-6 calculation and yellow alarm can be configured to meet the requirements of a J1 interface.

In E1 mode the MT9071 meets or supports the latest ITU-T Recommendations for PCM30 and ISDN primary rate including G.703, G.704, G.706, G.732, G.775, G.796, G.823, G.964 (V5.1), G.965 (V5.2) and I.431. It also meets or supports ETSI TBR4, TBR13, ETS 300 233, ETS 300 324 (V5.1) and ETS 300 347 (V5.2).

1.2   Microprocessor Port

A 16-bit parallel Motorola or Intel non-multiplexed microprocessor interface is used to access the control and status registers.

1.3   LIU

The MT9071 LIU interfaces the digital framer functions to a T1 or E1 transformer-isolated four wire line.

In T1 mode, the LIU can pre-equalize the transmit signal to meet the T1.403 and T1.102 pulse templates after attenuation by 0 - 655 feet of 22 AWG PIC cable, alternatively it can provide line build outs of 7.5dB, 15dB and 22.5dB. In T1 mode the receiver can recover signals attenuated by up to 36dB at 772kHz.

In E1 mode, the LIU transmits signals that meet the G.703 2.048 Mbit/s pulse template and the receiver can recover signals attenuated by up to 40dB at 1024kHz.

1.4   Reference Switching PLL

The MT9071 PLL can switch its source of network synchronization from between the four internal LIUs and/or an external timing source without causing bit errors or loss of frame synchronization. During a reference switch the MTIE (Maximum Time Interval Error) and the phase slope comply with the limits recommended in Telcordia: GR-1244-CORE for a Stratum 3 clock, and ITU-T G.812 for a Type IV clock. In the event of reference loss, the PLL enters holdover mode with frequency accuracy of 0.05ppm.

The MT9071 PLL attenuates jitter from 1.9 Hz with a roll-off of 20 dB/decade. The intrinsic jitter is less than 0.02 UI. In all timing modes the low jitter output of the PLL provides timing to the transmit side of the four LIUs.

1.5   Slip Buffers

In T1 mode, the receive and transmit paths both include two-frame slip buffers. The transmit slip buffer delay is programmable.

In E1 mode, the receive path includes a two-frame slip buffer and the transmit path contains a 128 bit Jitter Attenuator (JA) FIFO with programmable depth.

1.6 Interface to the System Backplane

On the system side the MT9071 framers can interface to a 2.048Mbit/s or 8.192Mbit/s ST-BUS backplane.

1.7 Framing Modes

The MT9071 framers operate in either termination or transparent modes. In the receive transparent mode, the received line data is channelled to the DSTo pin with arbitrary frame alignment. In the transmit transparent mode, no framing is imposed on the data transmitted from the DSTi pin onto the line.

In T1 mode, the framers operate in any of the following framing modes: D4, Extended Superframe (ESF) or T1DM.

In E1 mode, the framers run three framing algorithms: basic frame alignment, signalling multiframe alignment and CRC-4 multiframe alignment. The Remote Alarm Indication (RAI) bit is automatically controlled by an internal state machine.

1.8 Access to the Maintenance Channel

The T1 ESF Facility Data Link (FDL) bits can be accessed in the following three ways: Receive FDL through the RxD pin; transmit and receive FDL through internal registers for Bit Oriented Messages; through the embedded HDLC.

In E1 mode, the Sa bits (bits 4-8 of the non-frame alignment signal) can be accessed in four ways: Receive data link through the RxD pin; transmit and receive data link through single byte transmit and receive registers; through five byte transmit and receive national bit buffers; through the embedded HDLC.

1.9 Robbed Bit Signaling / Channel Associated Signaling

Robbed bit signaling and channel associated information can be accessed two ways: Via the microport; via the CSTi and CSTo pins. Signaling information is frozen upon loss of multiframe alignment.

In T1 mode, the MT9071 supports AB and ABCD robbed bit signaling. Robbed bit signaling can be enabled on a channel by channel basis.

In E1 mode, the MT9071 supports Channel Associated Signaling (CAS) multiframing.

1.10 Common Channel Signaling

MT9071 supports Common Channel Signaling (CCS) with an embedded HDLC and with the capability to assign CSTi/CSTo channels to transmit/receive timeslots.

In T1 mode, CCS is supported in any one channel by using the embedded HDLC. Alternatively, the CSTi and CSTo pins can be used to map an external HDLC channel to/from any one transmit/receive T1 channel.

In E1 mode, CCS is supported in any one timeslot by using the embedded HDLC. Alternatively, the CSTi and CSTo pins can be used to map external HDLC channels to/from any of the transmit/receive E1 timeslots 15, 16 and 31.

1.11 HDLC

The MT9071 provides one embedded HDLC per framer with 32 byte deep transmit and receive FIFOs.

In T1 mode, the embedded HDLC can be assigned to the FDL or any channel. It can operate at 4kbit/s (FDL), 56kbit/s or 64kbit/s.

In E1 mode, the embedded HDLC can be assigned to timeslot 0 Sa bits (bits 4-8 of the non-frame alignment signal), or any other timeslot. It can operate at 4,8,12,16,20 (Data Link) or 64kbit/s.

1.12 Performance Monitoring and Debugging

The MT9071 has a comprehensive suite of performance monitoring and debugging features. These include error counters, loopbacks, deliberate error insertion and a 2^{15} –1 QRS/PRBS generator/detector.

1.13 Interrupts

The MT9071 provides a comprehensive set of maskable interrupts. Interrupt sources consist of: synchronization status, alarm status, counter indication and overflow, timer status, slip indication, maintenance functions and receive signaling bit changes.

2.0   Line Interface Unit (LIU)

2.1   LIU Receiver

The receiver portion of the MT9071 LIU consists of an input signal peak detector, an equalizer with two separate high pass sections, a smoothing filter, data and clock slicers and a clock extractor. Receive equalization gain can be set manually (i.e., software) or it can be determined automatically by peak detectors.

The output of the receive equalizer is conditioned by a smoothing filter and is passed on to the clock and data slicer. The clock slicer output generates an extracted clock (RxCK[3:0]). This extracted clock, together with the internal PLL clock output is used to sample the output of the data comparator.

In T1 mode, the receiver portion of the LIU can recover clock and data from line signals attenuated by up to 36dB at 722kHz and tolerate jitter to the maximum specified by AT&T TR 62411 (see Figure 16 - AT&T Jitter Tolerance). In E1 mode, the receiver portion of the LIU can recover clock and data from a line signal attenuated by up to 40db at 1024 kHz.

In E1 mode, as specified by G.703, the receiver portion of the LIU can recover clock and data from the line signal in the presence of a signal to noise ratio of at least 18dB. The receiver recovers error free a signal whose amplitude may vary 10% from the nominal value, and is subsequently mixed with crosstalk 18dB lower, the combined signal being subject to 0 - 6dB sqrt(f) attenuation. The jitter tolerance of the clock extractor circuit exceeds the requirements of G.823 and TBR 4 in E1 mode, see Figure 18 - ETSI Jitter Tolerance.

In T1 and E1 mode, an LIU loss of signal indication is provided with status register bit LLOS (see Table 170 - T1 & E1 LIU and JA Status - R Address YE0). This status register bit indicates when the receive signal level is lower than a specified analog signal threshold level for at least 1 millisecond.

In T1 mode, the LLOS analog threshold is fixed at -40 dB.

In E1 mode, the LLOS analog threshold is either of -20 dB or -40 dB as set by the E1 LLOS threshold criteria control register bit ELOS (see Table 173 - T1 & E1 LIU Control - R/W Address YE3).

For LIU receiver connection to line application circuits, see Figure 29 - 100 ohm T1 & 120 ohm E1 Analog Line Interface and Figure 30 - 75 ohm E1 Analog Line Interface.

2.2   LIU Transmitter

The transmit portion of the MT9071 LIU consists of a jitter attenuator (for E1 mode only), a high speed digital-to-analog converter and complementary line drivers.

When a pulse is to be transmitted, a sequence of digital values are read out of a ROM by a high speed clock. These values drive the digital-to-analog converter to produce an analog signal, which is passed to the complementary line drivers.

For T1 & E1 modes, the pulse amplitude may be adjusted with control register bits TXL2-0 (see Table 172 - T1 & E1 LIU Transmitter Control - R/W Address YE2). For application details, refer to Section 23.8 T1 & E1 Analog Line Interface.

3.0   Timing

3.1   Timing Modes of Operation

Numerous timing options are available including Free-Run Mode, Bus Synchronization Mode, Line Synchronization Mode, External Synchronization Mode, Holdover Mode and Auto-Holdover Mode as summarized in Table 1 - E1 and T1 Timing Modes Summary. In all cases, all four line extracted clocks are output directly on RxCK[n] and are not dejittered. All timing modes are selected with control register bits MS2-1, $\overline{BUSM}$ & $\overline{ESYNI}$ (see Table 73 - T1 & E1 Global Timing Control - R/W Address 905), other timing details are controlled with other control register bits in this same register. For circuit details, refer to Figure 4 - T1 & E1 Bus Sync Mode and Figure 5 - T1 & E1 Free-Run, Line and External Sync Mode.

Timing Mode	Register and Bits	Source for MT9071 Timing	Enable Jitter Attenuator For:
	T1 & E1 Global Timing Control - R/W Address 905		
	MS2 MS1 BUSM ESYNI		
Bus Sync	000X	CKb pin or FPb pin (these are in input mode CKi, FPi)	E1 Always & T1/E1 RLBK
Free-Run	101X	OSCi input pin	T1/E1 RLBK Only
Line Sync	001X	One of 4 receive clock signals at the RXCK[n] pins (extracted from RTIP[n] and RRNG[n])	T1/E1 RLBK Only
External Sync	0010	ESYN pin	T1/E1 RLBK Only
Auto-Holdover	001X	This mode is only applicable during Line Sync Mode or External Sync Mode after the source timing is corrupted. Timing is based on a combination of the OSCi input pin and either one of the receive line signals at the RTIP[n] and RRNG[n] pins or the ESYN pin	T1/E1 RLBK Only
Holdover	011X	This mode is only applicable following Line Sync Mode or External Sync Mode. Timing is based on a combination of the OSCi input pin and either one of the receive line signals at the RTIP[n] and RRNG[n] pins or the ESYN pin	T1/E1 RLBK Only

Notes:
1. The transmit jitter is always attenuated by the timing signal from the internal PLL, consequently, the timing mode does not affect the intrinsic transmit jitter.
2. The backplane jitter (i.e. CSTo and DSTo) is attenuated for all modes except Bus Sync Mode where the jitter from the CKb and FPb pins is passed to the backplane circuitry unfiltered.
3. When in E1 mode and Bus Sync Mode, the jitter attenuator must be enabled. This guarantees that the jitter free transmit clock is in phase with the transmit data which may be jittered.

Table 1 - E1 and T1 Timing Modes Summary

3.1.1 Bus Synchronization Mode

Bus Synchronization is typically used when a slave clock source, synchronized to the backplane bus is required.

In Bus Synchronization Mode, the MT9071 uses an internal PLL to provide jitter free timing which is synchronized to the clock or frame pulse signals which are externally applied to the CKb and FPb pins. Only the transmit clock uses the internal jitter free timing. Consequently, when in E1 Mode, the jitter attenuator should be enabled to ensure the data sent to the transmitter is in sync with the jitter free transmit clock. The accuracy of the transmit timing is equal to the accuracy of the clock at the CKb/FPb pin.

For circuit details, refer to Figure 4 - T1 & E1 Bus Sync Mode.
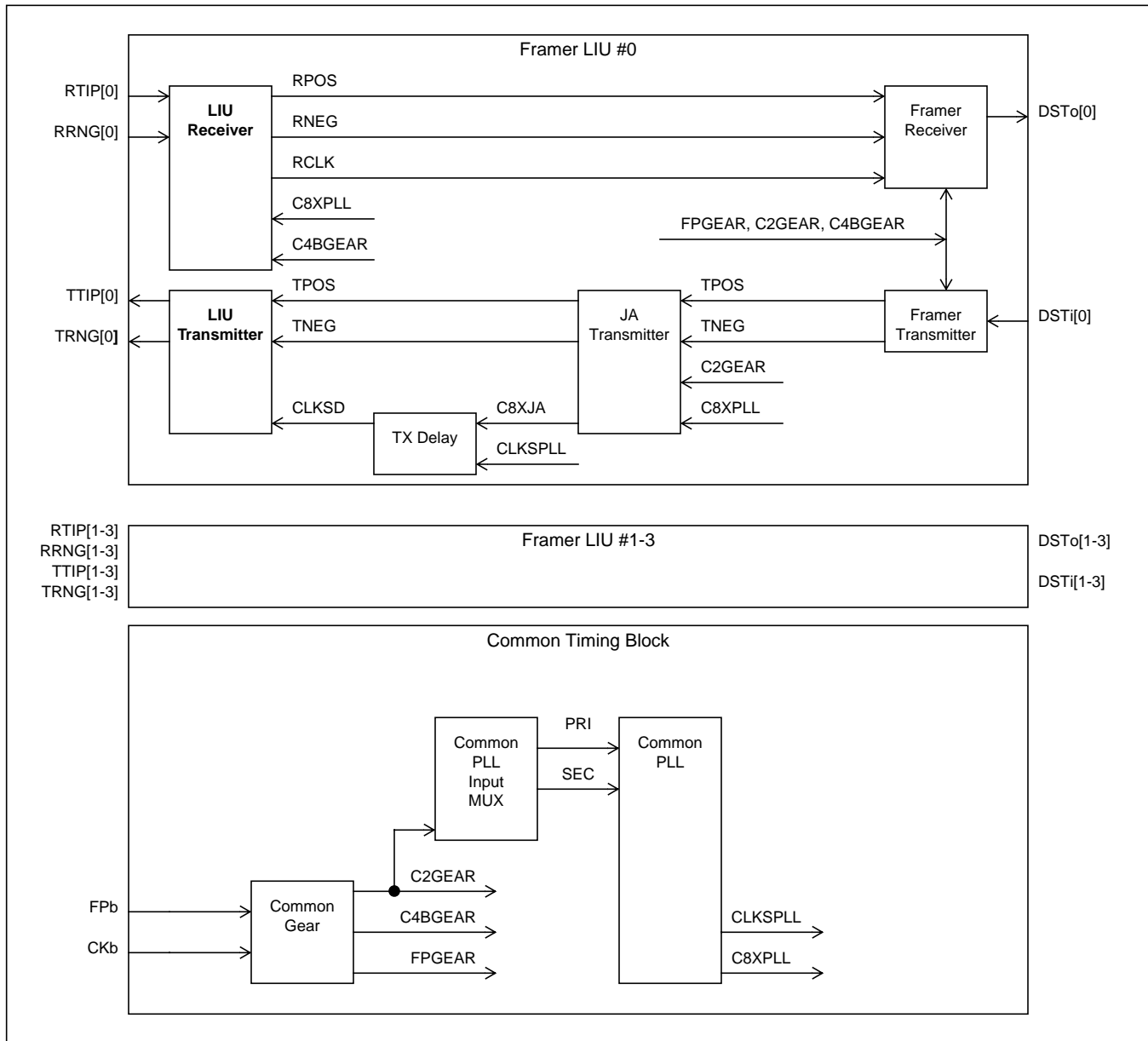
Figure 4 - T1 & E1 Bus Sync Mode

3.1.2   Free-Run Mode

Freerun Mode is typically used when a master clock source is required, or immediately following system power-up before network synchronization is achieved.

In Freerun Mode, the MT9071 uses an internal PLL to provide jitter free timing which is based on the master clock frequency (OSCi) only, and is not synchronized to any reference signal (i.e. RxCK[n], ESYN, CKb). The backplane bus and the transmit data are synchronized to the internally generated timing which also output as a clock and frame pulse at the CKb and FPb pins. The accuracy of the timing is equal to the accuracy of the master clock (OSCi). So if a ±32ppm output clock is required, the master clock must also be ±32ppm (see Section 23.1 Master Clock). For circuit details, refer to Figure 5 - T1 & E1 Free-Run, Line and External Sync Mode.

3.1.3 Line Synchronization Mode

Line Synchronization is typically used when a slave clock source, synchronized to the network is required.

In Line Synchronization Mode, the MT9071 uses an internal PLL to provide jitter free timing which is synchronized to one of the four clock signals RxCK[n] which is extracted from the receive data (RTIP[n], RRNG[n] pins). The selection of reference source is control and state dependent (see Table 3 - PLL State Table and Figure 7 - PLL State Diagram). The backplane bus and the transmit data are synchronized to the internal timing which is also output as a clock and frame pulse at the CKb and FPb pins. The accuracy of the timing is equal to the accuracy of the selected reference source. For circuit details, refer to Figure 5 - T1 & E1 Free-Run, Line and External Sync Mode.

3.1.4 External Synchronization Mode

External Synchronization is typically used when a slave clock source, from another device (such as another MT9071), synchronized to the network is required.

In External Synchronization Mode, the MT9071 uses an internal PLL to provide jitter free timing which is synchronized to the clock signal which is externally applied to the ESYN pin. The backplane bus and the transmit data are synchronized to the internal timing which is also output as a clock and frame pulse at the CKb and FPb pins. The accuracy of the timing is equal to the accuracy of the selected reference source. For circuit details, refer to Figure 5 - T1 & E1 Free-Run, Line and External Sync Mode.
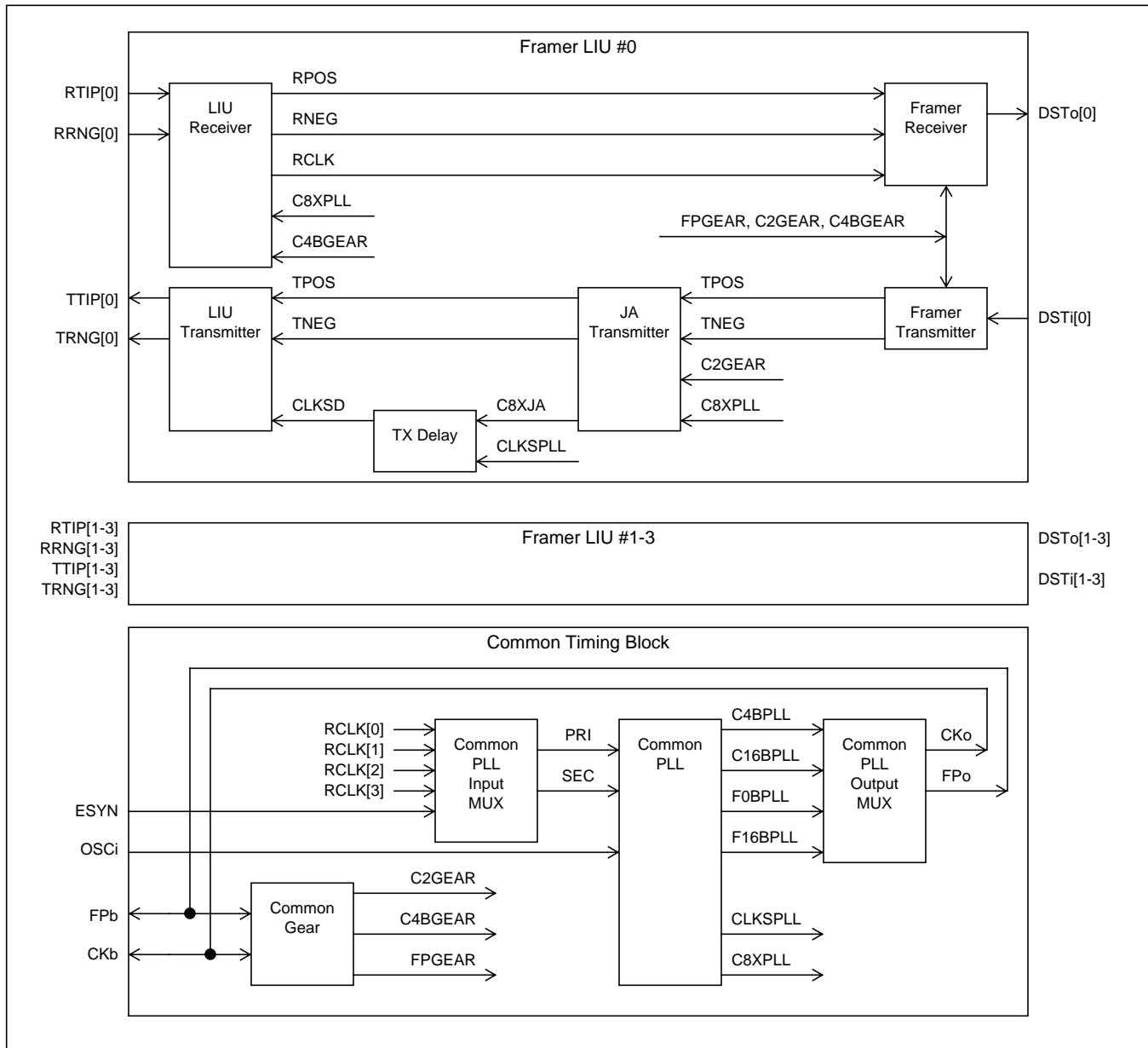
Figure 5 - T1 & E1 Free-Run, Line and External Sync Mode

3.1.5   Auto-Holdover Mode

An Input Impairment Monitor circuit monitors the input signal to the DPLL and automatically enables the Holdover Mode (Auto-Holdover) when the frequency of the incoming signal is outside the auto-holdover capture range (see AC Electrical Characteristics - Performance). This includes a complete loss of incoming signal, or a large frequency shift in the incoming signal. When the incoming signal returns to normal, the DPLL is returned to Line or External Synchronization Mode with the output signal locked to the input signal. The holdover output signal is based on the incoming signal 30ms minimum to 60ms prior to entering the Holdover Mode. The amount of phase drift while in holdover is negligible (for short durations i.e. 1 second) because the Holdover Mode is very accurate (e.g., ±0.05ppm).

3.1.6   Holdover Mode

Holdover Mode is typically used for short durations (e.g. 2 seconds) while network synchronization is temporarily disrupted.

In Holdover Mode, the MT9071 provides timing and synchronization signals, which are not locked to an external reference signal, but are based on storage techniques. The storage value is determined while the device is in Line or External Synchronization Mode and locked to an external reference signal.

When in Line or External Synchronization Mode, and locked to the input reference signal, a numerical value corresponding to the MT9071 output reference frequency is stored alternately in two memory locations every 30ms. When the device is switched into Holdover Mode, the value in memory from between 30ms and 60ms is used to set the output frequency of the device.

The frequency accuracy of Holdover Mode is ±0.05ppm, which translates to a worst case 35 frame (125us) slips in 24 hours.

Two factors affect the accuracy of Holdover Mode. One is drift on the Master Clock while in Holdover Mode, drift on the Master Clock directly affects the Holdover Mode accuracy. Note that the absolute Master Clock (OSCi) accuracy does not affect Holdover accuracy, only the change in OSCi accuracy while in Holdover. For example, a ±32ppm master clock may have a temperature coefficient of ±0.1ppm per degree C. So a 10 degree change in temperature, while the MT9071 is in Holdover Mode may result in an additional offset (over the ±0.05ppm) in frequency accuracy of ±1ppm. Which is much greater than the ±0.05ppm of the MT9071.

The other factor affecting accuracy is large jitter on the reference input prior (30ms to 60ms) to the mode switch. For instance, jitter of 7.5UI at 700Hz may reduce the Holdover Mode accuracy from 0.05ppm to 0.10ppm.

3.2   Remote Loopback

In normal T1 mode (not remote loopback), the jitter attenuator should not be enabled because the transmit data is synchronized with the transmit clock as it passes through the transmit slip buffer. However, when in T1 mode and in remote loopback, the jitter attenuator must be enabled, (see Table 172 - T1 & E1 LIU Transmitter Control - R/W Address YE2), since the transmit data is no longer passed through the slip buffer, and the transmit data must be in sync with the transmit clock. In addition, when in E1 mode and in remote loopback, the jitter attenuator must be enabled since the transmit data is no longer in sync with the transmit clock.
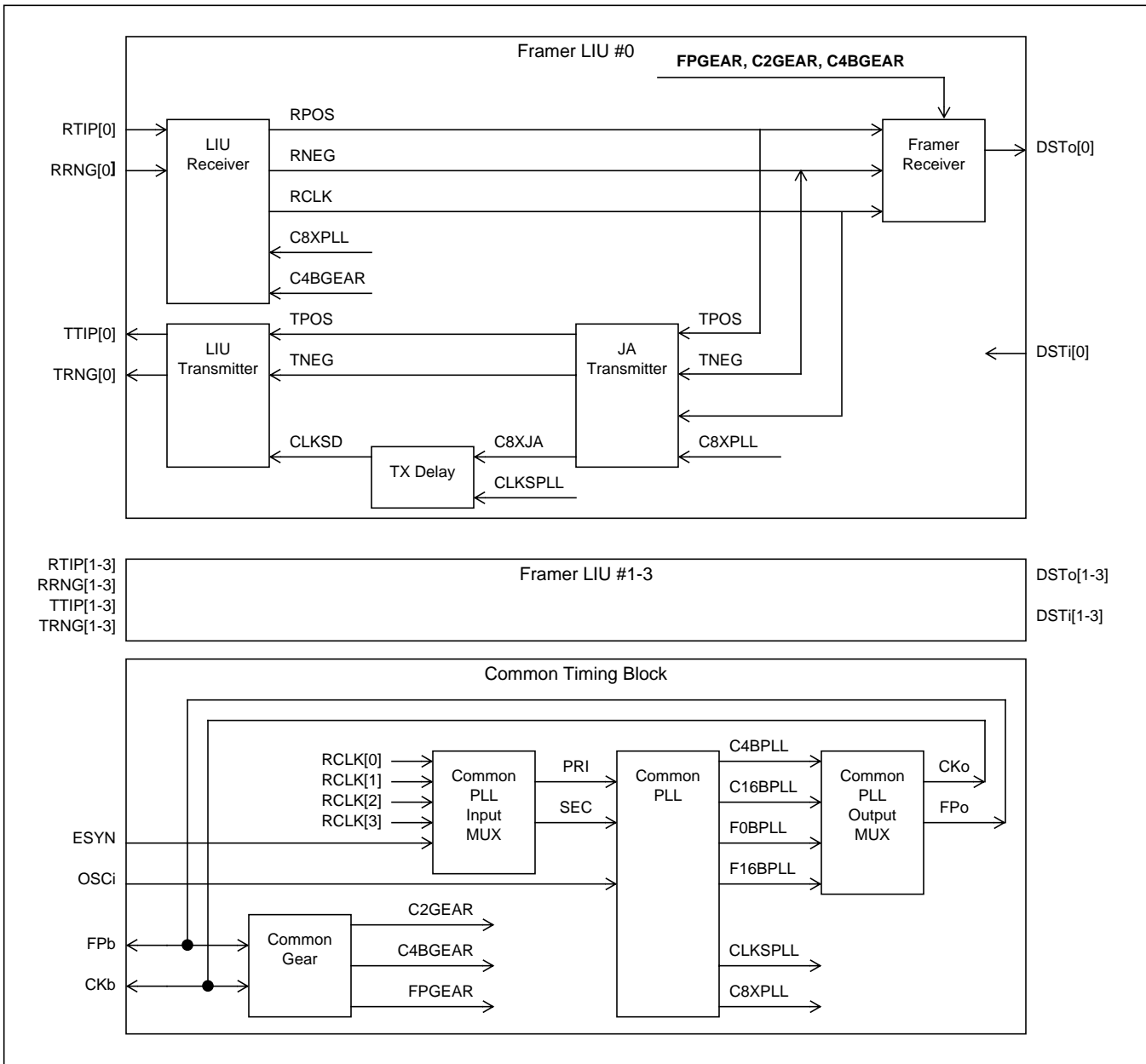
Figure 6 - T1 & E1 Remote Loopback (shown in Free-Run, Line and External Sync Mode)

3.3 Reference Switching

The MT9071 PLL accepts two simultaneous reference input signals referred to as the primary reference signal and the secondary reference signal. The input reference frequency must match the frequency selected with control register bits FS2-1 (see Table 73 - T1 & E1 Global Timing Control - R/W Address 905), also refer to Table 2 - Reference Selection Summary.

Framer Mode	PLL Input Frequency	*Compatible Input Reference Sources (Must be at the PLL Input Frequency)	Timing Mode
E1	2.048MHz	CKb, RxCK[3], RxCK[2], RxCK[1], RxCK[0] or ESYN	Bus, Line or External
E1	1.544MHz	ESYN	External
E1	8kHz	FPb or ESYN	Bus or External
T1	2.048MHz	CKb or ESYN	Bus or External
T1	1.544MHz	RxCK[3], RxCK[2], RxCK[1], RxCK[0] or ESYN	Line or External
T1	8kHz	FPb or ESYN	Bus or External
*The Compatible Input Reference Sources must be at the PLL Input Frequency with the exception of CKb. CKb is automatically divided down to 2.048MHz in both 2.048MHz and 8.192MHz backplane modes.			

Table 2 - Reference Selection Summary

A reference switch is made with a two step process using control register bits PR2-0, SR2-0 and RSEL (see Table 73 - T1 & E1 Global Timing Control - R/W Address 905). First, select a new compatible input reference source (see Table 73 - T1 & E1 Global Timing Control - R/W Address 905) for the non-current primary or secondary input with either PR2-0 and SR2-0 respectively. Next, toggle the RSEL control register bit.

For example, if the PLL is currently using primary reference RxCK[3], select a desired secondary reference (i.e. RxCK[0]) with SR2-0 (without changing the primary reference). Then, after waiting at least one frame (i.e. 125us), toggle RSEL from 0 to 1. Typically, the secondary reference is known and selected well in advance.

3.4 PLL State Changes

For state change details refer to Table 3 - PLL State Table and Figure 7 - PLL State Diagram.

Register and Bits				State				
T1 & E1 Global Timing Control - R/W Address 905				Freerun	Normal (Primary)	Normal (Secondary)	Holdover (Primary)	Holdover (Secondary)
MS2	MS1	RSEL	TIEE	S0	S1	S2	S1H	S2H
0	0	0	0	S1	-	S1 MTIE	S1	S1 MTIE
0	0	0	1	S1	-	S1 MTIE	S1 MTIE	S1 MTIE
0	0	1	X	S2	S2 MTIE	-	S2 MTIE	S2 MTIE
0	1	0	X	/	S1H	/	-	/
0	1	1	X	/	S2H	S2H	/	-
1	0	X	X	-	S0	S0	S0	S0
- No Change / Not Valid MTIE State change occurs with TIE Corrector Circuit Refer to Manual Control State Diagram for state changes to and from Auto-Holdover State								

Table 3 - PLL State Table

NOTES:
(XXX)MS2 MS1 RSEL
{A}Invalid Reference Signal

Movement to Normal State from any
state requires a valid input signal

——————— Phase Re-Alignment
– – – Phase Continuity Maintained (without TIE Corrector Circuit)
. . . . . Phase Continuity Maintained (with TIE Corrector Circuit)
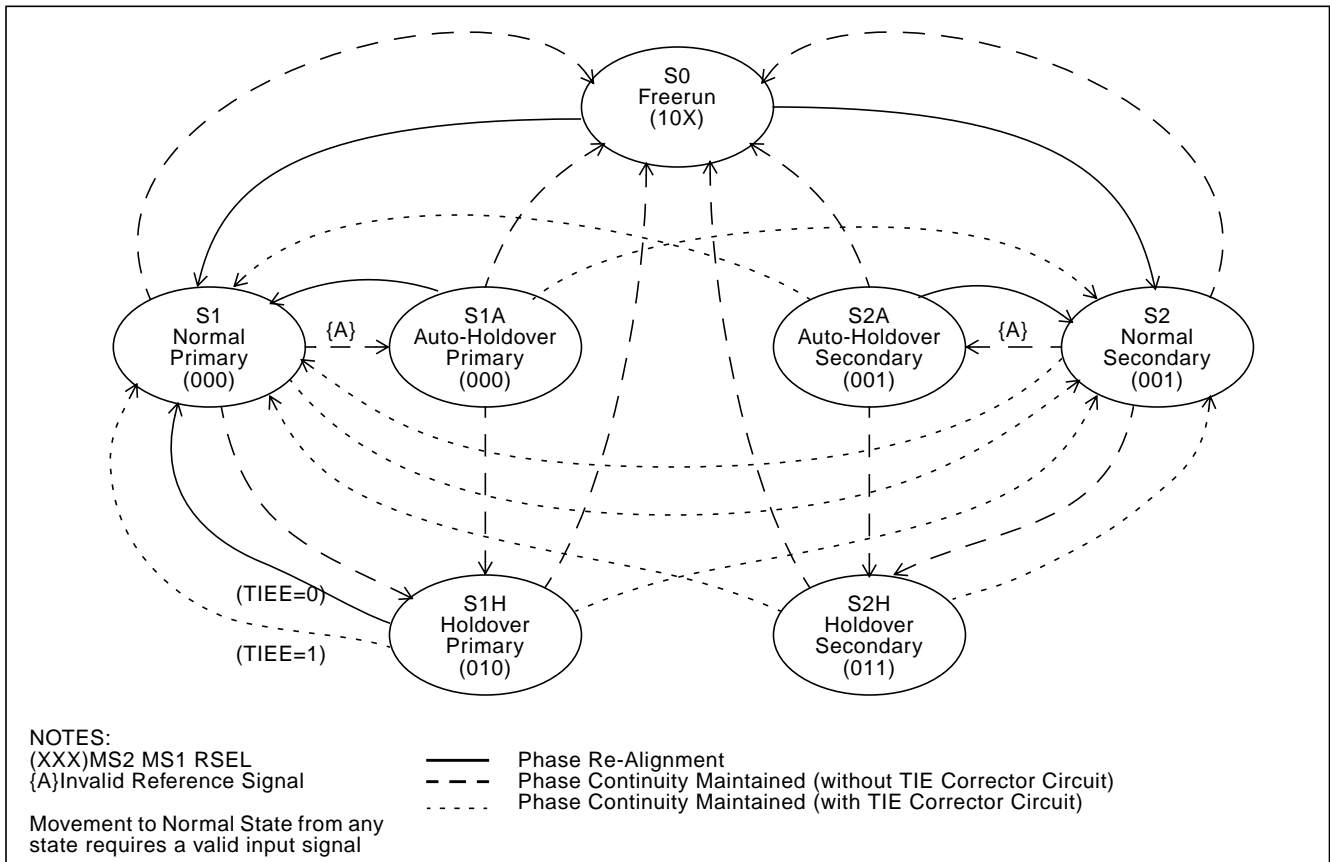
Figure 7 - PLL State Diagram

3.5   Master Clock

The MT9071 can use either a clock or crystal as the master timing source. For recommended master timing circuits, see Section 25.1 Master Clock.

3.6   Auxiliary Output Signals

The MT9071 provides four programmable output signals. All outputs are selected with control register bits ACC3-0 and ACF2-0 detailed in Table 70 - T1 & E1 Global Mode Control - R/W Address 900. See Table 4 - Auxiliary Output Signals Summary.

Register Bits		Functional Description	Output Pins Function			
ACC3-0	**ACF2-0**		**AUX3**	**AUX2**	**AUX1**	**AUX0**
0000	000	The value of ACC3-0 appears at AUX3-0.	0	0	0	0
0001			0	0	0	1
0010			0	0	1	0
etc.			etc.	etc.	etc.	etc.
1110			1	1	1	0
1111			1	1	1	1

Table 4 - Auxiliary Output Signals Summary

Register Bits		Functional Description	Output Pins Function			
ACC3-0	ACF2-0		AUX3	AUX2	AUX1	AUX0
not used	001	A TCLK (a 2MHz inverted ST-BUS C2 clock), SCLK (a 16MHz ST-BUS $\overline{C16}$ clock), RSP (a positive 8kHz frame pulse occurring after the ST-BUS $\overline{F0}$ frame pulse) and TSP (a positive 8kHz frame pulse occurring before the ST-BUS $\overline{F0}$ frame pulse). These signals are useful for interfacing to some multichannel external HDLC devices.	SCLK	TCLK	TSP	RSP
	010	Reserved.	RSV[3]	RSV[2]	RSV[1]	RSV[0]
	011	An active low receive multiframe boundary signal from each framer appears at the AUX3-0 pins.	$\overline{RXMF}$[3]	$\overline{RXMF}$[2]	$\overline{RXMF}$[1]	$\overline{RXMF}$[0]
	110-111	Reserved.	RSV[3]	RSV[2]	RSV[1]	RSV[0]

Table 4 - Auxiliary Output Signals Summary

4.0   Interface and Framing

4.1   T1 Interface Overview

In T1 mode, DS1 frames are 193 bits long and are transmitted at a frame repetition rate of 8000 Hz, which results in an aggregate bit rate of 193 bits x 8000 Hz = 1.544 Mb/s.   The actual bit rate is 1.544 Mb/s +/-50 ppm.

DS1 frames are divided into 24 DS0 channels numbered 1 to 24. Each channel is 8 bits in length and is transmitted most significant bit first. This results in a single channel data rate of 8 bits x 8000 Hz = 64 kb/s (see Figure 8 - DS1 Link Frame Format).

It should be noted that the bits of a DS0 channel are numbered one to eight, with one being most significant, while the bits of a ST-BUS channel are numbered seven to zero, with seven being most significant. Therefore, ST-BUS bit 7 is synonymous with DS0 bit 1. Refer to AC Electrical Characteristics - DS0, PCM30 and ST-BUS Frame Format in Section 24.0 AC and DC Electrical Characteristics.
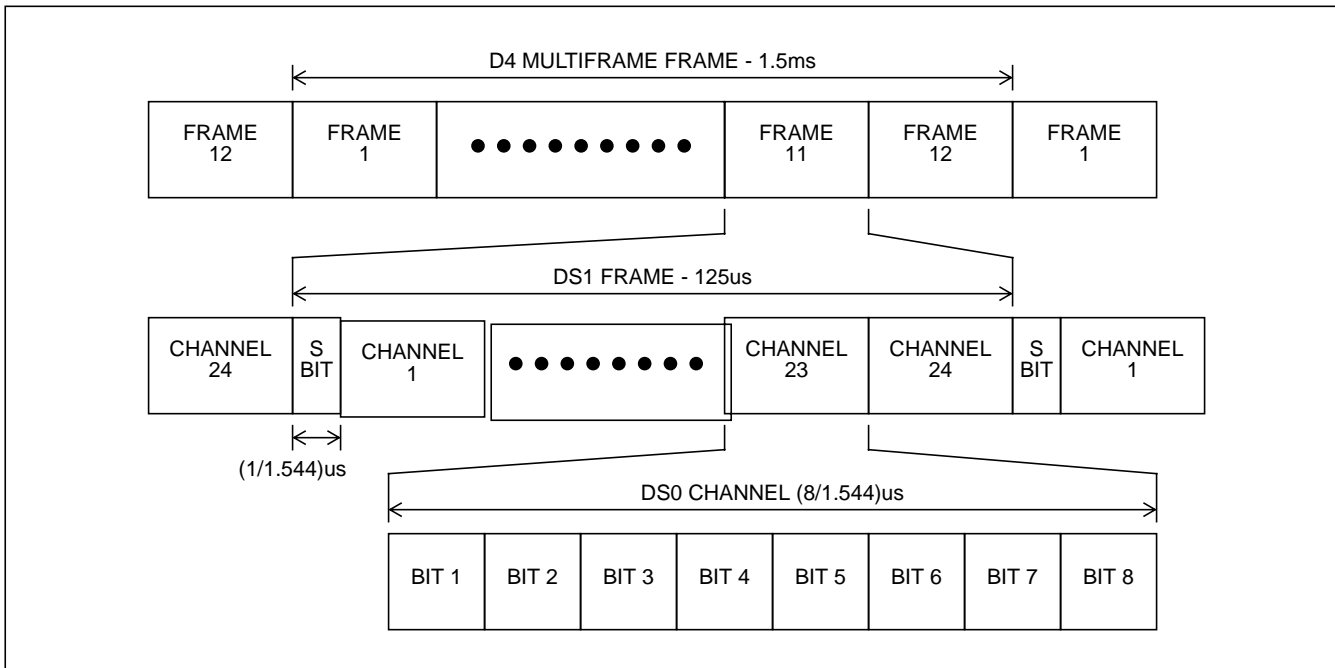
Figure 8 - DS1 Link Frame Format

The first bit of a DS1 frame is reserved for basic frame alignment, D4 and ESF multiframe alignment and the communication of maintenance information (data link). The remaining 24 timeslots (referred to as channels) carry either PCM encoded voice signals or digital data. Channel alignment and bit numbering is consistent with timeslot alignment and bit numbering. Also see Table 28 - T1 DS1 & ST-BUS DSTi/DSTo Timeslot Relationship.

4.1.1　T1 Encoding and Decoding Options

Numerous encoding options are selectable in the transmit direction with control register bit TZCS2-0 and TXB8ZS (see Table 80 - T1 Line Coding Control - R/W Address Y01), these include:

- No Zero Code Suppression.
- GTE Zero Code Suppression (bit 8 of an all zero channel byte is replaced by a one, except in signaling frames where bit 7 is forced to a one).
- DDS Zero Code Suppression (an all zero byte is replaced by 10011000).
- Bell Zero Code Suppression (bit 1, second bit of an all zero channel is replaced by a one).
- Jammed Bit 8 (bit 0 of all channels are replaced by a one).
- B8ZS.

Numerous decoding options are selectable in the receive direction with control register bits RZCS2-0 and RXB8ZS (see Table 80 - T1 Line Coding Control - R/W Address Y01), these include:

- No Zero Code Suppression.
- GTE Zero Code Suppression (bit 8 of an all zero channel byte is replaced by a one, except in signaling frames where bit 7 is forced to a one).
- DDS Zero Code Suppression (an all zero byte is replaced by 10011000).
- Bell Zero Code Suppression (bit 1, second bit of an all zero channel is replaced by a one).
- B8ZS.

Note: If a suppression code is enabled for a channel the B8ZS coding will not take place for the channel. Although 8 consecutive zeros in a non-channel boundary will be subjected to B8ZS suppression. Note that the bit designations are with respect to the PCM24 side where bit 1 is sent and received first. In all cases, Alternate Mark Inversion (AMI) is used in both transmit and receive directions.

4.1.2   T1 Pulse Density

Status register bit PDV (see Table 104 - T1 Synchronization and Alarm Status - R Address Y10) toggles if the receive data fails to meet ones density requirements. It will toggle upon detection of 16 consecutive zeros on the line data, or if there are fewer than N ones in a window of 8(N+1) bits - where N = 1 to 23.

If control register bit TPDV (see Table 80 - T1 Line Coding Control - R/W Address Y01) is set, then the output T1 data to be sent is monitored and if the 12.5% density requirement is detected over a maximum 192 bit window a one is inserted in a non-framing and non-signaling bit. The window and PDV criteria is the same as the received PDV. If this option is disabled the transmit data is sent unaltered.

4.2   T1 Frame Alignment

In T1 mode, the MT9071 will synchronize to DS1 lines formatted with either the D4 or ESF protocol. In either mode the framer maintains a running 3 bit history of received data for each of the candidate bit positions. Candidate bit positions whose incoming patterns fail to match the predicted pattern (based on the 3 bit history) are winnowed out. If, after a 10 bit history has been examined, only one candidate bit position remains within the framing bit period, the receive side timebase is forced to align to that bit position. If no candidates remain after a 10 bit history, the process is re-initiated. If multiple candidates exist after a 24 bit history time-out period, the framer forces the receive side timebase to synchronize to the next incoming valid candidate bit position. In the event of a reframe, the framer starts searching at the next bit position over. This prevents persistent locking to a mimic as the controller may initiate a software controlled reframe in the event of locking to a mimic.

Under software control the framing criteria may be tuned with control register bit CXC (see Table 78 - T1 Framing Mode Control - R/W Address Y00).

Selecting D4 framing invites a further decision whether or not to include a cross check of Fs bits along with the Ft bits. If Fs bits are checked (set CXC control register bit high), multiframe alignment is forced at the same time as terminal frame alignment. If only Ft bits are checked, multiframe alignment is forced separately, upon detection of the Fs bit history of 00111 (for normal D4 trunks). For D4 trunks, a reframe on the multiframe alignment may be forced at any time without affecting terminal frame alignment.

In ESF mode the circuit will optionally confirm the CRC-6 bits before forcing a new frame alignment. This is programmed by setting control register bit CXC high. A CRC-6 confirmation adds a minimum of 6 milliseconds to the reframe time. If no CRC-6 match is found after 16 attempts, the framer moves to the next valid candidate bit position (assuming other bit positions contain a match to the framing pattern) or re-initiates the whole framing procedure (assuming no bit positions have been found to match the framing pattern).

The framing circuit is off - line. During a reframe, the rest of the circuit operates synchronous with the last frame alignment. Until such time as a new frame alignment is achieved, the signaling bits are frozen in their states at the time that frame alignment was lost, and error counting for Ft, Fs, ESF framing pattern or CRC-6 bits is suspended.

4.3   T1 Reframe

The MT9071 will automatically force a reframe if the framing bit error density exceeds the threshold programmed with control register bits RS1-0 (see Table 78 - T1 Framing Mode Control - R/W Address Y00). RS1 = RS0 = 0 forces a reframe for 2 errors out of a sliding window of 4 framing bits. RS1 = 0, RS0 = 1 forces a reframe with 2 errors out of 5. RS1 = 1, RS0 = 0 forces a reframe with 2 errors out of 6. RS1 = RS0 = 1 disables the automatic reframe.

In ESF mode all framing bits are checked.

In D4 mode, bit checking selection is done with control register bit FSI (see Table 78 - T1 Framing Mode Control - R/W Address Y00). If FSI is set low, only Ft bits are checked. If FSI is set high, both Ft and Fs bits are

checked. If the D4 secondary yellow alarm is enabled with control register bit D4SECY (see Table 82 - T1 Transmit Alarm Control - R/W Address Y02), then the Fs bit of frame 12 is not verified for the loss of frame circuit.

In T1DM mode, the synchronization error criteria for the receiver will be the same as D4.

No reframing is forced by the device when in transparent mode, selected by setting control register bit TRANSP (see Table 78 - T1 Framing Mode Control - R/W Address Y00).

The user may initiate a software reframe at any time by setting control register bit REFR (see Table 78 - T1 Framing Mode Control - R/W Address Y00). Once the circuit has commenced reframing, the signaling bits are frozen until multiframe synchronization has been achieved.

4.4 T1 Multiframing

In T1 mode, DS1 trunks contain 24 bytes of serial voice/data channels bundled with an overhead bit. The frame overhead bit contains a fixed repeating pattern used to enable DS1 receivers to delineate frame boundaries. Overhead bits are inserted once per frame at the beginning of the transmit frame boundary. The DS1 frames are further grouped in bundles of frames, generally 12 (for D4 applications) or 24 frames (for ESF - extended superframe applications) deep.

The protocol (D4 or ESF) appropriate for the application is selected with control register bit ESF (see Table 78 - T1 Framing Mode Control - R/W Address Y00). In T1 mode, the MT9071 is capable of generating the overhead bit framing pattern and for ESF links, the CRC remainder for transmission onto the DS1 trunk. The beginning of the transmit multiframe may be determined by any of the following criteria:

(i) It may free - run with the internal multiframe counters;

(ii) The multiframe counters may be reset with the external hardware pin $\overline{\text{TxMF}}$. If this signal is not synchronous with the current transmit frame count it may cause the far end to go temporarily out of sync.

(iii) Under software control by setting control register bit TXSYNC (see Table 78 - T1 Framing Mode Control - R/W Address Y00). The transmit multiframe counters will be synchronized to the framing pattern present in the overhead bits multiplexed into channel 31 bit 0 of the incoming 2.048 Mb/s digital stream DSTi. Note that the overhead bits extracted from the receive signal are multiplexed into outgoing DSTo channel 31 bit 0.

4.4.1 T1 D4 Multiframing
For D4 links, the frame structure contains an alternating 101010... pattern inserted into every second overhead bit position. These bits are intended for determination of frame boundaries, and they are referred to as Ft bits. A separate fixed pattern, repeating every superframe, is interleaved with the Ft bits. This fixed pattern (001110), is used to delineate the 12 frame superframe. These bits are referred to as the Fs bits. In D4 frames # 6 and #12, the LSB of each channel byte may be replaced with A bit (frame #6) and B bit (frame #12) signaling information.

Frame #	SBit		Signaling Bits (LSB of Each Channel)
	Ft	Fs	
1	1		
2		0	
3	0		
4		0	
5	1		
6		1	A
7	0		
8		1	
9	1		
10		1	
11	0		
12		0	B

Table 5 - T1 D4 Superframe Structure

4.4.2 T1 T1DM Mode

The Ft and Fs bits are identical to the D4 format. However, channel 24 of each frame has a synchronization byte consisting of 10111YR0. Y is used to indicate a yellow alarm and is active low. R bit is reserved by AT&T as an 8 kb/s communication channel. The synchronization is first declared if the Ft bit is in sync and subsequently 6 consecutive T1DM synchronization bytes are received. The synchronization error criteria for the receiver will be the same as D4 (i.e. 2 out of 4, 5 or 6).The OOF error selection criteria of 2 errors out of 4, 5, 6 bits is also applicable to the T1DM synchronization byte format. The received synchronization byte can be monitored by the status register bits (see Table 104 - T1 Synchronization and Alarm Status - R Address Y10). The R and Y bits can be set with control register bits TT1DMR and TT1DMY (see Table 82 - T1 Transmit Alarm Control - R/W Address Y02).

Frame #	SBit		Signaling Bits (LSB of Each Channel)	Synchronization Byte
	Ft	Fs		
1	1			10111YR0
2		0		"
3	0			"
4		0		"
5	1			"
6		1	A	"
7	0			"
8		1		"
9	1			"
10		1		"
11	0			"
12		0	B	"

Table 6 - T1 T1DM Superframe Structure

4.4.3 T1 ESF Multiframing

For ESF links the 6 bit framing pattern 001011, inserted into every 4th overhead bit position, is used to delineate both frame and superframe boundaries. Frames #6, 12, 18 and 24 contain the A, B, C and D signaling bits, respectively. A 4 kHz Data Link (FDL) is embedded in the overhead bit position, interleaved between the framing pattern sequence (FPS) and the transmit CRC-6 remainder which was calculated on the previous superframe (see Table 7 - T1 ESF Superframe Structure).

Frame #	SBit			Signaling Bits (LSB of Each Channel)	Frame #	SBit			Signaling Bits (LSB of Each Channel)
	FPS	FDL	CRC			FPS	FDL	CRC	
1		X			13		X		
2			CB1		14			CB4	
3		X			15		X		
4	0				16	0			
5		X			17		X		
6			CB2	A	18			CB5	C
7		X			19		X		
8	0				20	1			
9		X			21		X		
10			CB3		22			CB6	
11		X			23		X		
12	1			B	24	1			D

Table 7 - T1 ESF Superframe Structure

5.0 E1 Interface and Framing

5.1 E1 Interface Overview

In E1 mode, PCM30 basic frames are 256 bits long and are transmitted at a frame repetition rate of 8000 Hz, which results in an aggregate bit rate of 256 bits x 8000 Hz = 2.048Mb/s. The actual bit rate is 2.048Mb/s +/-50 ppm.

Basic frames are divided into 32 timeslots numbered 0 to 31. Each timeslot is 8 bits in length and is transmitted most significant bit first. This results in a single timeslot data rate of 8 bits x 8000 Hz = 64 kb/s (see Figure 9 - PCM30 Link Frame Format).

It should be noted that the bits of a PCM30 channel are numbered one to eight, with one being most significant, while the bits of a ST-BUS channel are numbered seven to zero, with seven being most significant. Therefore, ST-BUS bit 7 is synonymous with PCM30 bit 1. Refer to AC Electrical Characteristics - DS0, PCM30 and ST-BUS Frame Format in Section 24.0 AC and DC Electrical Characteristics.
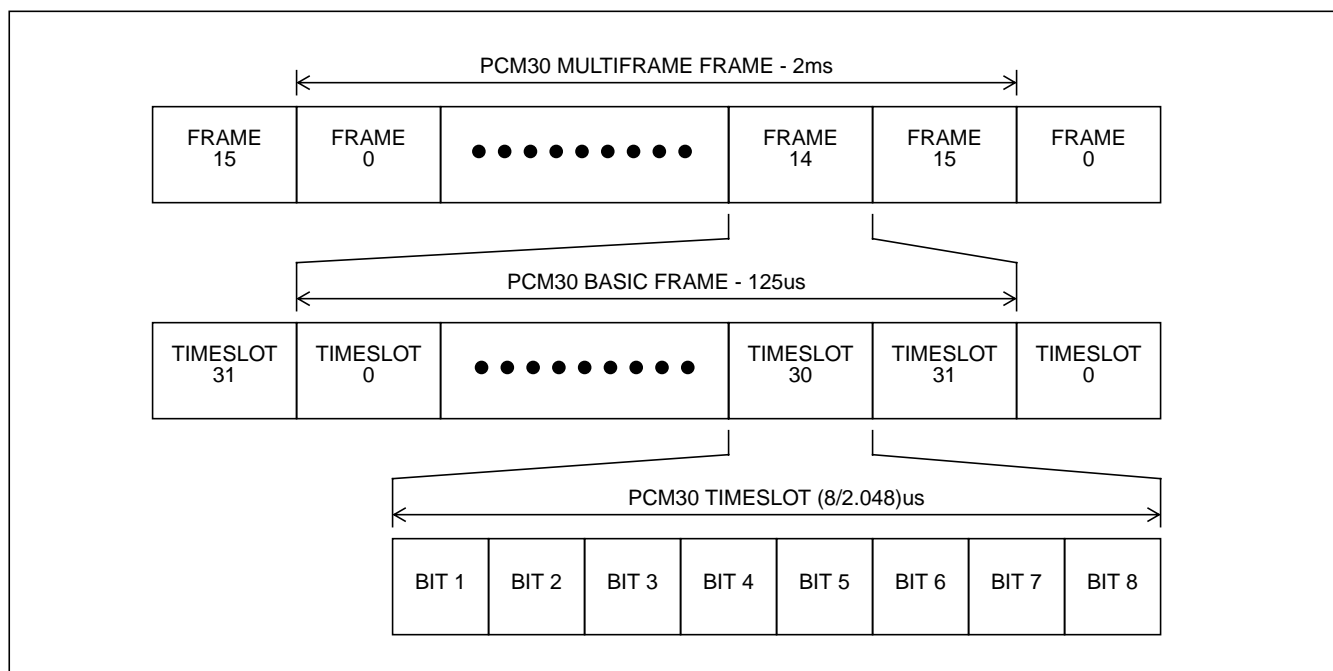
Figure 9 - PCM30 Link Frame Format

PCM30 timeslot 0 is reserved for basic frame alignment, CRC-4 multiframe alignment and the communication of maintenance information (data link). In most configurations, timeslot 16 is reserved for either CAS or CCS. For V5.2 applications, timeslots 15, 16 and 31 may be used for CCS. The remaining timeslots (referred to as channels) carry either PCM encoded voice signals or digital data. Channel alignment and bit numbering is consistent with timeslot alignment and bit numbering. However, channels are numbered 1 to 30 and do not directly relate to timeslots. Also see Table 28 - T1 DS1 & ST-BUS DSTi/DSTo Timeslot Relationship.

5.1.1 E1 Encoding and Decoding Options

Two encoding options are available in the transmit and receive directions. These encoding options include High Density Bipolar 3 (HDB3) encoding and no encoding.

These options are selectable with control register bit $\overline{THDB3}$ and $\overline{RHDB3}$ (see Table 83 - E1 Interrupts and I/O Control - R/W Address Y02).

In all cases, Alternate Mark Inversion (AMI) is used in both transmit and receive directions.

5.2 E1 Frame Alignment

Timeslot 0 of every 125us frame is reserved for basic frame alignment and contains a Frame Alignment Signal (FAS) or a Non-Frame Alignment Signal (NFAS). FAS and NFAS occur in consecutive basic frames (see Table 8 - E1 CRC-4 FAS and NFAS Structure).

Bit one of the FAS can be either a CRC-4 remainder bit or an international usage bit.

Bit one of the NFAS can be either a CRC-4 multiframe alignment signal, an E-bit or an international usage bit. Refer to an approvals laboratory and national standards bodies for specific requirements.

Bit two of the FAS and NFAS is used to distinguish between FAS (bit two = 0) and NFAS (bit two = 1) frames.

Bits three to eight of the FAS are used for basic frame alignment. Basic frame alignment is initiated by a search for the bit sequence 0011011 which appears in the last seven bit positions of the FAS, see Section 5.5 E1 Framing Algorithms.

Bit three of the NFAS (designated as "A"), the Remote Alarm Indication (RAI), is used to indicate the near end basic frame synchronization status to the far end of a link. Under normal operation, the A (RAI) bit should be set to 0, while in alarm condition, it is set to 1.

Bits four to eight of the NFAS (i.e., Sa4-8) are additional spare bits which may be used as follows:

- Sa4-8 may be used in specific point-to-point applications (e.g. transcoder equipment conforming to G.761).
- Sa4 may be used as a message-based data link for operations, maintenance and performance monitoring.
- Sa5-Sa8 are for national usage.

Note that for simplicity all Sa bits including Sa4 are collectively called national bits throughout this document. For accessing the national bits see Section 11.2 E1 Data Link Operation.

5.3   E1 Reframe

The MT9071 will automatically force a reframe, if three consecutive frame alignment patterns or three consecutive non-frame alignment bits are in error.

5.4   E1 Multiframing

5.4.1   E1 CAS Multiframing
Refer to Section 10.2 E1 CAS.

5.4.2   E1 CRC-4 Multiframing
The primary purpose for CRC-4 multiframing is to provide a verification of the current basic frame alignment, although it can also be used for other functions such as bit error rate estimation. The CRC-4 multiframe consists of 16 basic frames numbered 0 to 15, and has a repetition rate of 16 frames X 125us/frame = 2ms.

CRC-4 multiframe alignment is based on the 001011 bit sequence, which appears in bit position one of the first six NFASs of a CRC-4 multiframe.

The CRC-4 multiframe is divided into two sub multiframes, numbered 1 and 2, which are each eight basic frames or 2048 bits in length.

CRC-4	CRC-4 Frame/Type	PCM30 Timelsot Zero							
		1	2	3	4	5	6	7	8
Sub Multi Frame 1	0/FAS	C_1	0	0	1	1	0	1	1
	1/NFAS	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	2/FAS	C_2	0	0	1	1	0	1	1
	3/NFAS	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	4/FAS	C_3	0	0	1	1	0	1	1
	5/NFAS	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	6/FAS	C_4	0	0	1	1	0	1	1
	7/NFAS	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
Sub Multi Frame 2	8/FAS	C_1	0	0	1	1	0	1	1
	9/NFAS	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	10/FAS	C_2	0	0	1	1	0	1	1
	11/NFAS	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	12/FAS	C_3	0	0	1	1	0	1	1
	13/NFAS	E_1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	14/FAS	C_4	0	0	1	1	0	1	1
	15/NFAS	E_2	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}

Table 8 - E1 CRC-4 FAS and NFAS Structure

☐ indicates position of CRC-4 multiframe alignment signal.

The CRC-4 frame alignment verification functions as follows. Initially, the CRC-4 operation must be activated and CRC-4 multiframe alignment must be achieved at both ends of the link. At the local end of a link, all the bits of every transmit submultiframe are passed through a CRC-4 polynomial (multiplied by X^4 then divided by $X^4 + X + 1$), which generates a four bit remainder. This remainder is inserted in bit position one of the four FASs of the following submultiframe before it is transmitted (see Table 8 - E1 CRC-4 FAS and NFAS Structure).

The submultiframe is then transmitted and, at the far end, the same process occurs. That is, a CRC-4 remainder is generated for each received submultiframe. These bits are compared with the bits received in position one of the four FASs of the next received submultiframe. This process takes place in both directions of transmission.

When more than 914 CRC-4 errors (out of a possible 1000) are counted in a one second interval, the framing algorithm will force a search for a new basic frame alignment (see Section 5.5 E1 Framing Algorithms).

The result of the comparison of the received CRC-4 remainder with the locally generated remainder will be transported to the far end by the E-bits. Therefore, if $E_1 = 0$, a CRC-4 error was discovered in a submultiframe 1 received at the far end; and if $E_2 = 0$, a CRC-4 error was discovered in a submultiframe 2 received at the far end. No submultiframe sequence numbers or re-transmission capabilities are supported with layer 1 PCM30 protocol (see ITU-T G.704 and G.706 for more details on the operation of CRC-4 and E-bits).

5.4.3 E1 Automatic CRC-4 Interworking

The MT9071 framing algorithm supports automatic interworking of interfaces with and without CRC-4 processing capabilities when control register bit $\overline{\text{AUTC}}$ (see Table 79 - E1 Alarms and Framing Control - R/W Address Y00) is set to zero. That is, if an interface with CRC-4 capability, achieves valid basic frame alignment, but does not achieve CRC-4 multiframe alignment by the end of a predefined period, the distant end is

considered to be a non-CRC-4 interface. When the distant end is a non-CRC-4 interface, the near end automatically suspends receive CRC-4 functions, continues to transmit CRC-4 data to the distant end with its E-bits set to zero, and provides a status indication. Naturally, if the distant end initially achieves CRC-4 synchronization, CRC-4 processing will be carried out by both ends.

When control register bit $\overline{AUTC}$ is one, Automatic CRC-4 Interworking is deactivated. In this case, if control register bit $\overline{ARAI}$ (see Table 79 - E1 Alarms and Framing Control - R/W Address Y00) is low, and if CRC-4 multiframe alignment is not found in 400ms, then the transmit RAI will be continuously high until CRC-4 multiframe alignment is achieved.

The transmit E bits control register bit TE (see Table 79 - E1 Alarms and Framing Control - R/W Address Y00) will have the same function in both states of $\overline{AUTC}$. That is, when CRC-4 synchronization is not achieved the state of the transmit E-bits will be the same as the state of the TE control register bit. When CRC-4 synchronization is achieved, the transmit E-bits will function as per ITU-T G.704 as (see Section 5.4.2 E1 CRC-4 Multiframing, Table 9 -E1 Operation of $\overline{AUTC}$, $\overline{ARAI}$ and TALM Control Register Bits, and Table 10 - E1 CRC Interworking Status Register Bits).

Register Bits			Description		
$\overline{AUTC}$	$\overline{ARAI}$	TALM	Before the 400ms Timer Expires		After the 400ms Timer Expires
			No Valid CRC MFAS	Valid CRC MFAS	
0	0	X	If no valid CRC MFAS is being received, the device will search for a new basic frame alignment signal every 8ms for 400ms. During this cycle, the transmit RAI will flicker high with every reframe (8ms).	If a valid CRC MFAS is received during the 400ms period, the device will set status register bits CSYNCB = 0, CRCIW = 1 as (see Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10), and will set the transmit E-bits as per G.703 and will send RAI low continuously.	Following the 400ms, the device will continue to transmit CRC-4 remainders, will set the transmit E-bits to be the same state as the TE control register bit (see Table 79 - E1 Alarms and Framing Control - R/W Address Y00), will send RAI low continuously, and will indicate CRC-to-non-CRC operation with status register bit CRCIW = 0 (see Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10). The device will continue searching for CRC MFAS, however, the above operation (CRC-to-non-CRC) will not change if CRC MFAS sync is found, as indicated with status register bits CSYNCB = 0, CRCIW = 0 (see Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10).
1	0	X			Following the 400ms, the device will continue to transmit CRC-4 remainders, will set the transmit E-bits to be the same state as the TE control register bit (see Table 79 - E1 Alarms and Framing Control - R/W Address Y00), will send RAI high continuously, and will indicate that it is attempting CRC-to-CRC operation with status register bit CRCIW = 1 (see Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10). The device will continue searching for CRC MFAS, and if found, will set status register bits CSYNCB = 0, CRCIW = 1 as (see Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10), and will set the transmit E-bits as per G.703 and will send RAI low continuously
X	1	0	Transmit RAI is low continuously.		
X	1	1	Transmit RAI is high continuously.		

Table 9 - E1 Operation of $\overline{AUTC}$, $\overline{ARAI}$ and TALM Control Register Bits

Status	CRCIW	CSYNC
CRC to Non-CRC Interworking, CRC sync acquired after the 400ms timer, but interworking operation does not change.	0	0
CRC to Non-CRC Interworking, CRC sync not yet acquired.	0	1
CRC to CRC Interworking, CRC sync acquired.	1	0
CRC to CRC Interworking, CRC sync not yet acquired.	1	1

Table 10 - E1 CRC Interworking Status Register Bits

5.5 E1 Framing Algorithms

The MT9071 contains three distinct framing algorithms: basic frame alignment, signaling multiframe alignment and CRC-4 multiframe alignment. To see how these algorithms interact, see Figure 10 - E1 Synchronization State Diagram.

After power-up, the basic frame alignment framer will search for a frame alignment signal (FAS) in the PCM30 receive bit stream. Once the FAS is detected, the corresponding bit 2 of the non-frame alignment signal (NFAS) is checked. If bit 2 of the NFAS is zero a new search for basic frame alignment is initiated. If bit 2 of the NFAS is one and the next FAS is correct, the algorithm declares that basic frame synchronization has been found and sets status register bit $\overline{BSYNC}$ =0 (see Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10).

Once basic frame alignment is acquired the signaling and CRC-4 multiframe searches will be initiated. The signaling multiframe algorithm will align to the first multiframe alignment signal pattern (MFAS = 0000) it receives in the most significant nibble of channel 16 and sets status register bit $\overline{MSYNC}$ = 0 (see Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10).Signaling multiframing will be lost when two consecutive multiframes are received in error.

The CRC-4 multiframe alignment signal is a 001011 bit sequence that appears in PCM30 bit position one of the NFAS in frames 1, 3, 5, 7, 9 and 11 (see Table 8 - E1 CRC-4 FAS and NFAS Structure). In order to achieve CRC-4 synchronization, two consecutive CRC-4 multiframe alignment signals must be received without error, this is indicated with status register bit $\overline{CSYNC}$ = 0 (see Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10).

The MT9071 framing algorithm supports automatic interworking of interfaces with and without CRC-4 processing capabilities. That is, if an interface with CRC-4 capability, achieves valid basic frame alignment, but does not achieve CRC-4 multiframe alignment by the end of a predefined period, the distant end is considered to be a non-CRC-4 interface. When the distant end is a non-CRC-4 interface, the near end automatically suspends receive CRC-4 functions, continues to transmit CRC-4 data to the distant end with its E-bits set to zero, and provides a status indication. Naturally, if the distant end initially achieves CRC-4 synchronization, CRC-4 processing will be carried out by both ends. This feature is selected when control register bit $\overline{AUTC}$ =0 (see Table 79 - E1 Alarms and Framing Control - R/W Address Y00).

Out of Basic Sync
($\overline{\text{BSYNC}}$ = 1)

No

Search for Basic Sync

Yes

Basic Sync Acquired
($\overline{\text{BSYNC}}$ = 0)
If ARAI=0 Send RAI = 0
Start Checking for Loss of

$\overline{\text{AUTC}}$=1
&
$\overline{\text{CSYN}}$=1

No

Yes

Send
FAS Bit1 = TIU0

CRC to CRC
(CRCIW = 1)

CRC-4
Multiframing Path

Out of CRC4 Sync

Start 400ms timer

Start 8ms timer

Parallel Search for
New Basic Sync

Search for CRC4 Sync
Verify 2 Consecutive
multiframes

No

8ms timer

No

Yes

Align to
New Basic Frame

Yes

No

400ms timer

If $\overline{\text{ARAI}}$ = 0
Send RAI = Flickered

CRC4 Sync Acquired
($\overline{\text{CSYNC}}$ = 0)

Yes

$\overline{\text{AUTC}}$ = 0

No

If $\overline{\text{ARAI}}$ = 0
Send RAI = 1

If $\overline{\text{ARAI}}$ = 0
Send RAI = 0

Send E1 E2 as per G.703
(Note 7,8 & 9)

Yes

If $\overline{\text{ARAI}}$ = 1
Send RAI = TALM

CAS
Multiframe Alignment Signal

Out of MAS Sync
($\overline{\text{MSYNCB}}$ = 1)

No

Search for MAS Sync
Verify as per G.732

Yes

No

MAS Sync Acquired
($\overline{\text{MSYNCB}}$ = 0)
Start Checking for Loss of
MAS Sync

Yes

CRC to Non-CRC
Multiframing Path

CRC to Non-CRC
(CRCIW = 0)
Send CRC4 Framing

If $\overline{\text{ARAI}}$ = 0
Send RAI = 0

Send E1 E2 = TE

Search for CRC4 Sync
Verify 2 Consecutive
multiframes (Note 7)

No

Yes

CRC4 Sync Acquired
($\overline{\text{CSYNC}}$ = 0)
Continue Operating With
CRC to Non-CRC
(Note 7)

Figure 10 - E1 Synchronization State Diagram

Note 1. The basic frame alignment, signaling multiframe alignment, and CRC-4 multiframe alignment functions operate in parallel and are independent.
Note 2. The receive CAS bits and signaling multiframe alignment bit will be frozen when multiframe alignment is lost.
Note 3. Manual re-framing of the receive basic frame alignment and signaling multiframe alignment functions can be performed at any time.
Note 4. The transmit RAI bit will be one until basic frame alignment is established, then it will be zero.
Note 5. E-bits can be optionally set to zero until the equipment interworking relationship is established. When this has been determined one of the following will take place:
 a. CRC-to-non-CRC operation - E-bits = 0,
 b. CRC-to-CRC operation - E-bits as per G.704 and I.431.
Note 6. All manual re-frames and new basic frame alignment searches start after the current frame alignment signal position.
Note 7. After basic frame alignment has been achieved, loss of frame alignment will occur any time three consecutive incorrect basic frame alignment signals are received. Loss of basic frame alignment will reset the complete framing algorithm.
Note 8. When CRC-4 multiframing has been achieved, the primary basic frame alignment and resulting multiframe alignment will be adjusted to the basic frame alignment determined during CRC-4 synchronization. Therefore, the primary basic frame alignment will not be updated during the CRC-4 multiframing search, but will be updated when the CRC-4 multiframing search is complete.
Note 9. 915 or more CRC errors in one second will reset the complete framing algorithm.

6.0   Slip Buffers and Jitter Attenuators

6.1   T1 Slip Buffer

In T1 mode MT9071 contains two sets of slip buffers, one on the transmit side, and one on the receive side. Both sides may perform a controlled slip. The mechanisms that govern the slip function are a function of backplane timing and the mapping between the ST-BUS channels and the DS1 channels. The slip mechanisms are different for the transmit and receive slip buffers. The extracted 1.544 MHz clock (RxCK) and the internally generated transmit 1.544 MHz clock are distinct. Slips on the transmit side are independent from slips on the receive side.

6.1.1   T1 Transmit Slip Buffer

The transmit slip buffer has data written to it from the near end 2.048 Mb/s stream. The data is clocked out of the buffer using signals derived from the internal transmit 1.544 MHz clock. The transmit 1.544 MHz clock is always phase locked to the DSTi 2.048 Mb/s stream. If the system backplane clock (CKb is an output) is internally generated, then it is hard locked to the 1.544 MHz clock. No phase drift or wander can exist between the two signals - therefore no slips will occur. The delay through the transmit elastic buffer is then fixed, and is a function of the relative mapping between the DSTi channels and the DS1 timeslots. These delays vary with the position of the channel in the frame. For example, DS1 timeslot 1 sits in the elastic buffer for approximately 1us and DS1 timeslot 24 sits in the elastic buffer for approximately 32us. Note that the system backplane clock (CKb) is internally generated for all timing modes except Bus Sync mode, see Table 1 - E1 and T1 Timing Modes Summary.
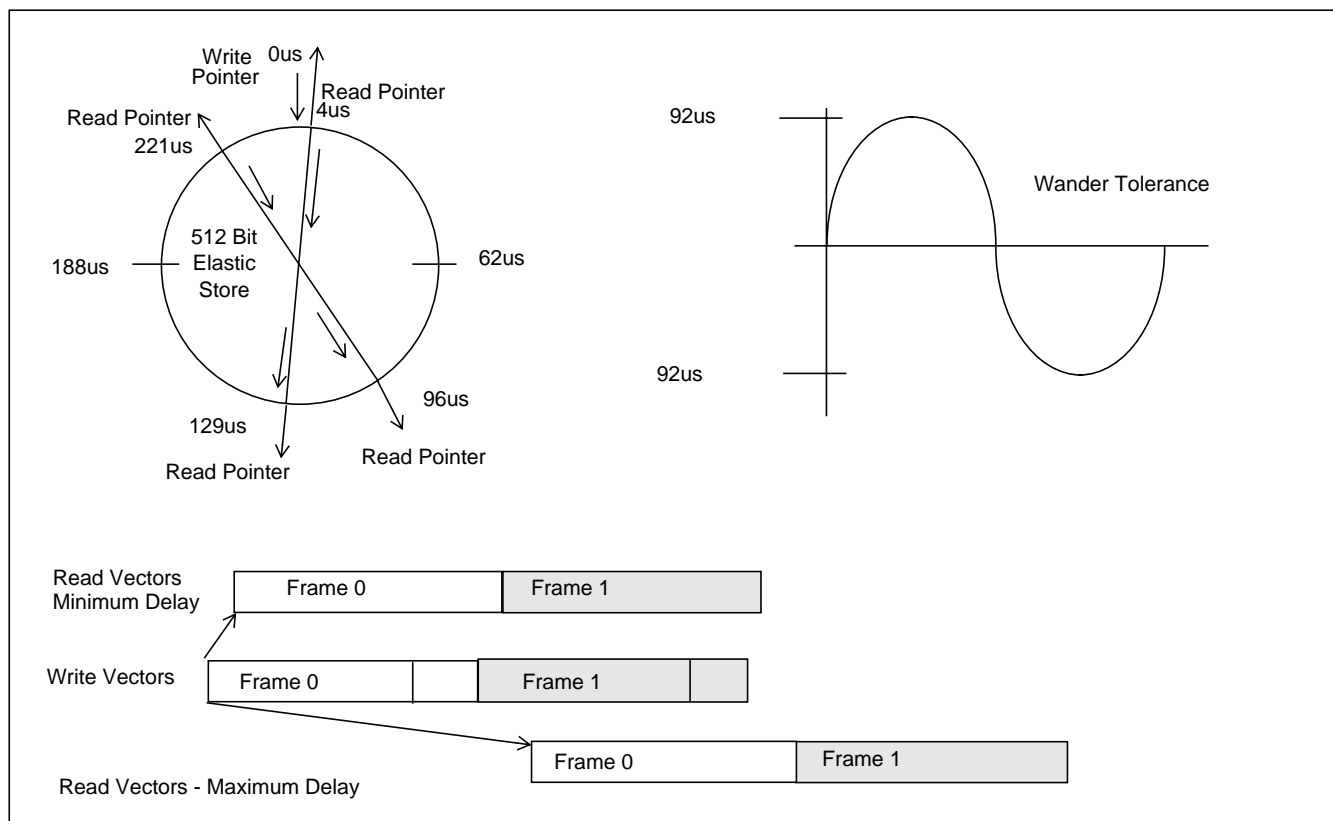
Figure 11 - Read and Write Pointers in the T1 Transmit Slip Buffers

If the system backplane clock (CKb) is externally generated, the transmit 1.544 MHz clock is phase locked to it, but the PLL is designed to filter jitter present in the CKb clock. As a result phase drift will result between the two signals. The delay through the transmit elastic buffer will vary in accordance with the input clock drift, as well as being a function of the relative mapping between the DSTi channels and the DS1 timeslots. If the read pointers approach the write pointers (to within approximately 1us) or the delay through the transmit buffer exceeds

218us, a controlled slip will occur. The contents of a single frame of DS1 data will be skipped or repeated, this will cause the following events to occur:

- The status register bit TSLP will toggle (see Table 112 - T1 Transmit Elastic Buffer Status - R Address Y14).
- The latched status register bit TSLPL = 1 (see Table 136 - T1 Elastic Store Status Latch - R Address Y26).
- The interrupt status register bit TSLPI = 1 (see Table 153 - T1 Elastic Store Interrupt Status - R Address Y36), if unmasked with mask control register bit TSLPM = 0 (see Table 160 - T1 Elastic Store Interrupt Mask - R/W Address Y46).

The direction of the slip is indicated with status register bit TSLPD (see Table 112 - T1 Transmit Elastic Buffer Status - R Address Y14). The relative phase delay between the system frame boundary and the transmit elastic frame read boundary is measured every second frame and reported in the status register bits TXSBMSB, TXTS4-0 and TXBC2-0 (see Table 112 - T1 Transmit Elastic Buffer Status - R Address Y14). In addition the relative offset between these frame boundaries may be programmed by writing to control register bits TXSD7-0 (see Table 184 - T1 Transmit Elastic Buffer Set Delay - R/W Address YF7. Every write to this register resets the transmit elastic frame count status register bit TXSBMSB. After a write, the delay through the slip buffer is less than 1 frame in duration. Each write operation will result in a disturbance of the transmit DS1 frame boundary, causing the far end to go out of sync.

Writing BC (hex) into register bits TXSD7-0 maximizes the wander tolerance before a controlled slip occurs. Under normal operation no slips should occur in the transmit path. Slips will only occur if the input CKb clock has excess wander, or the register bits TXSD7-0 are initialized to close to the slip pointers after system initialization.

6.1.2   T1 Receive Slip Buffer

The two frame receive elastic buffer is attached between the 1.544 Mb/s DS1 receive side and the 2.048 Mb/s ST-BUS side of the MT9071. Besides performing rate conversion, this elastic buffer is configured as a slip buffer which absorbs wander and low frequency jitter in multi-trunk applications. The received DS1 data is clocked into the slip buffer with the RxCK clock and is clocked out of the slip buffer with the system CKb clock. The RxCK extracted clock is generated from, and is therefore phase-locked with, the receive DS1 data.

In the case of Line Sync Mode (see Table 1 - E1 and T1 Timing Modes Summary), the CKb clock is phase locked to one of the four extracted RxCK clocks by an internal phase locked loop (PLL).   Therefore for this single trunk, the receive data is in phase with the RxCK clock, the CKb clock is phase locked to the RxCK clock, and the read and write positions of the slip buffer track each other.

In a multi-trunk slave or loop-timed system (i.e., PABX application) a single trunk will be chosen as a network synchronizer, which will function as described in the previous paragraph. The remaining trunks will use the system timing derived from the synchronizer to clock data out of their slip buffers. Even though the DS1 signals from the network are synchronous to each other, due to multiplexing, transmission impairments and route diversity, these signals may jitter or wander with respect to the synchronizing trunk signal. Therefore, the RxCK clocks of non-synchronized trunks may wander with respect to the RxCK clock of the synchronizer and the system bus. Network standards state that, within limits, trunk interfaces must be able to receive error-free data in the presence of jitter and wander (refer to network requirements for jitter and wander tolerance). The MT9071 will allow 92us (140 UI, DS1 unit intervals) of wander and low frequency jitter before a frame slip will occur.

When the CKb and the RxCK clocks are not phase-locked, the rate at which data is being written into the slip buffer from the DS1 side may differ from the rate at which it is being read out onto the ST-BUS. If this situation persists, the delay limits stated in the previous paragraph will be violated and the slip buffer will perform a controlled frame slip. That is, the buffer pointers will be automatically adjusted so that a full DS1 frame is either repeated or lost. All frame slips occur on frame boundaries.

The minimum delay through the receive slip buffer is approximately 1us and the maximum delay is approximately 249us (see Figure 12 - Read and Write Pointers in the T1 Receive Slip Buffers). Measuring clockwise from the write pointer, if the read page pointer comes within 8us of the write page pointer a frame slip will occur, which will put the read page pointer 157us from the write page pointer. Conversely, if the read page pointer moves more than 249us from the write page pointer, a slip will occur, which will put the read page pointer 124us from the write page pointer. This provides a worst case hysteresis of 92us peak = 142 U.I.
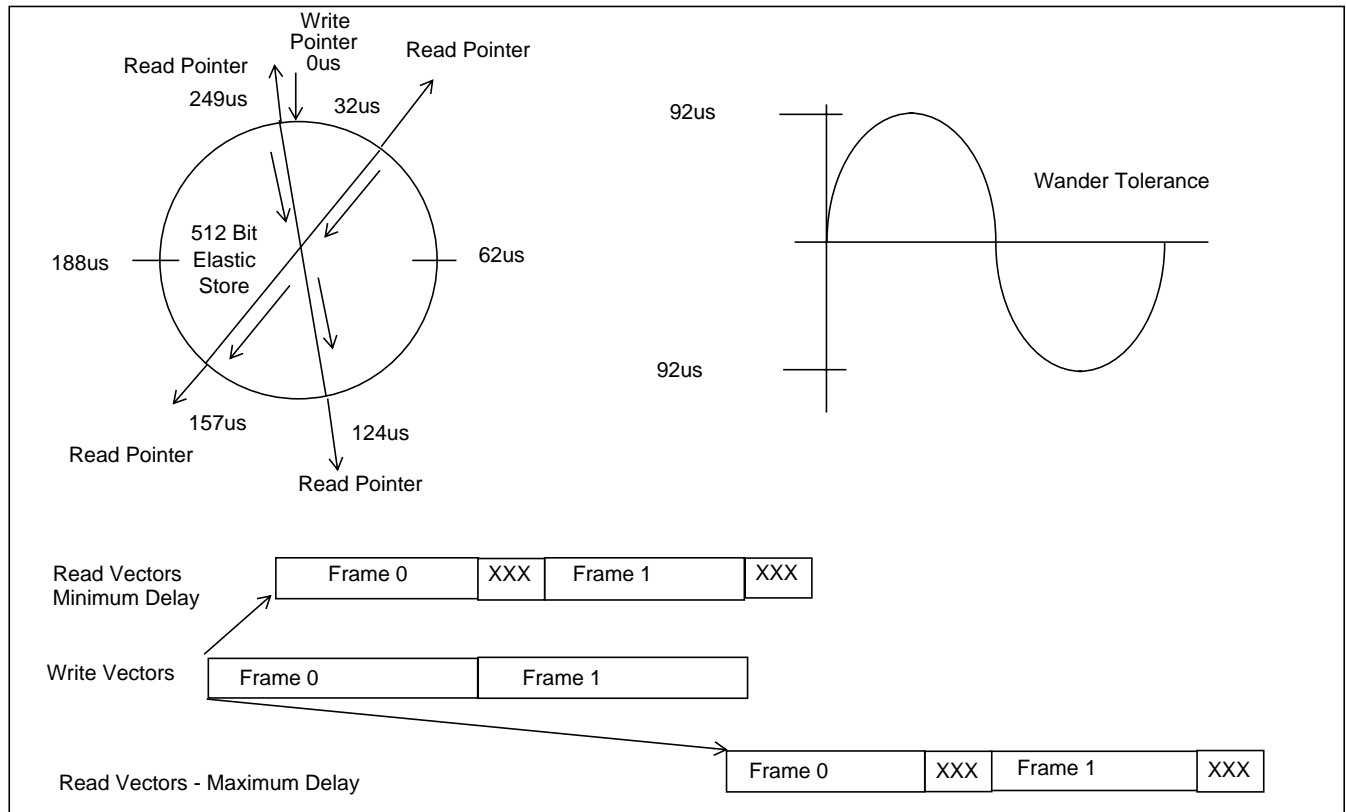
Figure 12 - Read and Write Pointers in the T1 Receive Slip Buffers

A slip will cause the following events to occur:

- The status register bit RSLP will toggle (see Table 110 - T1 Receive Elastic Buffer Status - R Address Y13).
- The latched status register bit RSLPL = 1 (see Table 136 - T1 Elastic Store Status Latch - R Address Y26).
- The interrupt status register bit RSLPI = 1 (see Table 153 - T1 Elastic Store Interrupt Status - R Address Y36), if unmasked with mask control register bit RSLPM = 0 (see Table 160 - T1 Elastic Store Interrupt Mask - R/W Address Y46).

The direction of the slip is indicated with status register bit RSLPD (see Table 110 - T1 Receive Elastic Buffer Status - R Address Y13). If RSLPD=0, the slip buffer has overflowed and a frame was lost; if RSLPD=1, an underflow condition occurred and a frame was repeated.

The relative phase delay between the system frame boundary and the receive elastic frame boundary is measured every second frame and reported in the status register bits RXTS4-0 and RXBC2-0 (see Table 110 - T1 Receive Elastic Buffer Status - R Address Y13).

6.1.3 T1 Receive Elastic Buffer Bypass

For applications which don't require the receive elastic buffer and require minimum delay, the receive elastic buffer may be bypassed by using the RxD pin output. This output contains all the PCM24 received data after

B8ZS decoding, but before passing through the elastic buffer. The output data is synchronous with the extracted clock (RxCK pin) output. Also synchronous with this output is the basic frame pulse provided at the $\overline{\text{RxBF}}$ pin output. This output can be used to identify the basic frame boundary of the RxD output data.

6.2   E1 Slip Buffer

In E1 mode, the MT9071 contains one slip buffer on the receive side which may perform a controlled slip.

6.2.1   E1 Receive Slip Buffer

In E1 mode, the MT9071 has a two frame receive elastic (or slip) buffer, which absorbs wander and low frequency jitter in multi-trunk applications. If desired, the elastic buffer can be bypassed (see Section 6.2.2 E1 Receive Slip Buffer Bypass). The received PCM30 data (RTIP and RRNG) is clocked into the elastic buffer with the extracted (RxCK pin) clock and is clocked out of the elastic buffer with the system (CKb pin) clock. The RxCK clock is generated from the receive PCM30 data, and is therefore phase-locked with that data. In ideal operation (no wander or jitter), the RxCK clock will be phase-locked to the CKb clock, the receive data will be in phase with the RxCK clock, and the read and write positions of the elastic buffer will remain fixed with respect to each other.

In a multi-trunk slave or loop-timed system (i.e., PABX application), a single trunk is chosen as a network synchronizer, where one RxCK clock is used as the reference source for the internal phase locked loop (PLL) which generates the system clock. In this case for the chosen single trunk, the elastic buffer will function as described in the previous paragraph.

The remaining trunks will use the system timing derived from the synchronizer to clock data out of their slip buffers. Even though the PCM30 signals from the network are synchronous to each other, due to multiplexing, transmission impairments and route diversity, these signals may jitter or wander with respect to the synchronizing trunk signal. Therefore, the RxCK clocks of non-synchronizer trunks may wander with respect to the RxCK clock of the synchronizer and the system bus.

Network standards state that, within limits, trunk interfaces must be able to receive error-free data in the presence of jitter and wander (refer to network requirements for jitter and wander tolerance). The MT9071 will allow +/- 26 channels (416 UI peak-to-peak) of wander and low frequency jitter before a frame slip will occur.

The minimum delay through the receive slip buffer is approximately 2 channels and the maximum delay is approximately 60 channels (see Figure 13 - Read and Write Pointers in the E1 Slip Buffers).

When the CKb and the RxCK clocks are not phase-locked, the rate at which data is being written into the slip buffer from the PCM30 side may differ from the rate at which it is being read out onto the ST-BUS. If this situation persists, the delay limits stated in the previous paragraph will be violated and the slip buffer will perform a controlled frame slip. That is, the buffer pointers will be automatically adjusted so that a full PCM30 frame is either repeated or lost. All frame slips occur on PCM30 frame boundaries.

A slip will cause the following events to occur:

- The status register bit RSLP will toggle (see Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10).
- The latched status register bit RSLPL = 1 (see Table 133 - E1 Sync Latched Status - R Address Y24).
- The interrupt status register bit RSLPI = 1 (see Table 150 - E1 Sync Interrupt Status - R Address Y34), if unmasked with mask control register bit RSLPM = 0 (see Table 157 - E1 Sync Interrupt Mask - R/W Address Y44).

The direction of the slip is indicated with status register bit RSLPD (see Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10). If RSLPD=0, the slip buffer has overflowed and a frame was lost; if RSLPD=1, an underflow condition occurred and a frame was repeated.

There is a specific relationship between the read and write pointers of the receive slip buffer (see Figure 13 - Read and Write Pointers in the E1 Slip Buffers). Measuring clockwise from the write pointer, if the read pointer comes within 2 channels of the write pointer a frame slip will occur, which will put the read pointer 34 channels from the write pointer. Conversely, if the read pointer moves more than 60 channels from the write pointer, a slip will occur, which will put the read pointer 28 channels from the write pointer. This provides a worst case hysteresis of 26 channels peak (52 channels peak-to-peak) or a wander tolerance of 416 UI peak-to-peak.
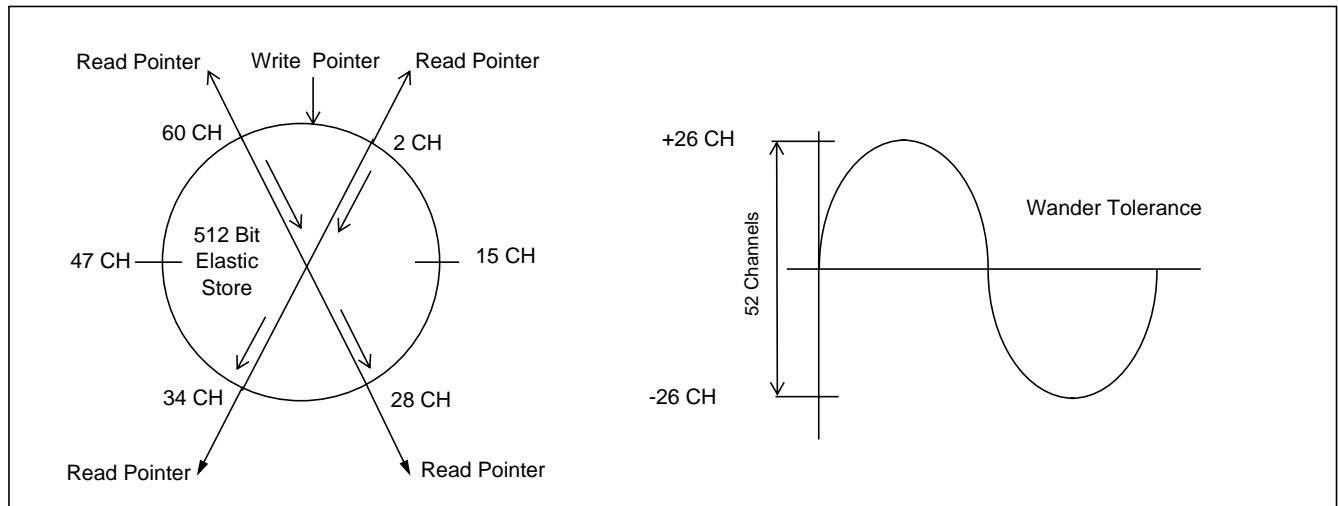
Figure 13 - Read and Write Pointers in the E1 Slip Buffers

6.2.2   E1 Receive Slip Buffer Bypass

For applications which don't require the elastic buffer and require minimum delay, the elastic buffer may be bypassed by using one of two methods. First, by setting the $\overline{\text{ELAS}}$ control register bit to one and using the DSTo output, or by using the RxD pin output (regardless of the $\overline{\text{ELAS}}$ setting). These outputs contain all the PCM30 received data after HDB3 decoding but before passing through the elastic buffer. The output data is synchronous with the extracted clock (RxCK pin) output. Also synchronous with the RxCK pin is the basic frame pulse provided at the $\overline{\text{RxBF}}$ pin output. This output can be used to identify the basic frame boundary of the RxD output data.

6.3   E1 Transmit Jitter Attenuator

In E1 mode, the MT9071 contains a jitter attenuator in the LIU transmitter portion of the device.

The MT9071 meets the E1 jitter transfer characteristics as specified by ETSI and ITU-T (see Figure 19 - ETSI Jitter Transfer and Figure 20 - ITU-T Jitter Transfer). Its intrinsic jitter is less than 0.02 UI.

The transmit jitter attenuator has data written to it from the system side 2.048 Mb/s stream. The data is clocked out of the buffer using a dejittered 16.384Mb/s clock (8 X 2.048Mb/s) from the internal PLL. The source signal to the PLL may be any one of the four extracted clocks (RxCK[3:0]), the external clock (ESYN), the backplane clock (CKb), the backplane frame pulse (FPb)or the master clock (OSCi). The transmit 2.048 MHz clock is always phase locked to one of these signals. The jitter attenuator is 128 bits deep allowing jitter and wander (128 U.I.) to occur between the PLL output signal and the system backplane (CKb).

Two internal elements determine the jitter attenuation. This includes the PLL's internal 1.9Hz low pass loop filter and the phase slope limiter. The phase slope limiter limits the output phase slope to 5ns/125us. Therefore, if the input signal exceeds this rate, such as for very large amplitude low frequency input jitter, the maximum output phase slope will be limited (i.e. attenuated) to 5ns/125us.

The jitter attenuator should only be necessary if timing is derived from the ST-BUS signals applied to the CKb and FPb pins and these signals contain jitter and wander in excess of the required amounts desired for transmission on the PCM30 link.

7.0 MT9071 Access and Control

7.1 Quad Transceiver Organization

The MT9071 contains 4 independent transceivers, referred to as transceiver 0 to transceiver 3. Each transceiver has its own unique pins and unique addressing. In 8.192Mb/s mode, transceivers 0 to 3 are grouped together on one ST-BUS stream. In addition, all 4 transceivers can be addressed together for write operations by enabling the upper most address bit (A11).

7.2 Processor Interface (A11-A0, D15-D0, I$\overline{M}$, $\overline{DS}$, R/$\overline{W}$, $\overline{CS}$, $\overline{IRQ}$, Pins)

The control and status of the MT9071 is achieved through a non-multiplexed parallel microprocessor port capable of accommodating 12 address bits and 16 data bits. The parallel port may be configured for Motorola style control signals (by setting pin I$\overline{M}$ low) or Intel style control signals (by setting pin I$\overline{M}$ high).

7.2.1 Transceiver and Register Access

The controlling microprocessor gains access to specific registers in the MT9071through a one step process.

The upper four address bits (A11-A8) access either a particular transceiver, a common write operation for all four transceivers, or a global register group.

The middle four address bits (A7-A4) access a particular register group (i.e. Control, Status, Interrupt Mask etc.).

The lower four address bits (A3-A0) access a particular register (i.e. CAS Control, Phase Status etc.).

See Table 11 - Tranceiver and Register Access.

Address		
A_{11},A_{10},A_9,A_8	A_7,A_6,A_5A_4	A_3,A_2,A_1,A_0
0 - Selects Transceiver 0 1 - Selects Transceiver 1 2 - Selects Transceiver 2 3 - Selects Transceiver 3 8 - Selects an all Tranceivers Write 9 - Selects a Global Register Group	Selects the register group (i.e. Control, Status, Interrupt Mask etc.)	Selects the particular register in the register group (i.e. CAS Control, Phase Status etc.)

Table 11 - Tranceiver and Register Access

For microprocessors with read/write cycles less than 165ns, a wait state is required. See Figure 35 - Motorola Microprocessor Read Timing, Figure 36 - Motorola Microprocessor Write Timing, Figure 37 - Intel Microprocessor Read Timing, and Figure 38 - Intel Microprocessor Write Timing for detailed timing requirements.

Through out this document, the upper four address bits (A11-A8) are referred to as Y, (where Y indicates any hex number between 0 and F). For detailed register descriptions, refer to the following sections:
- Section 19.0 T1 & E1 Transceiver Address Space
- Section 20.0 T1 & E1 Transceiver Registers Bit Summaries
- Section 21.0 T1 & E1 Transceiver Registers Bit Functions.

7.2.2 MT9071 Identification Code

The MT9071 includes a status register (Table 76 - T1 & E1 ID Rev Code Data - R Address 912) which contains an 8 bit identification code for the MT9071. This code identifies the product category, marketing revision and the transceiver type (E1 or T1). This byte allows user software to track device revisions, and device variances and provide system variations if necessary.

7.2.3 $\overline{\text{CS}}$ and $\overline{\text{IRQ}}$

The MT9071 includes a $\overline{\text{CS}}$ pin for applications where a single processor is controlling numerous peripherals, processor access can be disabled without affecting transceiver operation. Refer to the $\overline{\text{CS}}$ pin description for details.

An $\overline{\text{IRQ}}$ pin is provided with an extensive suite of maskable interrupts. Refer to the $\overline{\text{IRQ}}$ pin description and Section 18.0 T1 & E1 Interrupts.

7.3 ST-BUS Interface (DSTo, DSTo, CSTi, CSTo Pins)

The ST-BUS is used for PCM30 and DS0 data access only and does not carry any MT9071 control information. The ST-BUS can be used to access any timeslot. Typically, CCS and CAS is accessed through CSTi and CSTo, and payload data is accessed through DSTi and DSTo. Refer to the following sections:

Section 9.0 Common Channel Signaling (CCS) Operation
Section 10.0 CAS Operation
Section 11.0 Data Link Operation
Section 13.0 Transparent Mode Operation
Section 14.0 Payload Data Operation

7.3.1 ST-BUS 2.048Mb/s and 8.192Mb/s Mapping

The MT9071 provides both a 2.048Mb/s and a 8.192Mb/s backplane mode. In both modes, each of the four transceivers operate at 2.048Mb/s; but, in 8.192Mb/s mode, and overlay is provided which maps the four 2.048Mb/s transceivers to the 8.192Mb/s backplane (see Table 12 - ST-BUS 2.048Mb/s and 8.192Mb/s Timeslot Relationship).

T R A N C E I V E R		ST-BUS 2.048Mb/s CSTi/CSTo/CSTo/DSTo Timeslot																															
	0-3	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
		ST-BUS 8.192Mb/s CSTi/CSTo/CSTo/DSTo Timeslot																															
	0	0	4	8	12	16	20	24	28	32	36	40	44	48	52	56	60	64	68	72	76	80	84	88	92	96	100	104	108	112	116	120	124
	1	1	5	9	13	17	21	25	29	33	37	41	45	49	53	57	61	65	69	73	77	81	85	89	93	97	101	105	109	113	117	121	125
	2	2	6	10	14	18	22	26	30	34	38	42	46	50	54	58	62	66	70	74	78	82	86	90	94	98	102	106	110	114	118	122	126
	3	3	7	11	15	19	23	27	31	35	39	43	47	51	55	59	63	67	68	75	79	83	87	91	95	99	103	107	111	115	119	123	127

Table 12 - ST-BUS 2.048Mb/s and 8.192Mb/s Timeslot Relationship

7.4 Data Link Interface (RxD and RxCK Pins)

Dedicated Data Link pins are included which provide the user the option of bypassing the receive elastic buffer and accessing timeslot 0 Data Link data with an external controller. The MT9071 provides numerous additional methods for accessing the Data Link, refer to the Data Link sections for details.

7.5 CRC-4 and CAS Multiframe Boundary ($\overline{\text{TxMF}}$ Pins)

A dedicated multiframe boundary pin is included which provides the user the option of setting the multiframe boundaries with an external device. Refer to the $\overline{\text{TxMF}}$ pin description and to the CRC-4 and CAS sections for details.

7.6 Reset Operation ($\overline{\text{RESET}}$, $\overline{\text{TRST}}$ Pins)

On initial power up, a hard reset must be done using both the $\overline{\text{RESET}}$ pin and the $\overline{\text{TRST}}$ pin. A valid reset condition requires both of these inputs to be held low for a minimum of 100ns. These inputs should be set to zero during initial power up, then set to one.

After initial power up, the MT9071 can be reset using the hardware pin $\overline{\text{RESET}}$, or the control register bit RSTC (see Table 70 - T1 & E1 Global Mode Control - R/W Address 900). In addition, individual transceivers within the MT9071 may be reset with the control register bit RST (see Table 178 - T1 Interrupt and I/O Control - R/W Address YF1 and Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03). Note that the common control (global) registers can only be reset with $\overline{\text{RESET}}$ pin or the RSTC bit. When the device emerges from its reset state it will begin to function with default settings (see Table 13 - Reset Default Status). A reset operation takes 1 full frame (125 us) to complete.

Function	Status
Mode T1 or E1	T1
System Bus (Backplane)	2.048Mb/s
Counters	cleared
Counter Latches	cleared
Interrupts	all unmasked but suspended and cleared
Per Timeslot Control Buffer	All locations cleared
Loopbacks	deactivated
Error Insertion	deactivated
CAS ABCD Bit Debounce	deactivated
HDLC	deactivated

Table 13 - Reset Default Status

7.7 Control Pins

7.7.1 Transmit AIS Operation ($\overline{\text{TAIS}}$ Pin)

The $\overline{\text{TAIS}}$ pin allows all four transceivers of the MT9071 to transmit an all ones signal (AIS) at the TTIP and TRNG output pins from the point of power-up, without the need to write to any control registers. During this time the $\overline{\text{IRQ}}$ pin is in a high impedance state. After the interface has been initialized normal operation can take place by making $\overline{\text{TAIS}}$ high.

7.7.2 IEEE 1149.1-1990 Test Access Port (TAP)

Five signals (TDI, TDO, TMS, TCK & $\overline{\text{TRST}}$) make up the Test Access Port (TAP) of the IEEE 1149.1-1990 Standard Test Port and Boundary-Scan Architecture. The TAP provides access to test support functions built into the MT9071. The TAP is also referred to as a JTAG (Joint Test Action Group) port, see Section 8.0 JTAG Operation.

8.0   JTAG Operation

The MT9071 JTAG (Joint Test Action Group) interface conforms to the Boundary-Scan standard IEEE1149.1-1990. This standard specifies a design-for-testability technique called Boundary-Scan test (BST). The BST architecture is made up of four basic elements, see Figure 14 - Boundary Scan Test Circuit Block Diagram.

1. Test Access Port (TAP)
2. TAP Controller
3. Instruction Register (IR)
4. Test Data Registers (TDR)
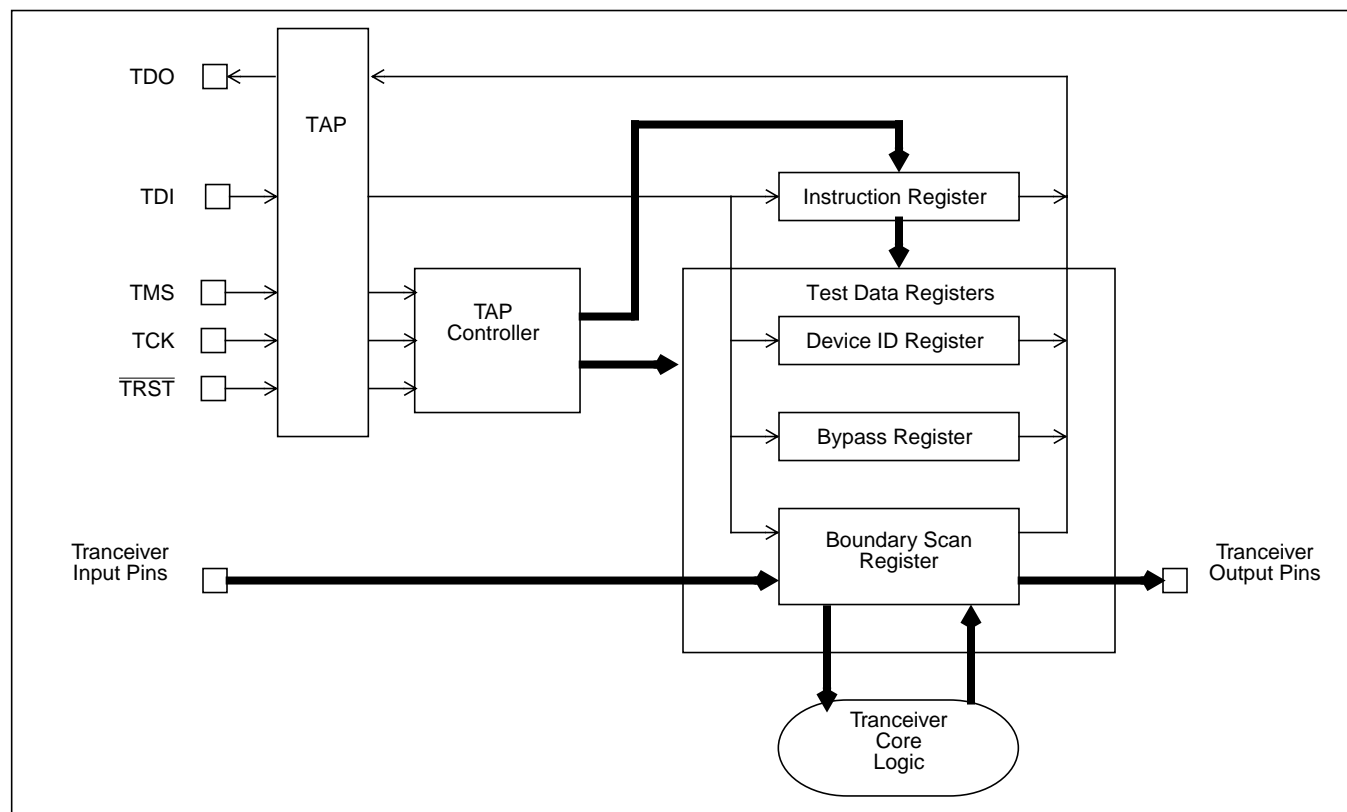
Figure 14 - Boundary Scan Test Circuit Block Diagram

8.1   Test Access Port (TAP)

The Test Access Port (TAP) provides access to the many test functions of the MT9071. It consists of four input pins and one output pin. The following pins are from the TAP.

Test Clock Input (TCK) - TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clocks and thus remains independent. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic. This pin is internally pulled up to device V_{DD}.

Test Mode Select Input (TMS) - The logic signals received at the TMS input are interpreted by the TAP Controller to control the test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled up to device V_{DD}.

Test Data Input (TDI) - Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled up to device V_{DD}.

Test Data Output (TDO) - Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out towards the TDO. The data out of the TDO is clocked on the falling edge of the TCK pulses. When no data is shifted through the boundary scan cells, the TDO driver is set to a high impedance state.

Test Reset ($\overline{TRST}$) - Reset the JTAG scan structure.This pin is internally pulled up to device V_{DD}.

8.2   Test Access Port (TAP) Controller

The TAP Controller generates clock and control signals for the Instruction Register (IR) and the Test Data Registers (TDR's). The TAP Controller operates synchronously with TCK input clock and responds to the TMS input signal to generate control signals which shift, capture, or update data through either the IR or the TDR's.

8.3   Instruction Register

The Instruction Register (IR) is a 3-bit register which allows one of four test instructions to be shifted into the device. Test instructions are serially loaded into the IR from the TDI pin by the TAP Controller (see Table 14 - JTAG Instruction Register). These test instructions provided by the MT9071 are in accordance with the IEEE 1149.1 standard.

MSB		LSB	Instruction Name	Functional Description
0	0	0	EXTEST	This instruction isolates the tranceiver logic (on chip logic) from the input and output pins. The signal states at the output pins is determined by the values programmed (earlier) in the Boundary Scan Register. This instruction allows testing of board level interconnects (i.e. open, stuck at, bridge).
0	1	0	SAMPLE/ PRELOAD	This instruction performs two functions. On the rising edge of TCK, the SAMPLE instruction is performed. With this instruction, the signal states at the input and output pins is loaded into the Boundary Scan Register. On the falling edge of TCK, the PRELOAD instruction is performed. With this instruction, the signal states at the output pins is determined by the values programmed (earlier) in the Boundary Scan Register.
0	0	1	IDCODE	This instruction forces the value of the 32 bit MT9071 Identification Register into the Instruction Registers parallel output latches. This is the default instruction loaded after a JTAG reset.
1	1	1	BYPASS	This instruction connects the Bypass Register between the TDI and TDO pins.
Note 1. The following optional JTAG instructions are not supported, INTEST, RUNBIST and USERCODE.				

Table 14 - JTAG Instruction Register

8.4   Test Data Registers

As specified in IEEE 1149.1, the JTAG Interface must contain as a minimum the boundary scan register and the bypass register. The device identification register although optional, is also included in the MT9071.

8.4.1   Identification Register

This is a 32 bit register (see Table 15 - JTAG MT9071 Identification Register). Note that the marketing revision is not the same as the silicon revision which is not supplied.

Version	Part Number	Manufacturer Identity	LSB=1
Marketing Revision	Marketing Number	Mitel	LSB
(4 bits)	(16 bits)	(11 bits)	(1 bit)
A	9071	Mitel	LSB=1
0000	1001 0000 0111 0001	0001 0100 101	1
0	9 0 7 1	1 4 B	
0 9 0 7 1 1 4 B			

Table 15 - JTAG MT9071 Identification Register

8.4.2   The Bypass Register

The Bypass Register is a single stage shift register that provides a one-bit path from TDI to its TDO.

8.4.3   The Boundary-Scan Register

The Boundary-Scan Register (BSR) provides an interface between the MT9071 core logic and the MT9071 input and output pins. This interface is controlled by the TAP Controller and Instruction Register. The BSR provides status of all digital input, output and bi-directional pins and control over all digital output and bi-directional pins. Power pins, analog pins, oscillator pins and test pins are not included in the chain. The BSR maps to the remaining pins. Each input pin maps to one BSR bit (input cell), each output pin maps to one or two BSR bits (output and enable cells), and each bi-directional pin maps to three BSR bits (input, output and enable cells). Bit 0 of the BSR is the last bit in the JTAG chain and the first bit clocked out. The JTAG chain starts at DSTo[0] and moves counterclockwise around the chip finishing at the $\overline{\text{RXBF}}$[3] pin (see Table 16 - JTAG Boundary-Scan Register).

Device Pin			Boundary-Scan Register Bits (0 to 117)		
Name	Type	Cell #	Enable Register Bit	Output Register Bit	Input Register Bit
			When this control/status bit is one, the corresponding pin is in a high impedance state. When zero, the corresponding pin operates normally.	When this control/status bit is one, the corresponding pin is high. When zero, the corresponding pin is low.	When this status bit is one, the corresponding pin is high. When zero, the corresponding pin is low.
DSTo[0]	output	1	0	1	NA
The sequence continues around the chip. Refer to the BSDL file for BSR bit mapping.					
$\overline{\text{RXBF}}$[3]	output	72	NA	117	NA

Table 16 - JTAG Boundary-Scan Register

8.5   Boundary Scan Description Language (BSDL) File

A Boundary Scan Description Language (BSDL) file is available for the MT9071 JTAG implementation. This ASCII (text) file provides all the information required for a JTAG test system to access the MT9071's boundary scan circuitry.

9.0   Common Channel Signaling (CCS) Operation

In CCS, an E1 PCM30 timeslot or a T1 DS0 channel is typically used to carry signaling information for all channels in a framed and formatted data packet according to some high level data link control method. One such method is the Link Access Procedure on the D-Channel (LAPD) ISDN protocol specified by CCITT. Other protocols include non-ISDN protocols such as the High Level Data Link Control (HDLC) and the LAPB

protocol that is specified in CCITT recommendation X.25. Differences between these protocols is limited to procedural functions handled by the high level data link controller, and consequently, protocols are not limited by the physical layer hardware (i.e. MT9071). Therefore, if required, the high level data link controller must be provided for with external components, the MT9071 does not provide high level data link control for CCS (only for data link). However, the MT9071 does provide a very convenient interface to numerous high level data link control devices such as the Siemens PEB 20320 Multichannel Network Interface Controller for HDLC (MUNICH32).

Access to the CCS PCM channel transmit and receive bytes may be either through ST-BUS channels at the CSTi and CSTo pins, or through the ST-BUS channels at the DSTi and DSTo pins. If the DST pins are used, the mapping of PCM channel to ST-BUS channel is fixed (see Table 28 - T1 DS1 & ST-BUS DSTi/DSTo Timeslot Relationship and Table 29 - E1 PCM30 & ST-BUS DSTi/DSTo Timeslot Relationship). If the CST pins are used, then mapping of PCM channel to ST-BUS channel is programmable. Regardless of which method is used (DSTi or CSTi), data will always be output at DSTo. The CST method is convenient in most applications when used with a multichannel HDLC (or LAPD) type of controller.

9.1   T1 CCS & ST-BUS CSTi/CSTo

In T1 CCS, a single DS1 channel is used to carry signaling information for all 23 payload channels in a framed and formatted data packet according to some high level data link control method as described above. Typically channel 24 is used for this purpose, however, Bellcore GR-303 specifies that any one channel may be required for CCS. The MT9071 accommodates these requirements.

T1 CCS mode is enabled with control register bit CSIGEN (see Table 86 - T1 Signalling Control - R/W Address Y04). Any one DS1 channel can be transparently mapped to any one CSTi/CSTo timeslot (0 to 23 only) with control register bits PCM4-0 and CST4-0 (see Table 100 - T1 CCS Map Control - R/W Address Y0B). All unselected CSTo timeslots are high impedance. Consequently, it is possible to connect up to 32 transceiver CSTi/CSTo streams together, to accommodate a single common channel signaling resource such as a 32 channel HDLC controller.

9.1.1   T1 CCS & ST-BUS CSTi/CSTo Timeslot Relationship

See Table 17 - T1 DS1 & ST-BUS CSTi/CSTo Timeslot Relationship.

DS1 Timeslot or Channel																															
Any one channel of 1-24																															
ST-BUS 2.048Mb/s CSTi/CSTo Timeslot																															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	-	-	-	-	-	-	-	-

Table 17 - T1 DS1 & ST-BUS CSTi/CSTo Timeslot Relationship

9.2   E1 CCS

In E1 CCS, up to three PCM30 timeslots are used to carry signaling information for all 30 payload channels in a framed and formatted data packet according to some high level data link control method as described above. Typically, timeslot 16 is used for this purpose, however, ETS 300 347-1 V5.2 specifies that timeslots 15, 16 and 31 may be required for CCS. The MT9071 accommodates these requirements.

E1 CCS mode is enabled with control register bit CSIG (see Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03). Up to three PCM30 timeslots can be transparently mapped to any three CSTi/CSTo timeslots. The three PCM30 timeslots are mapped with control register bits TS31E, TS16E and TS15E (see Table 91 - E1 HDLC and CCS ST-BUS Control - R/W Address Y06). The three CSTi/CSTo timeslots are mapped with control register bits 31C4-0, 16C4-0 and 15C4-0 (see Table 93 - E1 CCS CSTi and CSTo Map Control - R/W Address Y07). All unsettled CSTo timeslots are high impedance. Consequently, it is possible to

connect up to 32 transceiver CSTi/CSTo streams together, to accommodate a single common channel signaling resource such as a 32 channel HDLC controller.

9.2.1   T1 CCS & ST-BUS CSTi/CSTo Timeslot Relationship

See Table 18 - E1 PCM30 & ST-BUS CSTi/CSTo Timeslot Relationship.

PCM30 Timeslot																															
Any one, two or three timeslots of 15, 16 & 31																															
ST-BUS 2.048Mb/s CSTi/CSTo Timeslot																															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

Table 18 - E1 PCM30 & ST-BUS CSTi/CSTo Timeslot Relationship

10.0   CAS Operation

10.1 T1 CAS

Channel Associated Signaling (CAS) is also referred to as robbed bit signaling. The purpose of CAS is to provide a scheme that will allow the association of a specific ABCD (or AB) signaling nibble with the appropriate DS0 channel. The AB signaling bits from frames 6 and 12, or the ABCD signaling bits from frames 6, 12, 18 and 24 are mapped to storage rams and to the serial ST-BUS data stream.

10.1.1   T1 CAS Register and ST-BUS Access

For CAS operation, the robbed bit enable control register bit RBEN (see Table 86 - T1 Signalling Control - R/W Address Y04) must be set to one. In addition, CAS operation must be enabled on a per channel basis by setting the clear channel per timeslot control register bit CC (see Table 166 - T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7) to zero.

Access to the ABCD transmit and receive bits may be either through ST-BUS channels 1 to 24 at the CSTi and CSTo pins, or through transmit data registers (see Table 162 - T1 Transmit CAS Data Registers - R/W Address Y50-Y67) and receive data registers (see Table 164 - T1 Receive CAS Data Registers - R Address Y70-Y87) accessed by the parallel processor port, or through a mix of both methods.

The timeslot control register bits MPST(0-23) (see Table 166 - T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7) determine the source of the CAS data on a per channel basis. If zero, the transmit signaling information is constantly updated with the information from the equivalent channel on CSTi, if one, the transmit CAS data register are the source. Note that when changing the MPST(0-23) control register bits from ST-BUS source to register source on the fly (during normal operation as opposed to during power up), the transmit CAS data registers are updated one frame after the timeslot control register bits MPST(0-23) are changed. This is because the timeslot control register bits do not take effect immediately. Both destinations of CAS data are always enabled (i.e. ST-BUS CSTo and receive CAS data registers). The receive signaling bits are always mapped to the equivalent ST-BUS channels on CSTo (see Table 19 - T1 CAS & ST-BUS CSTi/CSTo Timeslot Relationship).

DS1 Timeslot or Channel																															
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	NA							
ST-BUS 2.048Mb/s CSTi/CSTo Timeslot																															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	z	z	z	z	z	z	z	z

Table 19 - T1 CAS & ST-BUS CSTi/CSTo Timeslot Relationship

The lower nibble of a CSTi/CSTo timeslot is used for the four signaling bits, the upper nibble on the CSTo timeslots is not used and is either high or low. All unused CSTo timeslots are high impedance. In order to facilitate multiplexing on the CSTo control streams, control register bit CSToEn (Table 178 - T1 Interrupt and I/O Control - R/W Address YF1) will place the whole stream in a high impedance state when set low.

In the case of D4 trunks, only AB bits are reported. The control register bits SM1-0 (Table 86 - T1 Signalling Control - R/W Address Y04) allow the user to program the 2 unused bits (CD) reported on CSTo.

A receive signaling bit debounce of 6ms can be selected with control register bit RSDB (Table 86 - T1 Signalling Control - R/W Address Y04). It should be noted that there may be as much as 3ms added to this duration because signaling equipment state changes are not synchronous with the D4 or ESF multiframe.

If multiframe synchronization is lost, as indicated by status register bit $\overline{\text{MFSYNC}}$ =1 (Table 104 - T1 Synchronization and Alarm Status - R Address Y10), then the CAS bits will be frozen (i.e. will retain their previous value and will not be updated). The CAS bits are unfrozen when multiframe synchronization is acquired (this is the same as terminal frame synchronization for ESF links).

CAS signaling freeze due to receiver slip is also available by setting control register bit RFS =1 (Table 86 - T1 Signalling Control - R/W Address Y04).

A CAS state change on any of the 24 receive channels will cause the following events to occur:

- The latched status register bit CASRL = 1 (see Table 134 - T1 Receive Line Status and Timer Latch - R Address Y25).
- The interrupt status register bit CASRI = 1 (see Table 151 - T1 Receive Line and Timer Interrupt Status - R Address Y35), if unmasked with mask control register bit CASRM = 0 (see Table 158 - T1 Receive Line and Timer Interrupt Mask - R/W Address Y45).

When the CASRI interrupt is unmasked, $\overline{\text{IRQ}}$ will become active when a signaling state change is detected in any of the 24 receive channels and the selectable 1/4/8/16 msec timer (see control bits SIP1,0 detailed Table 86 - T1 Signalling Control - R/W Address Y04) has expired. This function helps to reduce the frequency of interrupts generated due to signaling changes. For instance if 7 channels had a signaling change, only one interrupt will be generated in a 1/4/8/16 msec duration. Upon an interrupt, the user has to read the CAS registers (Table 164 - T1 Receive CAS Data Registers - R Address Y70-Y87) to determine the channels with a signaling change. Any channels marked as clear channels will not generate an interrupt due to changes in ABCD bits.

10.2 E1 CAS

The purpose of the CAS Multiframing algorithm is to provide a scheme that will allow the association of a specific ABCD signaling nibble with the appropriate PCM30 channel. A CAS multiframe consists of 16 basic frames (numbered 0 to 15), which results in a multiframe repetition rate of 2ms. It should be noted that the boundaries of the signaling multiframe may be completely distinct from those of the CRC-4 multiframe. CAS multiframe alignment is based on a multiframe alignment signal (a 0000 bit sequence), which occurs in the most significant nibble of timeslot 16 of basic frame 0 of the CAS multiframe. Bits 5, 7 and 8 (usually designated X) are spare bits and are normally set to one if not used. Bit 6 of this timeslot is the multiframe alarm bit (usually designated Y). When CAS multiframing is acquired on the receive side, the transmit Y-bit is zero; when CAS multiframing is not acquired, the transmit Y-bit is one. Refer to ITU-T G.704 and G.732 for more details on CAS multiframing requirements.

Timeslot 16 of the remaining 15 basic frames of the CAS multiframe (i.e., basic frames 1 to 15) are reserved for the ABCD signaling bits for the 30 payload channels. The most significant nibbles are reserved for channels 1 to 15 and the least significant nibbles are reserved for channels 16 to 30. That is, timeslot 16 of basic frame 1 has ABCD for channel 1 and 16, timeslot 16 of basic frame 2 has ABCD for channel 2 and 17, through to timeslot 16 of basic frame 15 has ABCD for channel 15 and 30. See Table 20 - E1 CAS Multiframe Structure.

	CAS Frame	**PCM30 Timeslot 16**							
		1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Channel Associated Signaling (CAS) Multiframe (not related to CRC-4 multiframing)	0	0000 (MAS)				XYXX (NMAS)			
	1	ABCD (ch 1 = ts1)				ABCD (ch 16 = ts 17)			
	2	ABCD (ch 2 = ts 2)				ABCD (ch 17 = ts 18)			
	3	ABCD (ch 3 = ts 3)				ABCD (ch 18 = ts 19)			
	4	ABCD (ch 4 = ts 4)				ABCD (ch 19 = ts 20)			
	5	ABCD (ch 5 = ts 5)				ABCD (ch 20 = ts 21)			
	6	ABCD (ch 6 = ts 6)				ABCD (ch 21 = ts 22)			
	7	ABCD (ch 7 = ts 7)				ABCD (ch 22 = ts 23)			
	8	ABCD (ch 8 = ts 8)				ABCD (ch 23 = ts 24)			
	9	ABCD (ch 9 = ts 9)				ABCD (ch 24 = ts 25)			
	10	ABCD (ch 10 = ts 10)				ABCD (ch 25 = ts 26)			
	11	ABCD (ch 11 = ts 11)				ABCD (ch 26 = ts 27)			
	12	ABCD (ch 12 = ts 12)				ABCD (ch 27 = ts 28)			
	13	ABCD (ch 13 = ts 13)				ABCD (ch 28 = ts 29)			
	14	ABCD (ch 14 = ts 14)				ABCD (ch 29 = ts 30)			
	15	ABCD (ch 15 = ts 15)				ABCD (ch 30 = ts 31)			

Table 20 - E1 CAS Multiframe Structure

MAS - Multiframe Alignment Signal
NMAS - Non-Multiframe Alignment Signal
X - Spare Bit = 1 if not used
Y - Remote Multiframe Alarm Signal

10.2.1 E1 CAS Register and ST-BUS Access

For CAS operation, the signaling bit enable control register bit CSIG (see Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) must be set to zero.

Access to the ABCD transmit and receive bits may be either through ST-BUS channels 1 to 15 and channels 17 to 31 at the CSTi and CSTo pins, or through transmit data registers (see Table 163 - E1 Transmit CAS Data Registers - R/W Address Y51-Y5F & Y61-Y6F) and receive data registers (see Table 165 - E1 Receive CAS Data Registers - R Address Y71-Y7F, Y81-Y8F) accessed by the parallel processor port, or through a mix of both methods.

The timeslot control register bits CASS(1-15,17-31) (see Table 167 - E1 Per Timeslot 0 to 31 Control Registers - R/W Address Y90-YAF) determine the source of the CAS data on a per channel basis. If zero, the transmit signaling information is constantly updated with the information from the equivalent channel on CSTi, if one, the transmit CAS data register is the source. Note that when changing the CASS(1-15,17-31) timeslot control register bits from ST-BUS source to register source on the fly (during normal operation as opposed to during power up), the transmit CAS data registers are updated one frame after the timeslot control register bits are changed. This is because the timeslot control register bits do not take effect immediately. Both destinations of CAS data are always enabled (i.e. ST-BUS CSTo and receive CAS data registers). The receive signaling bits are always mapped to the equivalent ST-BUS channels on CSTo (see Table 21 - E1 CAS & ST-BUS CSTi/CSTo Timeslot Relationship).

PCM30 Channel																															
-	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	-	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
ST-BUS 2.048Mb/s CSTi/CSTo Timeslot																															
z	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	z	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

Table 21 - E1 CAS & ST-BUS CSTi/CSTo Timeslot Relationship

The lower nibble of a CSTi/CSTo timeslot is used for the four signaling bits, the upper nibble on the CSTo timeslots is not used and is either high or low. All unused CSTo timeslots are high impedance. In order to facilitate multiplexing on the CSTo control streams, control register bit CSToE (Table 83 - E1 Interrupts and I/O Control - R/W Address Y02) will place the whole stream in a high impedance state when set low.

A receive signaling bit debounce of 14ms can be selected with control register bit DBNCE (Table 89 - E1 CAS Control and Data - R/W Address Y05). It should be noted that there may be as much as 2ms added to this duration because signaling equipment state changes are not synchronous with the multiframe.

If multiframe synchronization is lost, as indicated by status register bit $\overline{MSYNC}$ =1 (Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10), then the CAS bits will be frozen (i.e. will retain their previous value and will not be updated). The CAS bits are unfrozen when multiframe synchronization is acquired.

A CAS state change on any of the 30 receive channels will cause the following events to occur:

- The latched status register bit CASRL = 1 (see Table 135 - E1 Counter Latched Status - R Address Y25).
- The interrupt status register bit CASRI = 1 (see Table 152 - E1 Counter Interrupt Status - R Address Y35), if unmasked with mask control register bit CASRM = 0 (see Table 159 - E1 Counter Interrupt Mask - R/W Address Y45).

When the CASRI interrupt is unmasked, $\overline{IRQ}$ will become active when a signaling state change is detected in any of the 30 receive channels and the selectable 1/4/8/16 msec timer (see control bits SIP1,0 detailed Table 87 - E1 Signalling Control - R/W Address Y04) has expired. This function helps to reduce the frequency of interrupts generated due to signaling changes. For instance if 7 channels had a signaling change, only one interrupt will be generated in a 1/4/8/16 msec duration. Upon an interrupt, the user has to read the CAS registers (Table 165 - E1 Receive CAS Data Registers - R Address Y71-Y7F, Y81-Y8F) to determine the channels with a signaling change. Any channels marked as clear channels will not generate an interrupt due to changes in ABCD bits.

Both destinations of CAS data are always enabled (i.e. ST-BUS CSTo and receive data registers). ST-BUS CSTi and CSTo channels 0 and 16 are not used.

11.0   Data Link Operation

11.1 T1 Data Link Operation

The ESF protocol allows for carrier messages to be embedded in the overhead bit (S-bit) position. Refer to the FDL bit detailed in Table 7 - T1 ESF Superframe Structure. The MT9071 provides two separate means of accessing these data links.

*   With dedicated data registers for transmitting and receiving Bit-Oriented Messages.
*   With an internal HDLC operating at a bit rate of 4 kbits/sec.

11.1.1   T1 Bit-Oriented Messaging

For the structure of the Bit-Oriented Messages, refer to Table 22 - T1 Message Oriented Performance Report Structure (T1.403 and T1.408) and Table 23 - Bit Oriented Messages. Bit oriented messages may be periodically interrupted (up to once per second) for a duration of up to 100 milliseconds. This is to accommodate bursts of message oriented protocols.

In T1 mode, bit oriented messaging may be selected by setting control register bit BOMEN (Table 90 - T1 HDLC & DataLink Control - R/W Address Y06). The transmit data link will contain the repeating serial data stream of the form 1111 1111 0xxx xxx0, where the 0xxx xxx0 byte originates from the transmit data register bits TXBOM7-0 (Table 92 - T1 Transmit BOM Data - R/W Address Y07).

The receive data link will also contain a repeating serial data stream of the form 1111 1111 0xxx xxx0, where the 0xxx xxx0 byte is sourced to the receive data register bits RXBOM7-0 (Table 108 - T1 Receive Bit Oriented Message - R Address Y12). To prevent spurious inputs from creating false messages, a new message must be repeated in at least 8 of the last 10 appropriate byte positions before being loaded into the receive data register bits RXBOM7-0. When a new message has been received, and if RXBOM7-0 changes state, the following events will occur:

*   The latched status register bit BOML = 1 (Table 134 - T1 Receive Line Status and Timer Latch - R Address Y25).
*   The interrupt status register bit BOMI = 1 (Table 151 - T1 Receive Line and Timer Interrupt Status - R Address Y35), if unmasked with mask control register bit BOMM = 0 (Table 158 - T1 Receive Line and Timer Interrupt Mask - R/W Address Y45).

A bit oriented match register is also available. The control register bits RXBOMM7-0 (Table 94 - T1 Receive BOM Match Control - R/W Address Y08) are internally compared with the receive data register bits RXBOM7-0. When a new message has been received, and if RXBOM7-0 changes state and matches RXBOMM7-0, the following events will occur:

*   The latched status register bit BOMML = 1 (Table 134 - T1 Receive Line Status and Timer Latch - R Address Y25).
*   The interrupt status register bit BOMMI = 1 (Table 151 - T1 Receive Line and Timer Interrupt Status - R Address Y35), if unmasked with mask control register bit BOMMM = 0 (Table 158 - T1 Receive Line and Timer Interrupt Mask - R/W Address Y45).

Octet #	8	7	6	5	4	3	2	1	Content
1	F	L	A	G					01111110
2	S	A	P	I		C / R		EA	00111000 or 00111010
3	T	E	I					EA	00000001
4	C	O	N	T	R	O	L		00000011
5	G3	LV	G4	U1	U2	G5	SL	G6	to
6	FE	SE	LB	G1	R	G2	Nm	NI	to
7	G3	LV	G4	U1	U2	G5	SL	G6	to-1
8	FE	SE	LB	G1	R	G2	Nm	NI	to-1
9	G3	LV	G4	U1	U2	G5	SL	G6	to-2
10	FE	SE	LB	G1	R	G2	Nm	NI	to-2
11	G3	LV	G4	U1	U2	G5	SL	G6	to-3
12	FE	SE	LB	G1	R	G2	Nm	NI	to-3
13				F	C	S			VARIABLE
14									

Table 22 - T1 Message Oriented Performance Report Structure (T1.403 and T1.408)

Address	Interpretation
00111000 00111010 00000001	SAPI = 14, C/R = 0 (CI) EA = 0 SAPI = 14, C/R = 1(Carrier) EA = 0 TEI = 0, EA =1
Control	**Interpretation**
00000011	Unacknowledged Information Transfer
One Second Report	**Interpretation**
G1 = 1 G2 = 1 G3 = 1 G4 = 1 G5 = 1 G6 = 1 SE = 1 FE = 1 LV = 1 SL = 1 LB = 1 U1,U2 = 0 R = 0 NmNI = 00, 01, 10, 11	CRC Error Event = 1 1 < CRC Error Event < 5 5 < CRC Error Event < 10 10 < CRC Error Event < 100 100 < CRC Error Event < 319 CRC Error Event > 320 Severely - Errored Framing Event >= 1 Frame Synchronization Bit Error Event >= 1 Line code Violation Event >= 1 Slip Event >= 1 Payload Loopback Activated Under Study for sync. Reserved - set to 0 One Second Module 4 counter
FCS	**Interpretation**
VARIABLE	CRC16 Frame Check Sequence

Table 23 - Bit Oriented Messages

11.1.2 T1 HDLC

The data link may be connected to the internal HDLC, see Section 12.0 HDLC.

11.2 E1 Data Link Operation

The PCM30 frame structure allows for the transport of maintenance and performance monitoring information across the PCM30 link. The contents of the transmit and receive Frame Alignment Signals (FAS) and Non-frame Alignment Signals (NFAS) of timeslot zero of a PCM30 signal are shown in Table 8 - E1 CRC-4 FAS and NFAS Structure. Even numbered frames (CRC Frame # 0, 2, 4,...) are FASs and odd numbered frames (CRC Frame # 1, 3, 5,...) are NFASs. The bits of each channel are numbered 1 to 8, with bit 1 being the most significant and bit 8 the least significant. The data link bits, also referred to as National bits, are the Sa4, Sa5, Sa6, Sa7 and Sa8 bits of the PCM30 timeslot zero NFAS frames. Any number and combination of these bits may be used for the data link. The MT9071 provides five separate means of accessing these data links.

Transmit and Receive 5 byte data register bits TNnFm and RNnFm. See Table 168 - E1 Transmit National Bits Sa4 - Sa8 Data Registers - R/W Address YB0-YB4 and Table 169 - E1 Receive National Bit Sa4 - Sa8 Data Registers - R Address YC0-YC4.

Receive only RXD pin.

Transmit and Receive ST-BUS (DSTi/DSTo timeslot 0).

Transmit and Receive internal HDLC operating at a bit rate of 4 kbits/sec (for any one Sa bit). See Table 182 T1 & E1 HDLC Transmit FIFO Data - R/W Address YF5.

Receive only 5 bit data register bits RNU4-8. See Table 111 E1 NFAS Signal and FAS Status - R Address Y13.

In all cases, the data link access method is controlled with the SA control register bits detailed in Table 95 - E1 Data Link Control - R/W Address Y08.

Note that the user can source different Sa bits from a combination of the above methods. For instance the Sa_4 bit could be sourced from transmit 5 byte data register bits TN4Fm, the Sa_5 bit could be sourced from the transmit ST-BUS DSTi timeslot 0 and the Sa_6 bit could be sourced from the transmit HDLC.

Also note that the receive Sa bits are always sourced to the above five locations.

In order to facilitate conformance to ETS 300 233, numerous maskable interrupts are available for change of state of Sa bits in the receiver, these bits are detailed in Table 154 - E1 National Interrupt Status - R Address Y36.

11.2.1 E1 Data Link National Bit Buffer Access

When the National Bit Buffer transmit data registers access is enabled, the setting of 40 data bits in 5 registers (Table 168 - E1 Transmit National Bits Sa4 - Sa8 Data Registers - R/W Address YB0-YB4) determine the data link output on the PCM30 link corresponding to bit positions Sa4-8 over one complete CRC-4 Multiframe. The CRC-4 alignment status register bit CALN (Table 107 - E1 CRC-4 Timers & CRC-4 Local Status - R Address Y11) and corresponding maskable interrupt status register bit CALNI (Table 154 - E1 National Interrupt Status - R Address Y36) indicate the beginning of every received CRC-4 multiframe. Data for data link transmission should be written to the National Bit Buffer transmit data registers immediately following the CALN status indication (during basic frame 0) and before the start of basic frame 1.

Table 24 - E1 National Bit Buffers illustrates the organization of the MT9071 transmit and receive national bit buffers. Each row is an addressable byte of the MT9071 national bit buffer, and each column contains the national bits of an odd numbered frame of each CRC-4 Multiframe.

Addressable Bytes				NFAS Frames of a CRC-4 Multiframe							
Transmit	Address	Receive	Address	F1 B7	F3 B6	F5 B5	F7 B4	F9 B3	F11 B2	F13 B1	F15 B0
TN0	YB0	RN0	YC0	S_{a4}	S_{a4}	S_{a4}	S_{a4}	S_{a4}	S_{a4}	S_{a4}	S_{a4}
TN1	YB1	RN1	YC1	S_{a5}	S_{a5}	S_{a5}	S_{a5}	S_{a5}	S_{a5}	S_{a5}	S_{a5}
TN2	YB2	RN2	YC2	S_{a6}	S_{a6}	S_{a6}	S_{a6}	S_{a6}	S_{a6}	S_{a6}	S_{a6}
TN3	YB3	RN3	YC3	S_{a7}	S_{a7}	S_{a7}	S_{a7}	S_{a7}	S_{a7}	S_{a7}	S_{a7}
TN4	YB4	RN4	YC4	S_{a8}	S_{a8}	S_{a8}	S_{a8}	S_{a8}	S_{a8}	S_{a8}	S_{a8}

Table 24 - E1 National Bit Buffers

11.2.2 Data Link Pin Data (RxD) Received from PCM30 - With No Elastic Buffer

The RxD signal is aligned with the receive extracted clock RxCK. The HDB3 decoded receive data, at 2.048Mb/s, is clocked out of the device on the RxD pin with the rising edge of RxCK. No DL data will be lost or repeated when a receive frame slip occurs as the DL data does not pass through the elastic buffer. In order to facilitate the attachment of this data stream to a Data Link controller, the $\overline{RxBF}$ pin outputs a frame boundary indicating the start of timeslot 0 containing the Sa bits.

11.2.3 E1 Data Link ST-BUS Access

When the ST-BUS data link access is enabled, the setting of the ST-BUS DSTi data bits determine the data link output on the PCM30 link corresponding to bit positions four to eight (Sa4-8) over each Non-Frame Alignment Signal (NFAS) frame. Data for data link transmission should be written to DSTi immediately following the NFAS frame (during FAS frames) and before the start of the next NFAS frame.

Similarly, the data link data received on the PCM30 link is output to ST-BUS DSTo timeslot 0 during NFAS frames. However, the data link data on ST-BUS DSTo timeslot 0 of NFAS frames is always enabled, regardless the control register bit settings.

Table 25 - E1 National Bits mapping to ST-BUS DST shows the detailed bit mapping of DSTi timeslots to transmit PCM30 timeslots.

ST-BUS DSTi/DSTo			PCM30 Transmit/Receive		
CRC-4 Frame	Timeslot	Data Bits (B7-B0)	Timeslot	CRC-4 Frame	Data Bits (B1-B8)
All NFAS	0 for 2Mb/s 0,1,2,3 for 8Mb/s	Sa8, Sa7, Sa6, Sa5, Sa4, P3, P2, P1	0	All NFAS	P1, P2, P3, Sa4, Sa5, Sa6, Sa7, Sa8
Note 1. P1-3 are not transmitted from DSTi but are received on DSTo.					

Table 25 - E1 National Bits mapping to ST-BUS DST

11.2.4 E1 Data Link HDLC Access

The Data Link can be connected to the internal HDLC, operating at a bit rate of 4/8/12/16 or 20 kbits/s, depending on the number of Sa bits enabled for transmission/reception on the HDLC with the SA control register bits detailed in Table 95 - E1 Data Link Control - R/W Address Y08.

11.2.5 E1 Data Link 5 Bit Register Access

Receive only 5 bit data register bits RNU4-8. See Table 111 E1 NFAS Signal and FAS Status - R Address Y13.

12.0 HDLC

The MT9071 has four embedded HDLC controllers, one for each of the four transceiver's, each of which includes the following features:
- Independent transmit and receive FIFO's;
- Receive FIFO maskable interrupts for nearly full (programmable interrupt levels) and overflow conditions;
- Transmit FIFO maskable interrupts for nearly empty programmable interrupt levels) and underflow conditions;
- Maskable interrupts for transmit end-of-packet and receive end-of-packet;
- Maskable interrupts for receive bad-frame (includes frame abort);
- Transmit end-of-packet and frame-abort functions.

In E1 mode, each controller may be attached to a data link operating at 4, 8, 12, 16 or 20kb/s for the Sa4, Sa5, Sa6, Sa7 and or Sa8 data link bits of timeslot 0 of the PCM30 frame.

In T1 mode, each controller may be attached to a data link operating at 4kb/s for the synchronization bit (s-bit) of the DS1 frame.

In addition, in E1 or T1 mode, each controller may be attached to a common channel signaling channel operating at 64kb/s for any T1 or E1 channel (not including timeslot 0 for E1 mode).

12.1 HDLC Overview

The HDLC handles the bit oriented packetized data transmission as per X.25 level two protocol defined by CCITT. It provides flag and abort sequence generation and detection, zero insertion and deletion, and Frame Check Sequence (FCS) generation and detection. A single byte, dual byte and all call address in the received frame can be recognized. Access to the receive FCS and inhibiting of transmit FCS for terminal adaptation are also provided. Each HDLC controller has a 32 byte deep FIFO associated with it. Status and interrupt flags are provided.

12.1.1   HDLC Frame Structure

In T1 mode or E1 mode a valid HDLC frame begins with an opening flag, contains at least 16 bits of address and control or information, and ends with a 16 bit FCS followed by a closing flag. Data formatted in this manner is also referred to as a "packet". Refer to Table 26 - HDLC Frame Format.

Opening Flag = 7E hex	Data Field	FCS	Closing Flag = 7E hex
One Byte 01111110	n Bytes n 2	Two Bytes	One Byte 01111110

Table 26 - HDLC Frame Format

All HDLC frames start and end with a unique flag sequence "01111110". The transmitter generates these flags and appends them to the packet to be transmitted. The receiver searches the incoming data stream for the flags on a bit- by-bit basis to establish frame synchronization.

The data field consists of an address field, control field and information field. The address field consists of one or two bytes directly following the opening flag. The control field consists of one byte directly following the address field. The information field immediately follows the control field and consists of N bytes of data. The

HDLC does not distinguish between the control and information fields and a packet does not need to contain an information field to be valid.

The FCS field, which precedes the closing flag, consists of two bytes. A cyclic redundancy check utilizing the CRC-CCITT standard generator polynomial "$X^{16}+X^{12}+X^5+1$" produces the 16-bit FCS. In the transmitter the FCS is calculated on all bits of the address and data field. The complement of the FCS is transmitted, most significant bit first, in the FCS field. The receiver calculates the FCS on the incoming packet address, data and FCS field and compares the result to "F0B8". If no transmission errors are detected and the packet between the flags is at least 32 bits in length then the address and data are entered into the receive FIFO minus the FCS which is discarded.

12.1.2   Data Transparency (Zero Insertion/Deletion)

Transparency ensures that the contents of a data packet do not imitate a flag, go-ahead, frame abort or idle channel. The contents of a transmitted frame, between the flags, is examined on a bit-by-bit basis and a 0 bit is inserted after all sequences of 5 contiguous 1 bits (including the last five bits of the FCS). Upon receiving five contiguous 1s within a frame the receiver deletes the following 0 bit.

12.1.3   Invalid Frames

A frame is invalid if one of the following four conditions exists (Inserted zeros are not part of a valid count):

- If the FCS pattern generated from the received data does not match the "F0B8" pattern, then the last data byte of the packet is written to the received FIFO with a 'bad packet' indication.
- A short frame exists if there are less than 25 bits between the flags. Short frames are ignored by the receiver and nothing is written to the receive FIFO.
- Packets which are at least 25 bits in length but less than 32 bits between the flags are also invalid. In this case the data is written to the FIFO but the last byte is tagged with a "bad packet" indication.
- If a frame abort sequence is detected the packet is invalid. Some or all of the current packet will reside in the receive FIFO, assuming the packet length before the abort sequence was at least 26 bits long.

12.1.4   Frame Abort

The transmitter will abort a current packet by substituting a zero followed by seven contiguous 1s in place of the normal packet. The receiver will abort upon reception of seven contiguous 1s occurring between the flags of a packet which contains at least 26 bits.

Note that should the last received byte before the frame abort end with contiguous 1s, these are included in the seven 1s required for a receiver abort. This means that the location of the abort sequence in the receiver may occur before the location of the abort sequence in the originally transmitted packet. If this happens then the last data written to the receive FIFO will not correspond exactly with the last byte sent before the frame abort.

12.1.5   Interframe Time Fill and Link Channel States

When the HDLC transmitter is not sending packets it will wait in one of two states.

- Interframe Time Fill state: This is a continuous series of flags occurring between frames indicating that the channel is active but that no data is being sent.
- Idle state: An idle Channel occurs when at least 15 contiguous 1s are transmitted or received.

In both states the transmitter will exit the wait state when data is loaded into the transmitter FIFO.

12.1.6 Go-Ahead

A go ahead is defined as the pattern "011111110" (contiguous 7Fs) and is the occurrence of a frame abort sequence followed by a zero, outside of the boundaries of a normal packet. Being able to distinguish a proper (in packet) frame abort sequence from one occurring outside of a packet allows a higher level of signaling protocol which is not part of the HDLC specifications.

12.2 HDLC Functional Description

The HDLC transceiver can be reset by either the power reset input signal or by the HRST control register bit detailed in Table 180 - T1 & E1 HDLC Control 1 - R/W Address YF3. When reset, the HDLC control registers (see Table 48 - T1 & E1 HDLC Control Registers - Address YF2-YF6) are cleared, resulting in the transmitter and receiver being disabled. The Receiver and Transmitter can be enabled independent of one another through control register bits RXEN and TXEN detailed in Table 179 - T1 & E1 HDLC Control 0 - R/W Address YF2. Transmit to receive loopback as well as a receive to transmit loopback are also supported with control register bits RTLOOP and HLOOP detailed in Table 180 - T1 & E1 HDLC Control 1 - R/W Address YF3.

Received packets from the serial interface are sectioned into bytes by the HDLC receiver that detects flags, checks for go-ahead signals, removes inserted zeros, performs a cyclical redundancy check (CRC) on incoming data, and monitors the address if required. Packet reception begins upon detection of an opening flag. The resulting bytes are concatenated with status register bits RQ9 and RQ8 (see Table 128 - T1 & E1 HDLC Status - R/W Address Y1D), and placed in the receiver first-in-first-out (RX FIFO); a buffer register that generates status and interrupts for microprocessor read control.

In conjunction with the control circuitry, the microprocessor writes data bytes into a transmit buffer register (TX FIFO) that generates status and interrupts. Packet transmission begins when the microprocessor writes a byte to the TX FIFO. Two status register bits are added to the TX FIFO for transmitter control of frame aborts (FA) and end of packet (EOP) flags. Packets have flags appended, zeros inserted, and a CRC, also referred to as frame checking sequence (FCS), added automatically during serial transmission. When the TX FIFO is empty and finished sending a packet, Interframe Time Fill bytes (continuous flags (7E hex)), or Mark Idle (continuous ones) are transmitted to indicate that the channel is idle.

12.2.1 HDLC Transmitter

Following initialization and enabling, the transmitter is in the Idle Channel state (Mark Idle), continuously sending ones. Interframe Time Fill state (Flag Idle) is selected by setting the mark idle bit MI detailed in Table 179 - T1 & E1 HDLC Control 0 - R/W Address YF2 high. The Transmitter remains in either of these two states until data is written to the TX FIFO. Control register bits EOP (end of packet) and FA (Frame Abort) detailed in Table 179 - T1 & E1 HDLC Control 0 - R/W Address YF2 are set as status bits before the microprocessor loads 8 bits of data into the 10 bit wide FIFO (8 bits data and 2 bits status). To change the tag bits being loaded in the FIFO, the control register must be written to before writing to the FIFO. However, EOP and FA are reset after writing to the TX FIFO. The counter detailed in Table 183 - T1 & E1 HDLC Transmit Packet Size - R/W Address YF6 may also be used to tag an end of packet. The register is loaded with the number of bytes in the packet and decrements after every write to the TX FIFO. When a count of one is reached, the next byte written to the FIFO is tagged as an end of packet. The register may be made to cycle through the same count if the packets are of the same length by setting the CYCLE bit detailed in Table 179 - T1 & E1 HDLC Control 0 - R/W Address YF2.

If the transmitter is in the Idle Channel state when data is written to the TX FIFO, then an opening flag is sent and data from TX FIFO follows. Otherwise, data bytes are transmitted as soon as the current flag byte has been sent. TX FIFO data bytes are continuously transmitted until either the FIFO is empty or an EOP or FA status bit is read by the transmitter. After the last bit of the EOP byte has been transmitted, a 16-bit FCS is sent followed by a closing flag. When multiple packets of data are loaded into TX FIFO, only one flag is sent between packets.

Frame aborts (the transmission of 7F hex), are transmitted by tagging a byte previously written to the TX FIFO. When a byte has an FA tag, then an FA is sent instead of that tagged byte. That is, all bytes previous to but not including that byte are sent. After a Frame Abort, the transmitter returns to the Mark Idle or Interframe Time Fill state, depending on the state of the Mark idle control register bit.

TX FIFO underrun will occur if the FIFO empties and the last byte did not have either an EOP or FA tag. A frame abort sequence will be sent when an underrun occurs.

Below is an example of the transmission of a three byte packet ('AA' '03' '77' hex) (Interframe time fill).

(a) Set MI bit - Write '04' hex to the register detailed in Table 179 - T1 & E1 HDLC Control 0 - R/W Address YF2

(b) Load 1st data byte - Write 'AA' hex to the register detailed in Table 182 - T1 & E1 HDLC Transmit FIFO Data - R/W Address YF5

(c) Load 2nd data byte - Write '03' hex to the register detailed in Table 182 - T1 & E1 HDLC Transmit FIFO Data - R/W Address YF5

(d) Set MI, TXEN, EOP bits - Write '34' hex to the register detailed in Table 179 - T1 & E1 HDLC Control 0 - R/W Address YF2

(e) Load final data byte - Write '77' hex to the register detailed in Table 182 - T1 & E1 HDLC Transmit FIFO Data - R/W Address YF5

The transmitter may be enabled independently of the receiver. This is done by setting the TXEN bit of the control register detailed in Table 179 - T1 & E1 HDLC Control 0 - R/W Address YF2.

Enabling happens immediately upon writing to the register. Disabling using TXEN will occur after the completion of the transmission of the present packet; the contents of the FIFO are not cleared. Disabling will consist of stopping the transmitter clock. The Status and Interrupt Registers may still be read and the FIFO and Control Registers may be written to while the transmitter is disabled. The transmitted FCS may be inhibited using the TCRCI bit detailed in Table 179 - T1 & E1 HDLC Control 0 - R/W Address YF2. In this mode the opening flag followed by the data and closing flag is sent and zero insertion still included, but no CRC. That is, the FCS is injected by the microprocessor as part of the data field. This is used in V.120 terminal adaptation for synchronous protocol sensitive UI frames.

12.2.2 HDLC Receiver

After initialization and enabling, the receiver clocks in serial data, continuously checking for Go-aheads (0 1111 1110), flags (0111 1110), and Idle Channel states (at least fifteen ones). When a flag is detected, the receiver synchronizes itself to the serial stream of data bits, automatically calculating the FCS. If the data length between flags after zero removal is less than 25 bits, then the packet is ignored so no bytes are loaded into RX FIFO. When the data length after zero removal is between 25 and 31 bits, a first byte and bad FCS code are loaded into the RX FIFO (see definition of RQ8 and RQ9 below). For an error-free packet, the result in the CRC register should match the HEX pattern of 'F0B8' when a closing flag is detected.

If address recognition is required, the receiver address recognition register (see Table 181 - T1 & E1 HDLC Address Recognition Control - R/W Address YF4) is loaded with the desired address and the ADREC bit detailed in Table 179 - T1 & E1 HDLC Control 0 - R/W Address YF2 is set high. Control register bits A2EN and A1EN are used as an enable bit for the two bytes, thus allowing either or both of the first two bytes to be compared to the expected values. Bit 0 of the first byte of the address received (address extension bit) will be monitored to determine if a single or dual byte address is being received. If this bit is 0 then a two byte address is being received and then only the first six bits of the first address byte are compared. An all call condition is also monitored for the second address byte; and if received the first address byte is ignored (not compared with mask byte). If the address extension bit is a 1 then a single byte address is being received. In this case, an all call condition is monitored for in the first byte as well as the mask byte written to the comparison register and the second byte is ignored. Seven bits of address comparison can be realized on the first byte if this is a single byte address by setting control register bit SEVEN detailed in Table 179 - T1 & E1 HDLC Control 0 - R/W Address YF2.

The RQ8 and RQ9 status register bits detailed in Table 128 - T1 & E1 HDLC Status - R/W Address Y1D, are appended to each data byte as it is written to the RX FIFO. They indicate that a good packet has been received (good FCS and no frame abort), or a bad packet with either incorrect FCS or frame abort. The status and interrupt registers (see Table 148- T1 & E1 HDLC Interrupt Status - R Address Y33) should be read before reading the RX FIFO since status and interrupt information correspond to the byte at the output of the FIFO (i.e. the byte about to be read). The status register bits are encoded as follows:

RQ9	RQ8	Byte status
1	1	last byte (bad packet)
0	1	first byte
1	0	last byte (good packet)
0	0	packet byte

The end-of-packet-detect interrupt bit EOPDI (see Table 148 - T1 & E1 HDLC Interrupt Status - R Address Y33) indicates that the last byte written to the RX FIFO was an EOP byte (last byte in a packet). The end-of-packet-read (EOPRI) interrupt indicates that the byte about to be read from the RX FIFO is an EOP byte (last byte in a packet). The status register should be read to see if the packet is good or bad before the byte is read.

A minimum size packet has an 8-bit address, an 8-bit control byte, and a 16-bit FCS pattern between the opening and closing flags (see Section 12.1.1 HDLC Frame Structure). Thus, the absence of a data transmission error and a frame length of at least 32 bits results in the receiver writing a valid packet code with the EOP byte into RX FIFO. The last 16 bits before the closing flag are regarded as the FCS pattern and will not be transferred to the receiver FIFO. Only data bytes (Address, Control, Information) are loaded into the RX FIFO.

In the case of an RX FIFO overflow, no clocking occurs until a new opening flag is received. In other words, the remainder of the packet is not clocked into the FIFO. Also, the top byte of the FIFO will not be written over. If the FIFO is read before the reception of the next packet then reception of that packet will occur. If two beginning of packet conditions (RQ9=0;RQ8=1) are seen in the FIFO, without an intermediate EOP status, then overflow occurred for the first packet.

The receiver may be enabled independently of the transmitter. This is done by setting the RXEN bit detailed in Table 179- T1 & E1 HDLC Control 0 - R/W Address YF2. Enabling happens immediately upon writing to the register. Disabling using RXEN will occur after the present packet has been completely loaded into the FIFO. Disabling can occur during a packet if no bytes have been written to the FIFO yet. Disabling will consist of disabling the internal receive clock. The FIFO, Status, and Interrupt Registers may still be read while the receiver is disabled. Note that the receiver requires a flag before processing a frame, thus if the receiver is enabled in the middle of an incoming packet it will ignore that packet and wait for the next complete one.

The receive CRC can be monitored with the CRC15-0 status bits detailed in Table 129 - T1 & E1 HDLC Receive CRC Data - R/W Address Y1E. This register contains the actual CRC sent by the other transmitter in its original form; that is, MSB first and bits inverted. This register is updated by each end of packet (closing flag) received and therefore should be read when an end of packet is received so that the next packet does not overwrite the register.

13.0 Transparent Mode Operation

Both T1 and E1 modes provide a transparent mode of operation where framing is not imposed in the transmit direction.

13.1 T1 Transparent Mode Operation

Setting control register bit TRANSP (see Table 78 - T1 Framing Mode Control - R/W Address Y00) enables transparent mode operation which causes unframed data to be transmitted from DSTi channels 0 to 23 and channel 31 bit 7 onto the DS1 line. Unframed data received from the DS1 line is piped out on DSTo channels 0 to 23 and channel 31 bit 0.

13.2 E1 Transparent Mode Operation

13.2.1 Transmit Timeslot 0 all Frames from DSTi to PCM30

Setting control register bit TXTRS (see Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) enables transparent mode operation which causes unframed data to be transmitted from DSTi channels 0 to 31 onto the PCM30 line. Unframed data received from the PCM30 line is piped out on DSTo channels 0 to 31. In other words, timeslot 0 data on the transmit PCM30 link is sourced from the DSTi input. Table 27 - E1 Transmit/Receive Timeslot 0 from/to ST-BUS DSTi/DSTo shows the detailed bit mapping of DSTi timeslot 0 to transmit PCM30 timeslot 0.

ST-BUS DSTi/DSTo			PCM30 Transmit/Receive		
Frame	**Timeslot**	**Data Bits (B7-B0)**	**Timeslot**	**Frame**	**Data Bits (B1-B8)**
All	n	P8, P7, P6, P5, P4, P3, P2, P1	0	All	P1, P2, P3, P4, P5, P6, P7, P8
Note 1. For 2.048Mb/s operation, n=0. Note 2. For 8.192Mb/s operation, n =0,1,2,3 where n corresponds to the tranceiver number (i.e. n=0=tranceiver 0... n=3= tranceiver 3).					

Table 27 - E1 Transmit/Receive Timeslot 0 from/to ST-BUS DSTi/DSTo

13.2.2 Receive Timeslot 0 all Frames from PCM30 to DSTo

Timeslot 0 signal bits on the receive PCM30 link (bit positions one to eight of timeslot 0 of all frames) may be sourced to either data registers, data buffers, to the ST-BUS DSTo stream, to a modified ST-BUS DSTo stream, or to a mix of all; depending on the programming of control register bits detailed in Table 167 - E1 Per Timeslot 0 to 31 Control Registers - R/W Address Y90-YAF. If these register bits are disabled, then data to DSTo is mapped unaltered from the receive PCM30 link as shown in Table 27 - E1 Transmit/Receive Timeslot 0 from/to ST-BUS DSTi/DSTo.

14.0 Payload Data Operation

14.1 T1 DS1 Payload Data

The T1 DS1 payload usually consists of channels 1 to 24, refer to Section 4.1 T1 Interface Overview.

14.1.1 T1 DS1 & ST-BUS DSTi/DSTo Timeslot Relationship

When mapping to the DS1 payload, only the first 24 time slots of an ST-BUS are used. See Table 28 - T1 DS1 & ST-BUS DSTi/DSTo Timeslot Relationship. Note that ST-BUS timeslot 31 may be used for the framing bit (S-bit). All unused ST-BUS DSTo timeslots are high impedance.

		DS1 Timeslot or Channel																															
T	0-3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	S-bit							
R		ST-BUS 2.048Mb/s DSTi/DSTo Timeslot																															
A	0-3	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
N		ST-BUS 8.192Mb/s DSTi/DSTo Timeslot																															
C	0	0	4	8	12	16	20	24	28	32	36	40	44	48	52	56	60	64	68	72	76	80	84	88	92	96	100	104	108	112	116	120	124
E	1	1	5	9	13	17	21	25	29	33	37	41	45	49	53	57	61	65	69	73	77	81	85	89	93	97	101	105	109	113	117	121	125
I	2	2	6	10	14	18	22	26	30	34	38	42	46	50	54	58	62	66	70	74	78	82	86	90	94	98	102	106	110	114	118	122	126
V	3	3	7	11	15	19	23	27	31	35	39	43	47	51	55	59	63	67	68	75	79	83	87	91	95	99	103	107	111	115	119	123	127

Table 28 - T1 DS1 & ST-BUS DSTi/DSTo Timeslot Relationship

14.2 E1 PCM30 Payload Data

The E1 PCM30 payload usually consists of channels 1 to 30, refer to Section 5.1 E1 Interface Overview.

14.2.1   E1 PCM30 & ST-BUS DSTi/DSTo Timeslot Relationship

When mapping to the PCM30 payload, only the time slots 1 to 15 and 17 to 31 of an ST-BUS are used. See Table 29 - E1 PCM30 & ST-BUS DSTi/DSTo Timeslot Relationship. Note that ST-BUS timeslots 0 and 16 may be used in numerous modes of operation including transparent mode, CAS and CCS. In addition, PCM30 channels 15,16 and 31 may be used for CCS.

TRANCEIVER		PCM30 Timeslot																															
	0-3	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
		PCM30 Channel																															
		-	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	-	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
		ST-BUS 2.048Mb/s DSTi/DSTo Timeslot																															
	0-3	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
		ST-BUS 8.192Mb/s DSTi/DSTo Timeslot																															
	0	0	4	8	12	16	20	24	28	32	36	40	44	48	52	56	60	64	68	72	76	80	84	88	92	96	100	104	108	112	116	120	124
	1	1	5	9	13	17	21	25	29	33	37	41	45	49	53	57	61	65	69	73	77	81	85	89	93	97	101	105	109	113	117	121	125
	2	2	6	10	14	18	22	26	30	34	38	42	46	50	54	58	62	66	70	74	78	82	86	90	94	98	102	106	110	114	118	122	126
	3	3	7	11	15	19	23	27	31	35	39	43	47	51	55	59	63	67	68	75	79	83	87	91	95	99	103	107	111	115	119	123	127

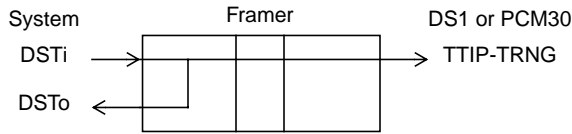**Table 29 - E1 PCM30 & ST-BUS DSTi/DSTo Timeslot Relationship**

15.0   Loopbacks

In order to meet PRI Layer 1 requirements and to assist in circuit fault sectionalization, the MT9071 has numerous loopback functions. Loopback functions are enabled through control registers as detailed in Table 30 - Loopback Control Register Summary. The loopback configurations for T1 and E1 are the same and are detailed in the following loopback descriptions.
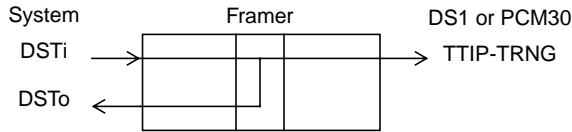
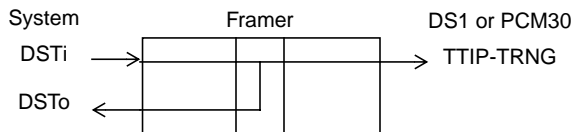| Loopback Type	Control Bit	T1 Mode Control Register	E1 Mode Control Register
ST-BUS	SLBK	Table 88 - T1 Loopback Control - R/W Address Y05	Table 81 - E1 Test, Error and Loopback Control - R/W Address Y01
Digital	DLBK		
Payload	PLBK		
Metallic	MLBK	Table 173 - T1 & E1 LIU Control - R/W Address YE3	
Remote	RLBK		
Local Timeslot	LTSL	Table 166 - T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7	Table 167 - E1 Per Timeslot 0 to 31 Control Registers - R/W Address Y90-YAF
Remote Timeslot	RTSL		

Table 30 - Loopback Control Register Summary

a) *ST-BUS Loopback* - Loops DSTi to DSTo at the system interface point.
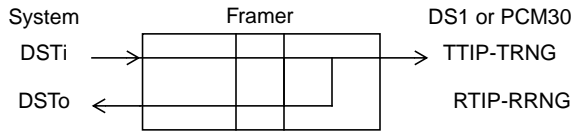
```
           System          Framer        DS1 or PCM30
           DSTi   ───→┌─────┬─────┬─────┐──→ TTIP-TRNG
                      │     │     │     │
           DSTo   ←───┘     │     │     │
                      └─────┴─────┴─────┘
```

b) *Digital Loopback* - Loops DSTi to DSTo at the Framer to LIU interface point.

```
           System          Framer        DS1 or PCM30
           DSTi   ───→┌─────┬─────┬─────┐──→ TTIP-TRNG
                      │     │     │     │
           DSTo   ←───┘     │     │     │
                      └─────┴─────┴─────┘
```

c) *Local Timeslot Loopback* - Loops selected timeslots from DSTi to DSTo at the Framer to LIU interface point.

```
           System          Framer        DS1 or PCM30
           DSTi   ───→┌─────┬─────┬─────┐──→ TTIP-TRNG
                      │     │     │     │
           DSTo   ←───┘     │     │     │
                      └─────┴─────┴─────┘
```

d) *Metallic Loopback* - Loops DSTi to DSTo at the DS1 or PCM30 interface point.

```
           System          Framer        DS1 or PCM30
           DSTi   ───→┌─────┬─────┬─────┐──→ TTIP-TRNG
                      │     │     │     │
           DSTo   ←───┘     │     │     │   RTIP-RRNG
                      └─────┴─────┴─────┘
```

e) *Remote Loopback* - Loops RTIP to TTIP and RRNG to TRNG at the Framer to LIU interface point. In order to accommodate the common timing applied to the LIU transmitter, the jitter attenuator must be manually enabled for this loopback (in both E1 and T1 modes).

```
           System          Framer        DS1 or PCM30
                      ┌─────┬─────┬─────┐──→ TTIP-TRNG
                      │     │     │     │
           DSTo   ←───┘     │     │     │←── RTIP-RRNG
                      └─────┴─────┴─────┘
```
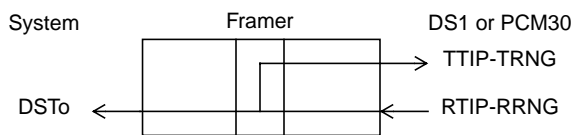
f) *Payload Loopback* - Loops RTIP to TTIP and RRNG to TRNG at the system interface point. When in T1 mode, ensure control register bit $\overline{\text{RXDO}}$ (Register Address YF1) is not enabled, $\overline{\text{RXDO}}$ = 1.

```
           System          Framer        DS1 or PCM30
                      ┌─────┬─────┬─────┐──→ TTIP-TRNG
                      │     │     │     │
           DSTo   ←───┘     │     │     │←── RTIP-RRNG
                      └─────┴─────┴─────┘
```
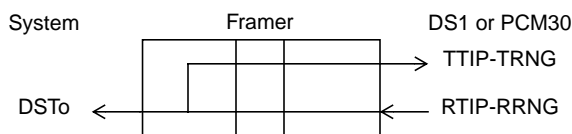
g) *Remote Timeslot Loopback* - Loops selected timeslots from RTIP to TTIP and RRNG to TRNG at the system interface point.

System	Framer	DS1 or PCM30

TTIP-TRNG

DSTo ← RTIP-RRNG
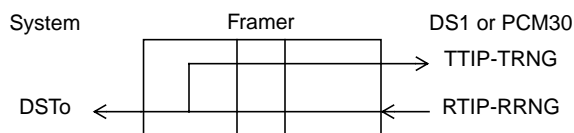
15.1 T1 Mode In Band Loopback Codes

T1.403 defines SF mode line loopback activate and deactivate codes. These codes are either a framed or unframed repeating bit sequence of 00001 for activation or 001 for deactivation. The standard goes on to say that these codes will persist for five seconds or more before the loopback action is taken. The MT9071 will detect both framed and unframed line activate and de-activate codes even in the presence of a BER of 3×10^{-3}. Status register bit LLDD (see Table 104 - T1 Synchronization and Alarm Status - R Address Y10) will be asserted when a repeating 001 pattern (either framed or unframed) has persisted for 48 milliseconds. Status register bit LLED (see Table 104 - T1 Synchronization and Alarm Status - R Address Y10) will be asserted when a repeating 00001 pattern (either framed or unframed) has persisted for 48 milliseconds.

Other loopup and down codes can be selected by writing to the transmit loop up and loop down code registers (see Table 101 - T1 Transmit Loop Activate Code Control - R/W Address Y0D and Table 102 - T1 Transmit Loop Deactivate Code Control - R/W Address Y0E).

The selection of the expected received loopup and loopdown code is done by writing to the receive loop up and loop down code match registers (see Table 103 - T1 Receive Loop Activate Code Match Control - R/W Address Y0F and Table 177 - T1 Receive Loop Deactivate Code Match - R/W Address YF0).

Maskable interrupt status bits LLEDI and LLDDI will be set upon detection of inband loopup or loopdown codes respectively (see Table 149 - T1 Receive and Sync Interrupt Status - R Address Y34 and Table 156 - T1 Receive and Sync Interrupt Mask - R/W Address Y44).

16.0 T1 Maintenance and Alarms

16.1 T1 Error Counters

The MT9071 has nine T1 error counters for each framer, which can be used for maintenance testing, for ongoing measure of the quality of a DS1 link and to assist the designer in meeting specifications such as TR62411 and T1.403. All counters can be preset or cleared by writing to the appropriate locations. In addition, all counters may be cleared by programming the counter clear bit CNCLR (see Table 178 - T1 Interrupt and I/O Control - R/W Address YF1) low to high. Associated with each counter is a maskable event occurrence interrupt and a maskable counter overflow interrupt. Overflow interrupts are useful when cumulative error counts are being recorded. Associated with four counters are the 1 second latched registers. These registers are updated with their corresponding counter values on a one second interval. Counters can automatically be cleared after their data is latched by setting control register bit ACCLR (see Table 178 - T1 Interrupt and I/O Control - R/W Address YF1) high.

For a full listing of all available T1 counters, latches, interrupts and masks, refer to Table 31 - T1 Error Counters Summary.

Counter	Counter 1 Sec. Latch	Counter Indication			Counter Overflow		
		Latch	Int.	Mask	Latch	Int.	Mask
Table 114 - T1 PRBS CRC Multiframe and PRBS Error Counter - R/W Address Y15	NA	NA Y25	NA Y35	NA Y45	Y24 Y24	Y34 Y34	Y44 Y44
PCC7-0 PEC7-0		NA PEIL	NA PEII	NA PEIM	PCOL PEOL	PCOI PEOI	PCOM PEOM
Table 116 - T1 Multiframe Out of Frame Counter - R/W Address Y16	Table 147 - T1 Multiframe Out of Frame Counter Latch - R Address Y2C	NA			Y24	Y34	Y44
MFC15-0	MFL15-0				MFOL	MFOI	MFOM
Table 118 - T1 Framing Bit Error Counter - R/W Address Y17	Table 139 - T1 Framing Bit Error Counter Latch - R Address Y28	Y24	Y34	Y44	Y24	Y34	Y44
BEC15-0	BEL15-0	BEIL	BEII	BEIM	BEOL	BEOI	BEOM
Table 120 - T1 Bipolar Violation Counter - R/W Address Y18	Table 141 - T1 Bipolar Violation Error Counter Latch - R Address Y29	Y25	Y35	Y45	Y24	Y34	Y44
VEC15-0	VEL15-0	VEIL	VEII	VEIM	VEOL	VEOI	VEOM
Table 122 - T1 CRC-6 Error Counter - R/W Address Y19	Table 143 - T1 CRC-6 Error Counter Latch - R Address Y2A	Y24	Y34	Y44	Y24	Y34	Y44
CEC15-0	CEL15-0	CEIL	CEII	CEIM	CEOL	CEOI	CEOM
Table 124 - T1 Out of Frame and Change of Frame Counters - R/W Address Y1A	Table 145 - T1 Out of Frame & Change of Frame Counter Latch - R Address Y2B	NA Y24	NA Y34	NA Y44	Y24 Y24	Y34 Y34	Y44 Y44
OFC7-0 CFC7-0	OFL7-0 CFL7-0	NA CFIL	NA CFII	NA CFIM	OFOL CFOL	OFOI CFOI	OFOM CFOM
Table 126 - T1 Excessive Zero's Counter - R/W Address Y1B	NA	Y26	Y36	Y46	Y26	Y36	Y46
EZC7-0		EZIL	EZII	EZIM	EZOL	EZOI	EZOM

Y24 - See Table 132 - T1 Receive Sync and Alarm Latch - R Address Y24
Y25 - See Table 134 - T1 Receive Line Status and Timer Latch - R Address Y25
Y26 - See Table 136 - T1 Elastic Store Status Latch - R Address Y26
Y34 - See Table 149 - T1 Receive and Sync Interrupt Status - R Address Y34
Y35 - See Table 151 - T1 Receive Line and Timer Interrupt Status - R Address Y35
Y36 - See Table 153 - T1 Elastic Store Interrupt Status - R Address Y36
Y44 - See Table 156 - T1 Receive and Sync Interrupt Mask - R/W Address Y44
Y45 - See Table 158 - T1 Receive Line and Timer Interrupt Mask - R/W Address Y45
Y46 - See Table 160 - T1 Elastic Store Interrupt Mask - R/W Address Y46

Table 31 - T1 Error Counters Summary

16.2 T1 Error Insertion

Six types of error conditions can be inserted into the transmit DS1 data stream through control register bits, which are detailed in Table 84 - T1 Transmit Error Control - R/W Address Y03. These error events include the bipolar violation errors (BPVE), CRC-6 errors (CRCE), Ft errors (FTE), Fs errors (FSE), payload (PERR) and a loss of signal condition (LOSE). If LOSE is one, the MT9071 transmits an all zeros signal (no pulses). Zero code suppression is overridden. If LOSE bit is zero, data is transmitted normally.

16.3 T1 Per Channel Control

There are 24 per channel control registers occupying a total of 24 unique addresses (see Table 166 - T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7). Each register controls a matching timeslot on the 24 transmit channels (onto the line) and the equivalent channel data on the receive (DSTo) data. For example,

register address Y90 of the first per channel control register contains program control for transmit channel 1 and DSTo timeslot 0.

16.3.1 T1 Per Channel Trunk Conditioning

The received data on a DSTo timeslot can be replaced by the idle code data bits RXIDC7-0 detailed in Table 96 - T1 Receive Idle Code Data - R/W Address Y09 on a per channel basis when programmed with control register bit MPDR in the per channel control registers detailed in Table 166 - T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7.

Similarly, the transmitted data from a DSTi timeslot can be replaced by the idle code data bits TXIDC7-0 detailed in Table 98 - T1 Transmit Idle Code Data - R/W Address Y0A on a per channel basis when programmed with control register bit MPDT in the per channel control registers detailed in Table 166 - T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7.

The received data on a DSto timeslot can also be inverted on a per channel basis by setting control bit RPCI detailed in Table 166 - T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7.

Similarly, the transmitted data from a DSTi timeslot can also be inverted on a per channel basis by setting control bit TPCI detailed in Table 166 - T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7.

16.3.2 T1 Per Channel Looping

See Section 15.0 Loopbacks.

16.3.3 T1 Per Channel PRBS Testing

The MT9071 includes both a pseudo random bit sequence (PRBS) generator of type (2^{15}-1), and a reverse PRBS generator (decoder), which operates on a bit sequence, and determines if it matches the transmitted PRBS type (2^{15}-1). Bits which don't match are counted by an internal error counter. This provides for powerful system debugging and testing without additional external hardware.

If control register bit ADSEQ (see Table 80 - T1 Line Coding Control - R/W Address Y01) is zero, any transmit (internal DSTi) timeslot or combination of transmit timeslots may be connected to the PRBS generator. Timeslot n is selected by setting the TTSTn bit detailed in Table 166 - T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7, where n is 0 to 23. Any data sent on DSTi is overwritten on the selected timeslots before being output to TTIP/TRNG.

Similarly, if control register bit ADSEQ is zero, any receive timeslot or combination of receive timeslots may be connected to the PRBS decoder. Timeslot n is selected by setting the RRSTn bit detailed in Table 166 - T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7, where n is 0 to 23

PRBS data is distributed to the transmit channels sequentially one byte at a time. Consequently, the data received must be in the same order that it was sent, in order for the PRBS decoder to correctly operate on the data.

If one channel is tested at a time, then the PRBS transmit timeslot does not have to match the PRBS receive timeslot. However, if more than one channel is tested, then the number of transmit timeslots must match the number of receive timeslots, and the order of the transmit timeslots must match the order of the receive timeslots. This will ensure that the sequential data bytes received by the PRBS decoder are in the correct order. Consequently, particular care must be taken when using an external loopback where the channel order may be reversed, or where the data has passed through a digital switch which doesn't buffer all channels to the same degree.

The PRBS decoder must have sufficient data pass through it before it begins to operate correctly, therefore, the errors generated by the decoder immediately following start-up should be ignored.

If the PRBS testing is performed in an external loop around using timeslot control, then both timeslot control register bits TTSTn and RRSTn should be set.

16.3.4   T1 Per Channel Mu-law Milliwatt

If the control register bit ADSEQ (see Table 80 - T1 Line Coding Control - R/W Address Y01) is one, the Mu-law digital milliwatt sequence (Table 32 - T1 Mu-Law Digital Milliwatt Pattern), defined by G.711, is available to be transmit on any combination of selected channels. Timeslot n is selected by setting the TTSTn bit detailed in Table 166 - T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7, where n is 0 to 23. Any data sent on DSTi is overwritten on the selected timeslots before being output to TTIP/TRNG. The same sequence is available to replace received data on any combination of DSTo channels. This is accomplished by setting the RRSTn control register bit for the corresponding channel.

PCM 24 Payload Data								
Hex	**Bit 1**	**Bit 2**	**Bit 3**	**Bit 4**	**Bit 5**	**Bit 6**	**Bit 7**	**Bit 8**
1E	0	0	0	1	1	1	1	0
0B	0	0	0	0	1	0	1	1
0B	0	0	0	0	1	0	1	1
1E	0	0	0	1	1	1	1	0
9E	1	0	0	1	1	1	1	0
8B	1	0	0	0	1	0	1	1
8B	1	0	0	0	1	0	1	1
9E	1	0	0	1	1	1	1	0

Table 32 - T1 Mu-Law Digital Milliwatt Pattern

16.4 T1 Alarms

The MT9071 is capable of detecting and transmitting numerous alarms. The status register bits provide real time status of the alarm, while the latched status registers provide a latched status indication and are cleared when read. The interrupt status registers also provide a latched status indication if unmasked, are also cleared when read and each interrupt status register may also generate a maskable interrupt (if unmasked). Note that reading either the latched or interrupt status register will clear both of these registers. See the register bit descriptions in the tables listed in Table 33 - T1 Alarms and Timers Register Summary for complete details.

Description	Receiver Status and Interrupt Register and Bit			
	Status	**Latched Status**	**Interrupt Status**	**Interrupt Mask**
	Table 104 - T1 Synchronization and Alarm Status - R Address Y10	**Table 134 - T1 Receive Line Status and Timer Latch - R Address Y25**	**Table 151 - T1 Receive Line and Timer Interrupt Status - R Address Y35**	**Table 158 - T1 Receive Line and Timer Interrupt Mask - R/W Address Y45**
D4 Yellow Alarm	D4Y	D4YL	D4YI	D4YM
D4 Yellow Alarm - 48 ms sample	D4Y48	D4Y48L	D4Y48I	D4Y48M
Secondary D4 Yellow Alarm	SECY	SECYL	SECYI	SECYM
AIS Alarm	AIS	AISL	AISI	AISM
ESF Yellow Alarm	ESFY	ESFYL	ESFYI	ESFYM
T1DM Yellow Alarm	T1DMY	T1DMYL	T1DMYI	T1DMYM
Description	**Transmitter Control Register and Bit**			
	Table 82 - T1 Transmit Alarm Control - R/W Address Y02			
Transmit ESF Yellow Alarm	TESFY			
Transmit Sec. D4 Yellow Alarm	TSECY			
Transmit All Ones	TAIS			
S-bit Override	SO			
Transmit T1DM Yellow Alarm	TT1DMY			

Table 33 - T1 Alarms and Timers Register Summary

17.0   E1 Maintenance and Alarms

17.1 E1 Error Counters

The MT9071 has eight error counters for each framer, which can be used for maintenance testing, for ongoing measure of the quality of a E1 link and to assist the designer in meeting specifications such as ITU-T I.431 and G.821. All counters can be preset or cleared by writing to the appropriate locations. In addition, all counters may be cleared by programming the counter clear bit CNCLR (see Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) low to high. Associated with each counter is a maskable event occurrence interrupt and a maskable counter overflow interrupt. Overflow interrupts are useful when cumulative error counts are being recorded. Associated with four counters are the 1 second latched registers. These registers are updated with their corresponding counter values on a one second interval. Counters can automatically be cleared after their data is latched by setting control register bit ACCLR (see Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) high.

For a full listing of all available E1 counters, latches and interrupts, refer to Table 34 - E1 Error Counters Summary.

Counter	Counter 1 Sec. Latch	Counter Indication			Counter Overflow		
		Latch	Int.	Mask	Latch	Int.	Mask
Table 115 - E1 PRBS Error Counter & PRBS CRC Multiframe Counter - R/W Address Y15	NA	Y25 NA	Y35 NA	Y45 NA	Y25 Y25	Y35 Y35	Y45 Y45
PEC7-0 PCC7-0		PEIL NA	PEII NA	PEIM NA	PEOL PCOL	PEOI PCOI	PEOM PCOM
Table 117 - E1 Loss of Basic Frame Sync Counter - R/W Address Y16	NA	NA			Y24	Y34	Y44
SLC15-0					SLOL	SLOI	SLOM
Table 119 - E1 E-bit Error Counter - R/W Address Y17	Table 140 - E1 E-Bit Error Count Latch - R Address Y28	Y25	Y35	Y45	Y25	Y35	Y45
EEC15-0	EEL15-0	EEIL	EEII	EEIM	EEOL	EEOI	EEOM
Table 121 - E1 Bipolar Violation Error Counter - R/W Address Y18	Table 142 - E1 Bipolar Violation Error Count Latch - R/W Address Y29	Y25	Y35	Y45	Y25	Y35	Y45
VEC15-0	VEL15-0	VEIL	VEII	VEIM	VEOL	VEOI	VEOM
Table 123 - E1 CRC-4 Error Counter - R/W Address Y19	Table 144 - E1 CRC-4 Error Count Latch - R/W Address Y2A	Y25	Y35	Y45	Y25	Y35	Y45
CEC15-0	CEL15-0	CEIL	CEII	CEIM	CEOL	CEOI	CEOM
Table 125 - E1 FAS Bit Error Counter & FAS Error Counter - R/W Address Y1A	Table 146 - E1 FAS Error Count Latch - R/W Address Y2B	Y25 Y25	Y35 Y35	Y45 Y45	Y25 Y25	Y35 Y35	Y45 Y45
BEC7-0 FEC7-0	BEL7-0 FEL7-0	BEIL FEIL	BEII FEII	BEIM FEIM	BEOL FEOL	BEOI FEOI	BEOM FEOM
Y25 - See Table 135 - E1 Counter Latched Status - R Address Y25 Y35 - See Table 152 - E1 Counter Interrupt Status - R Address Y35 Y45 - See Table 159 - E1 Counter Interrupt Mask - R/W Address Y45							

Table 34 - E1 Error Counters Summary

17.2 E1 Error Insertion

Six types of error conditions can be inserted into the transmit PCM 30 data stream through control register bits, which are detailed in Table 81 - E1 Test, Error and Loopback Control - R/W Address Y01. These error events include the bipolar violation errors (BVE), CRC-4 errors (CRCE), FAS errors (FASE), NFAS errors (NFSE), payload (PERR) and a loss of signal error (LOSE). The LOSE function overrides the HDB3 encoding function (no BPV are added). Also included are E1 and E2 error bit insertion on frames 13 and 15.

17.3 E1 Per Timeslot Control

There are 32 per timeslot control registers occupying a total of 32 unique addresses (see Table 167 - E1 Per Timeslot 0 to 31 Control Registers - R/W Address Y90-YAF). Each register controls a matching timeslot on the 32 transmit channels (onto the line) and the equivalent channel data on the receive (DSTo) data. For example, register address Y90 of the first per timeslot control register contains program control for transmit timeslot 0 and DSTo channel 0.

17.3.1   E1 Per Timeslot Trunk Conditioning

The received data on a DSTo timeslot can be replaced by the idle code data bits RXIDC7-0 detailed in Table 97 - E1 Receive Idle Code Data - R/W Address Y09 on a per channel basis when programmed with control register bit MPDR in the per channel control registers detailed in Table 167 - E1 Per Timeslot 0 to 31 Control Registers - R/W Address Y90-YAF.

Similarly, the transmitted data from a DSTi timeslot can be replaced by the idle code data bits TXIDC7-0 detailed in Table 99 - E1 Transmit Idle Code Data - R/W Address Y0A on a per channel basis when programmed with control register bit MPDT in the per channel control registers detailed in Table 167 - E1 Per Timeslot 0 to 31 Control Registers - R/W Address Y90-YAF.

The received data on a DSto timeslot can also be inverted on a per channel basis by setting control bit RPCI detailed in Table 167 - E1 Per Timeslot 0 to 31 Control Registers - R/W Address Y90-YAF.

Similarly, the transmitted data from a DSTi timeslot can also be inverted on a per channel basis by setting control bit TPCI detailed in Table 167 - E1 Per Timeslot 0 to 31 Control Registers - R/W Address Y90-YAF.

17.3.2   E1 Per Timeslot Looping
See Section 15.0 Loopbacks.

17.3.3   E1 Per Timeslot PRBS Testing

The MT9071 includes both a pseudo random bit sequence (PRBS) generator of type (2^{15}-1), and a reverse PRBS generator (decoder), which operates on a bit sequence, and determines if it matches the transmitted PRBS type (2^{15}-1). Bits which don't match are counted by an internal error counter. This provides for powerful system debugging and testing without additional external hardware.

If control register bit ADSEQ (see Table 81 - E1 Test, Error and Loopback Control - R/W Address Y01) is zero, any transmit (internal DSTi) timeslot or combination of transmit timeslots may be connected to the PRBS generator. Timeslot n is selected by setting the TTSTn bit detailed in Table 167 - E1 Per Timeslot 0 to 31 Control Registers - R/W Address Y90-YAF, where n is 0 to 31. Any data sent on DSTi is overwritten on the selected timeslots before being output to TTIP/TRNG.

Similarly, if control register bit ADSEQ is zero, any receive timeslot or combination of receive timeslots may be connected to the PRBS decoder. Timeslot n is selected by setting the RRSTn bit detailed in Table 167 - E1 Per Timeslot 0 to 31 Control Registers - R/W Address Y90-YAF, where n is 0 to 31. Data on DSTo is not affected.

PRBS data is distributed to the transmit channels sequentially one byte at a time. Consequently, the data received must be in the same order that it was sent, in order for the PRBS decoder to correctly operate on the data.

If one channel is tested at a time, then the PRBS transmit timeslot does not have to match the PRBS receive timeslot. However, if more than one channel is tested, then the number of transmit timeslots must match the number of receive timeslots, and the order of the transmit timeslots must match the order of the receive timeslots. This will ensure that the sequential data bytes received by the PRBS decoder are in the correct order. Consequently, particular care must be taken when using an external loopback where the channel order may be reversed, or where the data has passed through a digital switch which doesn't buffer all channels to the same degree.

The PRBS decoder must have sufficient data pass through it before it begins to operate correctly, therefore, the errors generated by the decoder immediately following start-up should be ignored.

If the PRBS testing is performed in an external loop around using timeslot control, then both timeslot control register bits TTSTn and RRSTn should be set.

17.3.4   E1 Per Timeslot A-law Milliwatt

If the control register bit ADSEQ (see Table 81 - E1 Test, Error and Loopback Control - R/W Address Y01) is one, the A-law digital milliwatt sequence (Table 35 - E1 A-Law Digital Milliwatt Pattern), defined by G.711, is available to be transmit on any combination of selected channels. Timeslot n is selected by setting the TTSTn bit detailed in Table 167 - E1 Per Timeslot 0 to 31 Control Registers - R/W Address Y90-YAF, where n is 0 to 31. Any data sent on DSTi is overwritten on the selected timeslots before being output to TTIP/TRNG. The same sequence is available to replace received data on any combination of DSTo channels. This is accomplished by setting the RRSTn control register bit for the corresponding channel.

PCM 30 Payload Data								
Hex	**Bit 1**	**Bit 2**	**Bit 3**	**Bit 4**	**Bit 5**	**Bit 6**	**Bit 7**	**Bit 8**
34	0	0	1	1	0	1	0	0
21	0	0	1	0	0	0	0	1
21	0	0	1	0	0	0	0	1
34	0	0	1	1	0	1	0	0
B4	1	0	1	1	0	1	0	0
A1	1	0	1	0	0	0	0	1
A1	1	0	1	0	0	0	0	1
B4	1	0	1	1	0	1	0	0

Table 35 - E1 A-Law Digital Milliwatt Pattern

17.4 E1 Alarms

The MT9071 is capable of detecting and transmitting numerous alarms. The status register bits provide real time status of the alarm, while the latched status registers provide a latched status indication and are cleared when read. The interrupt status registers also provide a latched status indication if unmasked, are also cleared when read and each interrupt status register may also generate a maskable interrupt (if unmasked). Note that reading either the latched or interrupt status register will clear both of these registers. See the register bit descriptions in the tables listed in Table 36 - E1 Alarms and Timers Register Summary for complete details. The persistent status registers provide latched status indication which is only cleared when read while the real time status register bit is not set.

Description	Receiver Status, Interrupt and Persistent Register and Bit				
	Status	**Latched Status**	**Interrupt Status**	**Interrupt Mask**	**Persistent Status**
	Table 109 - E1 Alarms & MAS Status - R Address Y12	**Table 133 - E1 Sync Latched Status - R Address Y24**	**Table 150 - E1 Sync Interrupt Status - R Address Y34**	**Table 157 - E1 Sync Interrupt Mask - R/W Address Y44**	**Table 138 - E1 Persistent Latched Status - R Address Y27**
Remote Alarm Indication	RAI	RAIL	RAII	RAIM	RAIP
Alarm Indication Signal	AIS	AISL	AISI	AISM	AISP
Alarm Indication Signal 100ms	KLVE	NA	NA	NA	NA
Ch. 16 Alarm Indication Signal	AIS16	AIS16L	AIS16I	AIS16M	NA
Auxiliary Pattern	AUXP	AUXPL	AUXPI	AUXPM	NA
Loss of Signal	LOSS	LOSSL	LOSSI	LOSSM	LOSSP
Remote Signaling Multiframe Alarm	Y	YL	YI	YM	NA
Description	Status	Latched Status	Interrupt Status	Interrupt Mask	
	Table 107 - E1 CRC-4 Timers & CRC-4 Local Status - R Address Y11	Table 137 - E1 National Latched Status - R Address Y26	Table 154 - E1 National Interrupt Status - R Address Y36	Table 161 - E1 National Interrupt Mask - R/W Address Y46	
T1 Timer	T1	T1L	T1I	T1M	
T2 Timer	T2	T2L	T2I	T2M	
Description	Transmitter Control Register and Bit				
	Table 79 - E1 Alarms and Framing Control - R/W Address Y00				
AIS Select	ASEL				
Automatic RAI Operation	ARAI				
Transmit Remote Alarm	TALM				
Transmit All Ones	TAIS				
Transmit All Ones in Timeslot 0	TAIS0				
Transmit All Ones in Timeslot 16	TAIS16				

Table 36 - E1 Alarms and Timers Register Summary

17.4.1 E1 Automatic Alarms

The transmission of a remote alarm indication signal (RAI) and signaling multiframe alarms can be made to function automatically with control register bits ARAI and AUTY detailed in Table 79 - E1 Alarms and Framing Control - R/W Address Y00. When ARAI = 0 and basic frame synchronization is lost ($\overline{\text{BSYNC}}$ = 1 in Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10), the MT9071 will automatically transmit the RAI alarm signal to the far end of the link. The transmission of this alarm signal will cease when basic frame alignment is acquired.

When AUTY = 0 and signaling multiframe alignment is not acquired ($\overline{\text{MSYNC}}$ = 1 in Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10), the MT9071 will automatically transmit the

multiframe alarm (Y-bit) signal to the far end of the link. This transmission will cease when signaling multiframe alignment is acquired.

18.0   T1 & E1 Interrupts

The MT9071 has an extensive suite of interrupts consisting of one maskable interrupt vector and 16 maskable interrupt status registers. See Figure 15 - T1 & E1 Interrupt Registers Overview. The set bits in the interrupt vector identify which of the 16 interrupt status registers are responsible for the interrupt. Reading the corresponding interrupt status registers identifies the exact source of the interrupt. Any set bit in the interrupt vector causes the IRQ pin to toggle low, providing the SPND bit is not enabled (see Section 18.1.1 T1 & E1 Interrupt Related Control Bits and Pins).

18.1 T1 & E1 Interrupt Status Register Overview

All 16 interrupt status registers are maskable with 16 corresponding interrupt mask registers. All interrupt status registers and all interrupt mask registers are 16 bit, although all 16 bits are not always used. Unused status register bits are zero if read.

When an unmasked interrupt occurs, one or more bits of the 16 interrupt status registers will go high causing one or more bits of the unmasked interrupt vector to go high. A high bit in the interrupt vector causes the output $\overline{IRQ}$ pin to go low. After an interrupt status register is read, it is automatically cleared. After all interrupt status registers are cleared, the interrupt vector is cleared causing the $\overline{IRQ}$ pin to return to a high impedance state.

If a new unmasked interrupt occurs while the interrupt status registers from a previous interrupt are being read, the affected interrupt status registers will be updated, the interrupt vector will be updated, and the $\overline{IRQ}$ pin will remain low until the interrupt vector is cleared (which occurs when all interrupt status registers are cleared).

If the interrupt status registers are unmasked, and the interrupt vector is masked, then the interrupt status registers will function normally but the interrupt vector status register will remain low and the $\overline{IRQ}$ pin will be in a high impedance state.

18.1.1   T1 & E1 Interrupt Related Control Bits and Pins

$\overline{SPND}$ - All interrupts for a particular transceiver may be suspended without changing the interrupt mask words, by setting the $\overline{SPND}$ control register bit to zero. For T1 mode see Table 178 - T1 Interrupt and I/O Control - R/W Address YF1. For E1 mode see Table 83 - E1 Interrupts and I/O Control - R/W Address Y02. All unmasked interrupt status registers will continue to be updated (and will be cleared when read), and the interrupt vector status register will continue to reflect the status of the interrupt status register bits. However, the transceivers with the $\overline{SPND}$ bits set to zero will not toggle the $\overline{IRQ}$ pin. If all four transceivers $\overline{SPND}$ bits are zero, then none of the transceivers can toggle the IRQ pin.

$\overline{INTA}$ - All interrupt status registers for a particular transceiver may be cleared (without reading the interrupt status registers) by setting the $\overline{INTA}$ control register bit to zero. For T1 mode see Table 178 - T1 Interrupt and I/O Control - R/W Address YF1. For E1 mode see Table 83 - E1 Interrupts and I/O Control - R/W Address Y02. Interrupt status registers for a particular transceiver will be cleared (and not updated) as long as $\overline{INTA}$ is low. Consequently, the selected transceivers interrupt vector bits will remain at zero, therefore that transceiver will not toggle the $\overline{IRQ}$ pin.

$\overline{TAIS}$ - During initial power up, all (4 transceivers) interrupt status registers are cleared without changing the interrupt mask words, when the $\overline{TAIS}$ control pin is held low. Consequently, the interrupt vector will remain clear and the $\overline{IRQ}$ pin will remain in a high impedance state. This allows for system initialization without spurious interrupts.   Interrupt status registers will not be updated, and the $\overline{IRQ}$ pin will be forced to a high impedance state as long as TAIS is low.

$\overline{RESET}$ **or RSTC or RST** - After a MT9071 reset, all interrupt status register bits are unmasked, but the $\overline{SPND}$ and $\overline{INTA}$ control register bits are set to zero.

Latched Status Registers - Reading the latched status registers also clears the corresponding interrupt status register. See Figure 15 - T1 & E1 Interrupt Registers Overview.
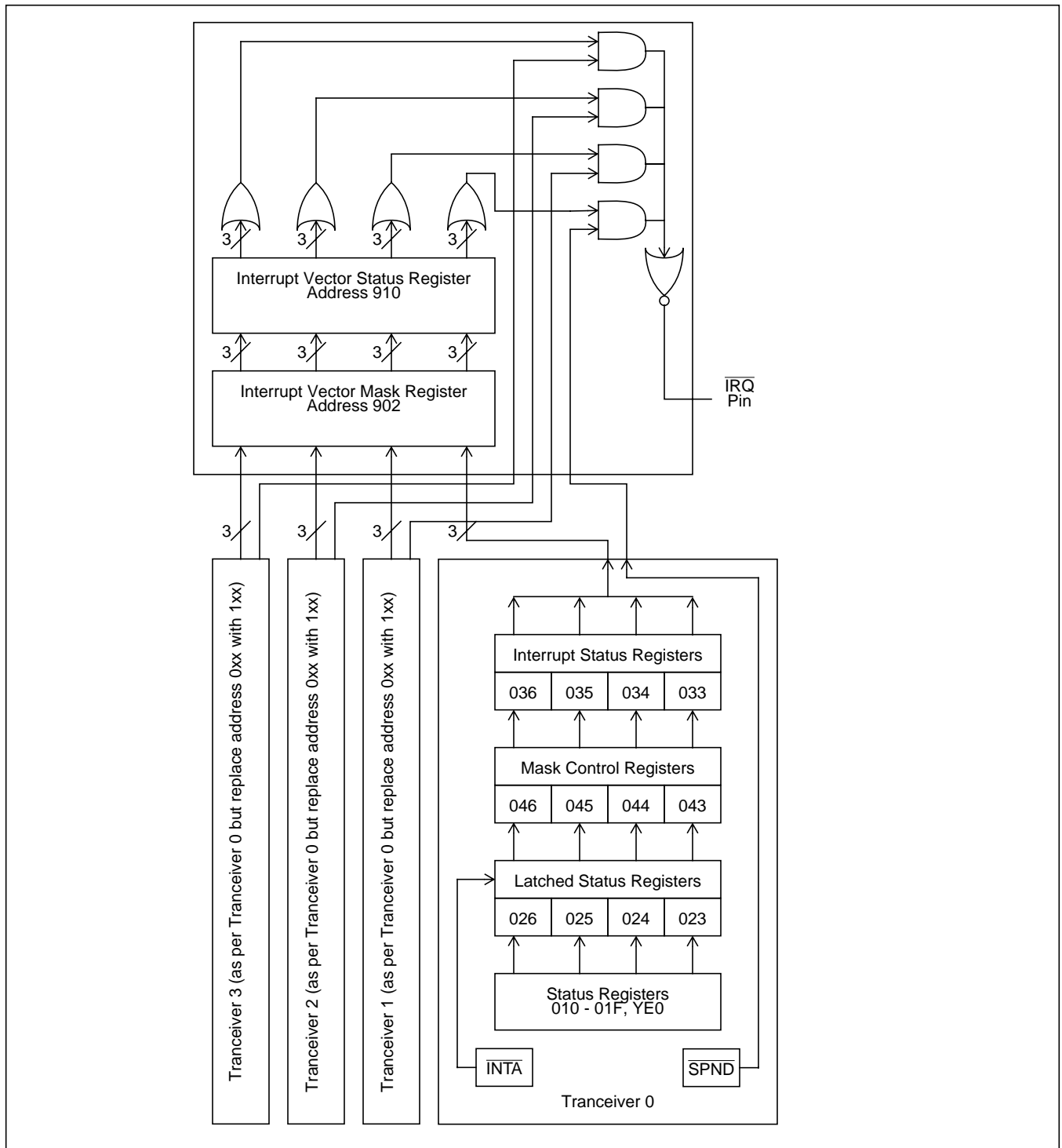

Figure 15 - T1 & E1 Interrupt Registers Overview

18.2 T1 & E1 Interrupt Servicing Methods

There are three common methods for identifying the source of the interrupt. The Polling Method is the simplest but uses the most processor time. The Vector Method requires a two step process, but uses the least amount of processor time. The Timer Polling Method interrupts the processor once a second using an internal timer.

18.2.1 T1 & E1 Polling Method

The $\overline{\text{IRQ}}$ pin goes low.

1. Read all 16 interrupt status registers. The set bits in these registers identify the source of the interrupt. As each register is read, it is cleared (all bits set to 0). When all registers are clear, the interrupt is cleared (the $\overline{\text{IRQ}}$ pin returns to logic high) and all sources of the interrupt are identified. Service the interrupt as each register is read, or all at once, after all registers are read and the interrupt is cleared.

18.2.2 T1 & E1 Vector Method

The $\overline{\text{IRQ}}$ pin goes low.

1. Read the interrupt vector. This vector identifies which of the 16 (or which combination of 16) interrupt status registers has a set bit.

2. Read the interrupt status register(s) identified in step 1. The set bits in these registers identify the source of the interrupt. Note that if multiple transceivers (i.e. transceiver 1 and 3), or multiple conditions caused the interrupt, more than one register may need to be read. As each register is read, it is cleared (all bits set to 0). When all interrupt status registers are cleared, the interrupt vector goes to zero and the $\overline{\text{IRQ}}$ pin returns to logic high. Service the interrupt as each register is read, or all at once, after all registers are read and the interrupt is cleared.

18.2.3 T1 & E1 Timer Polling Method

The $\overline{\text{IRQ}}$ pin goes low.

1. The one second timer caused the interrupt as this is the only unmasked interrupt bit, read the timer interrupt status register to clear the source of the interrupt.

2. Read the desired latched status registers (all the interrupt status registers are all masked except for the timer). Service the interrupt as each register is read, or all at once, after all registers are read.

18.2.4 T1 & E1 Hints

In some applications, a logic low at the $\overline{\text{IRQ}}$ pin lasting the full duration of the interrupt service routine may be undesirable. In these cases, immediately following the interrupt, set the control register bit $\overline{\text{SPND}}$ low until the interrupt service routine is finished.

18.3 T1 & E1 Interrupt Vector and Source Summary

Interrupt Vector Status		Interrupt Vector Mask		Latch Status, Interrupt Status and Interrupt Mask Register Source				
Bit Number	Bit Name	Bit Number	Bit Name	Latch Address	Status Address	Mask Address	Register Name	Tranceiver
Table 74 - T1 Interrupt Vector Status - R Address 910		Table 71 - T1 Interrupt Vector Mask - R/W Address 902		T1 Tranceiver (unique to T1 mode only)				
14	X3EI	14	X3EM	326	336	346	Elastic	3
13	X3RI	13	X3RM	325	335	345	Receive	3
12	X3SI	12	X3SM	324	334	344	Sync	3
10	X2EI	10	X2EM	226	236	246	Elastic	2
9	X2RI	9	X2RM	225	235	245	Receive	2
8	X2SI	8	X2SM	224	234	244	Sync	2
6	X1EI	6	X1EM	126	136	146	Elastic	1
5	X1RI	5	X1RM	125	135	145	Receive	1
4	X1SI	4	X1SM	124	134	144	Sync	1
2	X0EI	2	X0EM	026	036	046	Elastic	0
1	X0RI	1	X0RM	025	035	045	Receive	0
0	X0SI	0	X0SM	024	034	044	Sync	0
Table 75 - E1 Interrupt Vector Status - R Address 910		Table 72 - E1 Interrupt Vector Mask - R/W Address 902		E1 Tranceiver (unique to E1 mode only)				
14	X3NI	14	X3NM	326	336	346	National	3
13	X3CI	13	X3CM	325	335	345	Counter	3
12	X3SI	12	X3SM	324	334	344	Sync	3
10	X2NI	10	X2NM	226	236	246	National	2
9	X2SI	9	X2SM	225	235	245	Counter	2
8	X2CI	8	X2CM	224	234	244	Sync	2
6	X1NI	6	X1NM	126	136	146	National	1
5	X1SI	5	X1SM	125	135	145	Counter	1
4	X1CI	4	X1CM	124	134	144	Sync	1
2	X0NI	2	X0NM	026	036	046	National	0
1	X0SI	1	X0SM	025	035	045	Counter	0
0	X0CI	0	X0CM	024	034	044	Sync	0
T1 & E1 HDLC (common for either T1 or E1 mode)								
15	X3HI	15	X3HM	323	333	343	HDLC	3
11	X2HI	11	X2HM	223	233	243	HDLC	2
7	X1HI	7	X1HM	123	133	143	HDLC	1
3	X0HI	3	X0HM	023	033	043	HDLC	0

Table 37 - T1 & E1 Interrupt Vector and Source Summary

For a detailed description of the events triggering an interrupt, refer to the latch register descriptions at the address locations listed above.

19.0 T1 & E1 Transceiver Address Space

The most significant nibble of the address space is used to either access registers common to all four transceivers (referred to as global registers), or to access individual transceiver registers (referred to as unique registers). See Table 38 - T1 & E1 Tranceiver Registers Address Space Summary.

Access to transceiver global registers is when the most significant nibble of the address is "9".

Access to transceiver unique registers is when the most significant nibble (Y) of the address is either "0", "1", "2", or "3" to access transceiver "0", "1", "2" or "3" respectively. Also, when "Y" is "8", all four transceivers unique registers are simultaneously accessed with a common write.

The unique register group for T1 mode is different from the unique register group for E1 mode with the exception of the HDLCs and some LIU registers.

For T1 & E1 HDLC's, see Table 40 - T1 & E1 Unique HDLC Register Group Address Space.
For T1 & E1 LIU's, see Table 41 - T1 & E1 Unique LIU Register Group Address Space.
For T1 mode, see Table 42 - T1 Unique Framer Register Group Address Space.
For E1 mode, see Table 43 - E1 Unique Framer Register Group Address Space.

Hex Address $(A_{11}\text{-}A_0)$	Tranceiver Accessed	Registers Accessed
000-0FF	Tranceiver 0	All T1 & E1 Unique Transceiver Control, Status and Data Registers
100-1FF	Tranceiver 1	
200-2FF	Tranceiver 2	
300-3FF	Tranceiver 3	
800-8FF	All Tranceivers (0-3)	All T1&E1 Unique Transceiver Control and Data Registers-Write Mode Only
900-91F	All Tranceivers (0-3)	All T1 & E1 Global Transceiver Control and Status Registers
Note: address space 400-7FF and 920-FFF is not used		

Table 38 - T1 & E1 Tranceiver Registers Address Space Summary

19.1 T1 & E1 Transceiver Register Group Address Space Summaries 900-914 & Y00-YFA

	Hex Address $(A_{11}\text{-}A_0)$	Register
Table 44	Address 900, 902, 905, 906	T1 & E1 Global Transceiver Control Registers
Table 45	Address 910-914	T1 & E1 Global Transceiver Status Registers

Table 39 - T1 & E1 Global Transceiver Control & Status Register Group Address Space

	Hex Address $(A_{11}\text{-}A_0)$	Register
Table 46	Address Y1C-Y1F	T1 & E1 HDLC Status Registers
Table 47	Address Y23, Y33 & Y43	T1 & E1 HDLC Latched and Interrupt and Mask Registers
Table 48	Address YF2-YF6	T1 & E1 HDLC Control Registers

Table 40 - T1 & E1 Unique HDLC Register Group Address Space

	Hex Address $(A_{11}\text{-}A_0)$	Register
Table 49	Address YE0-YE1	T1 & E1 LIU Status Registers
Table 50	Address YE2-YE6	T1 & E1 LIU Control Registers

Table 41 - T1 & E1 Unique LIU Register Group Address Space

	Hex Address $(A_{11}\text{-}A_0)$	Register
Table 51	Address Y00-Y0F	T1 Master Control 1 Registers
Table 52	Address YF0,YF1,YF7	T1 Master Control 2 Registers
Table 53	Address Y10-Y1A	T1 Master Status Registers
Table 54	Address Y24-Y2C	T1 Latched Status Registers
Table 55	Address Y34-Y36	T1 Interrupt Status Registers
Table 56	Address Y44-Y46	T1 Interrupt Mask Registers
Table 57	Address Y50-Y67	T1 Transmit CAS Data Registers
Table 58	Address Y70-Y87	T1 Receive CAS Data Registers
Table 59	Address Y90-YA7	T1 Channel 1 to 24 Control Registers

Table 42 - T1 Unique Framer Register Group Address Space

	R/W Hex Address $(A_{11}\text{-}A_0)$	Register
Table 60	Address Y00-Y0A	E1 Master Control 1 Register Bit Summary
Table 61	Address Y10-Y1A	E1 Master Status Register Bit Summary
Table 62	Address Y24-Y2B	E1 Latched Status Register Bit Summary
Table 63	Address Y34-Y36	E1 Interrupt Status Register Bit Summary
Table 64	Address Y44-Y46	E1 Interrupt Mask Register Bit Summary
Table 65	Address Y51-Y5F, Y61-Y6F	E1 Transmit CAS Data Register Bit Summary
Table 66	Address Y71-Y7F, Y81-Y8F	E1 Receive CAS Data Register Bit Summary
Table 67	Address Y91-YAF	E1 Timeslot 0-31 Control Register Bit Summary
Table 68	Address YB0-YB4	E1 Transmit National Bits Data Register Bit Summary
Table 69	Address YC0-YC4	E1 Receive National Bits Data Register Bit Summary

Table 43 - E1 Unique Framer Register Group Address Space

20.0 T1 & E1 Transceiver Registers Bit Summaries

A "#" in the "Register Bits" column of these tables indicates that the corresponding data bit may have a logic state of 0 or 1 after a reset ($\overline{\text{RESET}}$, RSTC or RST).

20.1 T1 & E1 Global Transceiver Registers Bit Summary - Address 900-914

Tables 44 & 45 describe the bit summary for each of the T1 & E1 Global Registers in the MT9071.

	Hex Address (A_{11}-A_0)	R/W	Register	Register Bits (B15-B8 / B7-B0)
Table 70	900	R/W	T1 & E1 Global Mode Control	T1E0, RSV, ESEL1-0, ACC3-0, ACF2-0, CK1-0, PSLP, RSTP, RSTC
Table 71	902	R/W	T1 Interrupt Vector Mask	X3HM, X3EM, X3RM, X3SM, X2HM, X2EM, X2RM, X2SM, X1HM, X1EM, X1RM, X1SM,X0HM, X0EM, X0RM X0SM
Table 72	902	R/W	E1 Interrupt Vector Mask	X3HM, X3NM, X3CM, X3SM, X2HM, X2NM, X2CM, X2SM, X1HM, X1NM, X1CM, X1SM, X0HM, X0NM, X0CM, X0SM
Table 73	905	R/W	T1 & E1 Global Timing Control	PR2-0, SR2-0, FS2-1, MS2-1, RSEL, TIER, TIEE, $\overline{\text{BUSM}}$, $\overline{\text{ESYNI}}$, FLOCK

Table 44 - T1 & E1 Global Transceiver Control Registers - Address 900, 902, 905, 906

	Hex Address (A_{11}-A_0)	R/W	Register	Register Bits (B15-B8 / B7-B0)
Table 74	910	R	T1 Interrupt Vector Status	X3HI, X3EI, X3RI, X3SI, X2HI, X2EI, X2RI, X2SI, X1HI, X1EI, X1RI, X1SI,X0HI, X0EI, X0RI X0SI
Table 75	910	R	E1 Interrupt Vector Status	X3HI, X3NI, X3CI, X3SI, X2HI, X2NI, X2CI, X2SI, X1HI, X1NI, X1CI, X1SI, X0HI, X0NI, X0CI, X0SI
Table 76	912	R	T1 & E1 ID Rev Code Data	ID15-8, ID7-0
Table 77	914	R	T1 & E1 Global Status	#, #, #, #, #, #, #, #, #, #, #, #, #, #, #, AHLD

Table 45 - T1 & E1 Global Transceiver Status Registers - Address 910-914

20.2 T1 & E1 Unique HDLC Registers Bit Summary - Address Y1C-Y1F, Y23, Y33, Y43, YF2-YF6

Tables 46 - 48 describe the bit summary for each of the T1 & E1 Unique HDLC Registers in the MT9071.

	Hex Address (A_{11}-A_0)	R/W	Register	Register Bits (B15-B8 / B7-B0)
Table 127	Y1C	R/W	T1 & E1 HDLC Test and Transmit Byte Status	#, #, #, #, RXCLK, TXCLK, VCRC, VADDR, TBP7-0
Table 128	Y1D	R/W	T1 & E1 HDLC Status	#, #, #, #, #, #, #, #, #, IDC, RQ9-8, TFS2-1, RFS2-1
Table 129	Y1E	R/W	T1 & E1 HDLC Receive CRC Data	CRC15-0
Table 130	Y1F	R/W	T1 & E1 HDLC Receive FIFO Data	#, #, #, #, #, #, #, #, RXF7-0

Table 46 - T1 & E1 HDLC Status Registers - Address Y1C-Y1F

	Hex Address (A_{11}-A_0)	R/W	Register	Register Bits (B15-B8 / B7-B0)
Table 131	Y23	R/W	T1 & E1 HDLC Latched Status	#, #, #, #, #, #, #, GAL, EOPDL, TEOPL, EOPRL, TXFLL, FAL, TXFEL, RXFHL, RXFOL
Table 148	Y33	R	T1 & E1 HDLC Interrupt Status	#, #, #, #, #, #, #, GAI, EOPDI, TEOPI, EOPRI, TXFLI, FAI, TXFEI, RXFHI, RXFOI
Table 155	Y43	R/W	T1 & E1 HDLC Interrupt Mask	#, #, #, #, #, #, #, GAM, EOPDM, TEOPM, EOPRM, TXFLM, FAM, TXFEM, RXFHM, RXFOM

Table 47 - T1 & E1 HDLC Latched and Interrupt and Mask Registers - Address Y23, Y33 & Y43

	Hex Address (A_{11}-A_0)	R/W	Register	Register Bits (B15-B8 / B7-B0)
Table 179	YF2	R/W	T1 & E1 HDLC Control 0	#, #, #, #, #, ADREC, RXEN, TXEN, EOP, FA, MRKID, CYCLE, TCRCI, SEVEN, RXFRST, TXFRST
Table 180	YF3	R/W	T1 & E1 HDLC Control 1	#, #, #, #, #, #, #, #, #, #, HRST, RTLOOP, CRCTST, FTST, ADTST, HLOOP
Table 181	YF4	R/W	T1 & E1 HDLC Address Recognition Control	ADR26-20, A2EN, ADR16-10, A1EN
Table 182	YF5	R/W	T1 & E1 HDLC Transmit FIFO Data	#, #, #, #, #, #, #, #, TXF7-0
Table 183	YF6	R/W	T1 & E1 HDLC Transmit Packet Size	#, #, #, #, #, #, #, #, TPS7-0

Table 48 - T1 & E1 HDLC Control Registers - Address YF2-YF6

20.3 T1 & E1 Unique LIU Registers Bit Summary - Address YE0-YE4

Tables 49 & 50 describe the bit summary for each of the T1 & E1 Unique LIU Registers in the MT9071.

	Hex Address (A_{11}-A_0)	R/W	Register	Register Bits (B15-B8 / B7-B0)
Table 170	YE0	R	T1 & E1 LIU and JA Status	LLOS, PD6-0, #, JACS, JACF, JAE, JAF4, JAFC, JAE4, JAF
Table 171	YE1	R/W	T1 & E1 LIU Receive Peak Detector Status	APD7-0, EPD7-0

Table 49 - T1 & E1 LIU Status Registers - Address YE0-YE1

	Hex Address (A_{11}-A_0)	R/W	Register	Register Bits (B15-B8 / B7-B0)
Table 172	YE2	R/W	T1 & E1 LIU Transmitter Control	#, $\overline{\text{PDLY}}$, TXEN, WRAT, CPL, TXL2-0, JAS, JFC, JFD2-0, JACL, OPTCOR1, OPTCOR0
Table 173	YE3	R/W	T1 & E1 LIU Control	#, #, #, #, #, #, RLBK, MLBK, #, #, ELOS, REQC1-0, REQM2-0
Table 174	YE4	R/W	T1 & E1 LIU Transmit Pulse Phase 1 & Phase 2 Data	RSV, C1P6-0, RSV, C2P6-0
Table 175	YE5	R/W	T1 & E1 LIU Transmit Pulse Phase 3 & Phase 4 Data	RSV, C3P6-0, RSV, C4P6-0
Table 176	YE6	R/W	T1 & E1 LIU Receive Equalizer Threshold Control	EHT7-0, ELT7-0

Table 50 - T1 & E1 LIU Control Registers - Address YE2-YE6

20.4 T1 Unique Framer Registers Bit Summary - Address Y00- YF7

Tables 51 and 52 describe the bit summary for each of the T1 Unique Framer Registers in the MT9071.

	Hex Address (A_{11}-A_0)	R/W	Register	Register Bits (B15-B8 / B7-B0)
Table 78	Y00	R/W	T1Framing Mode Control	RSV, #, G802, JY, TRANSP, T1DM, ESF, RSV, CXC, RS1-0, FSI, REFR, MFREFR, JTS, TXSYNC
Table 80	Y01	R/W	T1 Line Coding Control	#, #, #, #, RZCS1-0, TZCS2-1, TZCS0, TPDV, TXB8ZS, RXB8ZS, ADSEQ, RZNRZ, UNIBI, CLKE
Table 82	Y02	R/W	T1 Transmit Alarm Control	#, #, #, #, #, #, #, #, TESFY, TXSECY, TD4Y, $\overline{\text{TAIS}}$, #, $\overline{\text{TT1DMY}}$, D4SECY, SO
Table 84	Y03	R/W	T1 Transmit Error Control	#, #, #, #, #, #, #, #, L32Z, BPVE, CRCE, FTE, FSE, LOSE, PERR
Table 86	Y04	R/W	T1 Signaling Control	#, #, #, #, #, #, CSIGEN, RBEN, #, RSDB, RFL, #, SM1-0, SIP1-0
Table 88	Y05	R/W	T1 LoopBack Control	#, #, #, #, #, #, #, #, #, #, DLBK, RSV, SLBK, PLBK, TLU, TLD
Table 90	Y06	R/W	T1 HDLC & DataLink Control	#, #, #, #, HCH4-1, HCH0, HPAYSEL, RSV, RSV, RSV, BOMEN, HDLCEN, H1R64
Table 92	Y07	R/W	T1 Transmit BOM Data	#, #, #, #, #, #, #, #, TXBOM7-0
Table 94	Y08	R/W	T1 Receive BOM Match Control	#, #, #, #, #, #, #, #, RXBOMM7-0
Table96	Y09	R/W	T1 Receive Idle Code Data	#, #, #, #, #, #, #, #, RXIDC7-0
Table 98	Y0A	R/W	T1 Transmit Idle Code Data	#, #, #, #, #, #, #, #, TXIDC7-0
Table 100	Y0B	R/W	T1 CCS Map Control	#, #, #, #, #, #, CST4-3, CST2-0, PCM4-0
Table 101	Y0D	R/W	T1 Transmit Loop Activate Code Control	#, #, #, #, #, #, TXLACL1-0, TXLAC7-0
Table 102	Y0E	R/W	T1 Transmit Loop Deactivate Code Control	#, #, #, #, #, #, TXLDCL1-0, TXLDC7-0
Table 103	Y0F	R/W	T1 Receive Loop Activate Code Match Control	#, #, #, #, #, #, RXLACL1-0, RXLACM7-0

Table 51 - T1 Master Control 1 Registers - Address Y00-Y0F

	Hex Address (A_{11}-A_0)	R/W	Register	Register Bits (B15-B8 / B7-B0)
Table 177	YF0	R/W	T1 Receive Loop Deactivate Code Match	#, #, #, #, #, #, RXLDCL1-0, RXLDCM7-0
Table 178	YF1	R/W	T1 Interrupt and I/O Control	#, #, #, #, #, TX8KE, $\overline{\text{RXDO}}$, TXMFSEL, $\overline{\text{SPND}}$, $\overline{\text{INTA}}$, DSTOE, CSTOE, $\overline{\text{RXCO}}$, CNCLR, ACCLR, RST
Table 184	YF7	R/W	T1 Transmit Elastic Buffer Set Delay	#, #, #, #, #, #, #, #, TXSD7-0

Table 52 - T1 Master Control 2 Registers - Address YF0,YF1,YF7

	Hex Address (A_{11}-A_0)	R/W	Register	Register Bits (B15-B8 / B7-B0)
Table 104	Y10	R	T1 Synchronization and Alarm Status	#, #, $\overline{\text{TFSYNC}}$, $\overline{\text{MFSYNC}}$, SEF, LOS, D4Y, D4Y48, SECY, ESFY, AIS, PDV, LLED, LLDD, T1DMR, $\overline{\text{T1DMY}}$
Table 106	Y11	R	T1 Timer Status	#, #, #, #, #, #, #, #, #, #, #, #, #, ONESEC, TWOSEC, #
Table 108	Y12	R	T1 Receive Bit Oriented Message	#, #, #, #, #, RXBOM, RXBOMM, RXBOM7-0
Table 110	Y13	R	T1 Receive Elastic Buffer Status	#, #, RXP2-0, RSLPD, RSLP, RXFRM, RXTS4-0, RXBC2-0
Table 112	Y14	R	T1 Transmit Elastic Buffer Status	#, #, #, #, #, TSLP, TSLPD, TXFRM, TXTS4-0, TXBC2-0
Table 114	Y15	R/W	T1 PRBS CRC Multiframe and PRBS Error Counter	PCC7-0, PEC7-0
Table 116	Y16	R/W	T1 Multiframe Out of Frame Counter	MFC15-0
Table 118	Y17	R/W	T1 Framing Bit Error Counter	BEC15-0
Table 120	Y18	R/W	T1 Bipolar Violation Counter	VEC15-0
Table 122	Y19	R/W	T1 CRC-6 Error Counter	CEC15-0
Table 124	Y1A	R/W	T1 Out of Frame and Change of Frame Counters	OFC7-0, CFC7-0
Table 126	Y1B	R/W	T1 Excessive Zeros Counter	#, #, #, #, #, #, #, #, EZC7-0

Table 53 - T1 Master Status Registers - Address Y10-Y1A

	Hex Address (A_{11}-A_0)	R/W	Register	Register Bits (B15-B8 / B7-B0)
Table 132	Y24	R	T1 Receive Sync and Alarm Latch	BEOL, CEOL, OFOL, CFOL, VEOL, PEOL, PCOL, MFOL, TFSYNL, MFSYNL, BEIL, CFIL, SEFL, AISL, CEIL, LOSL
Table134	Y25	R	T1 Receive Line Status and Timer Latch	D4YL, D4Y48L, SECYL, ESFYL, T1DMYL, #, VEIL, PEIL, PDVL, LLEDL, LLDDL, BOML, BOMML, CASRL, ONESECL, TWOSECL
Table 136	Y26	R	T1 Elastic Store Status Latch	#, #, #, #, #, #, #, #, #, #, #, #, EZOL, EZIL, TSLPL, RSLPL
Table 139	Y28	R	T1 Framing Bit Error Counter Latch	BEL15-0,
Table 141	Y29	R	T1 Bipolar Violation Error Counter Latch	VEL15-0
Table 143	Y2A	R	T1 CRC-6 Error Counter Latch	CEL15-0
Table 145	Y2B	R	T1 Out of Frame & Change of Frame Counter Latch	OFL7-0, CFL7-0
Table 147	Y2C	R	T1 Multiframe Out of Frame Counter Latch	MFL15-0

Table 54 - T1 Latched Status Registers - Address Y24-Y2C

	Hex Address (A$_{11}$-A$_0$)	R/W	Register	Register Bits (B15-B8 / B7-B0)
Table 149	Y34	R	T1 Receive and Sync Interrupt Status	BEOI, CEOI, OFOI, CFOI, VEOI, PEOI, PCOI, MFOI, TFSYNI, MFSYNI, BEII, CFII, SEFI, AISI, CEII, LOSI
Table 151	Y35	R	T1 Receive Line and Timer Interrupt Status	D4YI, D4Y48I, SECYI, ESFYI, T1DMYI, #, VEII, PEII, PDVI, LLEDI, LLDDI, BOMI, BOMMI, CASRI, ONESECI, TWOSECI
Table 153	Y36	R	T1 Elastic Store Interrupt Status	#, #, #, #, #, #, #, #, #, #, #, #, EZOI, EZII, TSLPI, RSLPI

Table 55 - T1 Interrupt Status Registers - Address Y34-Y36

	Hex Address (A$_{11}$-A$_0$)	R/W	Register	Register Bits (B15-B8 / B7-B0)
Table 156	Y44	R/W	T1 Receive and Sync Interrupt Mask	BEOM, CEOM, OFOM, CFOM, VEOM, PEOM, PCOM, MFOM, TFSYNM, MFSYNM, BEIM, CFIM, SEFM, AISM, CEIM, LOSM
Table 158	Y45	R/W	T1 Receive Line and Timer Interrupt Mask	D4YM, D4Y48M, SECYM, ESFYM, T1DMYM, #, VEIM, PEIM, PDVM, LLEDM, LLDDM, BOMM, BOMMM, CASRM, ONESECM, TWOSECM
Table 160	Y46	R/W	T1 Elastic Store Interrupt Mask	#, #, #, #, #, #, #, #, #, #, #, #, EZOM, EZIM, TSLPM, RSLPM

Table 56 - T1 Interrupt Mask Registers - Address Y44-Y46

Hex Address (A$_{11}$-A$_0$)	Register	Register Bits (B15-B0)
Y50	T1 Channel 1 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA1, TB1, TC1, TD1
Y51	T1 Channel 2 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA2, TB2, TC2, TD2
Y52	T1 Channel 3 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA3, TB3, TC3, TD3
Y53	T1 Channel 4 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA4, TB4, TC4, TD4
Y54	T1 Channel 5 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA5, TB5, TC5, TD5
Y55	T1 Channel 6 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA6, TB6, TC6, TD6
Y56	T1 Channel 7 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA7, TB7, TC7, TD7
Y57	T1 Channel 8 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA8, TB8, TC8, TD8
Y58	T1 Channel 9 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA9, TB9, TC9, TD9
Y59	T1 Channel 10 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA10, TB10, TC10, TD10
Y5A	T1 Channel 11 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA11, TB11, TC11, TD11
Y5B	T1 Channel 12 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA12, TB12, TC12, TD12
Y5C	T1 Channel 13 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA13, TB13, TC13, TD13
Y5D	T1 Channel 14 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA14, TB14, TC14, TD14
Y5E	T1 Channel 15 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA15, TB15, TC15, TD15
Y5F	T1 Channel 16 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA16, TB16, TC16, TD16
Y60	T1 Channel 17 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA17, TB17, TC17, TD17
Y61	T1 Channel 18 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA18, TB18, TC18, TD18

Table 57 - T1 Transmit CAS Data Registers - Address Y50-Y67

Hex Address (A$_{11}$-A$_0$)	Register	Register Bits (B15-B0)
Y62	T1 Channel 19 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA19, TB19, TC19, TD19
Y63	T1 Channel 20 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA20, TB20, TC20, TD20
Y64	T1 Channel 21 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA21, TB21, TC21, TD21
Y65	T1 Channel 22 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA22, TB22, TC22, TD22
Y66	T1 Channel 23 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA23, TB23, TC23, TD23
Y67	T1 Channel 24 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA24, TB24, TC24, TD24
Refer to Table 162 - T1 Transmit CAS Data Registers - R/W Address Y50-Y67		

Table 57 - T1 Transmit CAS Data Registers - Address Y50-Y67

Hex Address (A$_{11}$-A$_0$)	Register	Register Bits (B15-B0)
Y70	T1 Channel 1 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA1, RB1, RC1, RD1
Y71	T1 Channel 2 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA2, RB2, RC2, RD2
Y72	T1 Channel 3 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA3, RB3, RC3, RD3
Y73	T1 Channel 4 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA4, RB4, RC4, RD4
Y74	T1 Channel 5 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA5, RB5, RC5, RD5
Y75	T1 Channel 6 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA6, RB6, RC6, RD6
Y76	T1 Channel 7 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA7, RB7, RC7, RD7
Y77	T1 Channel 8 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA8, RB8, RC8, RD8
Y78	T1 Channel 9 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA9, RB9, RC9, RD9
Y79	T1 Channel 10 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA10, RB10, RC10, RD10
Y7A	T1 Channel 11 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA11, RB11, RC11, RD11
Y7B	T1 Channel 12 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA12, RB12, RC12, RD12
Y7C	T1 Channel 13 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA13, RB13, RC13, RD13
Y7D	T1 Channel 14 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA14, RB14, RC14, RD14
Y7E	T1 Channel 15 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA15, RB15, RC15, RD15
Y7F	T1 Channel 16 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA16, RB16, RC16, RD16
Y80	T1 Channel 17 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA17, RB17, RC17, RD17
Y81	T1 Channel 18 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA18, RB18, RC18, RD18
Y82	T1 Channel 19 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA19, RB19, RC19, RD19
Y83	T1 Channel 20 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA20, RB20, RC20, RD20
Y84	T1 Channel 21 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA21, RB21, RC21, RD21
Y85	T1 Channel 22 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA22, RB22, RC22, RD22
Y86	T1 Channel 23 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA23, RB23, RC23, RD23
Y87	T1 Channel 24 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA24, RB24, RC24, RD24
Refer to Table 164 - T1 Receive CAS Data Registers - R Address Y70-Y87		

Table 58 - T1 Receive CAS Data Registers - Address Y70-Y87

Hex Address (A$_{11}$-A$_0$)	Register	Register Bits (B15-B0)
Y90	T1 Ch 1 Control	#,#,#,#,#,#, RPCI1, MPDR1, MPST1, TPCI1, RTSL1, LTSL1, TTST1, RRST1, MPDT1, CC1
Y91	T1 Ch 2 Control	#,#,#,#,#,#, RPCI2, MPDR2, MPST2, TPCI2, RTSL2, LTSL2, TTST2, RRST2, MPDT2, CC2
Y92	T1 Ch 3 Control	#,#,#,#,#,#, RPCI3, MPDR3, MPST3, TPCI3, RTSL3, LTSL3, TTST3, RRST3, MPDT3, CC3
Y93	T1 Ch 4 Control	#,#,#,#,#,#, RPCI4, MPDR4, MPST4, TPCI4, RTSL4, LTSL4, TTST4, RRST4, MPDT4, CC4
Y94	T1 Ch 5 Control	#,#,#,#,#,#, RPCI5, MPDR5, MPST5, TPCI5, RTSL5, LTSL5, TTST5, RRST5, MPDT5, CC5
Y95	T1 Ch 6 Control	#,#,#,#,#,#, RPCI6, MPDR6, MPST6, TPCI6, RTSL6, LTSL6, TTST6, RRST6, MPDT6, CC6
Y96	T1 Ch 7 Control	#,#,#,#,#,#, RPCI7, MPDR7, MPST7, TPCI7, RTSL7, LTSL7, TTST7, RRST7, MPDT7, CC7
Y97	T1 Ch 8 Control	#,#,#,#,#,#, RPCI8, MPDR8, MPST8, TPCI8, RTSL8, LTSL8, TTST8, RRST8, MPDT8, CC8
Y98	T1 Ch 9 Control	#,#,#,#,#,#, RPCI9, MPDR9, MPST9, TPCI9, RTSL9, LTSL9, TTST9, RRST9, MPDT9, CC9
Y99	T1 Ch 10 Control	#,#,#,#,#,#, RPCI10, MPDR10, MPST10, TPCI10, RTSL10, LTSL10, TTST10, RRST10, MPDT10, CC10
Y9A	T1 Ch 11 Control	#,#,#,#,#,#, RPCI11, MPDR11, MPST11, TPCI11, RTSL11, LTSL11, TTST11, RRST11, MPDT11, CC11
Y9B	T1 Ch 12 Control	#,#,#,#,#,#, RPCI12, MPDR12, MPST12, TPCI12, RTSL12, LTSL12, TTST12, RRST12, MPDT12, CC12
Y9C	T1 Ch 13 Control	#,#,#,#,#,#, RPCI13, MPDR13, MPST13, TPCI13, RTSL13, LTSL13, TTST13, RRST13, MPDT13, CC13
Y9D	T1 Ch 14 Control	#,#,#,#,#,#, RPCI14, MPDR14, MPST14, TPCI14, RTSL14, LTSL14, TTST14, RRST14, MPDT14, CC14
Y9E	T1 Ch 15 Control	#,#,#,#,#,#, RPCI15, MPDR15, MPST15, TPCI15, RTSL15, LTSL15, TTST15, RRST15, MPDT15, CC15
Y9F	T1 Ch 16 Control	#,#,#,#,#,#, RPCI16, MPDR16, MPST16, TPCI16, RTSL16, LTSL16, TTST16, RRST16, MPDT16, CC16
YA0	T1 Ch 17 Control	#,#,#,#,#,#, RPCI17, MPDR17, MPST17, TPCI17, RTSL17, LTSL17, TTST17, RRST17, MPDT17, CC17
YA1	T1 Ch 18 Control	#,#,#,#,#,#, RPCI18, MPDR18, MPST18, TPCI18, RTSL18, LTSL18, TTST18, RRST18, MPDT18, CC18
YA2	T1 Ch 19 Control	#,#,#,#,#,#, RPCI19, MPDR19, MPST19, TPCI19, RTSL19, LTSL19, TTST19, RRST19, MPDT19, CC19
YA3	T1 Ch 20 Control	#,#,#,#,#,#, RPCI20, MPDR20, MPST20, TPCI20, RTSL20, LTSL20, TTST20, RRST20, MPDT20, CC20
YA4	T1 Ch 21 Control	#,#,#,#,#,#, RPCI21, MPDR21, MPST21, TPCI21, RTSL21, LTSL21, TTST21, RRST21, MPDT21, CC21
YA5	T1 Ch 22 Control	#,#,#,#,#,#, RPCI22, MPDR22, MPST22, TPCI22, RTSL22, LTSL22, TTST22, RRST22, MPDT22, CC22
YA6	T1 Ch 23 Control	#,#,#,#,#,#, RPCI23, MPDR23, MPST23, TPCI23, RTSL23, LTSL23, TTST23, RRST23, MPDT23, CC23
YA7	T1 Ch 24 Control	#,#,#,#,#,#, RPCI24, MPDR24, MPST24, TPCI24, RTSL24, LTSL24, TTST24, RRST24, MPDT24, CC24
Refer to Table 166 - T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7		

Table 59 - T1 Channel 1 to 24 Control Registers - Address Y90-YA7

20.5 E1 Unique Framer Registers Bit Summary - Address Y00 - YC4

Tables 79 to 161 describe the bit summary for the E1 Unique Framer Registers in the MT9071.

Binary Address	Hex Address (A_{11}-A_0)	R/W	Register	Register Bits (B15-B8 / B7-B0)
Table 79	Y00	R/W	E1 Alarms and Framing Control	#, ASEL, $\overline{ARAI}$, TALM, TAIS, TAIS0, TAI16, TE, TIU0, TIU1, $\overline{CSYN}$, REFRM, $\overline{AUTC}$, CRCM, $\overline{AUTY}$, MFRF
Table 81	Y01	R/W	E1 Test, Error and Loopback Control	#, #, L32Z, ADSEQ, DLBK, RSV, SLBK, PLBK, E1, E2, BVE, CRCE, FASE, NFSE, LOSE, PERR
Table 83	Y02	R/W	E1 Interrupts and I/O Control	COD1, COD0, $\overline{HDB3}$, T2OP, TXMFE, TX8KE, $\overline{SPND}$, $\overline{INTA}$, CLKE, #, RXBFE, $\overline{RXDO}$, $\overline{RXCO}$, CSTOE, DSTOE, MFSEL
Table 85	Y03	R/W	E1 DL, CCS, CAS and Other Control	#, #, #, #, #, #, #, #, #, $\overline{ELAS}$, ACCLR, RXTRS, TXTRS, CSIG, CNCLR, RST
Table 87	Y04	R/W	E1 Signaling Control	#, #, #, #, #, #, #, #, #, #, #, #, #, #, #, SIP1-0
Table 89	Y05	R/W	E1 CAS Control and Data	#, #, #, #, RFL, DBNCE, #, #, TMA1-4, X1, Y, X2, X3
Table 91	Y06	R/W	E1 HDLC and CCS ST-BUS Control	#, #, #, #, HCH4-1, HCH1, HPAYSEL, RSV, RSV, RSV, TS31E, TS16E, TS15E
Table 93	Y07	R/W	E1 CCS CSTi and CSTo Map Control	#, 31C4-0, 16C4-3, 16C2-0, 15C4-0
Table 95	Y08	R/W	E1 Data Link Control	#, SA4S1-0, SA5S1-0, SA6S1-0, SA7S1, SA7S0, SA8S1-0, #, #, #, RSV, RSV
Table 97	Y09	R/W	E1 Receive Idle Code Data	#, #, #, #, #, #, #, #, RXIDC7-0
Table 99	Y0A	R/W	E1 Transmit Idle Code Data	#, #, #, #, #, #, #, #, TXIDC7-0

Table 60 - E1 Master Control 1 Register Bit Summary - Address Y00-Y0A

Binary Address	Hex Address (A_{11}-A_0)	R/W	Register	Register Bits (B15-B8 / B7-B0)
Table 105	Y10	R	E1 Synchronization & CRC-4 Remote Status	#, RSLP, RSLPD, $\overline{BSYNC}$, $\overline{MSYNC}$, $\overline{CSYNC}$, RED, CEFS, #, RCRC0, RCRC1, RFAIL, REB1-2, RCRCR, CRCIW
Table 107	Y11	R	E1 CRC-4 Timers & CRC-4 Local Status	#, #, ONESEC, TWOSEC, T1, T2, T400, T8, #, #, #, CALN, CRCRF, CRCS1, CRCS2, #
Table 109	Y12	R	E1 Alarms & MAS Status	#, #, KLVE, LOSS, AIS16, AIS, RAI, AUXP, RMA1-4, X1, Y, X2, X3
Table 111	Y13	R	E1 NFAS Signal and FAS Status	RIU1, RNFA, RAI, RNU4-8, RIU0, RFA2-8
Table 113	Y14	R	E1 Phase Indicator Status	#, #, #, #, PI11-0
Table 115	Y15	R/W	E1 PRBS Error Counter & PRBS CRC Multiframe Counter	PEC7-0, PCC7-0
Table 117	Y16	R/W	E1 Loss of Basic Frame Sync Counter	SLC15-0
Table 119	Y17	R/W	E1 E-bit Error Counter	EEC15-0
Table 121	Y18	R/W	E1 Bipolar Violation Error Counter	VEC15-0
Table 123	Y19	R/W	E1 CRC-4 Error Counter	CEC15-0
Table 125	Y1A	R/W	E1 FAS Bit Error Counter & FAS Error Counter	BEC7-0, FEC7-0

Table 61 - E1 Master Status Register Bit Summary - Address Y10-Y1A

Binary Address	Hex Address (A_{11}-A_0)	R/W	Register	Register Bits (B15-B8 / B7-B0)
Table 133	Y24	R	E1 Sync Latched Status	0, RCRCRL, RSLPL, YL, AUXPL, RAIL, AISL, AIS16L, LOSSL, RCRC0L, RCRC1L, CEFSL, RFAILL, CSYNCL, MSYNCL, BSYNCL
Table 135	Y25	R	E1 Counter Latched Status	0, SLOL, FEOL, FEIL, BEOL, BEIL, CEOL, CEIL, VEOL, VEIL, EEOL, EEIL, PCOL, JAL, PEOL, PEIL
Table 137	Y26	R	E1 National Latched Status	0, Sa5VL, Sa6V3L, Sa6V2L, Sa6V1L, Sa6V0L, Sa6N8L, Sa6NL, SaNL, Sa5TL, SaTL, CASRL, CALNL, T2L, T1L, ONESECL
Table 138	Y27	R	E1 Persistent Latched Status	#, #, #, #, #, #, #, #, #, #, #, #, RAIP, AISP, LOSSP, BSYNCP
Table 140	Y29	R	E1 E-Bit Error Count Latch	EEL15-8, EEL7-0
Table 142	Y29	R/W	E1 Bipolar Violation Error Count Latch	VEL15-8, VEL7-0
Table 144	Y2A	R/W	E1 CRC-4 Error Count Latch	CEL15-8, CEL7-0
Table 146	Y2B	R/W	E1 FAS Error Count Latch	BEL7-0, FEL7-0

Table 62 - E1 Latched Status Register Bit Summary - Address Y24-Y2B

Binary Address	Hex Address (A_{11}-A_0)	R/W	Register	Register Bits (B15-B8 / B7-B0)
Table 150	Y34	R	E1 Sync Interrupt Status	0, RCRCRI, RSLPI, YI, AUXPI, RAII, AISI, AIS16I, LOSSI, RCRC0I, RCRC1I, CEFSI, RFAILI, CSYNCI, MSYNCI, BSYNCI
Table 152	Y35	R	E1 Counter Interrupt Status	0, SLOI, FEOI, FEII, BEOI, BEII, CEOI, CEII, VEOI, VEII, EEOI, EEII, PCOI, JAI, PEOI, PEII
Table 154	Y36	R	E1 National Interrupt Status	0, Sa5VI, Sa6V3I, Sa6V2I, Sa6V1I, Sa6V0I, Sa6N8I, Sa6NI, SaNI, Sa5TI, SaTI, CASRI, CALNI, T2I, T1I, ONESECI

Table 63 - E1 Interrupt Status Register Bit Summary - Address Y34-Y36

Binary Address	Hex Address (A_{11}-A_0)	R/W	Register	Register Bits (B15-B8 / B7-B0)
Table 157	Y44	R/W	E1 Sync Interrupt Mask	0, RCRCRM, RSLPM, YM, AUXPM, RAIM, AISM, AIS16M, LOSSM, RCRC0M, RCRC1M, CEFSM, RFAILM, CSYNCM, MSYNCM, BSYNCM
Table 159	Y45	R/W	E1 Counter Interrupt Mask	0, SLOM, FEOM, FEIM, BEOM, BEIM, CEOM, CEIM, VEOM, VEIM, EEOM, EEIM, PCOM, JAM, PEOM, PEIM
Table 161	Y46	R/W	E1 National Interrupt Mask	0, Sa5VM, Sa6V3M, Sa6V2M, Sa6V1M, Sa6V0M, Sa6N8M, Sa6NM, SaNM, Sa5TM, SaTM, CASRM, CALNM, T2M, T1M, ONESECM

Table 64 - E1 Interrupt Mask Register Bit Summary - Address Y44-Y46

Hex Address (A$_{11}$-A$_0$)	Register	Register Bits (B15-B0)
Y51	E1 Channel 1 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA1, TB1, TC1, TD1
Y52	E1 Channel 2 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA2, TB2, TC2, TD2
Y53	E1 Channel 3 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA3, TB3, TC3, TD3
Y54	E1 Channel 4 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA4, TB4, TC4, TD4
Y55	E1 Channel 5 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA5, TB5, TC5, TD5
Y56	E1 Channel 6 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA6, TB6, TC6, TD6
Y57	E1 Channel 7 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA7, TB7, TC7, TD7
Y58	E1 Channel 8 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA8, TB8, TC8, TD8
Y59	E1 Channel 9 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA9, TB9, TC9, TD9
Y5A	E1 Channel 10 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA10, TB10, TC10, TD10
Y5B	E1 Channel 11 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA11, TB11, TC11, TD11
Y5C	E1 Channel 12 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA12, TB12, TC12, TD12
Y5D	E1 Channel 13 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA13, TB13, TC13, TD13
Y5E	E1 Channel 14 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA14, TB14, TC14, TD14
Y5F	E1 Channel 15 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA15, TB15, TC15, TD15
Y61	E1 Channel 16 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA16, TB16, TC16, TD16
Y62	E1 Channel 17 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA17, TB17, TC17, TD17
Y63	E1 Channel 18 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA18, TB18, TC18, TD18
Y64	E1 Channel 19 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA19, TB19, TC19, TD19
Y65	E1 Channel 20 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA20, TB20, TC20, TD20
Y66	E1 Channel 21 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA21, TB21, TC21, TD21
Y67	E1 Channel 22 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA22, TB22, TC22, TD22
Y68	E1 Channel 23 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA23, TB23, TC23, TD23
Y69	E1 Channel 24 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA24, TB24, TC24, TD24
Y6A	E1 Channel 25 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA25, TB25, TC25, TD25
Y6B	E1 Channel 26 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA26, TB26, TC26, TD26
Y6C	E1 Channel 27 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA27, TB27, TC27, TD27
Y6D	E1 Channel 28 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA28, TB28, TC28, TD28
Y6E	E1 Channel 29 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA29, TB29, TC29, TD29
Y6F	E1 Channel 30 Transmit CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, TA30, TB30, TC30, TD30
Refer to Table 163 - E1 Transmit CAS Data Registers - R/W Address Y51-Y5F & Y61-Y6F		

Table 65 - E1 Transmit CAS Data Register Bit Summary - Address Y51-Y5F, Y61-Y6F

Hex Address (A$_{11}$-A$_0$)	Register	Register Bits (B15-B0)
Y71	E1 Channel 1 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA1, RB1, RC1, RD1
Y72	E1 Channel 2 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA2, RB2, RC2, RD2
Y73	E1 Channel 3 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA3, RB3, RC3, RD3
Y74	E1 Channel 4 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA4, RB4, RC4, RD4
Y75	E1 Channel 5 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA5, RB5, RC5, RD5
Y76	E1 Channel 6 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA6, RB6, RC6, RD6
Y77	E1 Channel 7 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA7, RB7, RC7, RD7
Y78	E1 Channel 8 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA8, RB8, RC8, RD8
Y79	E1 Channel 9 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA9, RB9, RC9, RD9
Y7A	E1 Channel 10 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA10, RB10, RC10, RD10
Y7B	E1 Channel 11 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA11, RB11, RC11, RD11
Y7C	E1 Channel 12 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA12, RB12, RC12, RD12
Y7D	E1 Channel 13 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA13, RB13, RC13, RD13
Y7E	E1 Channel 14 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA14, RB14, RC14, RD14
Y7F	E1 Channel 15 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA15, RB15, RC15, RD15
Y81	E1 Channel 1 & 16 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA16, RB16, RC16, RD16
Y82	E1 Channel 2 & 17 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA17, RB17, RC17, RD17
Y83	E1 Channel 3 & 18 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA18, RB18, RC18, RD18
Y84	E1 Channel 4 & 19 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA19, RB19, RC19, RD19
Y85	E1 Channel 5 & 20 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA20, RB20, RC20, RD20
Y86	E1 Channel 6 & 21 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA21, RB21, RC21, RD21
Y87	E1 Channel 7 & 22 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA22, RB22, RC22, RD22
Y88	E1 Channel 8 & 23 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA23, RB23, RC23, RD23
Y89	E1 Channel 9 & 24 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA24, RB24, RC24, RD24
Y8A	E1 Channel 10 & 25 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA25, RB25, RC25, RD25
Y8B	E1 Channel 11 & 26 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA26, RB26, RC26, RD26
Y8C	E1 Channel 12 & 27 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA27, RB27, RC27, RD27
Y8D	E1 Channel 13 & 28 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA28, RB28, RC28, RD28
Y8E	E1 Channel 14 & 29 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA29, RB29, RC29, RD29
Y8F	E1 Channel 15 & 30 Receive CAS Data	#, #, #, #, #, #, #, #, #, #, #, #, RA30, RB30, RC30, RD30

Refer to Table 165 - E1 Receive CAS Data Registers - R Address Y71-Y7F, Y81-Y8F

Table 66 - E1 Receive CAS Data Register Bit Summary - Address Y71-Y7F, Y81-Y8F

Hex Address (A$_{11}$-A$_0$)	Register	Register Bits (B15-B0)
Y91	E1 TS 1 Control	#,#,#,#,#,#, RPCI1, MPDR1, MPST1, TADI1, RTSL1, LTSL1, TTST1, RRST1, MPDT1, #
Y92	E1 TS 2 Control	#,#,#,#,#,#, RPCI2, MPDR2, MPST2, TADI2, RTSL2, LTSL2, TTST2, RRST2, MPDT2, #
Y93	E1 TS 3 Control	#,#,#,#,#,#, RPCI3, MPDR3, MPST3, TADI3, RTSL3, LTSL3, TTST3, RRST3, MPDT3, #
Y94	E1 TS 4 Control	#,#,#,#,#,#, RPCI4, MPDR4, MPST4, TADI4, RTSL4, LTSL4, TTST4, RRST4, MPDT4, #
Y95	E1 TS 5 Control	#,#,#,#,#,#, RPCI5, MPDR5, MPST5, TADI5, RTSL5, LTSL5, TTST5, RRST5, MPDT5, #
Y96	E1 TS 6 Control	#,#,#,#,#,#, RPCI6, MPDR6, MPST6, TADI6, RTSL6, LTSL6, TTST6, RRST6, MPDT6, #
Y97	E1 TS 7 Control	#,#,#,#,#,#, RPCI7, MPDR7, MPST7, TADI7, RTSL7, LTSL7, TTST7, RRST7, MPDT7, #
Y98	E1 TS 8 Control	#,#,#,#,#,#, RPCI8, MPDR8, MPST8, TADI8, RTSL8, LTSL8, TTST8, RRST8, MPDT8, #
Y99	E1 TS 9 Control	#,#,#,#,#,#, RPCI9, MPDR9, MPST9, TADI9, RTSL9, LTSL9, TTST9, RRST9, MPDT9, #
Y9A	E1 TS 10 Control	#,#,#,#,#,#, RPCI10, MPDR10, MPST10, TADI10, RTSL10, LTSL10, TTST10, RRST10, MPDT10, #
Y9B	E1 TS 11 Control	#,#,#,#,#,#, RPCI11, MPDR11, MPST11, TADI11, RTSL11, LTSL11, TTST11, RRST11, MPDT11, #
Y9C	E1 TS 12 Control	#,#,#,#,#,#, RPCI12, MPDR12, MPST12, TADI12, RTSL12, LTSL12, TTST12, RRST12, MPDT12, #
Y9D	E1 TS 13 Control	#,#,#,#,#,#, RPCI13, MPDR13, MPST13, TADI13, RTSL13, LTSL13, TTST13, RRST13, MPDT13, #
Y9E	E1 TS 14 Control	#,#,#,#,#,#, RPCI14, MPDR14, MPST14, TADI14, RTSL14, LTSL14, TTST14, RRST14, MPDT14, #
Y9F	E1 TS 15 Control	#,#,#,#,#,#, RPCI15, MPDR15, MPST15, TADI15, RTSL15, LTSL15, TTST15, RRST15, MPDT15, #
YA0	E1 TS 16 Control	#,#,#,#,#,#, RPCI16, MPDR16, MPST16, TADI16, RTSL16, LTSL16, TTST16, RRST16, MPDT16, #
YA1	E1 TS 17 Control	#,#,#,#,#,#, RPCI17, MPDR17, MPST17, TADI17, RTSL17, LTSL17, TTST17, RRST17, MPDT17, #
YA2	E1 TS 18 Control	#,#,#,#,#,#, RPCI18, MPDR18, MPST18, TADI18, RTSL18, LTSL18, TTST18, RRST18, MPDT18, #
YA3	E1 TS 19 Control	#,#,#,#,#,#, RPCI19, MPDR19, MPST19, TADI19, RTSL19, LTSL19, TTST19, RRST19, MPDT19, #
YA4	E1 TS 20 Control	#,#,#,#,#,#, RPCI20, MPDR20, MPST20, TADI20, RTSL20, LTSL20, TTST20, RRST20, MPDT20, #
YA5	E1 TS 21 Control	#,#,#,#,#,#, RPCI21, MPDR21, MPST21, TADI21, RTSL21, LTSL21, TTST21, RRST21, MPDT21, #
YA6	E1 TS 22 Control	#,#,#,#,#,#, RPCI22, MPDR22, MPST22, TADI22, RTSL22, LTSL22, TTST22, RRST22, MPDT22, #
YA7	E1 TS 23 Control	#,#,#,#,#,#, RPCI23, MPDR23, MPST23, TADI23, RTSL23, LTSL23, TTST23, RRST23, MPDT23, #

Table 67 - E1 Timeslot 0-31 Control Register Bit Summary - Address Y91-YAF

Hex Address (A$_{11}$-A$_0$)	Register	Register Bits (B15-B0)
YA8	E1 TS 24 Control	#,#,#,#,#,#, RPCI24, MPDR24, MPST24, TADI24, RTSL24, LTSL24, TTST24, RRST24, MPDT24, #
YA9	E1 TS 25 Control	#,#,#,#,#,#, RPCI25, MPDR25, MPST25, TADI25, RTSL25, LTSL25, TTST25, RRST25, MPDT25, #
YAA	E1 TS 26 Control	#,#,#,#,#,#, RPCI26, MPDR26, MPST26, TADI26, RTSL26, LTSL26, TTST26, RRST26, MPDT26, #
YAB	E1 TS 27 Control	#,#,#,#,#,#, RPCI27, MPDR27, MPST27, TADI27, RTSL27, LTSL27, TTST27, RRST27, MPDT27, #
YAC	E1 TS 28 Control	#,#,#,#,#,#, RPCI28, MPDR28, MPST28, TADI28, RTSL28, LTSL28, TTST28, RRST28, MPDT28, #
YAD	E1 TS 29 Control	#,#,#,#,#,#, RPCI29, MPDR29, MPST29, TADI29, RTSL29, LTSL29, TTST29, RRST29, MPDT29, #
YAE	E1 TS 30 Control	#,#,#,#,#,#, RPCI30, MPDR30, MPST30, TADI30, RTSL30, LTSL30, TTST30, RRST30, MPDT30, #
YAF	E1 TS 31 Control	#,#,#,#,#,#, RPCI31, MPDR31, MPST31, TADI31, RTSL31, LTSL31, TTST31, RRST31, MPDT31, #
Refer to Table 167 - E1 Per Timeslot 0 to 31 Control Registers - R/W Address Y90-YAF		

Table 67 - E1 Timeslot 0-31 Control Register Bit Summary - Address Y91-YAF

Hex Address (A$_{11}$-A$_0$)	Register	Register Bits (B15-B8 / B7-B0)
YB0	E1 Transmit Sa4 National Bits	#, #, #, #, #, #, #, #, Sa4T1, Sa4T3, Sa4T5, Sa4T7, Sa4T9, Sa4T11, Sa4T13, Sa4T15
YB1	E1 Transmit Sa5 National Bits	#, #, #, #, #, #, #, #, Sa5T1, Sa5T3, Sa5T5, Sa5T7, Sa5T9, Sa5T11, Sa5T13, Sa5T15
YB2	E1 Transmit Sa6 National Bits	#, #, #, #, #, #, #, #, Sa6T1, Sa6T3, Sa6T5, Sa6T7, Sa6T9, Sa6T11, Sa6T13, Sa6T15
YB3	E1 Transmit Sa7 National Bits	#, #, #, #, #, #, #, #, Sa7T1, Sa7T3, Sa7T5, Sa7T7, Sa7T9, Sa7T11, Sa7T13, Sa7T15
YB4	E1 Transmit Sa8 National Bits	#, #, #, #, #, #, #, #, Sa8T1, Sa8T3, Sa8T5, Sa8T7, Sa8T9, Sa8T11, Sa8T13, Sa8T15
Refer to Table 168 - E1 Transmit National Bits Sa4 - Sa8 Data Registers - R/W Address YB0-YB4		

Table 68 - E1 Transmit National Bits Data Register Bit Summary - Address YB0-YB4

Hex Address (A$_{11}$-A$_0$)	Register	Register Bits (B15-B8 / B7-B0)
YC0	E1 Receive Sa4 National Bits	#, #, #, #, #, #, #, #, Sa4R1, Sa4R3, Sa4R5, Sa4R7, Sa4R9, Sa4R11, Sa4R13, Sa4R15
YC1	E1 Receive Sa5 National Bits	#, #, #, #, #, #, #, #, Sa5R1, Sa5R3, Sa5R5, Sa5R7, Sa5R9, Sa5R11, Sa5R13, Sa5R15
YC2	E1 Receive Sa6 National Bits	#, #, #, #, #, #, #, #, Sa6R1, Sa6R3, Sa6R5, Sa6R7, Sa6R9, Sa6R11, Sa6R13, Sa6R15
YC3	E1 Receive Sa7 National Bits	#, #, #, #, #, #, #, #, Sa7R1, Sa7R3, Sa7R5, Sa7R7, Sa7R9, Sa7R11, Sa7R13, Sa7R15
YC4	E1 Receive Sa8 National Bits	#, #, #, #, #, #, #, #, Sa8R1, Sa8R3, Sa8R5, Sa8R7, Sa8R9, Sa8R11, Sa8R13, Sa8R15
Refer to Table 169 - E1 Receive National Bit Sa4 - Sa8 Data Registers - R Address YC0-YC4		

Table 69 - E1 Receive National Bits Data Register Bit Summary - Address YC0-YC4

21.0 T1 & E1 Transceiver Registers Bit Functions

A (0), (1) or (#) in the "Name" column of these tables indicates the state of the data bits after a reset ($\overline{\text{RESET}}$, RSTC or RST). The (#) indicates that a (0) or (1) is possible.

21.1 T1 & E1 Global Transceiver Register Bit Functions - in Address Order

Bit	Name	Functional Description
15	T1E0 (1)	**T1 or E1 Enable.** If zero, E1 mode is enabled. If one, T1 mode is enabled. Toggling this bit resets the T1/E1 unique control registers.
14	RSV (0)	**Reserved**. Must be set to 0 for normal operation.
13 12	ESEL1 ESEL0 (00)	**ESYN Output Select.** These two input select bits determine the extracted clock source output at the ESYN pin (when $\overline{\text{ESYNI}}$ = 1 of T1 and E1 Global Timing Control Register - R/W Address 905) as follows. ESEL1 ESEL0 Extracted Clock 0 0 RxCK[0] 0 1 RxCK[1] 1 0 RxCK[2] 1 1 RxCK[3]
11 10 9 8	ACC3 ACC2 ACC1 ACC0 (0000)	**Auxiliary Clock Output Control.** If zero, the corresponding AUX pin is zero. If one, the corresponding AUX pin is one. These control bits must first be enabled with register bits ACF2-0.
7 6 5	ACF2 ACF1 ACF0 (000)	**Auxiliary Clock Selection.** These three select bits determine the type of signals output at the auxiliary clock pins. For a detailed description of these output signals refer to Section 3.6 Auxiliary Output SIgnals.
4 3	CK1 CK0 (01)	**Clock Rate.** These two clock select bits determine the system clock at the CKb pin as follows (See Figures 10 to 13). CK1 CK0 Clock System Bus 0 0 Reserved NA 0 1 4.096MHz 2.048Mb/s 1 0 16.384MHz 8.192Mb/s 1 1 Reserved NA For a detailed description of these clocks refer to Section 7.3 ST-BUS Interface (DSTo, DSTo, CSTi, CSTo Pins).
2	PSLP (0)	**Phase Slope.** If one, the rate of phase change (phase slope) of the clocks output by the PLL is limited to 5ns per 125 μs. Phase slope limiting is used to meet the requirements of some synchronization interface standards such as ANSI T1.101 Stratum 4E. If zero, the rate of phase change is not limited. This bit will normally be set to zero.
1	RSTP (0)	**PLL Reset.** If one, the PLL circuit is reset, the rest of the device is unaffected. This is typically used after changing the state of the FS1, FS2 bits at address 905H.
0	RSTC (0)	**Common Reset.** When this bit is changed from zero to one, all four transceivers will reset to their default mode. This software reset has the same effect as the $\overline{\text{RESET}}$ pin. See Section 7.6 Reset Operation (RESET, TRST Pins) for the default settings. Note that the global registers (i.e. 900, 902, and 905) are also reset.

Table 70 - T1 & E1 Global Mode Control - R/W Address 900

Bit	Name	Functional Description
15	X3HM (0)	**T1 Transceiver 3 HDLC Mask.** This is the mask bit for the corresponding Transceiver 3 X3HI bit in the T1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
14	X3EM (0)	**T1 Transceiver 3 Elastic Mask.** This is the mask bit for the corresponding Transceiver 3 X3EI bit in the T1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
13	X3RM (0)	**T1 Transceiver 3 Receive Line Mask.** This is the mask bit for the corresponding Transceiver 3 X3RI bit in the T1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
12	X3SM (0)	**T1 Transceiver 3 Sync Mask.** This is the mask bit for the corresponding Transceiver 3 X3SI bit in the T1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
11	X2HM (0)	**T1 Transceiver 2 HDLC Mask.** This is the mask bit for the corresponding Transceiver 2 X2HI bit in the T1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
10	X2EM (0)	**T1 Transceiver 2 Elastic Mask.** This is the mask bit for the corresponding Transceiver 2 X2EI bit in the T1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
9	X2RM (0)	**T1 Transceiver 2 Receive Line Mask.** This is the mask bit for the corresponding Transceiver 2 X2RI bit in the T1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
8	X2SM (0)	**T1 Transceiver 2 Sync Mask.** This is the mask bit for the corresponding Transceiver 2 X2SI bit in the T1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
7	X1HM (0)	**T1 Transceiver 1 HDLC Mask.** This is the mask bit for the corresponding Transceiver 1 X1HI bit in the T1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
6	X1EM (0)	**T1 Transceiver 1 Elastic Mask.** This is the mask bit for the corresponding Transceiver 1 X1EI bit in the T1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
5	X1RM (0)	**T1 Transceiver 1 Receive Line Mask.** This is the mask bit for the corresponding Transceiver 1 X1RI bit in the T1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
4	X1SM (0)	**T1 Transceiver 1 Sync Mask.** This is the mask bit for the corresponding Transceiver 1 X1SI bit in the T1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
3	X0HM (0)	**T1 Transceiver 0 HDLC Mask.** This is the mask bit for the corresponding Transceiver 0 X0HI bit in the T1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
2	X0EM (0)	**T1 Transceiver 0 Elastic Mask.** This is the mask bit for the corresponding Transceiver 0 X0EI bit in the T1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
1	X0RM (0)	**T1 Transceiver 0 Receive Line Mask.** This is the mask bit for the corresponding Transceiver 0 X0RI bit in the T1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
0	X0SM (0)	**T1 Transceiver 0 Sync Mask.** This is the mask bit for the corresponding Transceiver 0 X0SI bit in the T1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.

Table 71 - T1 Interrupt Vector Mask - R/W Address 902

Bit	Name	Functional Description
15	X3HM (0)	**E1 Transceiver 3 HDLC Mask.** This is the mask bit for the corresponding Transceiver 3 X3HI bit in the E1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
14	X3NM (0)	**E1 Transceiver 3 National Mask.** This is the mask bit for the corresponding Transceiver 3 X3NI bit in the E1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
13	X3CM (0)	**E1 Transceiver 3 Counter Mask.** This is the mask bit for the corresponding Transceiver 3 X3CI bit in the E1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
12	X3SM (0)	**E1 Transceiver 3 Sync Mask.** This is the mask bit for the corresponding Transceiver 3 X3SI bit in the E1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
11	X2HM (0)	**E1 Transceiver 2 HDLC Mask.** This is the mask bit for the corresponding Transceiver 2 X2HI bit in the E1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
10	X2NM (0)	**E1 Transceiver 2 National Mask.** This is the mask bit for the corresponding Transceiver 2 X2NI bit in the E1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
9	X2CM (0)	**E1 Transceiver 2 Counter Mask.** This is the mask bit for the corresponding Transceiver 2 X2CI bit in the E1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
8	X2SM (0)	**E1 Transceiver 2 Sync Mask.** This is the mask bit for the corresponding Transceiver 2 X2SI bit in the E1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
7	X1HM (0)	**E1 Transceiver 1 HDLC Mask.** This is the mask bit for the corresponding Transceiver 1 X1HI bit in the E1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
6	X1NM (0)	**E1 Transceiver 1 National Mask.** This is the mask bit for the corresponding Transceiver 1 X1NI bit in the E1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
5	X1CM (0)	**E1 Transceiver 1 Counter Mask.** This is the mask bit for the corresponding Transceiver 1 X1CI bit in the E1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
4	X1SM (0)	**E1 Transceiver 1 Sync Mask.** This is the mask bit for the corresponding Transceiver 1 X1SI bit in the E1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
3	X0HM (0)	**E1 Transceiver 0 HDLC Mask.** This is the mask bit for the corresponding Transceiver 0 X0HI bit in the E1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
2	X0NM (0)	**E1 Transceiver 0 National Mask.** This is the mask bit for the corresponding Transceiver 0 X0NI bit in the E1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
1	X0CM (0)	**E1 Transceiver 0 Counter Mask.** This is the mask bit for the corresponding Transceiver 0 X0CI bit in the E1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
0	X0SM (0)	**E1 Transceiver 0 Sync Mask.** This is the mask bit for the corresponding Transceiver 0 X0SI bit in the E1 Interrupt Vector Status - R Address 910. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.

Table 72 - E1 Interrupt Vector Mask - R/W Address 902

Bit	Name	Functional Description
15 14 13	PR2 PR1 PR0 (101)	**Primary Reference Source.** These three select bits determine the primary reference clock source for the internal PLL. The clock frequency at the selected reference source must match the PLL frequency selection. PR2 PR1 PR0 Primary Reference Source 0 0 0 RXCK[0] 0 0 1 RXCK[1] 0 1 0 RXCK[2] 0 1 1 RXCK[3] 1 0 0 ESYN 1 0 1 CKb 1 1 0 FPb 1 1 1 Reserved
12 11 10	SR2 SR1 SR0 (000)	**Secondary Reference Source.** These three select bits determine the secondary reference clock source for the internal PLL. The clock frequency at the selected reference source must match the PLL frequency selection. SR2 SR1 SR0 Secondary Reference Source 0 0 0 RXCK[0] 0 0 1 RXCK[1] 0 1 0 RXCK[2] 0 1 1 RXCK[3] 1 0 0 ESYN 1 0 1 CKb 1 1 0 FPb 1 1 1 Reserved
9 8	FS2 FS1 (11)	**PLL Frequency Selection.** These two select bits determine the input reference clock frequency for the internal PLL.The clock frequency at the selected reference source must match the PLL frequency selection. FS2 FS1 PLL Input Frequency 0 0 Reserved 0 1 8kHz 1 0 1.544MHz 1 1 2.048MHz When CKb is selected as a reference source, the clock rate at the CKb pin is divided down to 2.048MHz (CKb/2 in 2Mb/s mode and CKb/8 in 8Mb/s mode). After changing these bits, the PLL reset bit (Table 70, "T1 & E1 Global Mode Control - R/W Address 900," on page 106) should be toggled.
7 6	MS2 MS1 (00)	**PLL Mode Selection.** These two select bits determine the mode of operation of the internal PLL. MS2 MS1 PLL Operating Mode 0 0 Normal 0 1 Holdover 1 0 Freerun 1 1 Reserved When CKb is selected as a reference source, the clock rate at the CKb pin is divided down to 2.048MHz; CKb/2 in 2Mb/s mode and CKb/8 in 8Mb/s mode.
5	RSEL (0)	**Reference Select.** When low, the primary reference source is used as the timing source to the PLL. When high, the secondary reference is used as the timing source to the PLL.
4	TIER (1)	**TIE Circuit Reset.** When low, the PLL time interval error correction circuit is reset, resulting in a re-alignment of input phase and output phase.
3	TIEE (1)	**TIE Circuit Enable.** When high, the PLL time interval error correction circuit is enabled for mode switches from Primary Holdover to Primary Normal. When low, it is disabled.
2	BUSM (0)	**Buss Mode.** When zero, the device is in Bus Sync mode, the bi-directional CK and FP pins are inputs. When one, the device is in PLL Sync mode, the bi-directional CK and FP pins are outputs. For a detailed description of these modes refer to Section 3.0 Timing.

Table 73 - T1 & E1 Global Timing Control - R/W Address 905

Bit	Name	Functional Description
1	ESYNI (0)	**ESYN Input Enable.** When zero, the bi-directional ESYN pin is an input. When one, the bi-directional ESYN pin is an output. Set this in accordance with the timing mode detailed in Section 3.0 Timing.
0	FLOCK (0)	**Fast Lock.** When one, the PLL is underdamped and it acquires lock faster than normal. This is typically used in conjunction with the PSLP control bit detailed in T1 & E1 Global Mode Control - R/W Address 900. When zero, the PLL behaves normally.

Table 73 - T1 & E1 Global Timing Control - R/W Address 905

Bit	Name	Functional Description
15	X3HI (0)	**T1 Transceiver 3 HDLC Interrupt.** When any bit in the T1 Transceiver 3 - T1 & E1 HDLC Interrupt Status - R Address Y33 (Y=3) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the T1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
14	X3EI (0)	**T1 Transceiver 3 Elastic Interrupt.** When any bit in the T1 Transceiver 3 - T1 Elastic Store Interrupt Status - R Address Y36 (Y=3) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the T1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
13	X3RI (0)	**T1 Transceiver 3 Receive Interrupt.** When any bit in the T1 Transceiver 3 - T1 Receive Line and Timer Interrupt Status - R Address Y35 (Y=3) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the T1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
12	X3SI (0)	**T1 Transceiver 3 Sync Interrupt.** When any bit in the T1 Transceiver 3 - T1 Receive and Sync Interrupt Status - R Address Y34 (Y=3) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the T1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
11	X2HI (0)	**T1 Transceiver 2 HDLC Interrupt.** When any bit in the T1 Transceiver 2 - T1 & E1 HDLC Interrupt Status - R Address Y33 (Y=2) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the T1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
10	X2EI (0)	**T1 Transceiver 2 Elastic Interrupt.** When any bit in the T1 Transceiver 2 - T1 Elastic Store Interrupt Status - R Address Y36 (Y=2) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the T1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
9	X2RI (0)	**T1 Transceiver 2 Receive Interrupt.** When any bit in the T1 Transceiver 2 - T1 Receive Line and Timer Interrupt Status - R Address Y35 (Y=2) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the T1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
8	X2SI (0)	**T1 Transceiver 2 Sync Interrupt.** When any bit in the T1 Transceiver 2 - T1 Receive and Sync Interrupt Status - R Address Y34 (Y=2) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the T1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
7	X1HI (0)	**T1 Transceiver 1 HDLC Interrupt.** When any bit in the T1 Transceiver 1 - T1 & E1 HDLC Interrupt Status - R Address Y33 (Y=1) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the T1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
6	X1EI (0)	**T1 Transceiver 1 Elastic Interrupt.** When any bit in the T1 Transceiver 1 - T1 Elastic Store Interrupt Status - R Address Y36 (Y=1) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the T1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.

Table 74 - T1 Interrupt Vector Status - R Address 910

Bit	Name	Functional Description
5	X1RI (0)	**T1 Transceiver 1 Receive Interrupt.** When any bit in the T1 Transceiver 1 - T1 Receive Line and Timer Interrupt Status - R Address Y35 (Y=1) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the T1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
4	X1SI (0)	**T1 Transceiver 1 Sync Interrupt.** When any bit in the T1 Transceiver 1 - T1 Receive and Sync Interrupt Status - R Address Y34 (Y=1) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the T1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
3	X0HI (0)	**T1 Transceiver 0 HDLC Interrupt.** When any bit in the T1 Transceiver 0 - T1 & E1 HDLC Interrupt Status - R Address Y33 (Y=0) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the T1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
2	X0EI (0)	**T1 Transceiver 0 Elastic Interrupt.** When any bit in the T1 Transceiver 0 - T1 Elastic Store Interrupt Status - R Address Y36 (Y=0) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the T1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
1	X0RI (0)	**T1 Transceiver 0 Receive Interrupt.** When any bit in the T1 Transceiver 0 - T1 Receive Line and Timer Interrupt Status - R Address Y35 (Y=0) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the T1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
0	X0SI (0)	**T1 Transceiver 0 Sync Interrupt.** When any bit in the T1 Transceiver 0 - T1 Receive and Sync Interrupt Status - R Address Y34 (Y=0) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the T1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.

Table 74 - T1 Interrupt Vector Status - R Address 910

Bit	Name	Functional Description
15	X3HI (0)	**E1 Transceiver 3 HDLC Interrupt.** When any bit in the E1 Transceiver 3 - T1 & E1 HDLC Interrupt Status - R Address Y33 (Y=3) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the E1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
14	X3NI (0)	**E1 Transceiver 3 National Interrupt.** When any bit in the E1 Transceiver 3 - E1 National Interrupt Status - R Address Y36 (Y=3) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the E1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
13	X3CI (0)	**E1 Transceiver 3 Counter Interrupt.** When any bit in the E1 Transceiver 3 - E1 Counter Interrupt Status - R Address Y35 (Y=3) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the E1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
12	X3SI (0)	**E1 Transceiver 3 Sync Interrupt.** When any bit in the E1 Transceiver 3 - E1 Sync Interrupt Status - R Address Y34 (Y=3) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the E1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
11	X2HI (0)	**E1 Transceiver 2 HDLC Interrupt.** When any bit in the E1 Transceiver 2 - T1 & E1 HDLC Interrupt Status - R Address Y33 (Y=2) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the E1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.

Table 75 - E1 Interrupt Vector Status - R Address 910

Bit	Name	Functional Description
10	X2NI (0)	**E1 Transceiver 2 National Interrupt.** When any bit in the E1 Transceiver 2 - E1 National Interrupt Status - R Address Y36 (Y=2) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the E1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
9	X2CI (0)	**E1 Transceiver 2 Counter Interrupt.** When any bit in the E1 Transceiver 2 - E1 Counter Interrupt Status - R Address Y35 (Y=2) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the E1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
8	X2SI (0)	**E1 Transceiver 2 Sync Interrupt.** When any bit in the E1 Transceiver 2 - E1 Sync Interrupt Status - R Address Y34 (Y=2) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the E1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
7	X1HI (0)	**E1 Transceiver 1 HDLC Interrupt.** When any bit in the E1 Transceiver 1 - T1 & E1 HDLC Interrupt Status - R Address Y33 (Y=1) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the E1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
6	X1NI (0)	**E1 Transceiver 1 National Interrupt.** When any bit in the E1 Transceiver 1 - E1 National Interrupt Status - R Address Y36 (Y=1) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the E1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
5	X1CI (0)	**E1 Transceiver 1 Counter Interrupt.** When any bit in the E1 Transceiver 1 - E1 Counter Interrupt Status - R Address Y35 (Y=1) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the E1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
4	X1SI (0)	**E1 Transceiver 1 Sync Interrupt.** When any bit in the E1 Transceiver 1 - E1 Sync Interrupt Status - R Address Y34 (Y=1) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the E1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
0	X0HI (0)	**E1 Transceiver 0 HDLC Interrupt.** When any bit in the E1 Transceiver 0 - T1 & E1 HDLC Interrupt Status - R Address Y33 (Y=0) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the E1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
2	X0NI (0)	**E1 Transceiver 0 National Interrupt.** When any bit in the E1 Transceiver 0 - E1 National Interrupt Status - R Address Y36 (Y=0) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the E1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
1	X0CI (0)	**E1 Transceiver 0 Counter Interrupt.** When any bit in the E1 Transceiver 0 - E1 Counter Interrupt Status - R Address Y35 (Y=0) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the E1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.
0	X0SI (0)	**E1 Transceiver 0 Sync Interrupt.** When any bit in the E1 Transceiver 0 - E1 Sync Interrupt Status - R Address Y34 (Y=0) is set to one, this status bit is one; otherwise, it is zero. The corresponding bit in the E1 Interrupt Vector Mask - R/W Address 902 must be unmasked for this operation to function.

Table 75 - E1 Interrupt Vector Status - R Address 910

Bit	Name	Functional Description	
15 14 13 12	ID15 ID14 ID13 ID12 (0010)	These four bits provide an indication to the number of devices within the IC; where the number of devices is 2 ^ (ID15-12). The MT9071A has four transceivers.	This byte allows user software to track device variances, revisions and capabilities, and provide system variations, if necessary. The ID Code for the MT9071A is hex 20F0.
11 10 9 8	ID9 ID8 ID7 ID6 (0000)	Reserved.	
7	ID7 (1)	If one, the device has internal HDLC capability. If zero, internal HDLC capability is not included.	
6	ID6 (1)	If one, the device has internal LIU capability. If zero, internal LIU capability is not included.	
5	ID5 (1)	If one, the device has T1 framing capability. If zero, T1 framing is not supported.	
4	ID4 (1)	If one, the device has E1 framing capability. If zero, E1 framing is not supported.	
3	ID3 (0)	Reserved.	
2 1 0	ID2 ID1 ID0 (001)	These 3 bits make up a binary code which identify the marketing code revision. Rev A corresponds to 000, Rev B to 001 etc. (The marketing code revision is indicated on the device package just before the package type, devices without a revision letter are implicitly an A).	

Table 76 - T1 & E1 ID Rev Code Data - R Address 912

Bit	Name	Functional Description
15-1	(#### #### #### ###)	Not Used
0	AHLD (0)	**Auto Holdover.** If one, the internal PLL is in Auto-Holdover mode.

Table 77 - T1 & E1 Global Status - R Address 914

21.2 T1 & E1 Unique Transceiver Register Bit Functions - in Address Order

Bit	Name	Functional Description
15	RSV (0)	**Reserved**. Must be set to 0 for normal operation.
14	(#)	Not Used
13	G802 (0)	**G.802 Mode**. If one, the device operates with embedded framing as per G.802. The backplane operates at 2.048Mb/s with an E1 PCM30 format. The link operates as a T1 DS1 link. If zero, device operates normally.
12	JY (0)	**Japan Yellow Alarm** Set this bit high to select a pattern of 16 ones (1111111111111111) as the ESF yellow alarm, both for the case when an ESF yellow alarm is to be transmit, or in recognizing a received yellow alarm. In order to transmit the japan yellow alarm the TESFY bit has to be set.
11	TRANSP (0)	**Transparent Mode Select.** Setting this bit causes unframed data from DSTi channels 0 to 23 and channel 31 bit 7 to be transmitted transparently onto the DS1 line. Unframed data received from the DS1 line is piped out on DSTo channels 0 to 23 and channel 31 bit 0.
10	T1DM (0)	**T1DM Mode Select**. If one, T1 DM Mode is selected. The Ft and Fs pattern is the same as the D4 Mode but a 1011YR0 pattern is sent and detected in Channel 24 of the T1 interface. Bit Y is used to indicate a yellow Alarm and R bit is used by AT&T for a 8kb/s communication channel.
9	ESF (0)	**Extended Super Frame**. Setting this bit enables transmission and reception of the 24 frame superframe DS1 protocol.
8	RSV (0)	**Reserved**. Must be set to 0 for normal operation.
7	CXC (0)	**Cross Check.** Setting this bit in ESF mode enables a cross check of the CRC-6 remainder before the frame synchronizer pulls into sync. This process adds at least 6 milliseconds to the frame synchronization time.
6 5	RS1 RS0 (00)	**Reframe Select**. These bits set the criteria for an automatic reframe in the event of framing bits errors. The combinations available are: RS1 - 0, RS0 - 0 = sliding window of 2 errors out of 4. RS1 - 0, RS0 - 1 = sliding window of 2 errors out of 5. RS1 - 1, RS0 - 0 = sliding window of 2 errors out of 6. RS1 - 1, RS0 - 1 = no reframes due to framing bit errors. Note that for T1DM mode, the frame boundary starts at the channel 1 data including synchronization byte (10111YR0) and the following 'S' bit.
4	FSI (0)	**Fs Bit Include**. Only applicable in D4 mode (not ESF). Setting this bit causes errored Fs bits to be included as framing bit errors. A bad Fs bit will increment the Framing Error Bit Counter, and will potentially cause a reframe (if it is the second bad framing bit out of 5). The Fs bit of the receive frame 12 will only be included if D4SECY is set. Setting this bit in D4 (not ESF) mode enables a check of the Fs bits in addition to the Ft bits during frame synchronization.
3	REFR (0)	**Reframe**. Setting this bit causes an automatic reframe.
2	MFREFR (0)	**MultiFrame Reframe**. Only applicable in D4 mode. Setting this bit causes an automatic multiframe reframe. The signaling bits are frozen until multiframe synchronization is achieved. Terminal frame synchronization is not affected.
1	JTS (0)	**Japan Telecom Synchronization.** If one, the S bit is included in the CRC6 calculation for the ESF framing Mode.
0	TXSYNC (0)	**Transmit Synchronization.** Setting this bit causes the transmit multiframe boundary to be internally synchronized to the incoming S-bits on DSTi channel 31 bit 0.

Table 78 - T1 Framing Mode Control - R/W Address Y00

Bit	Name	Functional Description
15	(0)	Not Used
14	ASEL (0)	**AIS Select.** This bit selects the criteria on which the detection of a valid alarm indication signal AIS=1 (see Table 109 - E1 Alarms & MAS Status - R Address Y12) is based. If zero, the criteria is less than three zeros in a two frame period (512 bits). If one, the criteria is less than three zeros in each of two consecutive double-frame periods (512 bits per double-frame).
13	$\overline{ARAI}$ (0)	**Automatic Remote Alarm Indication (RAI) Operation.** This bit determines the source for the Remote Alarm Indication bit (the A bit) of the transmit PCM30 signal (time-slot 0 bit 3 of NFAS frames). If zero, the source for the A bit is the RAI status bit (see Table 107 - E1 CRC-4 Timers & CRC-4 Local Status - R Address Y11), and consequently, will change automatically. That is, A=0 when basic synchronization has been acquired (RAI=0), and A=1 when basic synchronization has not been acquired (RAI=1). If the $\overline{ARAI}$ bit is set to one, the A bit is controlled through the TALM control bit (see this register).
12	TALM (0)	**Transmit Remote Alarm**. This bit is the source for the Remote Alarm Indication bit (the A bit) of the transmit PCM30 signal (timeslot 0 bit 3 of NFAS frames) when the $\overline{ARAI}$ control bit (this register) is set to one. The TALM bit is used to signal an alarm to the remote end of the PCM 30 link (one - alarm, zero - normal).
11	TAIS (0)	**Transmit Alarm Indication Signal.** If one, an all ones signal is transmitted in all timeslots except zero and 16. If zero, timeslots functions normally.
10	TAIS0 (0)	**Transmit AIS Timeslot Zero.** If one, an all ones signal is transmitted in timeslot zero. If zero, timeslot zero functions normally.
9	TAI16 (0)	**Transmit AIS Timeslot 16.** If one, an all ones signal is transmitted in timeslot 16. If zero, timeslot functions normally.
8	TE (0)	**Transmit E bits.** If CRC-4 synchronization is not achieved $\overline{CSYNC}$=1 (see Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10), then this bit is transmitted on the PCM30 link E-bits (E1 is bit 1 of timeslot 0, of NFAS frame 13; E2 is bit 1 of timeslot 0, of NFAS frame15). If CRC-4 synchronization is achieved $\overline{CSYNC}$=0, this control bit is ignored.
7	TIU0 (0)	**Transmit International Use Zero.** This bit is transmitted on the PCM 30 2048kb/s link in bit position one of time-slot 0 of all the frame-alignment signal (FAS) frames when CRC-4 operation is disabled $\overline{CSYN}$=1 (see this register). The TIU0 bit is reserved for international use and should normally be kept at one. If CRC-4 operation is enabled ($\overline{CSYN}$=0), this bit is ignored.
6	TIU1 (1)	**Transmit International Use One.** This bit is transmitted on the PCM 30 2048kb/s link in bit position one of timeslot 0 of all the Non-Frame Alignment Signal (NFAS) frames when CRC-4 operation is disabled $\overline{CSYN}$=1 (see this register). The TIU1 bit is reserved for international use and should normally be kept at one. If CRC-4 operation is enabled ($\overline{CSYN}$=0), this bit is ignored.
5	$\overline{CSYN}$ (0)	**CRC-4 Synchronization.** If zero, basic CRC-4 synchronization processing is activated. If one and $\overline{AUTC}$ (see this register) is one, CRC-4 synchronization is disabled, and the first bits of time-slot 0 are used as international use bits and are programmed by the TIU0 and TIU1bits (see this register).
4	REFRM (0)	**Reframe.** A one-to-zero transition of this bit results in the execution of the reframing function (the search for a new basic frame position).
3	$\overline{AUTC}$ (0)	**Automatic CRC-interworking.** If zero, automatic CRC-interworking is activated. If one, it is deactivated. See Section 5.0 E1 Interface and Framing for a detailed description.
2	CRCM (0)	**CRC-4 Modification.** If one, the transmit CRC-4 remainder is modified when the device is in transmit transparent mode TxTRS=1 (see Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03). The received CRC-4 remainder is modified to reflect only the changes in the transmit DL. If zero, time-slot 0 data from DSTi will not be modified in transmit transparent mode.

Table 79 - E1 Alarms and Framing Control - R/W Address Y00

Bit	Name	Functional Description
1	$\overline{\text{AUTY}}$ (0)	**Automatic Y-Bit Operation.** This bit determines the source for the Remote Multiframe Alarm Indication bit (the Y bit) of the transmit PCM30 signal (time-slot 16 bit 6 of every frame 0 of the CAS multiframe). If zero, the source for the Y bit is the $\overline{\text{MSYNC}}$ status bit (see Table 105 E1 Synchronization & CRC-4 Remote Status - R Address Y10), and consequently, will change automatically. That is, Y=0 when multiframe alignment has been acquired ($\overline{\text{MSYNC}}$=0), and Y=1 when multiframe alignment has not been acquired ($\overline{\text{MSYNC}}$=1). If the $\overline{\text{AUTY}}$ bit is set to one, the Y bit is controlled through the Y control bit (see Table 89 - E1 CAS Control and Data - R/W Address Y05).
0	MFRF (0)	**Multiframe Reframe.** If one, for at least one frame, and then cleared, the selected framer (Y) will initiate a search for a new signaling multiframe position. Reframing function is activated on the one-to-zero transition of the MFRF bit.

Table 79 - E1 Alarms and Framing Control - R/W Address Y00

Bit	Name	Functional Description
15-12	(####)	Not Used
11 10	RZCS1 RZCS0 (00)	Receive Zero Code Suppression. RZCS1 RZCS0 Suppression 0 0 No Zero Code Suppression 0 1 GTE Zero Code Suppression 1 0 DDS Zero Code Suppression 1 1 Bell Zero Code Suppression See Section 4.1.1 T1 Encoding and Decoding Options.
9 8 7	TZCS2 TZCS1 TZCS0 (000)	Transmit Zero Code Suppression. TZCS2 TZCS1 TZCS0 Suppression 0 0 0 No Zero Code Suppression 0 0 1 GTE Zero Code Suppression 0 1 0 DDS Zero Code Suppression 0 1 1 Bell Zero Code Suppression 1 0 0 Jammed Bit 8 1 1 X Reserved 1 X 1 Reserved See Section 4.1.1 T1 Encoding and Decoding Options.
6	TPDV (0)	**Transmit PDV.** The output of the T1 data to be sent is monitored over a T1 frame and if the density is less than 12.5%, a bit is added in the non-framing bit.
5	TXB8ZS (0)	**Transmit Bipolar Eight Zero Substitution.** If one, all zero octets in the transmit path are substituted with B8ZS codes.
4	RXB8ZS (0)	**Receive Bipolar Eight Zero Substitution**. If one, B8ZS code words in the receive path are substituted with all zero octets. Bipolar violations associated with incoming B8ZS words will not be counted (see Table 120 - T1 Bipolar Violation Counter - R/W Address Y18).
3	ADSEQ (0)	**Digital Milliwatt or Digital Test Sequence.** If one, the mu-law digital milliwatt analog test sequence will be selected by the Per Timeslot Control bits TTSTn and RTSTn (see Table 166 - T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7). If zero, the PRBS 2^{15}-1 bit error rate test sequence will be selected by control bits TTSTn and RTSTn. The PRBS generator is reset whenever this bit is set to 1.
2	RZNRZ (0)	**Return to zero Non Return to zero.** If one return to zero input and outputs are expected at the framer-LIU interface. If zero, non return to zero input and output are expected. This is normally set to zero.

Table 80 - T1 Line Coding Control - R/W Address Y01

Bit	Name	Functional Description
1	UNIBI (0)	**Unipolar/Bipolar.** If one the input and output at the framer-LIU interface is assumed to be unipolar. The stream RPOS is the input and TPOS is the output. Setting this bit low causes the device to accept complementary bipolar inputs on RPOS/RNEG and to transmit complementary outputs on TPOS/TNEG. This is normally set to zero.
0	CLKE (0)	**Clock Edge.** If one, the NRZ data at the framer-LIU interface (RPOS/RNEG and TPOS/TNEG) is sampled on the rising edge of the extracted clock and transmitted on the falling edge of the transmitted clock. If zero, the opposite edges are used. This selection is only applicable in NRZ mode. This is normally set to zero.

Table 80 - T1 Line Coding Control - R/W Address Y01

Bit	Name	Functional Description
15-14	(00)	Not Used
13	L32Z (0)	**Digital Loss of Signal Selection**. If one, the threshold for digital loss of signal is 32 successive zeros. If zero, the threshold is set to 192 successive zeros. See the LOSS bit detailed in Table 109 - E1 Alarms & MAS Status - R Address Y12.
12	ADSEQ (0)	**Digital Milliwatt or Digital Test Sequence.** If one, the A-law digital milliwatt analog test sequence will be selected by the Per Timeslot Control bits TTSTn and RTSTn (see Table 167 - E1 Per Timeslot 0 to 31 Control Registers - R/W Address Y90-YAF). If zero, the PRBS 2^{15}-1 bit error rate test sequence will be selected by control bits TTSTn and RTSTn. The PRBS generator is reset whenever this bit is set to 1.
11	DLBK (0)	**Digital Loopback.** If one, all timeslots of DSTi are connected to DSTo at the framer to LIU interface point of the selected framer (Y). If zero, this feature is disabled. See Section 16.0 Loopbacks.
10	RSV (0)	**Reserved**. Must be set to 0 for normal operation.
9	SLBK (0)	**ST-BUS Loopback.** If one, all timeslots of DSTi are connected to DSTo on the ST-BUS side of the selected framer (Y). If zero, this feature is disabled. See Section 15.0 Loopbacks.
8	PLBK (0)	**Payload Loopback.** If one, all timeslots received on RTIP/RRNG are connected to TTIP/TRNG on the ST-BUS side of the selected framer (Y) (this excludes time-slot 0). If zero, this feature is disabled. See Section 15.0 Loopbacks.
7	E1 (0)	**E1 Error Insertion.** A zero-to-one transition of this bit inserts a single E1 error into the transmit PCM 30 data (bit position 1 of frame 13 of the CRC-4 Multiframe). A one, zero or one-to-zero transition has no function.
6	E2 (0)	**E2 Error Insertion.** A zero-to-one transition of this bit inserts a single E2 error into the transmit PCM 30 data (bit position 1 of frame 15 of the CRC-4 Multiframe). A one, zero or one-to-zero transition has no function.
5	BVE (0)	**Bipolar Violation Error Insertion.** A zero-to-one transition of this bit inserts a single bipolar violation error into the transmit PCM 30 data. A one, zero or one-to-zero transition has no function.
4	CRCE (0)	**CRC-4 Error Insertion.** A zero-to-one transition of this bit inserts a single CRC-4 error into the transmit PCM 30 data. A one, zero or one-to-zero transition has no function.
3	FASE (0)	**Frame Alignment Signal Error Insertion.** A zero-to-one transition of this bit inserts a single error into the timeslot zero frame alignment signal of the transmit PCM 30 data. A one, zero or one-to-zero transition has no function.
2	NFSE (0)	**Non-frame Alignment Signal Error Insertion.** A zero-to-one transition of this bit inserts a single error into bit two of the timeslot zero non-frame alignment signal of the transmit PCM 30 data. A one, zero or one-to-zero transition has no function.

Table 81 - E1 Test, Error and Loopback Control - R/W Address Y01

Bit	Name	Functional Description
1	LOSE (0)	**Loss of Signal Error Insertion.** If one, the selected framer (Y) transmits an all zeros signal (no pulses) in every PCM 30 timeslot, and, the $\overline{HDB3}$ control bit (see Table 83 - E1 Interrupts and I/O Control - R/W Address Y02) has no effect. If zero, data is transmitted normally.
0	PERR (0)	**Payload Error Insertion.** A zero-to-one transition of this bit inserts a single error in the transmit payload. A one, zero or one-to-zero transition has no function.

Table 81 - E1 Test, Error and Loopback Control - R/W Address Y01

Bit	Name	Functional Description
15-8	(#### ####)	Not Used
7	TESFY (0)	**Transmit ESF Yellow Alarm.** If one, while in ESF Mode, a repeating pattern of eight 1's followed by eight 0's is sent in the transmit FDL. In addition, this bit must be one if the japan yellow alarm is to be sent. See control bit JY detailed in Table 78 - T1 Framing Mode Control - R/W Address Y00
6	TXSECY (0)	**Transmit Secondary Yellow Alarm.** If one, the transmit secondary D4 yellow alarm is sent which causes the S bit for transmit frame 12 to be set.
5	TD4Y (0)	**Transmit D4 Yellow Alarm.** If one, bit 2 of all DS0 channels is forced low.
4	$\overline{TAIS}$ (1)	**Transmit All Ones.** if zero, this control bit forces a framed or unframed (depending on the state of Transmit Alarm Control bit 0) all ones to be transmit at TTIP and TRING.
3	(#)	Not Used
2	$\overline{TT1DMY}$ (1)	**Transmit T1DM Yellow Alarm.** If this bit is 0 a T1DM yellow alarm is sent on the 24th timeslot bit 2.
1	D4SECY (0)	**D4 Secondary Alarm.** Set this bit for trunks employing the secondary Yellow Alarm. The Fs bit in the 12th frame will not be used for counting errored framing bits. If a one is received in the Fs bit position of the 12th frame a Secondary Yellow Alarm Detect bit will be set.
0	SO (0)	**S-bit Override.** If set, this bit forces the S-bits to be inserted as an overlay on any of the following alarm conditions: i) transmit all ones ii) loop up code insertion iii) loop down code insertion.

Table 82 - T1 Transmit Alarm Control - R/W Address Y02

Bit	Name	Functional Description
15 14	COD1 COD0 (1 0)	**Line Coding.** These two coding select bits determine the transmit and receive coding options as follows: **COD1** **COD0** **Function** 0 0 RZ (Return to Zero, Dual Rail) 0 1 NRZ (Non-return to Zero, Single Rail) 1 0 NRZB (Non-return to Zero, Dual Rail) - Default 1 1 no function This is normally set to zero.
13	$\overline{RHDB3}$ (0)	**HDB3 (High Density Bipolar 3) RX decoding.** If zero, HDB3 decoding is enabled in the receive direction. If one, AMI (Alternate Mark Inversion) signal without HDB3 encoding is enabled in the receive direction.

Table 83 - E1 Interrupts and I/O Control - R/W Address Y02

Bit	Name	Functional Description
12	T2OP (0)	**T2o Polarity.** This is normally set to zero. If one, the T2o pin will output a 2.048MHz clock whose rising edge is in the center of the transmitted PCM30 bit cell at the TPOS and TNEG transmit pins. This clock is equivalent to the internal ST-BUS $\overline{C2}$ clock. If zero, the T2o pin will output a 2.048MHz clock whose falling edge is in the center of the transmitted PCM30 bit cell at the TPOS and TNEG transmit pins. This clock is equivalent to the internal ST-BUS C2 clock.
11	TXMFE (0)	**Transmit Multiframe Enable.** If one, the $\overline{TxMF}$ pin will be enabled. If zero, the $\overline{TxMF}$ pin will be disabled. See the $\overline{TxMF}$ pin description.
10	TX8KE (0)	**Transmit 8 KHz Enable.** This is normally set to zero but may be used in conjunction with the auxiliary signals, see Section 3.6 Auxiliary Output Signals. If one, the pin $\overline{RxMF}$ (AUX pin, see Section 3.6 Auxiliary Output Signals) transmits a positive 8 KHz frame pulse synchronous with the serial data stream transmit on TTIP/TRNG. If zero, the pin $\overline{RxMF}$ transmits a negative frame pulse synchronous with the multiframe boundary of data coming out of DSTo.
9	$\overline{SPND}$ (0)	**Suspend Interrupts.** If zero, the selected tranceivers contribution to the $\overline{IRQ}$ pin output will be a high impedance state, but all interrupt and latched status registers will continue to be updated. If one, the selected tranceivers contribution to the $\overline{IRQ}$ output will be normal operation.
8	$\overline{INTA}$ (0)	**Interrupt Acknowledge.** If zero, all interrupt and latched status registers are cleared and consequently, the selected tranceivers contribution to the $\overline{IRQ}$ pin output will be a high impedance state. If one, all interrupt and latched status registers operate normally, and the selected tranceivers contribution to the $\overline{IRQ}$ output will be normal operation.
7	CLKE (0)	**Clock Edge.** This is normally set to zero. If one, the NRZ data at the framer-LIU interface (RPOS/RNEG and TPOS/TNEG) is sampled on the rising edge of the extracted clock and transmitted on the falling edge of the transmitted clock. If zero, the opposite edges are used. This selection is only applicable in NRZ mode.
6	$\overline{THDB3}$ (0)	**HDB3 (High Density Bipolar 3) TX encoding.** If zero, HDB3 encoding is enabled in the transmit direction. If one, AMI (Alternate Mark Inversion) signal without HDB3 encoding is enabled in the transmit direction.
5	RXBFE (0)	**Receive Basic Frame Enable.** If one, the $\overline{RxBF}$ pin operates normally. If zero, the $\overline{RxBF}$ pin is low.
4	$\overline{RXDO}$ (0)	**Receive DSTo All Ones.** If one, the DSTo pin operates normally. If zero, all timeslots (0-31) of DSTo are set to one.
3	$\overline{RXCO}$ (0)	**Receive CSTo All Ones.** If one, the CSTo pin operates normally. If zero, all timeslots (0-31) of CSTo are set to one.
2	CSTOE (0)	**Output CSTo Enable.** If one, the CSTo pin operates normally. If zero, CSTo will be at high impedance. Note in 8 Meg mode all CSTOE for all framers have to be 0 to obtain high impedance.
1	DSTOE (0)	**Output DSTo Enable.** If one, the DSTo pin operates normally. If zero, DSTo will be at high impedance.
0	MFSEL (0)	**Multiframe Select.** This is normally set to zero but may be used in conjunction with the auxiliary signals, see Section 3.6 Auxiliary Output SIgnals. This bit determines which receive multiframe signal (CRC-4 or signaling) the frame pulse at the $\overline{RxMF}$ pin is aligned with. If zero, the frame pulse at the $\overline{RxMF}$ pin is aligned with the receive channel associated signaling (CAS) multiframe; if one, the receive CRC-4 multiframe.

Table 83 - E1 Interrupts and I/O Control - R/W Address Y02

Bit	Name	Functional Description
15-7	(#### #### #)	Not Used
6	L32Z (0)	**Digital Loss of Signal Selection**. If one, the threshold for digital loss of signal is 32 successive zeros. If zero, the threshold is set to 192 successive zeros. See the LOSS bit detailed in Table 104 - T1 Synchronization and Alarm Status - R Address Y10.

Table 84 - T1 Transmit Error Control - R/W Address Y03

Bit	Name	Functional Description
5	BPVE (0)	**Bipolar Violation Error Insertion.** A zero-to-one transition of this bit inserts a single bipolar violation error into the transmit DS1 data. A one, zero or one-to-zero transition has no function.
4	CRCE (0)	**CRC-6 Error Insertion.** A zero-to-one transition of this bit inserts a single CRC-6 error into the transmit ESF DS1 data. A one, zero or one-to-zero transition has no function.
3	FTE (0)	**Terminal Framing Bit Error Insertion.** A zero-to-one transition of this bit inserts a single error into the transmit D4 Ft pattern or the transmit ESF framing bit pattern (in ESF mode). A one, zero or one-to-zero transition has no function.
2	FSE (0)	**Signal Framing Bit Error Insertion.** A zero-to-one transition of this bit inserts a single error into the transmit Fs bits (in D4 mode only). A one, zero or one-to-zero transition has no function.
1	LOSE (0)	**Loss of Signal Error Insertion.** If one, the device transmits an all zeros signal (no pulses). Zero code suppression is overridden. If zero, data is transmitted normally.
0	PERR (0)	**Payload Error Insertion.** A zero-to-one transition of this bit inserts a single bit error in the transmit payload. A one, zero or one-to-zero transition has no function.

Table 84 - T1 Transmit Error Control - R/W Address Y03

Bit	Name	Functional Description
15-7	(#### #### #)	Not Used
6	ELAS (0)	**Elastic Buffer Enable.** When this bit is set to zero, the elastic buffer is enabled, and DSTo operates synchronously with the clock at the CKi pin. When this bit is set to one, the data at DSTo is a 2.048Mb/s serial output stream which contains all 32 timeslots of the received PCM30 link data after HDB3 decoding. This data does not pass through the elastic buffer and is clocked out with the falling edge of the extracted clock. The data at the DSTo pin is identical to the data at the RXD pin.
5	ACCLR (0)	**Automatic Counter Clear.** When this bit is set to one, all latchable status counters are cleared automatically by the one second timer bit ONESEC (Table 107 - E1 CRC-4 Timers & CRC-4 Local Status - R Address Y11) immediately following the counter latch operation. If zero, all latchable status counters operate normally.
4	RXTRS (0)	**Receive Transparent Mode.** If one, the framing function is disabled on the receive side. Data coming from the receive line passes through the elastic buffer and drives DSTo with an arbitrary alignment. When zero, the receive framing function operates normally.
3	TXTRS (0)	**Transmit Transparent Mode.** If one, the MT9071 is in transmit transparent mode where no framing or signaling is imposed on data transmitted from DSTi onto the PCM30 line. In other words, timeslot 0 data on the transmit PCM30 link is sourced from the DSTi input. If zero, the MT9071 is in termination mode.
2	CSIG (0)	**CCS and CAS Signaling.** If one, the MT9071 is in Common Channel Signaling (CCS) mode. If zero, the MT9071 is in Channel Associated Signaling (CAS) mode.
1	CNCLR (0)	**Counter Clear.** When this bit is changed from zero to one, status counters are cleared. If zero, all status counters operate normally.
0	RST (0)	**Reset**. When this bit is changed from zero to one, the selected framer (Y) will reset to its default mode. See Section 7.6 Reset Operation (RESET, TRST Pins).

Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03

Bit	Name	Functional Description
15-10	(#### ##)	Not Used

Table 86 - T1 Signaling Control - R/W Address Y04

Bit	Name	Functional Description
9	CSIGEN (0)	Common Channel Signaling Enable. Setting this bit enables common channel Signaling. See Table 100 - T1 CCS Map Control - R/W Address Y0B for the mapping between the CST and PCM streams.
8	RBEN (0)	**Robbed Bit Signaling Enable.** Setting this bit multiplexes the AB or ABCD signaling bits into bit position 8 of all DS0 channels of every 6th frame; providing the control register bit CC detailed in Table 166 - T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7 is not set.
7	(#)	Not Used
6	RSDB (0)	**Receive Signaling Debounce.** Setting this bit causes incoming signaling bits to be debounced for a period of 6 to 9 milliseconds before reporting on CSTo streams or in the receive signaling data registers see Table 164 - T1 Receive CAS Data Registers - R Address Y70-Y87.
5	RFL (0)	**Receive Signaling Freeze due to Loss.** If one, the receive signaling is frozen if a receive loss of signal is detected. The freeze is cleared upon clearance of loss.
4	(#)	Not Used
3 2	SM1 SM0 (00)	**Signaling Message.** These two bits are used to fill the vacant bit positions available on CSTo when the device is operating on a D4 trunk. The first two bits of each reporting nibble of CST contain the AB signaling bits. The last two will contain SM1 and SM0 (in that order). When the device is connected to ESF trunks, four signaling bits (ABCD) are reported and the bits SM1-0 are unusable.
1-0	SIP1 SIP0	**Signaling Interrupt Period.** These two bits determine the update interval of the signaling interrupt bit CASRI detailed in Table 151 - T1 Receive Line and Timer Interrupt Status - R Address Y35. SIP1 SIP0 Function 0 0 1 msec period 0 1 4 msec period 1 0 8 msec period 1 1 16 msec period

Table 86 - T1 Signaling Control - R/W Address Y04

Bit	Name	Functional Description
15-2	(#### #### #### ##)	Not Used
1-0	SIP1 SIP0	**Signaling Interrupt Period.** These two bits determine the update interval of the signaling interrupt bit CASRI detailed in Table 154 - E1 National Interrupt Status - R Address Y36. SIP1 SIP0 Function 0 0 1 msec period 0 1 4 msec period 1 0 8 msec period 1 1 16 msec period

Table 87 - E1 Signaling Control - R/W Address Y04

Bit	Name	Functional Description
15-6	(#### #### ##)	Not Used
5	DLBK (0)	**Digital Loopback.** If one, all timeslots of DSTi are connected to DSTo at the framer to LIU interface point of the selected framer (Y). If zero, this feature is disabled. See Section 15.0 Loopbacks.

Table 88 - T1 LoopBack Control - R/W Address Y05

Bit	Name	Functional Description
4	RSV (0)	**Reserved**. Must be set to 0 for normal operation.
3	SLBK (0)	**ST-BUS Loopback.** If one, the first 24 timeslots and the last bit in the frame of DSTi are connected to DSTo on the ST-BUS side of the selected framer (Y). If zero, this feature is disabled. See Section 15.0 Loopbacks.
2	PLBK (0)	**Payload Loopback.** If one, all timeslots received on RTIP/RRNG are connected to TTIP/TRNG on the ST-BUS side of the selected framer (Y). If zero, this feature is disabled. See Section 15.0 Loopbacks.
1	TLU (0)	**Transmit Loop Up Code**. If this bit is set, inband line loop up code is sent. The loop up code to be sent is determined by the TXLACL data bits detailed in Table 101 - T1 Transmit Loop Activate Code Control - R/W Address Y0D. Note that the receiver will detect either framed or unframed inband loop codes.
0	TLD (0)	**Transmit Loop Down Code**. If this bit is set, inband line loop down code is sent. The loop down code to be sent is determined by the TXLDCL data bits detailed in Table 102 - T1 Transmit Loop Deactivate Code Control - R/W Address Y0E. Note that the receiver will detect either framed or unframed inband loop codes.

Table 88 - T1 LoopBack Control - R/W Address Y05

Bit	Name	Functional Description
15-11	(#### #)	Not Used
11	RFL (0)	**Receive Signaling Freeze due to Loss.** If one, the receive signaling is frozen if a receive loss of signal is detected. The freeze is cleared upon clearance of loss.
10	DBNCE (0)	**Debounce Select.** This bit selects the receive CAS debounce period. If one, 14 ms of debounce is used. There may be as much as 2 ms added to this duration because the state change of the signaling equipment is not synchronous with the PCM 30 signaling multiframe. If zero, no debounce is used.
9-8	(##)	Not Used
7 6 5 4	TMA1 TMA2 TMA3 TMA4 (0000)	**Transmit Multiframe Alignment Bits One to Four.** These bits are transmitted on the PCM30 link, in the Multiframe Alignment Signal (MFAS) positions (one to four of timeslot 16) of frame zero of every Channel Associated Signaling (CAS) multiframe. These bits are used by the far end to identify specific frames of a CAS multiframe. TMA1-4 = 0000 for normal operation.
3	X1 (1)	**Transmit Non-Multiframe Alignment Signal (NMAS) Spare Bit.** This bit is transmitted on the PCM30 link in bit position five of timeslot 16 of frame zero of every signaling multiframe. X1 is normally set to one.
2	Y (1)	**Transmit Remote Multiframe Alarm Signal.** This bit is transmitted on the PCM30 link in bit position six of timeslot 16 of frame zero of every signaling multiframe when control bit $\overline{AUTY}$ (see Table 79 - E1 Alarms and Framing Control - R/W Address Y00) is set to one. The Y bit is used to indicate the loss of multiframe alignment to the remote end of the link. If one, loss of multiframe alignment; if zero, multiframe alignment acquired.
1 0	X2 X3 (11)	**Transmit Non-Multiframe Alignment Signal (NMAS) Spare Bits.** These bits are transmitted on the PCM30 link in bit positions seven and eight respectively, of timeslot 16 of frame zero of every signaling multiframe. X2 and X3 are normally set to one.

Table 89 - E1 CAS Control and Data - R/W Address Y05

Bit	Name	Functional Description
15-12	(####)	Not Used

Table 90 - T1 HDLC & DataLink Control - R/W Address Y06

Bit	Name	Functional Description
11 10 9 8 7	HCH4 HCH3 HCH2 HCH1 HCH0 (0000 0)	**HDLC Channel 4-0.** This 5 bit number specifies the channel the HDLC will be attached to if enabled. Number 0 maps to the first channel in a frame. Number 23 maps to channel 24 (the last channel available in a T1 frame). The transmit HDLC data will replace DSTi data. And the receive line data before the elastic buffer will be loaded in the HDLC receiver. This feature is enabled wit the HPAYSEL control bit of this register.
6	HPAYSEL (0)	**HDLC Payload Select.** When one, the HDLC will be attached to the T1 channel as specified with the HCH4-0 control bits. When zero, and when the HDLCEN bit of this register is set, the HDLC is attached to the FDL when in ESF mode.
5 4 3	RSV (000)	**Reserved**. Must be set to 0 for normal operation.
2	BOMEN (0)	**Bit Oriented Message Enable.** Setting this bit enables transmission of bit - oriented messages on the ESF facility data link. The actual message transmitted at any one time is contained in the TXBOM data bits detailed in Table 92 - T1 Transmit BOM Data - R/W Address Y07.
1	HDLCEN (0)	**HDLC Enable.** Must be set to one for HDLC operation.
0	H1R64 (0)	**HDLC Rate Select**. Setting this pin high while an HDLC is activated on a timeslot enables 64 Kb/s operation. Setting this pin low while an HDLC is activated enables 56 Kb/s operation (this prevents data corruption due to forced bit stuffing).

Table 90 - T1 HDLC & DataLink Control - R/W Address Y06

Bit	Name	Functional Description
15-12	(####)	Not Used
11-7	HCH4 HCH3 HCH2 HCH1 HCH0 (0000 0)	**HDLC Channel 4-0.** This 5 bit number specifies the PCM30 timeslot the internal HDLC is assigned to. Timeslots 1 to 31 may be selected providing HPAYSEL of this register is one. HDLC data will be substituted for data from DSTi on the transmit side. Receive data is extracted from the incoming line data before the elastic buffer. Timeslot 0 is selected when HPAYSEL is zero.
6	HPAYSEL (0)	**HDLC Payload Select.** If one, the HDLC is assigned to one of the timeslots assigned with control bits HCH4-0 of this register. If zero, the HDLC may be assigned to timeslot 0 in accordance with the SA select bits detailed in Table 95 - E1 Data Link Control - R/W Address Y08.
5 4 3	RSV RSV RSV (000)	**Reserved**. Must be set to 0 for normal operation.
2	TS31E (0)	**Time Slot 31 CST Enable.** If one, the transmit PCM30 link timeslot 31 data will be sourced from a CSTi timeslot as selected by control bits 31C4 to 31C0 detailed in Table 93 - E1 CCS CSTi and CSTo Map Control - R/W Address Y07. And, the receive PCM30 link timeslot 31 data will be sourced to both DSTo timeslot 31 and to the above selected CSTo timeslot. This feature is used to link PCM30 CCS data to an external HDLC device through the CSTo and CSTi pins. If zero, the transmit PCM30 link timeslot 31 data will be sourced from DSTi timeslot 31. And, the receive PCM30 link timeslot 31 data will be sourced to DSTo timeslot 31 only. Common Channel Signaling (CSIG =1 detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) must be selected for these operations to be valid.

Table 91 - E1 HDLC and CCS ST-BUS Control - R/W Address Y06

Bit	Name	Functional Description
1	TS16E (0)	**Time Slot 16 CST Enable.** If one, the transmit PCM30 link timeslot 16 data will be sourced from a CSTi timeslot as selected by control bits 16C4 to 16C0 detailed in Table 93 - E1 CCS CSTi and CSTo Map Control - R/W Address Y07. And, the receive PCM30 link timeslot 16 data will be sourced to both DSTo timeslot 16 and to the above selected CSTo timeslot. This feature is used to link PCM30 CCS data to an external HDLC device through the CSTo and CSTi pins. If zero, the transmit PCM30 link timeslot 16 data will be sourced from DSTi timeslot 16. And, the receive PCM30 link timeslot 16 data will be sourced to DSTo timeslot 16 only. Common Channel Signaling (CSIG =1 detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) must be selected for these operations to be valid.
0	TS15E (0)	**Time Slot 15 CST Enable.** If one, the transmit PCM30 link timeslot 15 data will be sourced from a CSTi timeslot as selected by control bits 15C4 to 15C0 detailed in Table 93 - E1 CCS CSTi and CSTo Map Control - R/W Address Y07. And, the receive PCM30 link timeslot 15 data will be sourced to both DSTo timeslot 15 and to the above selected CSTo timeslot. This feature is used to link PCM30 CCS data to an external HDLC device through the CSTo and CSTi pins. If zero, the transmit PCM30 link timeslot 15 data will be sourced from DSTi timeslot 15. And, the receive PCM30 link timeslot 15 data will be sourced to DSTo timeslot 15 only. Common Channel Signaling (CSIG =1 detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) must be selected for these operations to be valid.

Table 91 - E1 HDLC and CCS ST-BUS Control - R/W Address Y06

Bit	Name	Functional Description
15-8	(#### ####)	Not Used
7 6 5 4 3 2 1 0	TXBOM7 TXBOM6 TXBOM5 TXBOM4 TXBOM3 TXBOM2 TXBOM1 TXBOM0 (0000 0000)	**Transmit Bit Oriented Message.** The contents of this register are concatenated with a sequence of eight 1's and are continuously transmitted in the FDL bit position of ESF trunks. Normally, the first and last bit of this register are set to zero.

Table 92 - T1 Transmit BOM Data - R/W Address Y07

Bit	Name	Functional Description
15	(#)	Not Used
14 13 12 11 10	31C4 31C3 31C2 31C1 31C0 (11111)	**Timeslot 31 CST Map Bits.** The selection of these bits results in a mapping of the transmit PCM30 timeslot 31, from a specific CSTi timeslot; and similarly, maps receive PCM30 timeslot 31, to a specific CSTo timeslot. PCM30 timeslot 31 data is mapped to/from CST channel n (n=0 to 31), where n is the bcd equivalent of 31C4 to 31C0 with 31C4 being the most significant bit. 31C4 31C3 31C2 31C1 31C0 CST Timeslot 0 0 0 0 0 0 0 0 0 0 1 1 etc. 1 1 1 1 1 31 Control bit CSIG of E1 DL, CCS, CAS and Other Control - R/W Address Y03, and control bit TS31E of E1 HDLC and CCS ST-BUS Control - R/W Address Y06 must both be set for these operations to be valid.

Table 93 - E1 CCS CSTi and CSTo Map Control - R/W Address Y07

Bit	Name	Functional Description
9 8 7 6 5	16C4 16C3 16C2 16C1 16C0 (10000)	**Timeslot 16 CST Map Bits.** The selection of these bits results in a mapping of the transmit PCM30 timeslot 16, from a specific CSTi timeslot; and similarly, maps receive PCM30 timeslot 16, to a specific CSTo timeslot. PCM30 timeslot 16 data is mapped to/from CST channel n (n=0 to 31), where n is the bcd equivalent of 16C4 to 16C0 with 16C4 being the most significant bit. 16C4 16C3 16C2 16C1 16C0 CST Timeslot 0 0 0 0 0 0 0 0 0 0 1 1 etc. 1 1 1 1 1 31 Control bit CSIG of E1 DL, CCS, CAS and Other Control - R/W Address Y03, and control bit TS16E of E1 HDLC and CCS ST-BUS Control - R/W Address Y06 must both be set for these operations to be valid.
4 3 2 1 0	15C4 15C3 15C2 15C1 15C0 (01111)	**Timeslot 15 CST Map Bits.** The selection of these bits results in a mapping of the transmit PCM30 timeslot 15, from a specific CSTi timeslot; and similarly, maps receive PCM30 timeslot 15, to a specific CSTo timeslot. PCM30 timeslot 15 data is mapped to/from CST channel n (n=0 to 31), where n is the bcd equivalent of 15C4 to 15C0 with 15C4 being the most significant bit. 15C4 15C3 15C2 15C1 15C0 CST Timeslot 0 0 0 0 0 0 0 0 0 0 1 1 etc. 1 1 1 1 1 31 Control bit CSIG of E1 DL, CCS, CAS and Other Control - R/W Address Y03, and control bit TS15E of E1 HDLC and CCS ST-BUS Control - R/W Address Y06 must both be set for these operations to be valid.

Table 93 - E1 CCS CSTi and CSTo Map Control - R/W Address Y07

Bit	Name	Functional Description
15-8	(#### ####)	Not Used
7 6 5 4 3 2 1 0	RXBOMM7 RXBOMM6 RXBOMM5 RXBOMM4 RXBOMM3 RXBOMM2 RXBOMM1 RXBOMM0 (0000 0000)	**Receive Bit Oriented Message Match.** The contents of this register are compared to the received data bits detailed in Table 108 - T1 Receive Bit Oriented Message - R Address Y12, and an a maskable interrupt BOMMI (see Table 151 - T1 Receive Line and Timer Interrupt Status - R Address Y35) is generated if the contents match.

Table 94 - T1 Receive BOM Match Control - R/W Address Y08

Bit	Name	Functional Description
15	(#)	Not Used
14 13	SA4S1 SA4S0 (00)	**SA4 Source Select.** These 2 bits select the source of the Sa4 transmit data in timeslot 0 of the PCM30 link. The receive data is always sent to the T1 & E1 HDLC Receive CRC Data - R/W Address Y1E, the E1 Receive National Bit Sa4 Data Register - R Address YC0 and to DSTo timeslot 0 bit 4. SA4S1 SA4S0 Source Data for the Sa4 bit of Timeslot 0 0 0 E1 Transmit National Bits Sa4 - Sa8 Data Registers - R/W Address YB0-YB4 0 1 Reserved 1 0 ST-BUS DSTi timeslot 0 bit 4 1 1 HDLC transmitter T1 & E1 HDLC Transmit FIFO Data - R/W Address YF5
12 11	SA5S1 SA5S0 (00)	**SA5 Source Select.** These 2 bits select the source of the Sa5 transmit data in timeslot 0 of the PCM30 link. The receive data is always sent to the T1 & E1 HDLC Receive CRC Data - R/W Address Y1E, the E1 Receive National Bit Sa5 Data Register - R Address YC1 and to DSTo timeslot 0 bit 3. SA5S1 SA5S0 Source Data for the Sa5 bit of Timeslot 0 0 0 E1 Transmit National Bits Sa4 - Sa8 Data Registers - R/W Address YB0-YB4 0 1 Reserved 1 0 ST-BUS DSTi timeslot 0 bit 3 1 1 HDLC transmitter T1 & E1 HDLC Transmit FIFO Data - R/W Address YF5
10 9	SA6S1 SA6S0 (00)	**SA6 Source Select.** These 2 bits select the source of the Sa4 transmit data in timeslot 0 of the PCM30 link. The receive data is always sent to the T1 & E1 HDLC Receive CRC Data - R/W Address Y1E, the E1 Receive National Bit Sa6 Data Register - R Address YC2 and to DSTo timeslot 0 bit 2. SA6S1 SA6S0 Source Data for the Sa6 bit of Timeslot 0 0 0 E1 Transmit National Bits Sa4 - Sa8 Data Registers - R/W Address YB0-YB4 0 1 Reserved 1 0 ST-BUS DSTi timeslot 0 bit 2 1 1 HDLC transmitter T1 & E1 HDLC Transmit FIFO Data - R/W Address YF5
8 7	SA7S1 SA7S0 (00)	**SA7 Source Select.** These 2 bits select the source of the Sa4 transmit data in timeslot 0 of the PCM30 link. The receive data is always sent to the T1 & E1 HDLC Receive CRC Data - R/W Address Y1E, the E1 Receive National Bit Sa7 Data Register - R Address YC3 and to DSTo timeslot 0 bit 1. SA7S1 SA7S0 Source Data for the Sa7 bit of Timeslot 0 0 0 E1 Transmit National Bits Sa4 - Sa8 Data Registers - R/W Address YB0-YB4 0 1 Reserved 1 0 ST-BUS DSTi timeslot 0 bit 1 1 1 HDLC transmitter T1 & E1 HDLC Transmit FIFO Data - R/W Address YF5
6 5	SA8S1 SA8S0 (00)	**SA8 Source Select.** These 2 bits select the source of the Sa4 transmit data in timeslot 0 of the PCM30 link. The receive data is always sent to the T1 & E1 HDLC Receive CRC Data - R/W Address Y1E, the E1 Receive National Bit Sa8 Data Register - R Address YC4 and to DSTo timeslot 0 bit 0. SA8S1 SA8S0 Source Data for the Sa8 bit of Timeslot 0 0 0 E1 Transmit National Bits Sa4 - Sa8 Data Registers - R/W Address YB0-YB4 0 1 Reserved 1 0 ST-BUS DSTi timeslot 0 bit 0 1 1 HDLC transmitter T1 & E1 HDLC Transmit FIFO Data - R/W Address YF5
4-2	(###)	Not Used
1-0	RSV (00)	**Reserved**. Must be set to 0 for normal operation.

Table 95 - E1 Data Link Control - R/W Address Y08

Bit	Name	Functional Description
15-8	(#### ####)	Not Used
7 6 5 4 3 2 1 0	RXIDC7 RXIDC6 RXIDC5 RXIDC4 RXIDC3 RXIDC2 RXIDC1 RXIDC0 (0000 0000)	**Receive Idle Code.** This data is sent on the corresponding DSTo timeslot as selected by control bit MPDR in the T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7.

Table 96 - T1 Receive Idle Code Data - R/W Address Y09

Bit	Name	Functional Description
15-8	(#### ####)	Not Used
7 6 5 4 3 2 1 0	RXIDC7 RXIDC6 RXIDC5 RXIDC4 RXIDC3 RXIDC2 RXIDC1 RXIDC0 (0000 0000)	**Receive Idle Code.** This data is sent on the corresponding DSTo timeslot as selected by control bit MPDR in the E1 Per Timeslot 0 to 31 Control Registers - R/W Address Y90-YAF.

Table 97 - E1 Receive Idle Code Data - R/W Address Y09

Bit	Name	Functional Description
15-8	(#### ####)	Not Used
7 6 5 4 3 2 1 0	TXIDC7 TXIDC6 TXIDC5 TXIDC4 TXIDC3 TXIDC2 TXIDC1 TXIDC0 (0000 0000)	**Transmit Idle Code.**This data is sent on the corresponding DS1 channel as selected by control bit MPDT in the T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7.

Table 98 - T1 Transmit Idle Code Data - R/W Address Y0A

Bit	Name	Functional Description
15-8	(#### ####)	Not Used

Table 99 - E1 Transmit Idle Code Data - R/W Address Y0A

127

Bit	Name	Functional Description
7	TXIDC7	**Transmit Idle Code.** This data is sent on the corresponding PCM30 timeslot as selected by
6	TXIDC6	control bit MPDT in the E1 Per Timeslot 0 to 31 Control Registers - R/W Address Y90-YAF.
5	TXIDC5	
4	TXIDC4	
3	TXIDC3	
2	TXIDC2	
1	TXIDC1	
0	TXIDC0	
	(0000 0000)	

Table 99 - E1 Transmit Idle Code Data - R/W Address Y0A

Bit	Name	Functional Description
15-10	(#### ##)	Not Used
9 8 7 6 5	CST4 CST3 CST2 CST1 CST0 (00 000)	**CST CCS Map Bits.** These bits determine the CSTi and CSTo timeslots used for CCS. DS1 CCS channel data is mapped to/from CST timelsot n (n=0 to 23), where n is the bcd equivalent of CST4 to CST0 with CST4 being the most significant bit. CST4 CST3 CST2 CST1 CST0 CST Timeslot 0 0 0 0 0 0 0 0 0 0 1 1 etc. 1 0 1 1 1 23 For these operations to be valid, set the CCS enable control register bit CSIGEN (see Table 86 - T1 Signaling Control - R/W Address Y04). All unused CSTo timeslots are high impedance.
4 3 2 1 0	PCM4 PCM3 PCM2 PCM1 PCM0 (0 0000)	**PCM CCS Map Bits.** These bits determine the DS1 transmit and receive channels used for CCS. ST-BUS CSTi/CSTo timeslots are mapped to/from DS1 channel n (n=1 to 24), where n is one plus the bcd equivalent of PCM4 to PCM0 with PCM4 being the most significant bit. PCM4 PCM3 PCM2 PCM1 PCM0 DS1 Channel 0 0 0 0 0 1 0 0 0 0 1 2 1 0 1 1 1 24 For these operations to be valid, set the CCS enable control register bit CSIGEN (see Table 86 - T1 Signaling Control - R/W Address Y04).

Table 100 - T1 CCS Map Control - R/W Address Y0B

Bit	Name	Functional Description
15-10	(#### ##)	Not Used

9
8
	TXLACL1
	TXLACL0
	(00)
		Transmit Loop Activate Code Length. This 2 bits define the length of the transmit loop up code.
		    00-Code length is 5 bits
		    01-Code length is 6 or 3 bits
		    10-Code length is 7 bits
		    11-Code length is 8 or 4 bits
		Note if 4 bit code is required, the TXLAC7-0 bits (in this register) have to be repeated. For instance if the code 1011 is desired, the TXLAC7-0 has to be set to 10111011 and the length to 11.

7-0	TXLAC7 TXLAC6 TXLAC5 TXLAC4 TXLAC3 TXLAC2 TXLAC1 TXLAC0 (0000 0001)	**Transmit Loop Activate Code.** This byte specifies the inband loop up code to be transmitted. For example, if 00001 is to be transmitted as a loop up code; the register has to programmed to a value of 00100001 and the length has to be set to 5 bits (TXLACL1-0 = 00). The default values are the T1.403 values for loop activate code.

Table 101 - T1 Transmit Loop Activate Code Control - R/W Address Y0D

Bit	Name	Functional Description
15-10	(#### ##)	Not Used
9 8	TXLDCL1 TXLDCL0 (01)	**Transmit Loop Deactivate Code Length.** This 2 bits define the length of the transmit loop down code. 00-Code length is 5 bits 01-Code length is 6 or 3 bits 10-Code length is 7 bits 11-Code length is 8 or 4 bits
7 6 5 4 3 2 1 0	TXLDC7 TXLDC6 TXLDC5 TXLDC4 TXLDC3 TXLDC2 TXLDC1 TXLDC0 (0000 1001)	**Transmit Loop Deactivate Code.** This byte specifies the inband loop down code to be transmitted. For example, if 001 is to be transmitted as a loop down code; the register has to programmed to a value of 01001001and the length has to be set to 3 bits (TXLDCL1-0 = 01). The default values are the T1.403 values for loop deactivate code.

Table 102 - T1 Transmit Loop Deactivate Code Control - R/W Address Y0E

Bit	Name	Functional Description
15-10	(#### ##)	Not Used
9 8	RXLACL1 RXLACL0 (00)	**Receive Loop Activate Code Length.** This 2 bits define the length of the receive loop up code. 00-Code length is 5 bits 01-Code length is 6 or 3 bits 10-Code length is 7 bits 11-Code length is 8 or 4 bits
7 6 5 4 3 2 1 0	RXLACM7 RXLACM6 RXLACM5 RXLACM4 RXLACM3 RXLACM2 RXLACM1 RXLACM0 (0000 0001)	**Receive Loop Activate Code Match.**This byte specifies the match code for the receive loopback activate code. The contents of this register are compared to the received data, and a maskable interrupt LLEDI (see Table 151 - T1 Receive Line and Timer Interrupt Status - R Address Y35) is generated if the contents match.

Table 103 - T1 Receive Loop Activate Code Match Control - R/W Address Y0F

Bit	Name	Functional Description
15-14	(##)	Not Used
13	$\overline{\text{TFSYNC}}$ (0)	**Terminal Frame Synchronization**. Indicates the Terminal Frame Synchronization status (1 - loss; 0 - acquired). For ESF links, terminal frame synchronization and multiframe synchronization are synonymous. This bit is also used for indicating T1DM sync status.
12	$\overline{\text{MFSYNC}}$ (0)	**Multiframe Synchronization.** Indicates the Multiframe Synchronization status (1 - loss; 0 - acquired). For ESF links multiframe synchronization and terminal frame synchronization are synonymous.
11	SEF (0)	**Severely Errored Frame**. This bit toggles when 2 of the last 6 received framing bits are in error. The framing bits monitored are the ESF framing bits for ESF links and the Ft and Fs bits for D4 links (see Table 78 - T1 Framing Mode Control - R/W Address Y00).
10	LOS (0)	**Digital Loss of Signal.** This bit goes high after the detection of 192 or 32 consecutive zeros as set by the control bit L32Z detailed in Table 84 - T1 Transmit Error Control - R/W Address Y03. It returns low when the incoming pulse density exceeds 12.5% over a 250 microsecond period.
9	D4Y (0)	**D4 Yellow Alarm.** This bit is set if bit position 2 of virtually every DS0 channel is a zero for a period of 600 milliseconds. The alarm is tolerant of errors by permitting up to 16 ones in a 48 millisecond integration period. The alarm clears in 200 milliseconds after being removed from the line.
8	D4Y48 (0)	**D4 Yellow Alarm - 48 millisecond sample.** This bit is set if bit position 2 of virtually every DS0 channel is a zero for a period of 48 milliseconds. The alarm is tolerant of errors by permitting up to 16 ones in the integration period. This bit is updated every 48 milliseconds.
7	SECY (0)	**Secondary D4 Yellow Alarm.** This bit is set if 2 consecutive '1's are received in the S-bit position of the 12th frame of the D4 superframe.
6	ESFY (0)	**ESF Yellow Alarm.** This bit is set if the ESF yellow alarm (8 zero's followed by 8 one's) is received in seven or more codewords out of ten in the Bit Oriented Message location which are the FDL bits.
5	AIS (0)	**AIS Alarm.** This bit is set if less than 5 zeros are received in a 3 millisecond window. This bit is high after power up.
4	PDV (0)	**Pulse Density Violation.** This bit toggles if the receive data fails to meet ones density requirements. It will toggle upon detection of 16 consecutive zeros on the line data, or if there are less than N ones in a window of 8(N+1) bits - where N = 1 to 23.
3	LLED (0)	**Line Loopback Enable Detect.** This bit is set when a framed or unframed repeating pattern (default pattern is 00001) has been detected during a 48 millisecond interval. Up to fifteen errors are permitted per integration period. The code detected is dependent on the RXLACM7-0 data bits detailed in Table 103 - T1 Receive Loop Activate Code Match Control - R/W Address Y0F.
2	LLDD (0)	**Line Loopback Disable Detect.** This bit is set when a framed or unframed repeating pattern (default pattern is 001) has been detected during a 48 millisecond interval. Up to fifteen errors are permitted per integration period.The code detected is dependent on the RXLACM7-0 data bits detailed in Table 177 - T1 Receive Loop Deactivate Code Match - R/W Address YF0.
1	T1DMR (0)	**T1DM Received R bit**. If T1DM mode is selected, this bit indicates the status of the bit (R-bit) received on the DS1 link in bit position 1 of timeslot 24 of all frames. This bit is used for an AT&T 8 Kb/s communications channel. Updated on a frame basis.
0	$\overline{\text{T1DMY}}$ (1)	**T1DM Received Yellow Alarm**. If T1DM mode is selected, this bit indicates the status of the bit (Y-bit) received on the DS1 link in bit position 2 of timeslot 24 of all frames. If zero, there is currently a yellow alarm condition. Updated on a frame basis.

Table 104 - T1 Synchronization and Alarm Status - R Address Y10

Bit	Name	Functional Description
15	(#)	Not Used
14	RSLP	**Receive Slip.** This bit changes state when a receive controlled frame slip has occurred.
13	RSLPD	**Receive Slip Direction.** If one, indicates that the last received frame slip (RSLP of this register) resulted in a repeated frame. This would occur if the system clock (CKb/2) was faster than the network clock (RxCK). If zero, indicates that the last received frame slip (RSLP) resulted in a lost frame. This would occur if the system clock was slower than the network clock. Updated on an RSLP occurrence basis.
12	$\overline{\text{BSYNC}}$	**Receive Basic Frame Alignment.** If zero, indicates the received PCM30 link basic frame alignment pattern (x0011011 in timeslot 0 of alternate frames) is acquired; if one, the basic frame alignment pattern is lost or not acquired.
11	$\overline{\text{MSYNC}}$	**Receive Multiframe Alignment.** If zero, indicates the received PCM30 link signaling multiframe alignment signal (0000xxxx in timeslot 16 of every16th frame) is acquired; if one, the signaling multiframe alignment signal is lost or not acquired.
10	$\overline{\text{CSYNC}}$	**Receive CRC-4 Synchronization.** If zero, indicates the received PCM30 link CRC-4 multiframe alignment pattern (001011xx in timeslot 0, in bit position 1 of 16 alternate frames) is acquired; if one, the CRC-4 multiframe alignment pattern is lost or not acquired.
9	RED	**RED Alarm.** If one, indicates that basic frame alignment ($\overline{\text{BSYNC}}$ of this register) has been lost for at least 100 msec. This bit is cleared (zero) when basic frame alignment is acquired.
8	CEFS	**Consecutively Errored Frame Alignment Signal.** If one, the last two frame alignment signals (FAS=0011011) were received in error. If zero, at least one of the last two frame alignment signals were received without error. A non-errored FAS would result in the RFA2-8 status bits (see Table 111 - E1 NFAS Signal and FAS Status - R Address Y13) set as follows, 0011011. This bit is low when $\overline{\text{BSYNC}}$ is low.
7	(#)	Not Used
6	RCRC0	**Remote CRC-4 and RAI T10.** If one, the received A bits were one and either of the received E bits were zero (see RCRCR of this register) continuously for more than 10ms. See I.431 section 3.4.1.2 on RAI and continuous CRC error information.
5	RCRC1	**Remote CRC-4 and RAI T450.** If one, the received A bits were one and the received E bits were zero (see RCRCR of this register) continuously for more than 10ms but less than 450ms. See I.431 section 3.4.1.2 on RAI and continuous CRC error information.
4	RFAIL	**Remote CRC-4 Multiframe Generator/Detector Failure.** If one, each of the previous five seconds have an E-bit (E1 + E2) of error count of greater than 989 (E-bit counter 3DD hex or 11 1101 1101, see Table 119 - E1 E-bit Error Counter - R/W Address Y17), and for this same period the receive RAI bit (see Table 111 - E1 NFAS Signal and FAS Status - R Address Y13) was zero (no remote alarm), and for the same period the $\overline{\text{BSYNC}}$ bit (of this register) was equal to zero (basic frame alignment has been maintained). If zero, indicates normal operation.
3	REB1	**Receive E1 Bit Status.** Indicates the status of the bit (E1) received on the PCM30 link in bit position 1 of timeslot 0 in non-frame alignment signal (NFAS) frame 13. If zero, the remote end calculated a CRC-4 error in its received sub-multiframe one. If one, no error was calculated. Note that with the $\overline{\text{CSYNC}}$ bit (of this register) at one, the REB1 bit is one.
2	REB2	**Receive E2 Bit Status.** Indicates the status of the bit (E2) received on the PCM30 link in bit position 1 of timeslot 0 in non-frame alignment signal (NFAS) frame 15. If zero, the remote end calculated a CRC-4 error in its received sub-multiframe two. If one, no error was calculated. Note that with the $\overline{\text{CSYNC}}$ bit (of this register) at one, the REB2 bit is one.
1	RCRCR	**Remote CRC-4 and RAI.** This bit is one when the RAI (A) status bit (see Table 111 - E1 NFAS Signal and FAS Status - R Address Y13) is one, and either the REB1 (E1) or REB2 (E2) status bits (of this register) are zero. If zero, the above requirement is not met. This bit is updated with the PRBS CRC-4 multiframe counter clock (see Table 115 - E1 PRBS Error Counter & PRBS CRC Multiframe Counter - R/W Address Y15).

Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10

Bit	Name	Functional Description
0	CRCIW	**CRC-4 Interworking.** If one, indicates the CRC-4 interworking status is CRC-4 to CRC-4 (local to remote). The transmit PCM30 link is framed to CRC-4 with E1 and E2 bits sent, and the receive PCM30 link is treated as CRC-4 with E1 and E2 bits received. If zero, indicates the CRC-4 interworking status is CRC-4 to non-CRC (local to remote). In this case, the transmit PCM30 link is framed to CRC-4 but the E1 and E2 bits are not sent, and the receive PCM30 link is not treated as a CRC-4 multiframe but only as a basic frame and signaling multiframe frame only.

Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10

Bit	Name	Functional Description
15-3	(#### #### ####)	Not Used
2	ONESEC	**One Second Timer Status.** This bit toggles from low to high once every second, and is synchronous with the applied125us frame pulse at pin FPb.
1	TWOSEC	**Two Second Timer Status.** This bit toggles from low to high once every two seconds, and is synchronous with the applied125us frame pulse at pin FPb.
0	(#)	Not Used

Table 106 - T1 Timer Status - R Address Y11

Bit	Name	Functional Description
15-14	(##)	Not Used
13	ONESEC	**One Second Timer Status.** This bit toggles from low to high once every second, and is synchronous with the applied125us frame pulse at pin FPb.
12	TWOSEC	**Two Second Timer Status.** This bit toggles from low to high once every two seconds, and is synchronous with the applied125us frame pulse at pin FPb.
11	T1	**Timer 1.** If one, indicates that a receive PCM30 link with non-normal operational CRC-4 frames ($\overline{\text{CSYNC}}$=1, see Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10) has persisted for at least 100ms. This bit is zero when Timer 2 (T2 of this register) is one. Refer to I.431 Section 5.9.2.2.3.
10	T2	**Timer 2.** If one, indicates that a receive PCM30 link with normal operational CRC-4 frames ($\overline{\text{CSYNC}}$=0, see Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10) has persisted for at least 10ms. This bit is cleared (zero) when non-normal operational frames ($\overline{\text{CSYNC}}$=1) occur. Refer to I.431 Section 5.9.2.2.3.
9	T400	**400ms Timer Status.** This is the 400ms CRC-4 multiframe alignment timer. This bit initially changes state from zero to one synchronously with the T8 bit (of this register) after the T8 bit has consecutively toggled 50 times (400ms). While this condition persists (T8=0101 etc.), the T400 bit continues to stay high (one). The T400 bit is cleared (zero) with the T8 bit when CRC-4 multiframe synchronization is acquired ($\overline{\text{CSYNC}}$=0, see Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10).
8	T8	**8ms Timer Status.** This is the 8ms CRC-4 multiframe alignment timer. This bit initially changes state from zero to one synchronously with the CRCRF bit (of this register) when the received PCM30 link CRC-4 multiframe synchronization ($\overline{\text{CSYNC}}$ = 1, see Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10) could not be found within the time out period of 8 ms after detecting basic frame synchronization ($\overline{\text{BSYNC}}$=0, see Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10). While this condition persists (CRCRF=1), the T8 bit continues to change state every 8ms. The T8 bit is cleared (zero) with the CRCRF bit when CRC-4 multiframe synchronization is acquired ($\overline{\text{CSYNC}}$ =0).
7-5	(###)	Not Used

Table 107 - E1 CRC-4 Timers & CRC-4 Local Status - R Address Y11

Bit	Name	Functional Description
4	CALN	**CRC-4 Alignment 2ms Timer.** When CRC-4 multiframe alignment has not been achieved ($\overline{\text{CSYNC}}$=1, see Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10), this bit asynchronously changes state every 2 ms. When CRC-4 multiframe alignment has been achieved ($\overline{\text{CSYNC}}$ =0), this bit still changes state every 2 ms, but is synchronous with the receive CRC-4 multiframe signal.
3	CRCRF	**CRC-4 Reframe.** If one, indicates the received PCM30 link CRC-4 multiframe synchronization ($\overline{\text{CSYNC}}$=1, see Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10) could not be found within the time out period of 8ms after detecting basic frame synchronization ($\overline{\text{BSYNC}}$=0, see Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10). This bit is cleared (zero) when CRC-4 multiframe synchronization is acquired ($\overline{\text{CSYNC}}$ =0).
2	CRCS1	**Receive CRC-4 Error Status One.** If one, the CRC-4 evaluation of the last received PCM30 link submultiframe 1 resulted in an error (the calculated C1,C2,C3,C4 CRC-4 remainder bits did not match the received CRC-4 remainder C1,C2,C3,C4 bits). If zero, the last submultiframe 1 was error free. Updated on a submultiframe 1 basis.
1	CRCS2	**Receive CRC-4 Error Status Two.** If one, the CRC-4 evaluation of the last received PCM30 link submultiframe 2 resulted in an error (the calculated C1,C2,C3,C4 CRC-4 remainder bits did not match the received CRC-4 remainder C1,C2,C3,C4 bits). If zero, the last submultiframe 2 was error free. Updated on a submultiframe 2 basis.
0	(#)	Not Used

Table 107 - E1 CRC-4 Timers & CRC-4 Local Status - R Address Y11

Bit	Name	Functional Description
15-10	(#### ##)	Not Used
9	RXBOM (0)	**Receive Bit Oriented Message (BOM) Received.** This bit is set when a BOM byte RXBOM7-0 (of this register) is received.
8	RXBOMM (0)	**Receive Bit Oriented (BOM) Match.** This bit is set if there is a match between the received BOM byte RXBOM7-0 (of this register) and the BOM match register byte RXBOMM7-0 (see Table 94 - T1 Receive BOM Match Control - R/W Address Y08).
7 6 5 4 3 2 1 0	RXBOM7 RXBOM6 RXBOM5 RXBOM4 RXBOM3 RXBOM2 RXBOM1 RXBOM0 (#### ####)	**Receive Bit Oriented Message (BOM).** This is the received BOM. This register is updated after 7 out of 10 identical messages are received.

Table 108 - T1 Receive Bit Oriented Message - R Address Y12

Bit	Name	Functional Description
15-14	(##)	Not Used
13	KLVE	**Keep Alive.** If one, indicates that the AIS status bit (of this register) has been one for at least 100ms. This bit is zero when AIS is zero. Refer to I.431.
12	LOSS	**Loss of Signal Status Indication.** If one, indicates the presence of a loss of signal condition on the received PCM30 link. A loss of signal condition occurs after the detection of 192 or 32 consecutive zeros as set by the control bit L32Z detailed in Table 81 - E1 Test, Error and Loopback Control - R/W Address Y01. A loss of signal condition terminates when an average ones density of at least 12.5% has been received over a period of 255 contiguous pulse positions starting with a pulse. If zero, indicates normal operation.
11	AIS16	**Alarm Indication Signal 16 Status.** If one, indicates an all ones signal (1111 1111) is being received in timeslot16 of the received PCM30 link for the current frame. Updated on a basic frame basis. If zero, normal operation.
10	AIS	**Alarm Indication Status Signal.** If one, indicates that an Alarm Indication Signal (AIS) is detected on the received PCM30 link. The criteria (i.e. less than three zeros in a two frame period) for AIS detection is determined by the control bit ASEL (see Table 79 - E1 Alarms and Framing Control - R/W Address Y00). If the AIS bit is zero, indicates that an AIS signal is not being received.
9	RAI	**Remote Alarm Indication Status.** Indicates the status of the bit (A-bit) received on the PCM30 link in bit position 3 of timeslot 0 of the non-frame alignment signal (NFAS) frames. If one, there is currently a remote alarm condition. Updated on a NFAS frame basis. This bit is identical to the RAI bit detailed in Table 111 - E1 NFAS Signal and FAS Status - R Address Y13 and is duplicated here for convenience.
8	AUXP	**Auxiliary Pattern.** If one, an auxiliary pattern (101010) of at least 512 bits is being received on the PCM30 link. If zero, an auxiliary pattern is not being received. This pattern will be decoded in the presents of a bit error rate of as much as 10^{-3}.
7 6 5 4	RMA1 RMA2 RMA3 RMA4	**Receive Multiframe Alignment Bits One to Four.** Indicates the status of the bits received on the PCM30 link in bit positions one to four of timeslot 16 of frame 0 of the multiframe alignment signal (MAS). These bits should be 0000 for proper signaling multiframe alignment. Updated on a MAS frame basis.
3	X1	**Receive Spare Bit X1.** Indicates the status of the bit received on the PCM30 link in bit position five of timeslot 16 of frame 0 of the multiframe alignment signal (MAS). Updated on a MAS frame basis.
2	Y	**Receive Y-bit.** Indicates the status of the bit (Y-bit) received on the PCM30 link in bit position six of timeslot 16 of frame 0 of the multiframe alignment signal (MAS). Updated on a MAS frame basis. If one, typically indicates a loss of multiframe alignment at the remote end. If zero, typically indicates acquired multiframe alignment at the remote end.
1 0	X2 X3	**Receive Spare Bits X2 and X3.** Indicates the status of the bits received on the PCM30 link in bit positions seven and eight of timeslot 16 of frame 0 of the multiframe alignment signal (MAS). Updated on a MAS frame basis.

Table 109 - E1 Alarms & MAS Status - R Address Y12

Bit	Name	Functional Description
15-14	(##)	Not Used
13 12 11	RXP2 RXP1 RXP0	**Receive Phase Count.** A three bit counter that indicates the number of ST-BUS 1/8 bit times there are between the receive elastic buffer internal write frame boundary and the ST-BUS read frame boundary. The count is updated every 250 uS. The RXP2 bit indicates a 1/2 bit phase offset, the RXP1 bit indicates a 1/4 bit phase offset and the RXP0 bit indicates a 1/8 bit phase offset.

Table 110 - T1 Receive Elastic Buffer Status - R Address Y13

Bit	Name	Functional Description
10	RSLPD	**Receive Slip Direction.** If one, indicates that the last received frame slip (RSLP of this register) resulted in a repeated frame. This would occur if the system clock (CKb/2) was faster than the network clock (RxCK). If zero, indicates that the last received frame slip (RSLP) resulted in a lost frame. This would occur if the system clock was slower than the network clock. Updated on an RSLP occurrence basis.
9	RSLP	**Receive Slip.** This bit changes state when a receive controlled frame slip has occurred.
8	RXFRM	**Receive Frame Count.** The most significant bit of the receive phase status. If one, the delay through the receive elastic buffer is greater than one frame in length; if zero, the delay through the receive elastic buffer is less than one frame in length.
7 6 5 4 3	RXTS4 RXTS3 RXTS2 RXTS1 RXTS0	**Receive Time Slot Count.** A five bit counter that indicates the number of time slots between the receive elastic buffer internal write frame boundary and the ST-BUS read frame boundary. The count is updated every 250 uS.
2 1 0	RXBC2 RXBC1 RXBC0	**Receive Bit Count.** A three bit counter that indicates the number of ST-BUS bit times there are between the receive elastic buffer internal write frame boundary and the ST-BUS read frame boundary. The count is updated every 250 uS.

Table 110 - T1 Receive Elastic Buffer Status - R Address Y13

Bit	Name	Functional Description
15	RIU1	**Receive International Use 1.** Indicates the status of the bit received on the PCM30 link in bit position one of timeslot 0 of the non-frame alignment signal (NFAS) frames. This bit is the CRC-4 multiframe alignment bit (001011) of the NFAS frames (1,3,5,7,9,11) when CRC-4 multiframing is used. Or, this bit is used for international use.
14	RNFA	**Receive Non-Frame Alignment Bit.** Indicates the status of the bit received on the PCM30 link in bit position two of timeslot 0 of the non-frame alignment signal (NFAS) frames. This bit should be one and identifies the frame as an NFAS frame (the FAS frame should have a zero in bit position two of timeslot 0).
13	RAI	**Remote Alarm Indication Status.** Indicates the status of the bit (A-bit) received on the PCM30 link in bit position 3 of timeslot 0 of the non-frame alignment signal (NFAS) frames. If one, there is currently a remote alarm condition. Updated on a NFAS frame basis. This bit is identical to the RAI bit detailed in Table 109 - E1 Alarms & MAS Status - R Address Y12 and is duplicated here for convenience.
12 11 10 9 8	RNU4 RNU5 RNU6 RNU7 RNU8	**Receive National Use Four to Eight.** Indicates the value of the Sa bits received on the PCM30 link in bit positions four to eight of timeslot 0 of the non-frame alignment signal (NFAS) frames. Sa4 corresponds to RNU4, Sa5 to RNU5 and so on up to Sa8 to RNU8. Updated on a NFAS frame basis.
7	RIU0	**Receive International Use Zero.** Indicates the status of the bit received on the PCM30 link in bit position one of timeslot 0 of the frame alignment signal (FAS) frames. This bit is the CRC-4 remainder bit (C1,C2,C3 or C4) of the FAS frames when CRC-4 multiframing is used. Or, this bit is used for international use.
6 5 4 3 2 1 0	RFA2 RFA3 RFA4 RFA5 RFA6 RFA7 RFA8	**Receive Frame Alignment Signal (FAS) Bits 2 to 8.** Indicates the value of the bits received on the PCM30 link in bit positions two to eight of timeslot 0 of the frame alignment signal (FAS) frames. These bits form the FAS and should have the value of 0011011.

Table 111 - E1 NFAS Signal and FAS Status - R Address Y13

Bit	Name	Functional Description
15-11	(#### #)	Not Used
10	TSLP	**Transmit Slip.** A change of state indicates that a transmit controlled frame slip has occurred.
9	TSLPD	**Transmit Slip Direction.** If one, indicates that the last transmit frame slip resulted in a repeated frame, i.e., the internally generated 1.544 MHz transmit clock is faster than the system clock (CKb). If zero, indicates that the last transmit frame slip resulted in a lost frame, i.e., the internally generated 1.544 MHz. transmit clock is slower than system clock. Updated on an TSLP (in this register) occurrence basis.
8	TXFRM	**Transmit Frame Count.** The most significant bit of the transmit phase status which indicates the number of ST-BUS frames between the transmit elastic buffer ST-BUS write frame boundary and the internal transmit read frame boundary. The count is updated every 250 uS.
7 6 5 4 3	TXTS4 TXTS3 TXTS2 TXTS1 TXTS0	**Transmit Time Slot Count.** A five bit counter that indicates the number of ST-BUS time slots between the transmit elastic buffer ST-BUS write frame boundary and the internal transmit read frame boundary. The count is updated every 250 uS.
2 1 0	TXBC2 TXBC1 TXBC0	**Transmit Bit Count.** A three bit counter that indicates the number of ST-BUS bit times there are between the transmit elastic buffer ST-BUS write frame boundary and the internal read frame boundary. The count is updated every 250 uS.

Table 112 - T1 Transmit Elastic Buffer Status - R Address Y14

Bit	Name	Functional Description
15-12	(####)	Not Used
		Phase Indicator. These bits make up a 12 bit word that indicates the phase from the system basic frame pulse (FPb) to the receive basic frame pulse ($\overline{RXBF}$). The units are in one eighth bit times, with PI0 being the least significant bit (LSB). The accuracy of this indicator is approximately 1/16 of a bit. Updated on a basic frame basis.
11	PI11	This bit indicates a 1 frame (32 timeslot or 256 bit) phase offset.
10	PI10	This bit indicates a 16 timeslot (128 bit) phase offset.
9	PI9	This bit indicates a 4 timeslot (64 bit) phase offset.
8	PI8	This bit indicates a 3 timeslot (32 bit) phase offset.
7	PI7	This bit indicates a 2 timeslot (16 bit) phase offset.
6	PI6	This bit indicates a 1 timeslot (8 bit) phase offset.
5	PI5	This bit indicates a 4 bit phase offset.
4	PI4	This bit indicates a 2 bit phase offset.
3	PI3	This bit indicates a 1 bit phase offset.
2	PI2	This bit indicates a 1/2 bit phase offset.
1	PI1	This bit indicates a 1/4 bit phase offset.
0	PI0	This bit indicates a 1/8 bit phase offset.

Table 113 - E1 Phase Indicator Status - R Address Y14

Bit	Name	Functional Description
15 14 13 12 11 10 9 8	PCC7 PCC6 PCC5 PCC4 PCC3 PCC2 PCC1 PCC0 (0000 0000)	**CRC Counter for Pseudo Random Bit Sequence (PRBS).** These bits make up a counter which is incremented for each received CRC multiframe. PCC0 is the least significant bit (LSB). This counter is cleared with either: a) An overflow b) A hard reset ($\overline{\text{RESET}}$ pin) c) A unique soft reset (RST bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1) d) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W Address 900) e) A counter clear (CNCLR bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1) Or, this counter may be set by writing the desired value to it. The lower byte and upper byte of this register cannot be written to independently.
7 6 5 4 3 2 1 0	PEC7 PEC6 PEC5 PEC4 PEC3 PEC2 PEC1 PEC0 (0000 0000)	**Pseudo Random Bit Sequence (PRBS) Error Counter.** These bits make up a counter which is incremented for each pseudo random bit sequence (PRBS) (2^{15}-1) error detected on any of the DSTo receive channels connected to the PRBS error detector. ADSEQ=0 detailed in Table 80 - T1 Line Coding Control - R/W Address Y01; and RRSTn=1 detailed in Table 166 - T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7. PEC0 is the least significant bit (LSB). This counter is cleared with either: a) An overflow b) A hard reset ($\overline{\text{RESET}}$ pin) c) A unique soft reset (RST bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1) d) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W Address 900) e) A counter clear (CNCLR bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1) Or, this counter may be set by writing the desired value to it. The lower byte and upper byte of this register cannot be written to independently.

Table 114 - T1 PRBS CRC Multiframe and PRBS Error Counter - R/W Address Y15

Bit	Name	Functional Description
15 14 13 12 11 10 9 8	PEC7 PEC6 PEC5 PEC4 PEC3 PEC2 PEC1 PEC0 (0000 0000)	**Pseudo Random Bit Sequence (PRBS) Error Counter.** These bits make up a counter which is incremented for each pseudo random bit sequence (PRBS) (2^{15}-1) error detected on any of the DSTo receive channels connected to the PRBS error detector. ADSEQ=0 detailed in Table 81 - E1 Test, Error and Loopback Control - R/W Address Y01; and RRSTn=1 detailed in Table 167 - E1 Per Timeslot 0 to 31 Control Registers - R/W Address Y90-YAF. PEC0 is the least significant bit (LSB). This counter is cleared with either: a) An overflow b) A hard reset ($\overline{\text{RESET}}$ pin) c) A unique soft reset (RST bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) d) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W Address 900) e) A counter clear (CNCLR bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) Or, this counter may be set by writing the desired value to it. The lower byte and upper byte of this register cannot be written to independently.

Table 115 - E1 PRBS Error Counter & PRBS CRC Multiframe Counter - R/W Address Y15

Bit	Name	Functional Description
7 6 5 4 3 2 1 0	PCC7 PCC6 PCC5 PCC4 PCC3 PCC2 PCC1 PCC0 (0000 0000)	**CRC Multiframe Counter for Pseudo Random Bit Sequence (PRBS).** These bits make up a counter which is incremented for each received CRC-4 sub-multiframe. PCC0 is the least significant bit (LSB). This counts even without CRC-4 sync (i.e. $\overline{\text{CSYNC}}$ = 1). This counter is cleared with either: a) An overflow b) A hard reset ($\overline{\text{RESET}}$ pin) c) A unique soft reset (RST bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) d) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W Address 900) e) A counter clear (CNCLR bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) Or, this counter may be set by writing the desired value to it. The lower byte and upper byte of this register cannot be written to independently.

Table 115 - E1 PRBS Error Counter & PRBS CRC Multiframe Counter - R/W Address Y15

Bit	Name	Functional Description
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	MFC15 MFC14 MFC13 MFC12 MFC11 MFC10 MFC9 MFC8 MFC7 MFC6 MFC5 MFC4 MFC3 MFC2 MFC1 MFC0 (0000 0000 0000 0000)	**Multiframe Out of Frame Counter.** These bits make up a counter which is incremented for each multiframe period in which multiframe frame synchronization is lost ($\overline{\text{MFSYNC}}$=1 detailed in Table 104 - T1 Synchronization and Alarm Status - R Address Y10). MFC0 is the least significant bit (LSB). This counter is cleared with either: a) An overflow b) A hard reset ($\overline{\text{RESET}}$ pin) c) A unique soft reset (RST bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1) d) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W Address 900) e) A counter clear (CNCLR bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1) f) By the one second timer bit when in automatic counter clear mode (ACCLR bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1) Or, this counter may be set by writing the desired value to it.

Table 116 - T1 Multiframe Out of Frame Counter - R/W Address Y16

Bit	Name	Functional Description
15	SLC15	**Loss of Basic Frame Synchronization Counter.** These bits make up a counter which is
14	SLC14	incremented for each 125us period in which basic frame synchronization ($\overline{BSYNC}$=1
13	SLC13	detailed in Table 105 - E1 Synchronization & CRC-4 Remote Status - R Address Y10) is
12	SLC12	lost. SLC0 is the least significant bit (LSB). This counter is cleared with either:
11	SLC11	a) An overflow
10	SLC10	b) A hard reset ($\overline{RESET}$ pin)
9	SLC9	c) A unique soft reset (RST bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control
8	SLC8	- R/W Address Y03)
7	SLC7	d) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W
6	SLC6	Address 900)
5	SLC5	e) A counter clear (CNCLR bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control
4	SLC4	- R/W Address Y03)
3	SLC3	f) A basic frame synchronization to a loss of basic frame synchronization state transition
2	SLC2	($\overline{BSYNC}$ bit detailed in Table 105 - E1 Synchronization & CRC-4 Remote Status - R
1	SLC1	Address Y10)
0	SLC0 (0000 0000 0000 0000)	Or, this counter may be set by writing the desired value to it.

Table 117 - E1 Loss of Basic Frame Sync Counter - R/W Address Y16

Bit	Name	Functional Description
15	BEC15	**Framing Bit Error Counter.** These bits make up a counter which is incremented for
14	BEC14	each error in the received frame pattern. In ESF mode the ESF framing bits are
13	BEC13	monitored. In D4 mode Fs bits may be monitored as well as Ft bits. The count is only
12	BEC12	active if the framer is in synchronization. BEC0 is the least significant bit (LSB). This
11	BEC11	counter is cleared with either:
10	BEC10	a) An overflow
9	BEC9	b) A hard reset ($\overline{RESET}$ pin)
8	BEC8	c) A unique soft reset (RST bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W
7	BEC7	Address YF1)
6	BEC6	d) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/
5	BEC5	W Address 900)
4	BEC4	e) A counter clear (CNCLR bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W
3	BEC3	Address YF1)
2	BEC2	f) By the one second timer bit when in automatic counter clear mode (ACCLR bit
1	BEC1	detailed in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1)
0	BEC0 (0000 0000 0000 0000)	Or, this counter may be set by writing the desired value to it.

Table 118 - T1 Framing Bit Error Counter - R/W Address Y17

Bit	Name	Functional Description
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	EEC15 EEC14 EEC13 EEC12 EEC11 EEC10 EEC9 EEC8 EEC7 EEC6 EEC5 EEC4 EEC3 EEC2 EEC1 EEC0 (0000 0000 0000 0000)	**E-bit Error Counter.** These bits make up a counter which is incremented for each received PCM30 CRC-4 submultiframe E-bit error. EEC0 is the least significant bit (LSB). This counter is cleared with either: a) An overflow b) A hard reset ($\overline{\text{RESET}}$ pin) c) A unique soft reset (RST bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) d) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W Address 900) e) A counter clear (CNCLR bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) f) By the one second timer bit when in automatic counter clear mode (ACCLR bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) Or, this counter may be set by writing the desired value to it.

Table 119 - E1 E-bit Error Counter - R/W Address Y17

Bit	Name	Functional Description
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	VEC15 VEC14 VEC13 VEC12 VEC11 VEC10 VEC9 VEC8 VEC7 VEC6 VEC5 VEC4 VEC3 VEC2 VEC1 VEC0 (0000 0000 0000 0000)	**Bipolar Violation Error Counter.** These bits make up a counter which is incremented for each received bipolar violation error. VEC0 is the least significant bit (LSB). This counter is cleared with either: a) An overflow b) A hard reset ($\overline{\text{RESET}}$ pin) c) A unique soft reset (RST bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1) d) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W Address 900) e) A counter clear (CNCLR bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1) f) By the one second timer bit when in automatic counter clear mode (ACCLR bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1) Or, this counter may be set by writing the desired value to it.

Table 120 - T1 Bipolar Violation Counter - R/W Address Y18

Bit	Name	Functional Description
15	VEC15	**Bipolar Violation Error Counter.** These bits make up a counter which is incremented for
14	VEC14	each received bipolar violation error. VEC0 is the least significant bit (LSB). This counter is
13	VEC13	cleared with either:
12	VEC12	a) An overflow
11	VEC11	b) A hard reset ($\overline{\text{RESET}}$ pin)
10	VEC10	c) A unique soft reset (RST bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control -
9	VEC9	R/W Address Y03)
8	VEC8	d) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W
7	VEC7	Address 900)
6	VEC6	e) A counter clear (CNCLR bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control -
5	VEC5	R/W Address Y03)
4	VEC4	f) By the one second timer bit when in automatic counter clear mode (ACCLR bit detailed in
3	VEC3	Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03)
2	VEC2	Or, this counter may be set by writing the desired value to it.
1	VEC1	
0	VEC0	
	(0000 0000 0000 0000)	

Table 121 - E1 Bipolar Violation Error Counter - R/W Address Y18

Bit	Name	Functional Description
15	CEC15	**CRC-6 Error Counter.** These bits make up a counter which is incremented for each
14	CEC14	calculated CRC-6 error. CEC0 is the least significant bit (LSB). This counter is cleared
13	CEC13	with either:
12	CEC12	a) An overflow
11	CEC11	b) A hard reset ($\overline{\text{RESET}}$ pin)
10	CEC10	c) A unique soft reset (RST bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W
9	CEC9	Address YF1)
8	CEC8	d) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W
7	CEC7	Address 900)
6	CEC6	e) A counter clear (CNCLR bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W
5	CEC5	Address YF1)
4	CEC4	f) By the one second timer bit when in automatic counter clear mode (ACCLR bit detailed
3	CEC3	in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1)
2	CEC2	Or, this counter may be set by writing the desired value to it.
1	CEC1	
0	CEC0	
	(0000 0000 0000 0000)	

Table 122 - T1 CRC-6 Error Counter - R/W Address Y19

Bit	Name	Functional Description
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	CEC15 CEC14 CEC13 CEC12 CEC11 CEC10 CEC9 CEC8 CEC7 CEC6 CEC5 CEC4 CEC3 CEC2 CEC1 CEC0 (0000 0000 0000 0000)	**CRC-4 Error Counter.** These bits make up a counter which is incremented for each calculated CRC-4 submultiframe error (see CRCS1 and CRCS2 bits detailed in Table 107 - E1 CRC-4 Timers & CRC-4 Local Status - R Address Y11). CEC0 is the least significant bit (LSB). This counter is cleared with either: a) An overflow b) A hard reset ($\overline{\text{RESET}}$ pin) c) A unique soft reset (RST bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) d) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W Address 900) e) A counter clear (CNCLR bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) f) By the one second timer bit when in automatic counter clear mode (ACCLR bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) Or, this counter may be set by writing the desired value to it.

Table 123 - E1 CRC-4 Error Counter - R/W Address Y19

Bit	Name	Functional Description
15 14 13 12 11 10 9 8	OFC7 OFC6 OFC5 OFC4 OFC3 OFC2 OFC1 OFC0 (0000 0000)	**Out Of Frame Counter.** These bits make up a counter which is incremented with every loss of receive frame synchronization. OFC0 is the least significant bit (LSB). This counter is cleared with either: a) An overflow b) A hard reset ($\overline{\text{RESET}}$ pin) c) A unique soft reset (RST bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1) d) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W Address 900) e) A counter clear (CNCLR bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1) f) By the one second timer bit when in automatic counter clear mode (ACCLR bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1) Or, this counter may be set by writing the desired value to it. The lower byte and upper byte of this register cannot be written to independently.

Table 124 - T1 Out of Frame and Change of Frame Counters - R/W Address Y1A

Bit	Name	Functional Description
7 6 5 4 3 2 1 0	CFC7 CFC6 CFC5 CFC4 CFC3 CFC2 CFC1 CFC0 (0000 0000)	**Change of Frame Alignment Counter.** This eight bit counter is incremented if a resynchronization is done which results in a shift in the frame alignment position. These bits make up a counter which is incremented if a resynchronization is done which results in a shift in the frame alignment position. CFC0 is the least significant bit (LSB). This counter is cleared with either: a) An overflow b) A hard reset ($\overline{\text{RESET}}$ pin) c) A unique soft reset (RST bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1) d) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W Address 900) e) A counter clear (CNCLR bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1) f) By the one second timer bit when in automatic counter clear mode (ACCLR bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1) Or, this counter may be set by writing the desired value to it. The lower byte and upper byte of this register cannot be written to independently.

Table 124 - T1 Out of Frame and Change of Frame Counters - R/W Address Y1A

Bit	Name	Functional Description
15 14 13 12 11 10 9 8	BEC7 BEC6 BEC5 BEC4 BEC3 BEC2 BEC1 BEC0 (0000 0000)	**Frame Alignment Signal (FAS) Bit Error Counter.** These bits make up a counter which is incremented for each individual error in the received PCM30 link basic frame alignment signal (FAS) pattern (x0011011 in timeslot 0 of alternate frames). BEC0 is the least significant bit (LSB). This counter is cleared with either: a) An overflow b) A hard reset ($\overline{\text{RESET}}$ pin) c) A unique soft reset (RST bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) d) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W Address 900) e) A counter clear (CNCLR bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) f) By the one second timer bit when in automatic counter clear mode (ACCLR bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) Or, this counter may be set by writing the desired value to it. The lower byte and upper byte of this register cannot be written to independently.
7 6 5 4 3 2 1 0	FEC7 FEC6 FEC5 FEC4 FEC3 FEC2 FEC1 FEC0 (0000 0000)	**Frame Alignment Signal (FAS) Error Counter.** These bits make up a counter which is incremented for each combined (one or more) error in the received PCM30 link basic frame alignment signal (FAS) pattern (x0011011 in timeslot 0 of alternate frames). FEC0 is the least significant bit (LSB). This counter is cleared with either: a) An overflow b) A hard reset ($\overline{\text{RESET}}$ pin) c) A unique soft reset (RST bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) d) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W Address 900) e) A counter clear (CNCLR bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) f) By the one second timer bit when in automatic counter clear mode (ACCLR bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) Or, this counter may be set by writing the desired value to it. The lower byte and upper byte of this register cannot be written to independently.

Table 125 - E1 FAS Bit Error Counter & FAS Error Counter - R/W Address Y1A

Bit	Name	Functional Description
15-8	(#### ####)	Not Used
7 6 5 4 3 2 1 0	EZC7 EZC6 EZC5 EZC4 EZC3 EZC2 EZC1 EZC0 (0000 0000)	**Excessive Zero Counter.** These bits make up a counter which is incremented for each detection of 8 or more zeros if B8ZS (see Table 80 - T1 Line Coding Control - R/W Address Y01) is turned on; or for each detection of 16 or more zeros if B8ZS is turned off. In other words, this counter counts groups of 8 or more or 16 or more zeros separated by ones.

Table 126 - T1 Excessive Zero's Counter - R/W Address Y1B

Bit	Name	Functional Description
15-12	(####)	Not Used.
11	RXCLK	**Receive Clock.** This bit represents the receiver clock generated after the RXEN bit detailed in Table 179 - T1 & E1 HDLC Control 0 - R/W Address YF2, but before zero deletion is considered.
10	TXCLK	**Transmit Clock.** This bit represents the transmit clock generated after the TXEN bit detailed in Table 179 - T1 & E1 HDLC Control 0 - R/W Address YF2, but before zero insertion is considered.
9	VCRC	**Valid CRC**. This is the CRC recognition status bit for the HDLC receiver. Data is clocked into the data register detailed in Table 129 - T1 & E1 HDLC Receive CRC Data - R/W Address Y1E. If the comparison was successful, then this bit will be high.
8	VADDR	**Valid Address.** This is the address recognition status bit for the HDLC receiver. Data is clocked into the device and compared with the data register detailed in Table 181 - T1 & E1 HDLC Address Recognition Control - R/W Address YF4. If the comparison was successful, then this bit will be high.
7 6 5 4 3 2 1 0	TBP7 TBP6 TBP5 TBP4 TBP3 TBP2 TBP1 TBP0	**Transmit Byte Counter Position.** These 8 bits provide the position of the next byte of data to be written into the Transmit FIFO (see Table 182 - T1 & E1 HDLC Transmit FIFO Data - R/W Address YF5). The initial transmit byte counter position is loaded from control register bits TPS7-0 detailed in Table 183 - T1 & E1 HDLC Transmit Packet Size - R/W Address YF6. The transmitter automatically decrements this register following each write to the Transmit FIFO. When this register reaches the count of one, the next write to the Transmit FIFO will be automatically tagged as an EOP byte. Consequently, following the last byte, the transmitter automatically sends the two byte FCS and then the 1 byte closing FLAG. If the CYCLE bit of the T1 & E1 HDLC Control 0 - R/W Address YF2 is set high, the counter will cycle through the programmed value continuously.

Table 127 - T1 & E1 HDLC Test and Transmit Byte Status - R/W Address Y1C

Bit	Name	Functional Description
15-7	(#### #### #)	Not Used
6	IDC	**Idle Channel State.** This bit is set to one when an idle channel state (15 or more ones) has been detected at the receiver. This is an asynchronous event. On power reset, this may be one, status becomes valid after the first zero or first15 bits are received.

Table 128 - T1 & E1 HDLC Status - R/W Address Y1D

Bit	Name	Functional Description
5 4	RQ9 RQ8	**Receive FIFO Byte Status.** These bits determine the status of the byte to be read from the Receive FIFO as follows: RQ9 RQ8 Byte to be Read Status 0 0 Packet Byte 0 1 First Byte 1 0 Last byte of a good packet. 1 1 Last byte of a bad packet. The Receive FIFO is accessed through the T1 & E1 HDLC Receive FIFO Data - R/W Address Y1F.
3 2	TFS2 TFS1	**Transmit FIFO Status.** These bits determine the status of the Transmit FIFO as follows: TFS2 TFS1 Transmit FIFO Status 0 0 Transmit FIFO full up to the selected status level or more. 0 1 The number of bytes in the Transmit FIFO is equal to or greater than 16 bytes. 1 0 Transmit FIFO empty. 1 1 The number of bytes in the Transmit FIFO is less than 16 bytes. The Transmit FIFO is accessed through the T1 & E1 HDLC Transmit FIFO Data - R/W Address YF5.
1 0	RFS2 RFS1	**Receive FIFO Status.** These bits determine the status of the Receive FIFO as follows: RFS2 RFS1 Receive FIFO Status 0 0 Receive FIFO empty. 0 1 The number of bytes in the Receive FIFO is less than 16 bytes. 1 0 Receive FIFO full. 1 1 The number of bytes in the Receive FIFO is equal to or greater than 16 bytes. The Receive FIFO is accessed through the T1 & E1 HDLC Receive FIFO Data - R/W Address Y1F.

Table 128 - T1 & E1 HDLC Status - R/W Address Y1D

Bit	Name	Functional Description
15 14 13 12 11 10 9 8	CRC15 CRC14 CRC13 CRC12 CRC11 CRC10 CRC9 CRC8	**The MSB Byte of the Received CRC**. These bits are as the transmitter sent them; that is, most significant bit first and inverted. This register is updated at the end of each received packet and therefore should be read when end of packet is detected.
7 6 5 4 3 2 1 0	CRC7 CRC6 CRC5 CRC4 CRC3 CRC2 CRC1 CRC0	**The LSB Byte of the Received CRC**. These bits are as the transmitter sent them; that is, most significant bit first and inverted. This register is updated at the end of each received packet and therefore should be read when end of packet is detected.

Table 129 - T1 & E1 HDLC Receive CRC Data - R/W Address Y1E

Bit	Name	Functional Description
15-8	(#### ####)	Not Used

Table 130 - T1 & E1 HDLC Receive FIFO Data - R/W Address Y1F

Bit	Name	Functional Description
7 6 5 4 3 2 1 0	RXF7 RXF6 RXF5 RXF4 RXF3 RXF2 RXF1 RXF0	**HDLC Receive FIFO Data.** This is the received data byte read from the Receive FIFO. The FIFO status is not changed immediately when a receiver write or processor read occurs. It is updated after the data has settled and the transfer to the last available position has finished.

Table 130 - T1 & E1 HDLC Receive FIFO Data - R/W Address Y1F

Bit	Name	Functional Description
15-9	(0000 000)	Not Used
8	GAL (0)	**Go Ahead Latch.** When the HDLC receiver detects a go-ahead pattern (01111111), this status bit is latched to one. This bit is cleared when either this register, or the T1 & E1 HDLC Interrupt Status - R Address Y33 is read.
7	EOPDL (0)	**End of Packet Detect Latch.** When the HDLC receiver writes an end of packet (EOP) byte into the Receive FIFO, this status bit is latched to one. This can be in the form of a flag (01111110), an abort sequence (x1111111x) or as an invalid packet. This bit is cleared when either this register, or the T1 & E1 HDLC Interrupt Status - R Address Y33 is read.
6	TEOPL (0)	**Transmit End of Packet Latch.** When the HDLC transmitter has finished sending the closing flag of a packet or after a packet has been aborted, this status bit is latched to one. This bit is cleared when either this register, or the T1 & E1 HDLC Interrupt Status - R Address Y33 is read.
5	EOPRL (0)	**End of Packet Read Latch.** When there is only one byte of data left in the Receive FIFO, and this data is the last byte of the packet, this status bit is latched to one. It is also set if the Receive FIFO is read and there is no data in it. This bit is cleared when either this register, or the T1 & E1 HDLC Interrupt Status - R Address Y33 is read.
4	TXFLL (0)	**Transmit FIFO Low Latch.** When the HDLC transmitter empties the Transmit FIFO below 16 bytes, this status bit is latched to one. This bit is cleared when either this register, or the T1 & E1 HDLC Interrupt Status - R Address Y33 is read.
3	FAL (0)	**Frame Abort Latch.** When the HDLC receiver detects an abort sequence (x1111111x), this status bit is latched to one. Note that it must be received after a minimum number of bits have been received (26), otherwise it is ignored. This bit is cleared when either this register, or the T1 & E1 HDLC Interrupt Status - R Address Y33 is read.
2	TXFEL (0)	**Transmit FIFO Empty Latch.** When the HDLC transmitter reads an empty Transmit FIFO, this status bit is latched to one. This bit is cleared when either this register, or the T1 & E1 HDLC Interrupt Status - R Address Y33 is read.
1	RXFHL (0)	**Receive FIFO High Latch.** When the Receive FIFO is filled above 16 bytes, this status bit is latched to one. This bit is cleared when either this register, or the T1 & E1 HDLC Interrupt Status - R Address Y33 is read.
0	RXFOL (0)	**Receive FIFO Overflow Latch.** When the HDLC receiver writes to an already full Receive FIFO, this status bit is latched to one. This bit is cleared when either this register, or the T1 & E1 HDLC Interrupt Status - R Address Y33 is read. The HDLC will disable the receiver once the receive overflow has been detected. The receiver will be re-enabled upon detection of the next flag, but will overflow again unless the Receive FIFO is read.

Table 131 - T1 & E1 HDLC Latched Status - R Address Y23

Bit	Name	Functional Description
15	BEOL (0)	**Framing Bit Error Counter Overflow Latch.** When the corresponding counter (T1 Framing Bit Error Counter - R/W Address Y17) overflows to 0, this status bit is latched to one. It is cleared when either this register, or the T1 Receive and Sync Interrupt Status - R Address Y34 is read.
14	CEOL (0)	**CRC-6 Error Counter Overflow Latch.** When the corresponding counter (T1 CRC-6 Error Counter - R/W Address Y19) overflows to 0, this status bit is latched to one. It is cleared when either this register, or the T1 Receive and Sync Interrupt Status - R Address Y34 is read.
13	OFOL (0)	**Out Of Frame Counter Overflow Latch.** When the corresponding counter (T1 Out of Frame and Change of Frame Counters - R/W Address Y1A) overflows (to 0), this status bit is latched to one. It is cleared when either this register, or the T1 Receive and Sync Interrupt Status - R Address Y34 is read.
12	CFOL (0)	**Change of Frame Alignment Counter Overflow Latch.** When the corresponding counter (T1 Out of Frame and Change of Frame Counters - R/W Address Y1A) overflows to 0, this status bit is latched to one. It is cleared when either this register, or the T1 Receive and Sync Interrupt Status - R Address Y34 is read.
11	VEOL (0)	**Bipolar Violation Counter Overflow Latch.** When the corresponding counter (T1 Bipolar Violation Counter - R/W Address Y18) overflows to 0, this status bit is latched to one. It is cleared when either this register, or the T1 Receive and Sync Interrupt Status - R Address Y34 is read.
10	PEOL (0)	**PRBS Error Counter Overflow Latch.** When the corresponding counter (T1 PRBS CRC Multiframe and PRBS Error Counter - R/W Address Y15) overflows to 0, this status bit is latched to one. It is cleared when either this register, or the T1 Receive and Sync Interrupt Status - R Address Y34 is read.
9	PCOL (0)	**PRBS CRC-6 Multiframe Counter Overflow Latch.** When the corresponding counter (T1 PRBS CRC Multiframe and PRBS Error Counter - R/W Address Y15) overflows to 0, this status bit is latched to one. It is cleared when either this register, or the T1 Receive and Sync Interrupt Status - R Address Y34 is read.
8	MFOL (0)	**Multiframe Out of Frame Counter Overflow Latch.** When the corresponding counter (T1 Multiframe Out of Frame Counter - R/W Address Y16) overflows to 0, this status bit is latched to one. It is cleared when either this register, or the T1 Receive and Sync Interrupt Status - R Address Y34 is read.
7	TFSYNL (0)	**Terminal Out Of Sync Latch.** When the $\overline{\text{TFSYNC}}$ status bit (T1 Synchronization and Alarm Status - R Address Y10) toggles from zero to one, or from one to zero, this status bit is latched to one. It is cleared when either this register, or the T1 Receive and Sync Interrupt Status - R Address Y34 is read.
6	MFSYNL (0)	**Multiframes Out Of Sync Latch.** When the $\overline{\text{MFSYNC}}$ status bit (T1 Synchronization and Alarm Status - R Address Y10) toggles from zero to one, or from one to zero, this status bit is latched to one. It is cleared when either this register, or the T1 Receive and Sync Interrupt Status - R Address Y34 is read.
5	BEIL (0)	**Framing Bit Error Counter Indication Latch.** When the corresponding counter (T1 Framing Bit Error Counter - R/W Address Y17) is incremented by one, this status bit is latched to one. It is cleared when either this register, or the T1 Receive and Sync Interrupt Status - R Address Y34 is read.
4	CFIL (0)	**Change of Frame Counter Indication Latch.** When the corresponding counter (T1 Out of Frame and Change of Frame Counters - R/W Address Y1A) is incremented by one, this status bit is latched to one. It is cleared when either this register, or the T1 Receive and Sync Interrupt Status - R Address Y34 is read.

Table 132 - T1 Receive Sync and Alarm Latch - R Address Y24

Bit	Name	Functional Description
3	SEFL (0)	**Severely Errored Frame Latch.** When the SEF status bit (T1 Synchronization and Alarm Status - R Address Y10) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the T1 Receive and Sync Interrupt Status - R Address Y34 is read.
2	AISL (0)	**AIS Latch.** When the AIS status bit (T1 Synchronization and Alarm Status - R Address Y10) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the T1 Receive and Sync Interrupt Status - R Address Y34 is read.
1	CEIL (0)	**CRC-6 Error Counter Indication Latch**. When the corresponding counter (T1 CRC-6 Error Counter - R/W Address Y19) is incremented by one, this status bit is latched to one. It is cleared when either this register, or the T1 Receive and Sync Interrupt Status - R Address Y34 is read.
0	LOSL (0)	**Digital Loss of Signal Latch.** When the LOS status bit (T1 Synchronization and Alarm Status - R Address Y10) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the T1 Receive and Sync Interrupt Status - R Address Y34 is read.

Table 132 - T1 Receive Sync and Alarm Latch - R Address Y24

Bit	Name	Functional Description
15	(0)	Not Used
14	RCRCRL	**Remote CRC-4 and RAI Latch.** When the RCRCR status bit (E1 Synchronization & CRC-4 Remote Status - R Address Y10) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the E1 Sync Interrupt Status - R Address Y34 is read.
13	RSLPL	**Receive Slip Latch.** When the RSLP status bit (E1 Synchronization & CRC-4 Remote Status - R Address Y10) toggles from zero to one, or from one to zero, this status bit is latched to one. It is cleared when either this register, or the E1 Sync Interrupt Status - R Address Y34 is read.
12	YL	**Receive Y-bit Latch.** When the Y status bit (E1 Alarms & MAS Status - R Address Y12) toggles from zero to one, or from one to zero, this status bit is latched to one. It is cleared when either this register, or the E1 Sync Interrupt Status - R Address Y34 is read.
11	AUXPL	**Auxiliary Pattern Latch.** When the AUXP status bit (E1 Alarms & MAS Status - R Address Y12) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the E1 Sync Interrupt Status - R Address Y34 is read.
10	RAIL	**Remote Alarm Indication Status Latch.** When the RAI (A) status bit (E1 Alarms & MAS Status - R Address Y12) toggles from zero to one, or from one to zero, this status bit is latched to one. It is cleared when either this register, or the E1 Sync Interrupt Status - R Address Y34 is read.
9	AISL	**Alarm Indication Status Signal Latch.** When the AIS status bit (E1 Alarms & MAS Status - R Address Y12) toggles from zero to one, or from one to zero, this status bit is latched to one. It is cleared when either this register, or the E1 Sync Interrupt Status - R Address Y34 is read.
8	AIS16L	**Alarm Indication Signal 16 Status Latch.** When the AIS16 status bit (E1 Alarms & MAS Status - R Address Y12) toggles from zero to one, or from one to zero, this status bit is latched to one. It is cleared when either this register, or the E1 Sync Interrupt Status - R Address Y34 is read.
7	LOSSL	**Loss of Signal Status Indication Latch.** When the LOSS status bit (E1 Alarms & MAS Status - R Address Y12) toggles from zero to one, or from one to zero, this status bit is latched to one. It is cleared when either this register, or the E1 Sync Interrupt Status - R Address Y34 is read.

Table 133 - E1 Sync Latched Status - R Address Y24

Bit	Name	Functional Description
6	RCRC0L	**Remote CRC-4 and RAI T10 Latch.** When the RCRC0 status bit (E1 Synchronization & CRC-4 Remote Status - R Address Y10) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the E1 Sync Interrupt Status - R Address Y34 is read.
5	RCRC1L	**Remote CRC-4 and RAI T450 Latch.** When the RCRC1 status bit (E1 Synchronization & CRC-4 Remote Status - R Address Y10) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the E1 Sync Interrupt Status - R Address Y34 is read.
4	CEFSL	**Consecutively Errored Frame Alignment Signal Latch.** When the CEFS status bit (E1 Synchronization & CRC-4 Remote Status - R Address Y10) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the E1 Sync Interrupt Status - R Address Y34 is read.
3	RFAILL	**Remote CRC-4 Multiframe Generator/Detector Failure Latch.** When the RFAIL status bit (E1 Synchronization & CRC-4 Remote Status - R Address Y10) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the E1 Sync Interrupt Status - R Address Y34 is read.
2	CSYNCL	**Receive CRC-4 Synchronization Latch.** When the $\overline{\text{CSYNC}}$ status bit (E1 Synchronization & CRC-4 Remote Status - R Address Y10) toggles from zero to one, or from one to zero, this status bit is latched to one. It is cleared when either this register, or the E1 Sync Interrupt Status - R Address Y34 is read.
1	MSYNCL	**Receive Multiframe Alignment Latch.** When the $\overline{\text{MSYNC}}$ status bit (E1 Synchronization & CRC-4 Remote Status - R Address Y10) toggles from zero to one, or from one to zero, this status bit is latched to one. It is cleared when either this register, or the E1 Sync Interrupt Status - R Address Y34 is read.
0	BSYNCL	**Receive Basic Frame Alignment Latch.** When the $\overline{\text{BSYNC}}$ status bit (E1 Synchronization & CRC-4 Remote Status - R Address Y10) toggles from zero to one, or from one to zero, this status bit is latched to one. It is cleared when either this register, or the E1 Sync Interrupt Status - R Address Y34 is read.

Table 133 - E1 Sync Latched Status - R Address Y24

Bit	Name	Functional Description
15	D4YL (0)	**D4 Yellow Alarm Latch.** When the D4Y status bit (T1 Synchronization and Alarm Status - R Address Y10) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the T1 Receive Line and Timer Interrupt Status - R Address Y35 is read.
14	D4Y48L (0)	**D4 Yellow Alarm (48 milliseconds) Latch.** When the D4Y48 status bit (T1 Synchronization and Alarm Status - R Address Y10) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the T1 Receive Line and Timer Interrupt Status - R Address Y35 is read.
13	SECYL (0)	**Secondary D4 Yellow Alarm Latch.** When the SECY status bit (T1 Synchronization and Alarm Status - R Address Y10) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the T1 Receive Line and Timer Interrupt Status - R Address Y35 is read.
12	ESFYL (0)	**ESF Yellow Alarm Latch.** When the ESFY status bit (T1 Synchronization and Alarm Status - R Address Y10) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the T1 Receive Line and Timer Interrupt Status - R Address Y35 is read.
11	T1DMYL (0)	**T1DM Yellow Alarm Latched.** When the $\overline{\text{T1DMY}}$ status bit (T1 Synchronization and Alarm Status - R Address Y10) toggles from one to zero, this status bit is latched to one. It is cleared when either this register, or the T1 Receive Line and Timer Interrupt Status - R Address Y35 is read.
10	(0)	Not Used

Table 134 - T1 Receive Line Status and Timer Latch - R Address Y25

Bit	Name	Functional Description
9	VEIL (0)	**Bipolar Violation Counter Indication Latch.** When the corresponding counter (T1 Bipolar Violation Counter - R/W Address Y18) is incremented by one, this status bit is latched to one. It is cleared when either this register, or the T1 Receive Line and Timer Interrupt Status - R Address Y35 is read.
8	PEIL (0)	**PRBS Error Counter Indication Latch.** When the corresponding counter (T1 PRBS CRC Multiframe and PRBS Error Counter - R/W Address Y15) is incremented by one, this status bit is latched to one. It is cleared when either this register, or the T1 Receive Line and Timer Interrupt Status - R Address Y35 is read.
7	PDVL (0)	**Pulse Density Violation Latch.** When the PDV status bit (T1 Synchronization and Alarm Status - R Address Y10) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the T1 Receive Line and Timer Interrupt Status - R Address Y35 is read.
6	LLEDL (0)	**Line Loopback Enable Detect Latch.** When the LLED status bit (T1 Synchronization and Alarm Status - R Address Y10) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the T1 Receive Line and Timer Interrupt Status - R Address Y35 is read.
5	LLDDL (0)	**Line Loopback Disable Detect Latch.** When the LLDD status bit (T1 Synchronization and Alarm Status - R Address Y10) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the T1 Receive Line and Timer Interrupt Status - R Address Y35 is read.
4	BOML (0)	**Bit Oriented Message Latch.** When the RXBOM status bit (T1 Receive Bit Oriented Message - R Address Y12) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the T1 Receive Line and Timer Interrupt Status - R Address Y35 is read.
3	BOMML (0)	**Bit Oriented Message Match Latch.** When the RXBOMM status bit (T1 Receive Bit Oriented Message - R Address Y12) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the T1 Receive Line and Timer Interrupt Status - R Address Y35 is read.
2	CASRL (0)	**Channel Associated Signaling Received Latch.** When any of the 24 receive CAS (i.e. ABCD) bits in the T1 Receive CAS Data Registers - R Address Y70-Y87 change state, this status bit is latched to one. This bit is set on a basic frame (FPb) basis. It is cleared when either this register, or the T1 Receive Line and Timer Interrupt Status - R Address Y35 is read.
1	ONESECL (0)	**One Second Timer Status Latch.** When the ONESEC status bit (T1 Timer Status - R Address Y11) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the T1 Receive Line and Timer Interrupt Status - R Address Y35 is read.
0	TWOSECL (0)	**Two Second Timer Status Latch.** When the TWOSEC status bit (T1 Timer Status - R Address Y11) toggles from zero to one, this status bit is latched to one. It is cleared when either this register, or the T1 Receive Line and Timer Interrupt Status - R Address Y35 is read.

Table 134 - T1 Receive Line Status and Timer Latch - R Address Y25

Bit	Name	Functional Description
15	(0)	Not Used
14	SLOL	**Loss of Sync Counter Overflow Latch.** When the corresponding counter (E1 Loss of Basic Frame Sync Counter - R/W Address Y16) overflows to 0, this status bit is latched to one. It is cleared when either this register, or the E1 Counter Interrupt Status - R Address Y35 is read.
13	FEOL	**Frame Alignment Signal (FAS) Error Counter Overflow Latch.** When the corresponding counter (E1 FAS Bit Error Counter & FAS Error Counter - R/W Address Y1A) overflows to 0, this status bit is latched to one. It is cleared when either this register, or the E1 Counter Interrupt Status - R Address Y35 is read.

Table 135 - E1 Counter Latched Status - R Address Y25

Bit	Name	Functional Description
12	FEIL	**Frame Alignment Signal (FAS) Error Counter Indication Latch.** When the corresponding counter (E1 FAS Bit Error Counter & FAS Error Counter - R/W Address Y1A) is incremented by one, this status bit is latched to one. It is cleared when either this register, or the E1 Counter Interrupt Status - R Address Y35 is read.
11	BEOL	**Frame Alignment Signal (FAS) Bit Error Counter Overflow Latch.** When the corresponding counter (E1 FAS Bit Error Counter & FAS Error Counter - R/W Address Y1A) overflows to 0, this status bit is latched to one. It is cleared when either this register, or the E1 Counter Interrupt Status - R Address Y35 is read.
10	BEIL	**Frame Alignment Signal (FAS) Bit Error Counter Indication Latch.** When the corresponding counter (E1 FAS Bit Error Counter & FAS Error Counter - R/W Address Y1A) is incremented by one, this status bit is latched to one. It is cleared when either this register, or the E1 Counter Interrupt Status - R Address Y35 is read.
9	CEOL	**CRC-4 Error Counter Overflow Latch.** When the corresponding counter (E1 CRC-4 Error Counter - R/W Address Y19) overflows to 0, this status bit is latched to one. It is cleared when either this register, or the E1 Counter Interrupt Status - R Address Y35 is read.
8	CEIL	**CRC-4 Error Counter Indication Latch.** When the corresponding counter (E1 CRC-4 Error Counter - R/W Address Y19) is incremented by one, this status bit is latched to one. It is cleared when either this register, or the E1 Counter Interrupt Status - R Address Y35 is read.
7	VEOL	**Bipolar Violation Error Counter Overflow Latch.** When the corresponding counter (E1 Bipolar Violation Error Counter - R/W Address Y18) overflows to 0, this status bit is latched to one. It is cleared when either this register, or the E1 Counter Interrupt Status - R Address Y35 is read.
6	VEIL	**Bipolar Violation Error Counter Indication Latch.** When the corresponding counter (E1 Bipolar Violation Error Counter - R/W Address Y18) is incremented by one, this status bit is latched to one. It is cleared when either this register, or the E1 Counter Interrupt Status - R Address Y35 is read.
5	EEOL	**E-Bit Error Counter Overflow Latch.** When the corresponding counter (E1 E-bit Error Counter - R/W Address Y17) overflows to 0, this status bit is latched to one. It is cleared when either this register, or the E1 Counter Interrupt Status - R Address Y35 is read.
4	EEIL	**E-Bit Error Counter Indication Latch.** When the corresponding counter (E1 E-bit Error Counter - R/W Address Y17) is incremented by one, this status bit is latched to one. It is cleared when either this register, or the E1 Counter Interrupt Status - R Address Y35 is read.
3	PCOL	**PRBS CRC-4 Counter Overflow Latch.** When the corresponding counter (E1 PRBS Error Counter & PRBS CRC Multiframe Counter - R/W Address Y15) overflows to 0, this status bit is latched to one. It is cleared when either this register, or the E1 Counter Interrupt Status - R Address Y35 is read.
2	JAL	**Jitter Attenuator Latch.** This status bit is latched to one when either the JAF4 status bit toggles from one to zero, or the JAE4 status bit toggles from zero to one. These status bits are detailed in the T1 & E1 LIU and JA Status - R Address YE0. It is cleared when either this register, or the E1 Counter Interrupt Status - R Address Y35 is read.
1	PEOL	**PRBS Error Counter Overflow Latch.** When the corresponding counter (E1 PRBS Error Counter & PRBS CRC Multiframe Counter - R/W Address Y15) overflows to 0, this status bit is latched to one. It is cleared when either this register, or the E1 Counter Interrupt Status - R Address Y35 is read.
0	PEIL	**PRBS Error Counter Indication Latch.** When the corresponding counter (E1 PRBS Error Counter & PRBS CRC Multiframe Counter - R/W Address Y15) is incremented by one, this status bit is latched to one. It is cleared when either this register, or the E1 Counter Interrupt Status - R Address Y35 is read.

Table 135 - E1 Counter Latched Status - R Address Y25

Bit	Name	Functional Description
15-4	(0000 0000 0000)	Not Used
3	EZOL (0)	**Excessive Zero Counter Overflow Latch.** When the corresponding counter (T1 Excessive Zero's Counter - R/W Address Y1B) overflows to 0, this status bit is latched to one. It is cleared when either this register, or the T1 Elastic Store Interrupt Status - R Address Y36 is read.
2	EZIL (0)	**Excessive Zero Counter Indication Latch.** When the corresponding counter (T1 Excessive Zero's Counter - R/W Address Y1B) is incremented by one, this status bit is latched to one. It is cleared when either this register, or the T1 Elastic Store Interrupt Status - R Address Y36 is read.
1	TSLPL (0)	**Transmit SLIP Latch.** When the TSLP status bit (T1 Transmit Elastic Buffer Status - R Address Y14) toggles from zero to one, or from one to zero, this status bit is latched to one. It is cleared when either this register, or the T1 Elastic Store Interrupt Status - R Address Y36 is read.
0	RSLPL (0)	**Receive SLIP Latch.** When the RSLP status bit (T1 Receive Elastic Buffer Status - R Address Y13) toggles from zero to one, or from one to zero, this status bit is latched to one. It is cleared when either this register, or the T1 Elastic Store Interrupt Status - R Address Y36 is read.

Table 136 - T1 Elastic Store Status Latch - R Address Y26

Bit	Name	Functional Description
15	(0)	Not Used
14	Sa5VL	**Sa5 Bit Value Latch.** This is the latched value of the Sa5 National bit when the Sa6N8L bit (of this register) toggles to one. It is cleared when either this register, or the E1 National Interrupt Status - R Address Y36 is read.
13 12 11 10	Sa6V3L Sa6V2L Sa6V1L Sa6V0L	**Sa6 Nibble (bit 3 to 0) Value Latch.** This is the latched value of the Sa6 National bits nibble (bits 3 to 0) when the Sa6N8L bit (of this register) toggles to one. They are cleared when either this register, or the E1 National Interrupt Status - R Address Y36 is read.
9	Sa6N8L	**Sa6 Nibble Eight Consecutive Times Status Latch.** When eight consecutive identical receive Sa6 National bit nibble patterns are received (per sub-multiframe), this status bit is latched to one. This bit is set on a CRC-4 sub-multiframe basis. It is cleared when either this register, or the E1 National Interrupt Status - R Address Y36 is read.
8	Sa6NL	**Sa6 Nibble Change Status Latch.** When a received Sa6 National bit nibble (per sub-multiframe) changes value, this status bit is latched to one. This bit is set on a CRC-4 sub-multiframe basis. This bit is cleared when either this register, or the corresponding interrupt status register (register address Y36) is read.
7	SaNL	**Sa Nibble Change Status Latch.** When any receive National (i.e. Sa5,Sa6,Sa7 or Sa8) bits nibbles changes value, this status bit is latched to one. This bit is set on a CRC-4 sub-multiframe basis. It is cleared when either this register, or the E1 National Interrupt Status - R Address Y36 is read.
6	Sa5TL	**Sa5 Bit Change Status Latch.** When a received Sa5 National bit changes value, this status bit is latched to one. This bit is set on a CRC-4 NFAS frame basis. It is cleared when either this register, or the E1 National Interrupt Status - R Address Y36 is read.
5	SaTL	**Sa Bit Change Status Latch.** When any receive National (i.e. Sa5,Sa6,Sa7 or Sa8) bit changes value, this status bit is latched to one. This bit is set on a CRC-4 NFAS frame basis. It is cleared when either this register, or the E1 National Interrupt Status - R Address Y36 is read.

Table 137 - E1 National Latched Status - R Address Y26

Bit	Name	Functional Description
4	CASRL	**Receive Channel Associated Signaling (CAS) Change Latch.** When any of the receive CAS (i.e. ABCD) bits in the E1 Receive CAS Data Registers - R Address Y71-Y7F, Y81-Y8F change state, this status bit is latched to one. This bit is set on a basic frame (FPb) basis. It is cleared when either this register, or the E1 National Interrupt Status - R Address Y36 is read.
3	CALNL	**CRC-4 Alignment 2ms Timer Latch.** When the CALN status bit (E1 Synchronization & CRC-4 Remote Status - R Address Y10) toggles from zero to one, this status bit is latched to one. This bit is set on a 2ms or CRC-4 multiframe frame basis. It is cleared when either this register, or the E1 National Interrupt Status - R Address Y36 is read.
2	T2L	**Timer 2 Latch.** When the CRC-4 T2 (10ms) status bit (E1 CRC-4 Timers & CRC-4 Local Status - R Address Y11) toggles from zero to one, this status bit is latched to one. This bit is set on a basic frame (FPb) basis. It is cleared when either this register, or the E1 National Interrupt Status - R Address Y36 is read.
1	T1L	**Timer 1 Latch.** When the CRC-4 T1 (100ms) status bit (E1 CRC-4 Timers & CRC-4 Local Status - R Address Y11) toggles from zero to one, this status bit is latched to one. This bit is set on a basic frame (FPb) basis. It is cleared when either this register, or the E1 National Interrupt Status - R Address Y36 is read.
0	ONESECL	**One Second Timer Status Latch.** When the ONESEC status bit (E1 CRC-4 Timers & CRC-4 Local Status - R Address Y11) toggles from zero to one, this status bit is latched to one. This bit is set on a basic frame (FPb) basis. It is cleared when either this register, or the E1 National Interrupt Status - R Address Y36 is read.

Table 137 - E1 National Latched Status - R Address Y26

Bit	Name	Functional Description
15-4	(#### #### ###)	Not Used
3	RAIP	**Remote Alarm Indication Status Persistent Latch.** When the RAI (A) status bit (E1 Alarms & MAS Status - R Address Y12) toggles from zero to one, this status bit is latched to one. This bit is cleared when this register is read while the RAI status bit is zero.
2	AISP	**Alarm Indication Status Signal Persistent.** When the AIS status bit (E1 Alarms & MAS Status - R Address Y12) toggles from zero to one, this status bit is latched to one. This bit is cleared when this register is read while the AIS status bit is zero.
1	LOSSP	**Loss of Signal Status Indication Persistent Latch.** When the LOSS status bit (E1 Alarms & MAS Status - R Address Y12) toggles from zero to one, this status bit is latched to one. This bit is cleared when this register is read while the LOSS status bit is zero.
0	BSYNCP	**Receive Basic Frame Alignment Persistent Latch.** When the $\overline{BSYNC}$ status bit (E1 Synchronization & CRC-4 Remote Status - R Address Y10) toggles from zero to one, this status bit is latched to one. This bit is cleared when this register is read while the $\overline{BSYNC}$ status bit is zero.

Table 138 - E1 Persistent Latched Status - R Address Y27

Bit	Name	Functional Description
15	BEL15	**Framing Bit Error Count Latch.** These bits make up a latch which samples the current value
14	BEL14	of the corresponding counter (T1 Framing Bit Error Counter - R/W Address Y17) on the rising
13	BEL13	edge of the internal one second timer status bit ONESEC (T1 Timer Status - R Address Y11).
12	BEL12	BEL0 is the least significant bit (LSB). This latch is cleared with either:
11	BEL11	a) A hard reset ($\overline{\text{RESET}}$ pin)
10	BEL10	b) A unique soft reset (RST bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W
9	BEL9	Address YF1)
8	BEL8	c) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W
7	BEL7	Address 900)
6	BEL6	
5	BEL5	
4	BEL4	
3	BEL3	
2	BEL2	
1	BEL1	
0	BEL0	

Table 139 - T1 Framing Bit Error Counter Latch - R Address Y28

Bit	Name	Functional Description
15	EEL15	**E-bit Error Count Latch.** These bits make up a latch which samples the current value of the
14	EEL14	corresponding counter (E1 E-bit Error Counter - R/W Address Y17) on the rising edge of the internal
13	EEL13	one second timer status bit ONESEC (E1 CRC-4 Timers & CRC-4 Local Status - R Address Y11).
12	EEL12	EEL0 is the least significant bit (LSB). This latch is cleared with either:
11	EEL11	a) A hard reset ($\overline{\text{RESET}}$ pin)
10	EEL10	b) A unique soft reset (RST bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W
9	EEL9	Address Y03)
8	EEL8	c) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W
7	EEL7	Address 900)
6	EEL6	
5	EEL5	
4	EEL4	
3	EEL3	
2	EEL2	
1	EEL1	
0	EEL0	

Table 140 - E1 E-Bit Error Count Latch - R Address Y28

Bit	Name	Functional Description
15	VEL15	**Bipolar Violation Count Latch.** These bits make up a latch which samples the current
14	VEL14	value of the corresponding counter (T1 Bipolar Violation Counter - R/W Address Y18) on
13	VEL13	the rising edge of the internal one second timer status bit ONESEC (T1 Timer Status - R
12	VEL12	Address Y11). VEL0 is the least significant bit (LSB). This latch is cleared with either:
11	VEL11	a) A hard reset ($\overline{\text{RESET}}$ pin)
10	VEL10	b) A unique soft reset (RST bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W
9	VEL9	Address YF1)
8	VEL8	c) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/
7	VEL7	W Address 900)
6	VEL6	
5	VEL5	
4	VEL4	
3	VEL3	
2	VEL2	
1	VEL1	
0	VEL0	
	(0000 0000	
	0000 0000)	

Table 141 - T1 Bipolar Violation Error Counter Latch - R Address Y29

Bit	Name	Functional Description
15	VEL15	**Bipolar Violation Error Count Latch.** These bits make up a latch which samples the current value
14	VEL14	of the corresponding counter (E1 Bipolar Violation Error Counter - R/W Address Y18) on the rising
13	VEL13	edge of the internal one second timer status bit ONESEC (E1 CRC-4 Timers & CRC-4 Local Status
12	VEL12	- R Address Y11). VEL0 is the least significant bit (LSB). This latch is cleared with either:
11	VEL11	a) A hard reset ($\overline{\text{RESET}}$ pin)
10	VEL10	b) A unique soft reset (RST bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W
9	VEL9	Address Y03)
8	VEL8	c) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W
7	VEL7	Address 900)
6	VEL6	
5	VEL5	
4	VEL4	
3	VEL3	
2	VEL2	
1	VEL1	
0	VEL0	

Table 142 - E1 Bipolar Violation Error Count Latch - R/W Address Y29

Bit	Name	Functional Description

15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
	CEL15
	CEL14
	CEL13
	CEL12
	CEL11
	CEL10
	CEL9
	CEL8
	CEL7
	CEL6
	CEL5
	CEL4
	CEL3
	CEL2
	CEL1
	CEL0
	(0000 0000
	0000 0000)
		CRC-6 Error Count Latch. These bits make up a latch which samples the current value of the corresponding counter (T1 CRC-6 Error Counter - R/W Address Y19) on the rising edge of the internal one second timer status bit ONESEC (T1 Timer Status - R Address Y11). CEL0 is the least significant bit (LSB). This latch is cleared with either:
		    a) A hard reset ($\overline{\text{RESET}}$ pin)
		    b) A unique soft reset (RST bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1)
		    c) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W Address 900)

Table 143 - T1 CRC-6 Error Counter Latch - R Address Y2A

Bit	Name	Functional Description

15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
	CEL15
	CEL14
	CEL13
	CEL12
	CEL11
	CEL10
	CEL9
	CEL8
	CEL7
	CEL6
	CEL5
	CEL4
	CEL3
	CEL2
	CEL1
	CEL0
		CRC-4 Error Count Latch. These bits make up a latch which samples the current value of the corresponding counter (E1 CRC-4 Error Counter - R/W Address Y19) on the rising edge of the internal one second timer status bit ONESEC (E1 CRC-4 Timers & CRC-4 Local Status - R Address Y11). CEL0 is the least significant bit (LSB). This latch is cleared with either:
		    a) A hard reset ($\overline{\text{RESET}}$ pin)
		    b) A unique soft reset (RST bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03)
		    c) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W Address 900)

Table 144 - E1 CRC-4 Error Count Latch - R/W Address Y2A

Bit	Name	Functional Description

15
14
13
12
11
10
9
8
	OFL7
	OFL6
	OFL5
	OFL4
	OFL3
	OFL2
	OFL1
	OFL0
		Out of Frame Alignment Counter Latch. These bits make up a latch which samples the current value of the corresponding counter (T1 Out of Frame and Change of Frame Counters - R/W Address Y1A) on the rising edge of the internal one second timer status bit ONESEC (T1 Timer Status - R Address Y11). OFL0 is the least significant bit (LSB). This latch is cleared with either:
		    a) A hard reset ($\overline{\text{RESET}}$ pin)
		    b) A unique soft reset (RST bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W Address YF1)
		    c) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W Address 900)

Table 145 - T1 Out of Frame & Change of Frame Counter Latch - R Address Y2B

Bit	Name	Functional Description
7	CFL7	**Change of Frame Alignment Counter Latch.** These bits make up a latch which samples the current value of the corresponding counter (T1 Out of Frame and Change of Frame Counters - R/W Address Y1A) on the rising edge of the internal one second timer status bit ONESEC (T1 Timer Status - R Address Y11). CFL0 is the least significant bit (LSB). This latch is cleared with either:
6	CFL6	
5	CFL5	
4	CFL4	
3	CFL3	a) A hard reset ($\overline{\text{RESET}}$ pin)
2	CFL2	b) A unique soft reset (RST bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W
1	CFL1	Address YF1)
0	CFL0	c) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W Address 900)

Table 145 - T1 Out of Frame & Change of Frame Counter Latch - R Address Y2B

Bit	Name	Functional Description
15	BEL7	**Frame Alignment Signal (FAS) Bit Error Count Latch.** These bits make up a latch which samples the current value of the corresponding counter (E1 FAS Bit Error Counter & FAS Error Counter - R/W Address Y1A) on the rising edge of the internal one second timer status bit ONESEC (E1 CRC-4 Timers & CRC-4 Local Status - R Address Y11). BEL0 is the least significant bit (LSB). This latch is cleared with either:
14	BEL6	
13	BEL5	
12	BEL4	
11	BEL3	
10	BEL2	a) A hard reset ($\overline{\text{RESET}}$ pin)
9	BEL1	b) A unique soft reset (RST bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W
8	BEL0	Address Y03)
		c) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W Address 900)
7	FEL7	**Frame Alignment Signal (FAS) Error Count Latch.** These bits make up a latch which samples the current value of the corresponding counter (E1 FAS Bit Error Counter & FAS Error Counter - R/W Address Y1A) on the rising edge of the internal one second timer status bit ONESEC (E1 CRC-4 Timers & CRC-4 Local Status - R Address Y11). FEL0 is the least significant bit (LSB). This latch is cleared with either:
6	FEL6	
5	FEL5	
4	FEL4	
3	FEL3	
2	FEL2	a) A hard reset ($\overline{\text{RESET}}$ pin)
1	FEL1	b) A unique soft reset (RST bit detailed in Table 85 - E1 DL, CCS, CAS and Other Control - R/W
0	FEL0	Address Y03)
		c) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W Address 900)

Table 146 - E1 FAS Error Count Latch - R/W Address Y2B

Bit	Name	Functional Description
15	MFL15	**Multiframe Out of Frame Count Latch.** These bits make up a latch which samples the current
14	MFL14	value of the corresponding counter (T1 Multiframe Out of Frame Counter - R/W Address Y16) on
13	MFL13	the rising edge of the internal one second timer status bit ONESEC (T1 Timer Status - R Address
12	MFL12	Y11). MFL0 is the least significant bit (LSB). This latch is cleared with either:
11	MFL11	a) A hard reset ($\overline{\text{RESET}}$ pin)
10	MFL10	b) A unique soft reset (RST bit detailed in Table 178 - T1 Interrupt and I/O Control - R/W
9	MFL9	Address YF1)
8	MFL8	c) A global soft reset (RSTC bit detailed in Table 70 - T1 & E1 Global Mode Control - R/W
7	MFL7	Address 900)
6	MFL6	
5	MFL5	
4	MFL4	
3	MFL3	
2	MFL2	
1	MFL1	
0	MFL0	

Table 147 - T1 Multiframe Out of Frame Counter Latch - R Address Y2C

Bit	Name	Functional Description
15-9	(0000 000)	Not Used
8	GAI (0)	**Go Ahead Interrupt.** This bit is one when the corresponding GAL bit in the T1 & E1 HDLC Latched Status - R Address Y23 is set, and the corresponding GAM bit in the T1 & E1 HDLC Interrupt Mask - R/W Address Y43 is unmasked. This bit is cleared when either this register, or the latched status register is read.
7	EOPDI (0)	**End of Packet Detect Interrupt.** This bit is one when the corresponding EOPDL bit in the T1 & E1 HDLC Latched Status - R Address Y23 is set, and the corresponding EOPDM bit in the T1 & E1 HDLC Interrupt Mask - R/W Address Y43 is unmasked. This bit is cleared when either this register, or the latched status register is read.
6	TEOPI (0)	**Transmit End of Packet Interrupt.** This bit is one when the corresponding TEOPL bit in the T1 & E1 HDLC Latched Status - R Address Y23 is set, and the corresponding TEOPM bit in the T1 & E1 HDLC Interrupt Mask - R/W Address Y43 is unmasked. This bit is cleared when either this register, or the latched status register is read.
5	EOPRI (0)	**End of Packet Read Interrupt.** This bit is one when the corresponding EOPRL bit in the T1 & E1 HDLC Latched Status - R Address Y23 is set, and the corresponding EOPRM bit in the T1 & E1 HDLC Interrupt Mask - R/W Address Y43 is unmasked. This bit is cleared when either this register, or the latched status register is read.
4	TXFLI (0)	**Transmit FIFO Low Interrupt.** This bit is one when the corresponding TXFLL bit in the T1 & E1 HDLC Latched Status - R Address Y23 is set, and the corresponding TXFLM bit in the T1 & E1 HDLC Interrupt Mask - R/W Address Y43 is unmasked. This bit is cleared when either this register, or the latched status register is read.
3	FAI (0)	**Frame Abort Interrupt.** This bit is one when the corresponding FAL bit in the T1 & E1 HDLC Latched Status - R Address Y23 is set, and the corresponding FAM bit in the T1 & E1 HDLC Interrupt Mask - R/W Address Y43 is unmasked. This bit is cleared when either this register, or the latched status register is read.
2	TXFEI (0)	**Transmit FIFO Empty Interrupt.** This bit is one when the corresponding TXUNDERL bit in the T1 & E1 HDLC Latched Status - R Address Y23 is set, and the corresponding TXUNDERM bit in the T1 & E1 HDLC Interrupt Mask - R/W Address Y43 is unmasked. This bit is cleared when either this register, or the latched status register is read.

Table 148 - T1 & E1 HDLC Interrupt Status - R Address Y33

Bit	Name	Functional Description
1	RXFHI (0)	**Receive FIFO High Interrupt.** This bit is one when the corresponding RXFFL bit in the T1 & E1 HDLC Latched Status - R Address Y23 is set, and the corresponding RXFFM bit in the T1 & E1 HDLC Interrupt Mask - R/W Address Y43 is unmasked. This bit is cleared when either this register, or the latched status register is read.
0	RXFOI (0)	**Receive FIFO Overflow Interrupt.** This bit is one when the corresponding RXOVFLL bit in the T1 & E1 HDLC Latched Status - R Address Y23 is set, and the corresponding RXOVFLM bit in the T1 & E1 HDLC Interrupt Mask - R/W Address Y43 is unmasked. This bit is cleared when either this register, or the latched status register is read.

Table 148 - T1 & E1 HDLC Interrupt Status - R Address Y33

Bit	Name	Functional Description
15	BEOI (0)	**Framing Bit Error Counter Overflow Interrupt.** This bit is one when the corresponding BEOL bit in the T1 Receive Sync and Alarm Latch - R Address Y24 is set, and the corresponding BEOM bit in the T1 Receive and Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
14	CEOI (0)	**CRC-6 Error Counter Overflow Interrupt.** This bit is one when the corresponding CEOL bit in the T1 Receive Sync and Alarm Latch - R Address Y24 is set, and the corresponding CEOM bit in the T1 Receive and Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
13	OFOI (0)	**Out Of Frame Counter Overflow Interrupt.** This bit is one when the corresponding OFOL bit in the T1 Receive Sync and Alarm Latch - R Address Y24 is set, and the corresponding OFOM bit in the T1 Receive and Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
12	CFOI (0)	**Change of Frame Alignment Counter Overflow Interrupt**. This bit is one when the corresponding CFOL bit in the T1 Receive Sync and Alarm Latch - R Address Y24 is set, and the corresponding CFOM bit in the T1 Receive and Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
11	VEOI (0)	**Bipolar Violation Counter Overflow Interrupt.** This bit is one when the corresponding VEOL bit in the T1 Receive Sync and Alarm Latch - R Address Y24 is set, and the corresponding VEOM bit in the T1 Receive and Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
10	PEOI (0)	**PRBS Error Counter Overflow Interrupt.** This bit is one when the corresponding PEOL bit in the T1 Receive Sync and Alarm Latch - R Address Y24 is set, and the corresponding PEOM bit in the T1 Receive and Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
9	PCOI (0)	**Multiframe Counter Overflow Interrupt.** This bit is one when the corresponding PCOL bit in the T1 Receive Sync and Alarm Latch - R Address Y24 is set, and the corresponding PCOM bit in the T1 Receive and Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
8	MFOI (0)	**Multiframes Out Of Sync Overflow Interrupt.** This bit is one when the corresponding MFOL bit in the T1 Receive Sync and Alarm Latch - R Address Y24 is set, and the corresponding MFOM bit in the T1 Receive and Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
7	TFSYNI (0)	**Terminal Frame Synchronization Interrupt.** This bit is one when the corresponding TFSYNL bit in the T1 Receive Sync and Alarm Latch - R Address Y24 is set, and the corresponding TFSYNM bit in the T1 Receive and Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.

Table 149 - T1 Receive and Sync Interrupt Status - R Address Y34

Bit	Name	Functional Description
6	MFSYNI (0)	**Multiframe Synchronization Interrupt.** This bit is one when the corresponding MFSYNL bit in the T1 Receive Sync and Alarm Latch - R Address Y24 is set, and the corresponding MFSYNM bit in the T1 Receive and Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
5	BEII (0)	**Framing Bit Error Interrupt.** This bit is one when the corresponding BEIL bit in the T1 Receive Sync and Alarm Latch - R Address Y24 is set, and the corresponding BEIM bit in the T1 Receive and Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
4	CFII (0)	**Change of Frame Alignment Interrupt.** This bit is one when the corresponding CFIL bit in the T1 Receive Sync and Alarm Latch - R Address Y24 is set, and the corresponding CFIM bit in the T1 Receive and Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
3	SEFI (0)	**Severely Errored Frame Interrupt.** This bit is one when the corresponding SEFL bit in the T1 Receive Sync and Alarm Latch - R Address Y24 is set, and the corresponding SEFM bit in the T1 Receive and Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
2	AISI (0)	**Alarm Indication Signal Interrupt.** This bit is one when the corresponding AISL bit in the T1 Receive and Alarm Latch - R Address Y24 is set, and the corresponding AISM bit in the T1 Receive and Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
1	CEII	**CRC-6 Error Counter Indication Interrupt.** This bit is one when the corresponding CEIL bit in the T1 Receive Sync and Alarm Latch - R Address Y24 is set, and the corresponding CEIM bit in the T1 Receive and Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
0	LOSI (0)	**Digital Loss of Signal Interrupt.** This bit is one when the corresponding LOSL bit in the T1 Receive Sync and Alarm Latch - R Address Y24 is set, and the corresponding LOSM bit in the T1 Receive and Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.

Table 149 - T1 Receive and Sync Interrupt Status - R Address Y34

Bit	Name	Functional Description
15	(0)	Not Used
14	RCRCRI	**Remote CRC-4 and RAI Interrupt.** This bit is one when the corresponding RCRCRL bit in the E1 Sync Latched Status - R Address Y24 is set, and the corresponding RCRCRM bit in the E1 Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
13	RSLPI	**Receive Slip Interrupt.** This bit is one when the corresponding RSLPL bit in the E1 Sync Latched Status - R Address Y24 is set, and the corresponding RSLPM bit in the E1 Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
12	YI	**Receive Y-bit Interrupt.** This bit is one when the corresponding YL bit in the E1 Sync Latched Status - R Address Y24 is set, and the corresponding YM bit in the E1 Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
11	AUXPI	**Auxiliary Pattern Interrupt.** This bit is one when the corresponding AUXPL bit in the E1 Sync Latched Status - R Address Y24 is set, and the corresponding AUXPM bit in the E1 Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.

Table 150 - E1 Sync Interrupt Status - R Address Y34

Bit	Name	Functional Description
10	RAII	**Remote Alarm Indication Status Interrupt.** This bit is one when the corresponding RAIL bit in the E1 Sync Latched Status - R Address Y24 is set, and the corresponding RAIM bit in the E1 Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
9	AISI	**Alarm Indication Status Signal Interrupt.** This bit is one when the corresponding AISL bit in the E1 Sync Latched Status - R Address Y24 is set, and the corresponding AISM bit in the E1 Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
8	AIS16I	**Alarm Indication Signal 16 Status Interrupt.** This bit is one when the corresponding AIS16L bit in the E1 Sync Latched Status - R Address Y24 is set, and the corresponding AIS16M bit in the E1 Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
7	LOSSI	**Loss of Signal Status Indication Interrupt.** This bit is one when the corresponding LOSSL bit in the E1 Sync Latched Status - R Address Y24 is set, and the corresponding LOSSM bit in the E1 Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
6	RCRC0I	**Remote CRC-4 and RAI T10 Interrupt.** This bit is one when the corresponding RCRC0L bit in the E1 Sync Latched Status - R Address Y24 is set, and the corresponding RCRC0M bit in the E1 Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
5	RCRC1I	**Remote CRC-4 and RAI T450 Interrupt.** This bit is one when the corresponding RCRC1L bit in the E1 Sync Latched Status - R Address Y24 is set, and the corresponding RCRC1M bit in the E1 Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
4	CEFSI	**Consecutively Errored Frame Alignment Signal Interrupt.** This bit is one when the corresponding CEFSL bit in the E1 Sync Latched Status - R Address Y24 is set, and the corresponding CEFSM bit in the E1 Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
3	RFAILI	**Remote CRC-4 Multiframe Generator/Detector Failure Interrupt.** This bit is one when the corresponding RFAILL bit in the E1 Sync Latched Status - R Address Y24 is set, and the corresponding RFAILM bit in the E1 Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
2	CSYNCI	**Receive CRC-4 Synchronization Interrupt.** This bit is one when the corresponding CSYNCL bit in the E1 Sync Latched Status - R Address Y24 is set, and the corresponding CSYNCM bit in the E1 Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
1	MSYNCI	**Receive Multiframe Alignment Interrupt.** This bit is one when the corresponding MSYNCL bit in the E1 Sync Latched Status - R Address Y24 is set, and the corresponding MSYNCM bit in the E1 Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.
0	BSYNCI	**Receive Basic Frame Alignment Interrupt.** This bit is one when the corresponding BSYNCL bit in the E1 Sync Latched Status - R Address Y24 is set, and the corresponding BSYNCM bit in the E1 Sync Interrupt Mask - R/W Address Y44 is unmasked. This bit is cleared when either this register, or the latched status register is read.

Table 150 - E1 Sync Interrupt Status - R Address Y34

Bit	Name	Functional Description
15	D4YI (0)	**D4 Yellow Interrupt.** This bit is one when the corresponding D4YL bit in the T1 Receive Line Status and Timer Latch - R Address Y25 is set, and the corresponding D4YM bit in the T1 Receive Line and Timer Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
14	D4Y48I (0)	**D4 Y48 Interrupt.** This bit is one when the corresponding D4Y48L bit in the T1 Receive Line Status and Timer Latch - R Address Y25 is set, and the corresponding D4Y48M bit in the T1 Receive Line and Timer Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
13	SECYI (0)	**Secondary Yellow Interrupt.** This bit is one when the corresponding SECYL bit in the T1 Receive Line Status and Timer Latch - R Address Y25 is set, and the corresponding SECYM bit in the T1 Receive Line and Timer Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
12	ESFYI (0)	**ESF Yellow Interrupt.** This bit is one when the corresponding ESFYL bit in the T1 Receive Line Status and Timer Latch - R Address Y25 is set, and the corresponding ESFYM bit in the T1 Receive Line and Timer Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
11	T1DMYI (0)	**T1DM Yellow Interrupt.** This bit is one when the corresponding T1DMYL bit in the T1 Receive Line Status and Timer Latch - R Address Y25 is set, and the corresponding T1DMYM bit in the T1 Receive Line and Timer Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
10	(0)	Not Used
9	VEII (0)	**Bipolar Violation Counter Indication Interrupt.** This bit is one when the corresponding VEIL bit in the T1 Receive Line Status and Timer Latch - R Address Y25 is set, and the corresponding VEIM bit in the T1 Receive Line and Timer Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
8	PEII (0)	**PRBS Error Counter Indication Interrupt.** This bit is one when the corresponding PEIL bit in the T1 Receive Line Status and Timer Latch - R Address Y25 is set, and the corresponding PEIM bit in the T1 Receive Line and Timer Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
7	PDVI (0)	**Pulse Density Violation Interrupt.** This bit is one when the corresponding PDVL bit in the T1 Receive Line Status and Timer Latch - R Address Y25 is set, and the corresponding PDVM bit in the T1 Receive Line and Timer Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
6	LLEDI (0)	**Line Loop Code Enable Detected Interrupt.** This bit is one when the corresponding LLEDL bit in the T1 Receive Line Status and Timer Latch - R Address Y25 is set, and the corresponding LLEDM bit in the T1 Receive Line and Timer Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
5	LLDDI (0)	**Line Loop Code Disable Detected Interrupt.** This bit is one when the corresponding LLDDL bit in the T1 Receive Line Status and Timer Latch - R Address Y25 is set, and the corresponding LLDDM bit in the T1 Receive Line and Timer Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
4	BOMI (0)	**Bit Oriented Message Interrupt.** This bit is one when the corresponding BOML bit in the T1 Receive Line Status and Timer Latch - R Address Y25 is set, and the corresponding BOMM bit in the T1 Receive Line and Timer Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
3	BOMMI (0)	**Bit Oriented Message Match Interrupt.** This bit is one when the corresponding BOMML bit in the T1 Receive Line Status and Timer Latch - R Address Y25 is set, and the corresponding BOMMM bit in the T1 Receive Line and Timer Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.

Table 151 - T1 Receive Line and Timer Interrupt Status - R Address Y35

Bit	Name	Functional Description
2	CASRI (0)	**Signaling Interrupt Status.** This bit is one when the corresponding CASRL bit in the T1 Receive Line Status and Timer Latch - R Address Y25 is set, and the corresponding CASRM bit in the T1 Receive Line and Timer Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
1	ONESE CI (0)	**One Second Interrupt Status.** This bit is one when the corresponding ONESECL bit in the T1 Receive Line Status and Timer Latch - R Address Y25 is set, and the corresponding ONESECM bit in the T1 Receive Line and Timer Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
0	TWOSE CI (0)	**Two Second Interrupt Status.** This bit is one when the corresponding TWOSECL bit in the T1 Receive Line Status and Timer Latch - R Address Y25 is set, and the corresponding TWOSECM bit in the T1 Receive Line and Timer Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.

Table 151 - T1 Receive Line and Timer Interrupt Status - R Address Y35

Bit	Name	Functional Description
15	(0)	Not Used
14	SLOI (0)	**Loss of Sync Counter Overflow Interrupt.** This bit is one when the corresponding SLOL bit in the E1 Counter Latched Status - R Address Y25 is set, and the corresponding SLOM bit in the E1 Counter Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
13	FEOI (0)	**Frame Alignment Signal (FAS) Error Counter Overflow Interrupt.** This bit is one when the corresponding FEOL bit in the E1 Counter Latched Status - R Address Y25 is set, and the corresponding FEOM bit in the E1 Counter Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
12	FEII (0)	**Frame Alignment Signal (FAS) Error Counter Indication Interrupt.** This bit is one when the corresponding FEIL bit in the E1 Counter Latched Status - R Address Y25 is set, and the corresponding FEIM bit in the E1 Counter Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
11	BEOI (0)	**Frame Alignment Signal (FAS) Bit Error Counter Overflow Interrupt.** This bit is one when the corresponding BEOL bit in the E1 Counter Latched Status - R Address Y25 is set, and the corresponding BEOM bit in the E1 Counter Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
10	BEII (0)	**Frame Alignment Signal (FAS) Bit Error Counter Indication Interrupt.** This bit is one when the corresponding BEIL bit in the E1 Counter Latched Status - R Address Y25 is set, and the corresponding BEIM bit in the E1 Counter Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
9	CEOI (0)	**CRC-4 Error Counter Overflow Interrupt.** This bit is one when the corresponding CEOL bit in the E1 Counter Latched Status - R Address Y25 is set, and the corresponding CEOM bit in the E1 Counter Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
8	CEII (0)	**CRC-4 Error Counter Indication Interrupt.** This bit is one when the corresponding CEIL bit in the E1 Counter Latched Status - R Address Y25 is set, and the corresponding CEIM bit in the E1 Counter Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
7	VEOI (0)	**Bipolar Violation Error Counter Overflow Interrupt.** This bit is one when the corresponding VEOL bit in the E1 Counter Latched Status - R Address Y25 is set, and the corresponding VEOM bit in the E1 Counter Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.

Table 152 - E1 Counter Interrupt Status - R Address Y35

Bit	Name	Functional Description
6	VEII (0)	**Bipolar Violation Error Counter Indication Interrupt.** This bit is one when the corresponding VEIL bit in the E1 Counter Latched Status - R Address Y25 is set, and the corresponding VEIM bit in the E1 Counter Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
5	EEOI (0)	**E-Bit Error Counter Overflow Interrupt.** This bit is one when the corresponding EEOL bit in the E1 Counter Latched Status - R Address Y25 is set, and the corresponding EEOM bit in the E1 Counter Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
4	EEII (0)	**E-Bit Error Counter Indication Interrupt.** This bit is one when the corresponding EEIL bit in the E1 Counter Latched Status - R Address Y25 is set, and the corresponding EEIM bit in the E1 Counter Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
3	PCOI (0)	**PRBS CRC-4 Counter Overflow Interrupt.** This bit is one when the corresponding PCOL bit in the E1 Counter Latched Status - R Address Y25 is set, and the corresponding PCOM bit in the E1 Counter Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
2	JAI (0)	**Jitter Attenuator Interrupt.** This bit is one when the corresponding JAL bit in the E1 Counter Latched Status - R Address Y25 is set, and the corresponding JAM bit in the E1 Counter Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
1	PEOI (0)	**PRBS Error Counter Overflow Interrupt.** This bit is one when the corresponding PEOL bit in the E1 Counter Latched Status - R Address Y25 is set, and the corresponding PEOM bit in the E1 Counter Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.
0	PEII (0)	**PRBS Error Counter Indication Interrupt.** This bit is one when the corresponding PEIL bit in the E1 Counter Latched Status - R Address Y25 is set, and the corresponding PEIM bit in the E1 Counter Interrupt Mask - R/W Address Y45 is unmasked. This bit is cleared when either this register, or the latched status register is read.

Table 152 - E1 Counter Interrupt Status - R Address Y35

Bit	Name	Functional Description
15-4	(#### ##)	Not Used
3	EZOI (0)	**Excessive Zero Counter Overflow Interrupt.** This bit is one when the corresponding EZOL bit in the T1 Elastic Store Status Latch - R Address Y26 is set, and the corresponding EZOM bit in the T1 Elastic Store Interrupt Mask - R/W Address Y46 is unmasked. This bit is cleared when either this register, or the latched status register is read.
2	EZII(0)	**Excessive Zero Counter Indication Interrupt.** This bit is one when the corresponding EZIL bit in the T1 Elastic Store Status Latch - R Address Y26 is set, and the corresponding EZIM bit in the T1 Elastic Store Interrupt Mask - R/W Address Y46 is unmasked. This bit is cleared when either this register, or the latched status register is read.
1	TSLPI (0)	**Transmit SLIP Interrupt.** This bit is one when the corresponding TSLPL bit in the T1 Elastic Store Status Latch - R Address Y26 is set, and the corresponding TSLPM bit in the T1 Elastic Store Interrupt Mask - R/W Address Y46 is unmasked. This bit is cleared when either this register, or the latched status register is read.
0	RSLPI (0)	**Receive SLIP Interrupt.** This bit is one when the corresponding RSLPL bit in the T1 Elastic Store Status Latch - R Address Y26 is set, and the corresponding RSLPM bit in the T1 Elastic Store Interrupt Mask - R/W Address Y46 is unmasked. This bit is cleared when either this register, or the latched status register is read.

Table 153 - T1 Elastic Store Interrupt Status - R Address Y36

Bit	Name	Functional Description
15	(0)	Not Used
14	Sa5VI (0)	**Sa5 Value Bit Interrupt.** This bit is one when the corresponding Sa5VL bit in the E1 National Latched Status - R Address Y26 is set, and the corresponding Sa5VM bit in the E1 National Interrupt Mask - R/W Address Y46 is unmasked. This bit is cleared when either this register, or the latched status register is read.
13 12 11 10	Sa6V3I Sa6V2I Sa6V1I Sa6V0I (0000)	**Sa6 Value Bits 3-0 Interrupt.** This bit is one when the corresponding Sa6V*L bit in the E1 National Latched Status - R Address Y26 is set, and the corresponding Sa6V*M bit in the E1 National Interrupt Mask - R/W Address Y46 is unmasked. This bit is cleared when either this register, or the latched status register is read.
9	Sa6N8I (0)	**Eight Consecutive Sa6 Nibbles Interrupt.** This bit is one when the corresponding Sa6N8L bit in the E1 National Latched Status - R Address Y26 is set, and the corresponding Sa6N8M bit in the E1 National Interrupt Mask - R/W Address Y46 is unmasked. This bit is cleared when either this register, or the latched status register is read.
8	Sa6NI (0)	**Sa6 Nibble Change Interrupt.** This bit is one when the corresponding Sa6NL bit in the E1 National Latched Status - R Address Y26 is set, and the corresponding Sa6NM bit in the E1 National Interrupt Mask - R/W Address Y46 is unmasked. This bit is cleared when either this register, or the latched status register is read.
7	SaNI (0)	**Sa Nibble Change Interrupt.** This bit is one when the corresponding SaNL bit in the E1 National Latched Status - R Address Y26 is set, and the corresponding SaNM bit in the E1 National Interrupt Mask - R/W Address Y46 is unmasked. This bit is cleared when either this register, or the latched status register is read.
6	Sa5TI (0)	**Sa5 Bit Change Interrupt.** This bit is one when the corresponding Sa5TL bit in the E1 National Latched Status - R Address Y26 is set, and the corresponding Sa5TM bit in the E1 National Interrupt Mask - R/W Address Y46 is unmasked. This bit is cleared when either this register, or the latched status register is read.
5	SaTI (0)	**Sa Bit Change Interrupt.** This bit is one when the corresponding SaTL bit in the E1 National Latched Status - R Address Y26 is set, and the corresponding SaTM bit in the E1 National Interrupt Mask - R/W Address Y46 is unmasked. This bit is cleared when either this register, or the latched status register is read.
4	CASRI (0)	**Receive Channel Associated Signaling (CAS) Change Interrupt.** This bit is one when the corresponding CASRL bit in the E1 National Latched Status - R Address Y26 is set, and the corresponding CASRM bit in the E1 National Interrupt Mask - R/W Address Y46 is unmasked. This bit is cleared when either this register, or the latched status register is read.
3	CALNI (0)	**CRC-4 Alignment 2ms Timer Interrupt.** This bit is one when the corresponding CALNL bit in the E1 National Latched Status - R Address Y26 is set, and the corresponding CALNM bit in the E1 National Interrupt Mask - R/W Address Y46 is unmasked. This bit is cleared when either this register, or the latched status register is read.
2	T2I (0)	**Timer 2 Interrupt.** This bit is one when the corresponding T2L bit in the E1 National Latched Status - R Address Y26 is set, and the corresponding T2M bit in the E1 National Interrupt Mask - R/W Address Y46 is unmasked. This bit is cleared when either this register, or the latched status register is read.
1	T1I (0)	**Timer 1 Interrupt.** This bit is one when the corresponding T1L bit in the E1 National Latched Status - R Address Y26 is set, and the corresponding T1M bit in the E1 National Interrupt Mask - R/W Address Y46 is unmasked. This bit is cleared when either this register, or the latched status register is read.
0	ONESECI (0)	**One Second Timer Status Interrupt.** This bit is one when the corresponding ONESECL bit in the E1 National Latched Status - R Address Y26 is set, and the corresponding ONESECM bit in the E1 National Interrupt Mask - R/W Address Y46 is unmasked. This bit is cleared when either this register, or the latched status register is read.

Table 154 - E1 National Interrupt Status - R Address Y36

Bit	Name	Functional Description
15-9	(#### ###)	Not Used
8	GAM (0)	**Go Ahead Mask.** This is the mask bit for the corresponding GAI bit in the T1 & E1 HDLC Interrupt Status - R Address Y33. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
7	EOPDM (0)	**End of Packet Detect Mask.** This is the mask bit for the corresponding EOPDI bit in the T1 & E1 HDLC Interrupt Status - R Address Y33. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
6	TEOPM (0)	**Transmit End of Packet Mask.** This is the mask bit for the corresponding TEOPI bit in the T1 & E1 HDLC Interrupt Status - R Address Y33. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
5	EOPRM (0)	**End of Packet Read Mask.** This is the mask bit for the corresponding EOPRI bit in the T1 & E1 HDLC Interrupt Status - R Address Y33. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
4	TXFLM (0)	**Transmit FIFO Low Mask.** This is the mask bit for the corresponding TXFLI bit in the T1 & E1 HDLC Interrupt Status - R Address Y33. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
3	FAM (0)	**Frame Abort Mask.** This is the mask bit for the corresponding FAI bit in the T1 & E1 HDLC Interrupt Status - R Address Y33. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
2	TXFEM (0)	**Transmit FIFO Empty Mask.** This is the mask bit for the corresponding TXUNDERI bit in the T1 & E1 HDLC Interrupt Status - R Address Y33. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
1	RXFHM (0)	**Receive FIFO High Mask.** This is the mask bit for the corresponding RXFFI bit in the T1 & E1 HDLC Interrupt Status - R Address Y33. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
0	RXFOM (0)	**Receive FIFO Overflow Mask.** This is the mask bit for the corresponding RXOVFLI bit in the T1 & E1 HDLC Interrupt Status - R Address Y33. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.

Table 155 - T1 & E1 HDLC Interrupt Mask - R/W Address Y43

Bit	Name	Functional Description
15	BEOM (0)	**Framing Bit Error Counter Overflow Mask.** This is the mask bit for the corresponding BEOI bit in the T1 Receive and Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
14	CEOM (0)	**CRC-6 Error Counter Overflow Mask.** This is the mask bit for the corresponding CEOI bit in the T1 Receive and Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
13	OFOM (0)	**Out Of Frame Counter Overflow Mask**. This is the mask bit for the corresponding OFOI bit in the T1 Receive and Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
12	CFOM (0)	**Change of Frame Alignment Counter Overflow Mask.** This is the mask bit for the corresponding CFOI bit in the T1 Receive and Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
11	VEOM (0)	**Bipolar Violation Counter Overflow Mask.** This is the mask bit for the corresponding VEOI bit in the T1 Receive and Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.

Table 156 - T1 Receive and Sync Interrupt Mask - R/W Address Y44

Bit	Name	Functional Description
10	PEOM (0)	**PRBS Error Counter Overflow Mask.** This is the mask bit for the corresponding PEOI bit in the T1 Receive and Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
9	PCOM (0)	**Multiframe Counter Overflow Mask.** This is the mask bit for the corresponding PCOI bit in the T1 Receive and Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
8	MFOM (0)	**Multiframes Out Of Sync Overflow Mask.** This is the mask bit for the corresponding MFOI bit in the T1 Receive and Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
7	TFSYNM (0)	**Terminal Frame Synchronization Mask.** This is the mask bit for the corresponding TFSYNI bit in the T1 Receive and Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
6	MFSYNM (0)	**Multiframe Synchronization Mask.** This is the mask bit for the corresponding MFSYNI bit in the T1 Receive and Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
5	BEIM (0)	**Framing Bit Error Mask.** This is the mask bit for the corresponding BEII bit in the T1 Receive and Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
4	CFIM (0)	**Change of Frame Alignment Counter Indication Mask.** This is the mask bit for the corresponding CFII bit in the T1 Receive and Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
3	SEFM (0)	**Severely Errored Frame Mask.** This is the mask bit for the corresponding SEFI bit in the T1 Receive and Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
2	AISM (0)	**Alarm Indication Signal Mask.** This is the mask bit for the corresponding AISI bit in the T1 Receive and Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
1	CEIM (0)	**CRC-6 Error Counter Indication Mask.** This is the mask bit for the corresponding CEII bit in the T1 Receive and Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
0	LOSM (0)	**Digital Loss of Signal Mask.** This is the mask bit for the corresponding LOSI bit in the T1 Receive and Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.

Table 156 - T1 Receive and Sync Interrupt Mask - R/W Address Y44

Bit	Name	Functional Description
15	(0)	Not Used
14	RCRCRM (0)	**Remote CRC-4 and RAI Mask.** This is the mask bit for the corresponding RCRCRI bit in the E1 Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
13	RSLPM (0)	**Receive Slip Mask.** This is the mask bit for the corresponding RSLPI bit in the E1 Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
12	YM (0)	**Receive Y-bit Mask.** This is the mask bit for the corresponding YI bit in the E1 Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.

Table 157 - E1 Sync Interrupt Mask - R/W Address Y44

Bit	Name	Functional Description
11	AUXPM (0)	**Auxiliary Pattern Mask.** This is the mask bit for the corresponding AUXPI bit in the E1 Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
10	RAIM (0)	**Remote Alarm Indication Status Mask.** This is the mask bit for the corresponding RAII bit in the E1 Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
9	AISM (0)	**Alarm Indication Status Signal Mask.** This is the mask bit for the corresponding AISI bit in the E1 Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
8	$\overline{\text{AIS16M}}$ $\overline{(0)}$	**Alarm Indication Signal 16 Status Mask.** This is the mask bit for the corresponding AIS16I bit in the E1 Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
7	LOSSM (0)	**Loss of Signal Status Indication Mask.** This is the mask bit for the corresponding LOSSI bit in the E1 Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
6	RCRC0M (0)	**Remote CRC-4 and RAI T10 Mask.** This is the mask bit for the corresponding RCRC0I bit in the E1 Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
5	RCRC1M (0)	**Remote CRC-4 and RAI T450 Mask.** This is the mask bit for the corresponding RCRC1I bit in the E1 Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
4	CEFSM (0)	**Consecutively Errored Frame Alignment Signal Mask.** This is the mask bit for the corresponding CEFSI bit in the E1 Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
3	RFAILM (0)	**Remote CRC-4 Multiframe Generator/Detector Failure Mask.** This is the mask bit for the corresponding RFAILI bit in the E1 Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
2	CSYNCM (0)	**Receive CRC-4 Synchronization Mask.** This is the mask bit for the corresponding CSYNCI bit in the E1 Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
1	MSYNCM (0)	**Receive Multiframe Alignment Mask.** This is the mask bit for the corresponding MSYNCI bit in the E1 Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
0	BSYNCM (0)	**Receive Basic Frame Alignment Mask.** This is the mask bit for the corresponding BSYNCIS bit in the E1 Sync Interrupt Status - R Address Y34. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.

Table 157 - E1 Sync Interrupt Mask - R/W Address Y44

Bit	Name	Functional Description
15	D4YM (0)	**D4 Yellow Mask.** This is the mask bit for the corresponding D4YI bit in the T1 Receive Line and Timer Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
14	D4Y48M (0)	**D4 Y48 Mask.** This is the mask bit for the corresponding D4Y48I bit in the T1 Receive Line and Timer Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
13	SECYM (0)	**Secondary Yellow Mask.** This is the mask bit for the corresponding SECYI bit in the T1 Receive Line and Timer Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
12	ESFYM (0)	**ESF Yellow Mask.** This is the mask bit for the corresponding ESFYI bit in the T1 Receive Line and Timer Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
11	T1DMYM (0)	**T1DM Yellow Mask.** This is the mask bit for the corresponding T1DMYI bit in the T1 Receive Line and Timer Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
10	(0)	Not Used
9	VEIM (0)	**Bipolar Violation Counter Indication Mask.** This is the mask bit for the corresponding VEII bit in the T1 Receive Line and Timer Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
8	PEIM (0)	**PRBS Error Counter Indication Mask.** This is the mask bit for the corresponding PEII bit in the T1 Receive Line and Timer Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
7	PDVM (0)	**Pulse Density Violation Mask.** This is the mask bit for the corresponding PDVI bit in the T1 Receive Line and Timer Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
6	LLEDM (0)	**Loop Code Enable Detected Mask.** This is the mask bit for the corresponding LLEDI bit in the T1 Receive Line and Timer Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
5	LLDDM (0)	**Loop Code Disable Detected Mask.** This is the mask bit for the corresponding LLDDI bit in the T1 Receive Line and Timer Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
4	BOMM (0)	**Bit Oriented Message Mask.** This is the mask bit for the corresponding BOMI bit in the T1 Receive Line and Timer Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
3	BOMMM (0)	**Bit Oriented Message Match Mask.** This is the mask bit for the corresponding BOMMI bit in the T1 Receive Line and Timer Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
2	CASRM (0)	**Signaling Interrupt Status.** This is the mask bit for the corresponding CASRI bit in the T1 Receive Line and Timer Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
1	ONESECM (0)	**One Second Interrupt Status.** This is the mask bit for the corresponding ONESECI bit in the T1 Receive Line and Timer Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
0	TWOSECM (0)	**Two Second Interrupt Status.** This is the mask bit for the corresponding TWOSECI bit in the T1 Receive Line and Timer Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.

Table 158 - T1 Receive Line and Timer Interrupt Mask - R/W Address Y45

Bit	Name	Functional Description
15	(0)	Not Used
14	SLOM (0)	**Loss of Sync Counter Overflow Mask.** This is the mask bit for the corresponding SLOI bit in the E1 Counter Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
13	FEOM (0)	**Frame Alignment Signal (FAS) Error Counter Overflow Mask.** This is the mask bit for the corresponding FEOI bit in the E1 Counter Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
12	FEIM (0)	**Frame Alignment Signal (FAS) Error Counter Indication Mask.** This is the mask bit for the corresponding FEII bit in the E1 Counter Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
11	BEOM (0)	**Frame Alignment Signal (FAS) Bit Error Counter Overflow Mask.** This is the mask bit for the corresponding BEOI bit in the E1 Counter Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
10	BEIM (0)	**Frame Alignment Signal (FAS) Bit Error Counter Indication Mask.** This is the mask bit for the corresponding BEII bit in the E1 Counter Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
9	CEOM (0)	**CRC-4 Error Counter Overflow Mask.** This is the mask bit for the corresponding CEOI bit in the E1 Counter Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
8	CEIM (0)	**CRC-4 Error Counter Indication Mask.** This is the mask bit for the corresponding CEII bit in the E1 Counter Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
7	VEOM (0)	**Bipolar Violation Error Counter Overflow Mask.** This is the mask bit for the corresponding VEOI bit in the E1 Counter Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
6	VEIM (0)	**Bipolar Violation Error Counter Indication Mask.** This is the mask bit for the corresponding VEII bit in the E1 Counter Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
5	EEOM (0)	**E-Bit Error Counter Overflow Mask.** This is the mask bit for the corresponding EEOI bit in the E1 Counter Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
4	EEIM (0)	**E-Bit Error Counter Indication Mask.** This is the mask bit for the corresponding EEII bit in the E1 Counter Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
3	PCOM (0)	**PRBS CRC-4 Counter Overflow Mask.** This is the mask bit for the corresponding PCOI bit in the E1 Counter Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
2	JAM (0)	**Jitter Attenuator Mask.** This is the mask bit for the corresponding JAI bit in the E1 Counter Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
1	PEOM (0)	**PRBS Error Counter Overflow Mask.** This is the mask bit for the corresponding PEOI bit in the E1 Counter Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
0	PEIM (0)	**PRBS Error Counter Indication Mask.** This is the mask bit for the corresponding PEII bit in the E1 Counter Interrupt Status - R Address Y35. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.

Table 159 - E1 Counter Interrupt Mask - R/W Address Y45

Bit	Name	Functional Description
15-4	(#### #### ####)	Not Used
3	EZOM (0)	**Excessive Zero Counter Overflow Mask.** This is the mask bit for the corresponding EZOI bit in the T1 Elastic Store Interrupt Status - R Address Y36. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
2	EZIM (0)	**Excessive Zero Counter Indication Mask.** This is the mask bit for the corresponding EZII bit in the T1 Elastic Store Interrupt Status - R Address Y36. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
1	TSLPM (0)	**Transmit SLIP Mask.** This is the mask bit for the corresponding TSLPI bit in the T1 Elastic Store Interrupt Status - R Address Y36. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
0	RSLPM (0)	**Receive SLIP Mask.** This is the mask bit for the corresponding RSLPI bit in the T1 Elastic Store Interrupt Status - R Address Y36. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.

Table 160 - T1 Elastic Store Interrupt Mask - R/W Address Y46

Bit	Name	Functional Description
15	(#)	Not Used
14	Sa5VM	**Sa5 Value Bit Mask.** This is the mask bit for the corresponding Sa5VI bit in the E1 National Interrupt Status - R Address Y36. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
13 12 11 10	Sa6V3M Sa6V2M Sa6V1M Sa6V0M	**Sa6 Value Bits 3-0 Mask.** This is the mask bit for the corresponding Sa6V*I bit in the E1 National Interrupt Status - R Address Y36. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
9	Sa6N8M (0)	**Eight Consecutive Sa6 Nibbles Mask.** This is the mask bit for the corresponding Sa6N8I bit in the E1 National Interrupt Status - R Address Y36. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
8	Sa6NM (0)	**Sa6 Nibble Change Mask.** This is the mask bit for the corresponding Sa6NI bit in the E1 National Interrupt Status - R Address Y36. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
7	SaNM (0)	**Sa Nibble Change Mask.** This is the mask bit for the corresponding SaNI bit in the E1 National Interrupt Status - R Address Y36. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
6	Sa5TM (0)	**Sa5 Bit Change Mask.** This is the mask bit for the corresponding Sa5TI bit in the E1 National Interrupt Status - R Address Y36. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
5	SaTM (0)	**Sa Bit Change Mask.** This is the mask bit for the corresponding SaTI bit in the E1 National Interrupt Status - R Address Y36. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
4	CASRM (0)	**Receive Channel Associated Signaling (CAS) Change Mask.** This is the mask bit for the corresponding CASRI bit in the E1 National Interrupt Status - R Address Y36. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
3	CALNM (0)	**CRC-4 Alignment 2ms Timer Mask.** This is the mask bit for the corresponding CALNI bit in the E1 National Interrupt Status - R Address Y36. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.

Table 161 - E1 National Interrupt Mask - R/W Address Y46

Bit	Name	Functional Description
2	T2M (0)	**Timer 2 Mask.** This is the mask bit for the corresponding T2I bit in the E1 National Interrupt Status - R Address Y36. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
1	T1M (0)	**Timer 1 Mask.** This is the mask bit for the corresponding T1I bit in the E1 National Interrupt Status - R Address Y36. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.
0	ONESEC M (0)	**One Second Timer Status Mask.** This is the mask bit for the corresponding ONESECI bit in the E1 National Interrupt Status - R Address Y36. If this mask bit is one, the interrupt bit will remain inactive. If this mask bit is zero, the interrupt bit will function normally.

Table 161 - E1 National Interrupt Mask - R/W Address Y46

Bit	Name	Functional Description
15-4	(#### #### ####)	Not Used
3	TA(n) (#)	**Transmit Channel Associated Signaling (CAS) Bit A for Channel 1 to 24.** Address Y50 to Y67 correspond to n=1 to n=24 which correspond to channel 1 to 24 and the corresponding TA bit is transmitted on the DS1 link in bit position 8 of the 6th DS1 frame (within the 12 frame superframe structure for D4 superframes and the 24 frame structure for ESF superframes).
2	TB(n) (#)	**Transmit Channel Associated Signaling (CAS) Bit B for Channel 1 to 24.** Address Y50 to Y67 correspond to n=1 to n=24 which correspond to channel 1 to 24 and the corresponding TB bit is transmitted on the DS1 link in bit position 8 of the 12th DS1 frame (within the 12 frame superframe structure for D4 superframes and the 24 frame structure for ESF superframes).
1	TC(n) (#)	**Transmit Channel Associated Signaling (CAS) Bit C for Channel 1 to 24.** Address Y50 to Y67 correspond to n=1 to n=24 which correspond to channel 1 to 24 and the corresponding TC bit is transmitted on the DS1 link in bit position 8 of the 18th DS1 frame within the 24 frame structure for ESF superframes. These bits are not used in D4 mode.
0	TD(n) (#)	**Transmit Channel Associated Signaling (CAS) Bit D for Channel 1 to 24.** Address Y50 to Y67 correspond to n=1 to n=24 which correspond to channel 1 to 24 and the corresponding TD bit is transmitted on the DS1 link in bit position 8 of the 24th DS1 frame within the 24 frame structure for ESF superframes. These bits are not used in D4 mode.
For CAS operation, the robbed bit enable control register bit RBEN (see Table 86 - T1 Signaling Control - R/W Address Y04) must be set to one. In addition, CAS operation must be enabled on a per channel basis by setting the clear channel per timelsot control register bit CC (see Table 166 - T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7) to zero. Refer to 10.1 T1 CAS.		

Table 162 - T1 Transmit CAS Data Registers - R/W Address Y50-Y67

Bit	Name	Functional Description
15-4	(#### #### ####)	Not Used
3	TA(n) (#)	Transmit Channel Associated Signaling (CAS) Signaling Bits for Channel 1 to 30. Address Y51 to Y5F correspond to n=1 to n=15 which correspond to channel 1 to 15 and the corresponding TA, TB, TC & TD bits are transmitted on the PCM30 link in timeslot 16 in bit positions one to four respectively, in frame n.
2	TB(n) (#)	
1	TC(n) (#)	Address Y61 to Y6F correspond to n=17 to n=31 which correspond to channel 16 to 30 and the corresponding TA, TB, TC & TD bits are transmitted on the PCM30 link in timeslot 16 in bit positions five to eight respectively, in frame n-16.
0	TD(n) (#)	

For CAS operation, the signaling bit enable control register bit CSIG (see Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) must be set to zero. And, timeslot control must be selected with control register bit MPST(n)=1 in E1 Per Timeslot 0 to 31 Control Registers - R/W Address Y90-YAF.
Refer to Section 10.2 E1 CAS.

Table 163 - E1 Transmit CAS Data Registers - R/W Address Y51-Y5F & Y61-Y6F

Bit	Name	Functional Description
15-4	(#### #### ####)	Not Used
3	RA(n) (#)	**Receive Channel Associated Signaling (CAS) Bit A for Channel 1 to 24.** Address Y70 to Y87 correspond to n=1 to n=24 which correspond to channel 1 to 24 and the corresponding RA bit is received from the DS1 link from bit position 8 of the 6th DS1 frame (within the 12 frame superframe structure for D4 superframes and the 24 frame structure for ESF superframes).
2	RB(n) (#)	**Receive Channel Associated Signaling (CAS) Bit B for Channel 1 to 24.** Address Y70 to Y87 correspond to n=1 to n=24 which correspond to channel 1 to 24 and the corresponding RB bit is received from the DS1 link from bit position 8 of the 12th DS1 frame (within the 12 frame superframe structure for D4 superframes and the 24 frame structure for ESF superframes).
1	RC(n) (#)	**Receive Channel Associated Signaling (CAS) Bit C for Channel 1 to 24.** Address Y70 to Y87 correspond to n=1 to n=24 which correspond to channel 1 to 24 and the corresponding RC bit is received from the DS1 link from bit position 8 of the 18th DS1 frame within the 24 frame structure for ESF superframes. These bits are not used in D4 mode.
0	RD(n) (#)	**Receive Channel Associated Signaling (CAS) Bit D for Channel 1 to 24.** Address Y70 to Y87 correspond to n=1 to n=24 which correspond to channel 1 to 24 and the corresponding RD bit is received from the DS1 link from bit position 8 of the 24th DS1 frame within the 24 frame structure for ESF superframes. These bits are not used in D4 mode.

For CAS operation, the robbed bit enable control register bit RBEN (see Table 86 - T1 Signaling Control - R/W Address Y04) must be set to one. In addition, CAS operation must be enabled on a per channel basis by setting the clear channel per timelsot control register bit CC (see Table 166 - T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7) to zero.
Refer to 10.1 T1 CAS.

Table 164 - T1 Receive CAS Data Registers - R Address Y70-Y87

Bit	Name	Functional Description
15-4	(#### #### ####)	Not Used

Table 165 - E1 Receive CAS Data Registers - R Address Y71-Y7F, Y81-Y8F

Bit	Name	Functional Description
3	RA(n) (#)	Receive Channel Associated Signaling (CAS) Signaling Bits for Channel 1 to 30.

Address Y51 to Y5F correspond to n=1 to n=15 which correspond to channel 1 to 15 and the corresponding RA, RB, RC & RD bits are received from the PCM30 link in timeslot 16 in bit positions one to four respectively, in frame n. |
2	RB(n) (#)	
1	RC(n) (#)	Address Y61 to Y6F correspond to n=17 to n=31 which correspond to channel 16 to 30 and the corresponding RA, RB, RC & RD bits are received from the PCM30 link in timeslot 16 in bit positions five to eight respectively, in frame n-16.
0	RD(n) (#)	
For CAS operation, the signaling bit enable control register bit CSIG (see Table 85 - E1 DL, CCS, CAS and Other Control - R/W Address Y03) must be set to zero.
Refer to 10.2 E1 CAS.		

Table 165 - E1 Receive CAS Data Registers - R Address Y71-Y7F, Y81-Y8F

Bit	Name	Functional Description
15-10	(#### ##)	Not Used
9	RPCI(n) (0)	**Receive Per Channel inversion.** If one, the data received from the incoming DS1 channel is inverted before it emerges from the corresponding DSTo channel. If zero, this feature is disabled.
8	MPDR(n) (0)	**Micro Port Data Receive.** If one, the receive idle code data register bits RXIDC7-0 (See Table 96 - T1 Receive Idle Code Data - R/W Address Y09) replace the normal DSTo channel data. If zero, this feature is disabled.
7	MPST(n) (0)	**Micro Port Signaling Transmit.** If one, the transmit CAS bits (A,B,C & D) are sourced from the transmit CAS data register bits TAn, TBn, TCn & TDn (see Table 162 - T1 Transmit CAS Data Registers - R/W Address Y50-Y67) instead of the CSTi channel serial data stream. If zero, this feature is disabled.
6	TPCI(n) (0)	**Transmit Per Channel inversion.** If one, the data sourced from the DSTi channel is inverted before being transmitted onto the DS1 channel. If zero, this feature is disabled.
5	RTSL(n) (0)	**Remote Timeslot Loopback.** If one, the data received on the RTIP/RRNG channel is looped back to the transmit TTIP/TRNG channel. The received channel is also present on DSTo. If zero, this feature is disabled. See Section 15.0 Loopbacks.
4	LTSL(n) (0)	**Local Timeslot Loopback.** If one, the data sourced from the DSTi channel is looped back to the DSTo channel. The transmitted channel is also present on TTIP/TRNG. If zero, this feature is disabled. See Section 15.0 Loopbacks.
3	TTST(n) (0)	**Transmit Test.** If one, the mu-law digital milliwatt (if control bit ADSEQ is one, see Table 80 - T1 Line Coding Control - R/W Address Y01) or a PRBS generator (if control bit ADSEQ is zero) will be transmitted in the corresponding DS1 channel. More than one channel may be activated at once. If zero, this feature is disabled.
2	RRST(n) (0)	**Receive Test.** If one, the mu-law digital milliwatt (if control bit ADSEQ is one, see Table 80 - T1 Line Coding Control - R/W Address Y01) or a PRBS detector (if control bit ADSEQ is zero) will be transmitted in the corresponding DSTo channel. More than one channel may be activated at once. If zero, this feature is disabled.
1	MPDT(n) (0)	**Micro Port Data Transmit.** If one, the transmit idle code data register bits TXIDC7-0 (See Table 98 - T1 Transmit Idle Code Data - R/W Address Y0A) replace the normal DS1 channel data. If zero, this feature is disabled.
0	CC(n) (0)	**Clear Channel.** If one, no robbed bit signaling is inserted in the equivalent transmit DS1 channel. If zero, robbed bit signaling is enabled.
Note: Address Y90-YA7 corresponds to n=1 to n=24 which corresponds to DS1 channel 1 - 24		

Table 166 - T1 Per Channel 1 to 24 Control Registers - R/W Address Y90-YA7

Bit	Name	Functional Description
15-10	(#### ##)	Not Used
9	RPCI(n) (0)	**Receive Per Channel inversion.** If one, the data received from the incoming PCM30 channel is inverted before it emerges from the corresponding DSTo channel. If zero, this feature is disabled.
8	MPDR(n) (0)	**Micro Port Data Receive.** If one, the receive idle code data register bits RXIDC7-0 (See Table 97 - E1 Receive Idle Code Data - R/W Address Y09) replace the normal DSTo channel data. If zero, this feature is disabled.
7	MPST(n) (0)	**Micro Port Signaling Transmit.** If one, the transmit CAS bits (A,B,C,D) are sourced from the transmit CAS data register bits TAn, TBn TCn & TDn (see Table 163 - E1 Transmit CAS Data Registers - R/W Address Y51-Y5F & Y61-Y6F) instead of the CSTi channel serial data stream. If zero, this feature is disabled.
6	TPCI(n) (0)	**Transmit Per Channel inversion.** If one, the data sourced from the DSTi channel is inverted before being transmitted onto the PCM30 channel. If zero, this feature is disabled.
5	RTSL(n) (0)	**Remote Timeslot Loopback.** If one, the data received on the RTIP/RRNG channel is looped back to the transmit TTIP/TRNG channel. The received channel is also present on DSTo. If zero, this feature is disabled. See Section 16.0 Loopbacks.
4	LTSL(n) (0)	**Local Timeslot Loopback.** If one, the data sourced from the DSTi channel is looped back to the DSTo channel. The transmitted channel is also present on TTIP/TRNG. If zero, this feature is disabled. See Section 15.0 Loopbacks.
3	TTST(n) (0)	**Transmit Test.** If one, the a-law digital milliwatt (if control bit ADSEQ is one, see Table 81 - E1 Test, Error and Loopback Control - R/W Address Y01) or a PRBS generator (if control bit ADSEQ is zero) will be transmitted in the corresponding PCM30 channel. More than one channel may be activated at once. If zero, this feature is disabled.
2	RRST(n) (0)	**Receive Test.** If one, the a-law digital milliwatt (if control bit ADSEQ is one, see Table 81 - E1 Test, Error and Loopback Control - R/W Address Y01) or a PRBS detector (if control bit ADSEQ is zero) will be transmitted in the corresponding DSTo channel. More than one channel may be activated at once. If zero, this feature is disabled.
1	MPDT(n) (0)	**Micro Port Data Transmit.** If one, the transmit idle code data register bits TXIDC7-0 (See Table 99 - E1 Transmit Idle Code Data - R/W Address Y0A) replace the normal PCM30 channel data. If zero, this feature is disabled.
0	(#)	Not Used

Note 1: Address Y90-YAF corresponds to n=0 to n=31 which corresponds to PCM30 timeslot 0 to 31.
Note 2: For timeslot 0, address Y90, set all control bits to 0.

Table 167 - E1 Per Timeslot 0 to 31 Control Registers - R/W Address Y90-YAF

Bit	Name	Functional Description
15-8	(#### ####)	Not Used
		Transmit National Bit SanTm (n = 4 to 8, m = 1, 3, 5 etc. to 15). This bit is transmitted on the PCM30 link, in bit position n of Timeslot 0 during Frame m of NFAS frames when CRC-4 multiframe alignment is used, or of consecutive odd frames when CRC-4 multiframe alignment is not used. Bit SanTm is sourced from register address YBn as follows.

Table 168 - E1 Transmit National Bits Sa4 - Sa8 Data Registers - R/W Address YB0-YB4

Bit	Name	Functional Description					
		YB0	YB1	YB2	YB3	YB4	NFAS Frame #
7	SanT1	Sa4T1	Sa5T1	Sa6T1	Sa7T1	Sa8T1	1
6	SanT3	Sa4T3	Sa5T3	Sa6T3	Sa7T3	Sa8T3	3
5	SanT5	Sa4T5	Sa5T5	Sa6T5	Sa7T5	Sa8T5	5
4	SanT7	Sa4T7	Sa5T7	Sa6T7	Sa7T7	Sa8T7	7
3	SanT9	Sa4T9	Sa5T9	Sa6T9	Sa7T9	Sa8T9	9
2	SanT11	Sa4T11	Sa5T11	Sa6T11	Sa7T11	Sa8T11	11
1	SanT13	Sa4T13	Sa5T13	Sa6T13	Sa7T13	Sa8T13	13
0	SanT15	Sa4T15	Sa5T15	Sa6T15	Sa7T15	Sa8T15	15
	(0000 0000)						
There are 5 transmit national bits data registers in total, one 8-bit register for each Sa bit (Sa8-Sa4). Each register contains one byte (8-bits) of data corresponding to eight frames of a particular bit position in timeslot 0. There are 5 registers in total containing 5 bytes of data, occupying addresses YB0 to YB4. Address YB0 corresponds to bit position 4 (Sa4) and address YB4 corresponding to bit position 8 (Sa8).						

Table 168 - E1 Transmit National Bits Sa4 - Sa8 Data Registers - R/W Address YB0-YB4

Bit	Name	Functional Description					
15-8	(#### ####)	Not Used					
		Receive National Bit SanTm (n = 4 to 8, m = 1, 3, 5 etc. to 15). This bit is received from the PCM30 link, in bit position n of Timeslot 0 during Frame m of NFAS frames when CRC-4 multiframe alignment is used, or of consecutive odd frames when CRC-4 multiframe alignment is not used. Bit SanTm is sourced from register address YCn as follows.					
		YC0	YC1	YC2	YC3	YC4	NFAS Frame #
7	SanR1	Sa4R1	Sa5R1	Sa6R1	Sa7R1	Sa8R1	1
6	SanR3	Sa4R3	Sa5R3	Sa6R3	Sa7R3	Sa8R3	3
5	SanR5	Sa4R5	Sa5R5	Sa6R5	Sa7R5	Sa8R5	5
4	SanR7	Sa4R7	Sa5R7	Sa6R7	Sa7R7	Sa8R7	7
3	SanR9	Sa4R9	Sa5R9	Sa6R9	Sa7R9	Sa8R9	9
2	SanR11	Sa4R11	Sa5R11	Sa6R11	Sa7R11	Sa8R11	11
1	SanR13	Sa4R13	Sa5R13	Sa6R13	Sa7R13	Sa8R13	13
0	SanR15	Sa4R15	Sa5R15	Sa6R15	Sa7R15	Sa8R15	15
	(0000 0000)						
There are 5 receive national bits data registers in total, one 8-bit register for each Sa bit (Sa8-Sa4). Each register contains one byte (8-bits) of data corresponding to eight frames of a particular bit position in timeslot 0. There are 5 registers in total containing 5 bytes of data, occupying addresses YC0 to YC4. Address YC0 corresponds to bit position 4 (Sa4) and address YC4 corresponding to bit position 8 (Sa8).						

Table 169 - E1 Receive National Bit Sa4 - Sa8 Data Registers - R Address YC0-YC4

Bit	Name	Functional Description
15	LLOS	**LIU Loss of Signal indication**. In T1 mode, this bit will be high when the received analog AMI signal is less than 40 dB below the nominal value for a period of at least 1 msec. This bit will be low for normal operation. In E1 mode, this bit will be high when the received analog AMI signal is below the threshold selected by the control register bit ELOS described in Table 173 - T1 & E1 LIU Control - R/W Address YE3, for a period of at least 1 ms. This bit will be low for normal operation.

Table 170 - T1 & E1 LIU and JA Status - R Address YE0

Bit	Name	Functional Description
14 13 12 11 10 9 8	PD6 PD5 PD4 PD3 PD2 PD1 PD0	**Peak Detector Voltage Levels.** These five bits indicate the level of the received signal AMI pulses. PD6 PD5 PD4 PD3 PD2 PD1PD0Line Attenuation 0 0 0 0 1 less than 4 dB 1 0 0 0 0 more than 20 dB
7	(#)	Not Used
6	JACS	**Jitter Attenuated Clock Slow**. If one, indicates the dejittered clock period is increased by 1/16 UI (1UI = 1/1.544MHz for T1 and 1UI=1/2.048MHz for E1). If zero, the clock is at normal speed.
5	JACF	**Jitter Attenuated Clock Fast**. If one, indicates the dejittered clock period is decreased by 1/16 UI (1UI = 1/1.544MHz for T1 and 1UI=1/2.048MHz for E1). If zero the clock is at normal speed.
4	JAE	**Jitter Attenuator FIFO Empty**. If one, indicates the JA FIFO is empty.
3	JAF4	**Jitter Attenuator FIFO with 4 Full Locations**. If one, indicates the JA FIFO has at least 4 full locations (i.e. if 0, almost empty).
2	JAFC	**Jitter Attenuator Center Full.** If one, indicates the JA FIFO is at least half full.
1	JAE4	**Jitter Attenuator FIFO with 4 Empty Locations**. If one, indicates the JA FIFO has at most 4 empty locations (i.e. if 1, almost full).
0	JAF	**Jitter Attenuator FIFO Full**. If one, indicates the JA FIFO is full.

Table 170 - T1 & E1 LIU and JA Status - R Address YE0

Bit	Name	Functional Description
15 14 13 12 11 10 9 8	APD7 APD6 APD5 APD4 APD3 APD2 APD1 APD0 (0000 0000)	**Receive Analog Peak Detector Signal Strength.** This status register gives the output value of an 8 bit A/D converter connected to a peak detector on RTIP/RRING.
7 6 5 4 3 2 1 0	EPD7 EPD6 EPD5 EPD4 EPD3 EPD2 EPD1 EPD0 (0000 0000)	**Receive Analog Equalized Peak Detector Signal Strength.** This status register gives the output value of an 8 bit A/D converter connected to a peak detector on RTIP/RRING with an equalizer.

Table 171 - T1 & E1 LIU Receive Peak Detector Status - R Address YE1

Bit	Name	Functional Description
15	RSV (0)	**Reserved.** Must be 0 for normal operation

Table 172 - T1 & E1 LIU Transmitter Control - R/W Address YE2

Bit	Name	Functional Description
14	$\overline{\text{PDLY}}$ (0)	**Pulse Delay.** For T1 mode only. If zero, the transmitted mark (pulse) is stretched. Set to zero for normal operation where the T1 template needs to be met.
13	TXEN (0)	**LIU Transmitter Enable.** If zero, the TTIP and TRING output line drivers are disabled. If one, they are enabled.
12	TXPA (0)	**LIU Transmitter T1 & E1 Pulse Amplitude.** If zero, the pulse amplitude is set for T1 mode. If one, the pulse amplitude is set for E1 mode.
11	CPL (0)	**Custom Pulse Level Enable.** If one, the values in two control registers (see Table 174 - T1 & E1 LIU Transmit Pulse Phase 1 & Phase 2 Data - R/W Address YE4 and Table 175 - T1 & E1 LIU Transmit Pulse Phase 3 & Phase 4 Data - R/W Address YE5) are used for generating the transmit pulse shape. If zero, the internal ROM values are used.
10 9 8	TXL2 TXL1 TXL0 (000)	**T1 Mode Transmit Line Build Out Select.** Setting these bits shapes a correct transmit pulse according to expected line length. TXL2 TXL1 TXL0 Line Build Out RT(Ω) 0 0 0 0 to 133 feet/ 0 dB 0 0 0 1 133 to 266 feet 0 0 1 0 266 to 399 feet 0 0 1 1 399 to 533 feet 0 1 0 0 533 to 655 feet 0 1 0 1 -7.5 dB 0 1 1 0 -15 dB 0 1 1 1 -22.5 dB 0 Set TXPA=0, the transformer ratio is 1:2.42, and the series transmitter resistor (RT) is 0Ω.
		E1 Mode Transmit Line Pulse Amplitude. Setting these bits shapes a correct transmit pulse according to expected line impedance. TXL2 TXL1 TXL0 Line Z(Ω) RT(Ω) 0 0 0 120 0 1 1 0 75 6.04 All other combinations are reserved. Set TXPA=1, the transformer ratio is 1:2.42, and the series transmitter resistor (RT) is as indicated.
7	JAS (0)	**Jitter Attenuator Select.** If one, the Jitter Attenuator is enabled. If zero, it is disabled.
4	JFC (0)	**Jitter Attenuator FIFO Centre.** When this bit is toggled the read pointer on the jitter attenuator shall be centered. During this centering the jitter on the JA outputs is increased by 1/16 UI (1UI=1/2.048MHz for E1).
5 4 3	JFD2 JFD1 JFD0 (000)	**Jitter Attenuator FIFO Depth Control Bits.** These bits determine the depth of the jitter attenuator FIFO. JFD2 JFD1 JFD0 Depth 0 0 0 16 0 0 1 32 0 1 0 48 0 1 1 64 1 0 0 80 1 0 1 96 1 1 0 112 1 1 1 128
2	JACL (0)	**Jitter Attenuator FIFO Clear Bit.** If one, the Jitter Attenuator, its FIFO and status are reset. The status registers will identify the FIFO as being empty. However, the actual bit values of the data in the JA FIFO will not be reset.
1 0	OPTCOR1 OPTCOR2 (00)	For factory test purpose. Set to zero for normal operation.

Table 172 - T1 & E1 LIU Transmitter Control - R/W Address YE2

Bit	Name	Functional Description
15	RSV (0)	**Reserved.** Set to zero for normal operation.
14 13	RSV (00)	**Reserved**. Must be 00 for normal operation.
12	RSV (0)	**Reserved.** Must be 0 for normal operation.
11	RSV (0)	**Reserved.** Must be 0 for normal operation.
10	RSV (0)	**Reserved.** Must be 0 for normal operation.
9	RLBK (0)	**Remote Loopback**. If one, RTIP/RRNG are connected to TTIP/TRNG at the PCM30 side of the selected framer (Y). If zero, this feature is disabled. See Section 15.0 Loopbacks.
8	MLBK (0)	**Metallic Loopback**. If one, DSTi is connected to DSTo at the PCM30 side of the selected framer (Y). If zero, this feature is disabled. See Section 15.0 Loopbacks.
7	RSV (0)	**Reserved.** Set to zero for normal operation.
6	RSV (0)	**Reserved.** Set to zero for normal operation.
5	ELOS (0)	**E1 LLOS Threshold Criteria.** For E1 mode only. This bit sets the criteria for the LIU loss of signal status register bit LLOS described in Table 170 T1 & E1 LIU and JA Status - R Address YE0. If one, the analog loss of signal threshold to is set to 20dB below nominal. If zero, the analog loss of signal threshold is set to 40 dB below nominal.
4 3	REQC1 REQC0 (00)	**Receive Equalizer Control**. Setting these bits selects the equalization type applied to the incoming line data. REQC1 REQC0 Receive Equalization 0 0 Manual Equalization with control register bits REQM2-0 of this register 0 1 Automatic Equalization with Algorithm 1 - recommended default 1 0 Automatic Equalization with Algorithm 2 - for test purposes 1 1 Automatic Equalization with Algorithm 3 - with control bits detailed in Table 176 - T1 & E1 LIU Receive Equalizer Threshold Control - R/W Address YE6, typically set to HEX BB30.
2 1 0	REQM2 REQM1 REQM0 (000)	**Receive Equalization Manual**.Setting these pins forces a manual level of equalization of the incoming line data. REQM2 REQM1 REQM0 Receive Equalization 0 0 0 none 0 0 1 8 dB 0 1 0 16 dB 0 1 1 24 dB 1 0 0 32 dB 1 0 1 40 dB 1 1 0 48 dB 1 1 1 reserved These settings only have effect if control register bits REQC1,0 (this register) are set to 00.

Table 173 - T1 & E1 LIU Control - R/W Address YE3

Bit	Name	Functional Description
15	RSV (0)	**Reserved.** Must be kept at zero for normal operation.

Table 174 - T1 & E1 LIU Transmit Pulse Phase 1 & Phase 2 Data - R/W Address YE4

Bit	Name	Functional Description
14 13 12 11 10 9 8	C1P6 C1P5 C1P4 C1P3 C1P2 C1P1 C1P0 (0000 000)	**Custom Transmit Pulse Phase 1.** These bits provide the capability for programming the magnitude setting for the LIU line driver A/D converter during the first phase of a four phase mark. The greater the binary number loaded into the register, the greater the amplitude driven out. This feature is enabled with control bit CPL described in Table 172 - T1 & E1 LIU Transmitter Control - R/W Address YE2.
7	RSV (0)	**Reserved.** Must be kept at zero for normal operation.
6 5 4 3 2 1 0	C2P6 C2P5 C2P4 C2P3 C2P2 C2P1 C2P0 (0000 000)	**Custom Transmit Pulse Phase 2.** These bits provide the capability for programming the magnitude setting for the LIU line driver A/D converter during the second phase of a four phase mark. The greater the binary number loaded into the register, the greater the amplitude driven out. This feature is enabled with control bit CPL described in Table 172 - T1 & E1 LIU Transmitter Control - R/W Address YE2.

Table 174 - T1 & E1 LIU Transmit Pulse Phase 1 & Phase 2 Data - R/W Address YE4

Bit	Name	Functional Description
15	RSV (0)	**Reserved.** Must be kept at zero for normal operation.
14 13 12 11 10 9 8	C3P6 C3P5 C3P4 C3P3 C3P2 C3P1 C3P0 (0000 000)	**Custom Transmit Pulse Phase 3.** These bits provide the capability for programming the magnitude setting for the LIU line driver A/D converter during the third phase of a four phase mark. The greater the binary number loaded into the register, the greater the amplitude driven out. This feature is enabled with control bit CPL described in Table 172 - T1 & E1 LIU Transmitter Control - R/W Address YE2.
7	RSV (0)	**Reserved.** Must be kept at zero for normal operation.
6 5 4 3 2 1 0	C4P6 C4P5 C4P4 C4P3 C4P2 C4P1 C4P0 (0000 000)	**Custom Transmit Pulse Phase 4.** These bits provide the capability for programming the magnitude setting for the LIU line driver A/D converter during the fourth phase of a four phase mark. The greater the binary number loaded into the register, the greater the amplitude driven out. This feature is enabled with control bit CPL described in Table 172 - T1 & E1 LIU Transmitter Control - R/W Address YE2.

Table 175 - T1 & E1 LIU Transmit Pulse Phase 3 & Phase 4 Data - R/W Address YE5

Bit	Name	Functional Description
15 14 13 12 11 10 9 8	EHT7 EHT6 EHT5 EHT4 EHT3 EHT2 EHT1 EHT0 (0000 0000)	**Receive Equalizer High Threshold.** These bits set the highest possible binary count tolerable coming out of the equalized signal peak detector before a lower level of equalization is selected. This register is only used when A/D based automatic equalization is selected (see Table 173 - T1 & E1 LIU Control - R/W Address YE3).
7 6 5 4 3 2 1 0	ELT7 ELT6 ELT5 ELT4 ELT3 ELT2 ELT1 ELT0 (0000 0000)	**Receiver Equalization Low Threshold.** These bits set the lowest possible binary count tolerable coming out of the equalized signal peak detector before a higher level of equalization is selected. This register is only used when A/D based automatic equalization is selected (see Table 173 - T1 & E1 LIU Control - R/W Address YE3).

Table 176 - T1 & E1 LIU Receive Equalizer Threshold Control - R/W Address YE6

Bit	Name	Functional Description
15- 10	(#### ##)	Not Used
9 8	RXLDCL1 RXLDCL0 (01)	**Receive Loop Deactivate Code Length.** Setting these bits determines the length of the transmit loop down code as detailed in the table below: RXLDCL1 RXLDCL0 Receive Loop Deactivate Code Length 0 0 Code length is 5 bits. 0 1 Code length is 6 or 3 bits. 1 0 Code length is 7 bits. 1 1 Code length is 8 or 4 bits.
7 6 5 4 3 2 1 0	RXLDCM7 RXLDCM6 RXLDCM5 RXLDCM4 RXLDCM3 RXLDCM2 RXLDCM1 RXLDCM0 (0000 1001)	**Receive Loop Deactivate Code Match.** This byte specifies the match code for the receive loopback deactivate code. The contents of this register are compared to the received data, and an a maskable interrupt LLDDI (see Table 151 - T1 Receive Line and Timer Interrupt Status - R Address Y35) is generated if the contents match.

Table 177 - T1 Receive Loop Deactivate Code Match - R/W Address YF0

Bit	Name	Functional Description
15-8	(#### ####)	Not Used
10	TX8KE (0)	**Transmit 8 KHz Enable.** This is normally set to zero but may be used in conjunction with the auxiliary signals, see Section 3.6 Auxiliary Output SIgnals. If one, the pin $\overline{RxMF}$ (AUX pin, see Section 3.6 Auxiliary Output SIgnals) transmits a positive 8 KHz frame pulse synchronous with the serial data stream transmit on TTIP/TRNG. If zero, the pin $\overline{RxMF}$ transmits a negative frame pulse synchronous with the multiframe boundary of data coming out of DSTo.

Table 178 - T1 Interrupt and I/O Control - R/W Address YF1

Bit	Name	Functional Description
9	$\overline{\text{RXDO}}$ (0)	**Receive DSTo All Ones.** If one, the DSTo pin operates normally. If zero, all timeslots (0-31) of DSTo are set to one.
8	TXMFE (0)	**Transmit Multiframe Enable.** If one, the $\overline{\text{TxMF}}$ pin will be enabled. If zero, the $\overline{\text{TxMF}}$ pin will be disabled. See the $\overline{\text{TxMF}}$ pin description.
7	$\overline{\text{SPND}}$ (0)	**Suspend Interrupts.** If zero, the selected tranceivers contribution to the $\overline{\text{IRQ}}$ pin output will be a high impedance state, but all interrupt and latched status registers will continue to be updated. If one, the selected tranceivers contribution to the $\overline{\text{IRQ}}$ output will be normal operation.
6	$\overline{\text{INTA}}$ (0)	**Interrupt Acknowledge.** If zero, all interrupt and latched status registers are cleared and consequently, the selected tranceivers contribution to the $\overline{\text{IRQ}}$ pin output will be a high impedance state. If one, all interrupt and latched status registers operate normally, and the selected tranceivers contribution to the $\overline{\text{IRQ}}$ output will be normal operation.
5	DSTOE (0)	**Output DSTo Enable.** If one, the DSTo pin operates normally. If zero, DSTo will be at high impedance.
4	CSTOE (0)	**CSTo Enable.** If one, the CSTo pin operates normally. If zero, CSTo will be at high impedance.
3	$\overline{\text{RXCO}}$ (0)	**Receive CSTO All Ones.**If one, the CSTo pin operates normally. If zero, all timeslots of CSTo are set to one
2	CNCLR (0)	**Counter Clear.** When this bit is changed from zero to one, status counters are cleared. If zero, all status counters operate normally.
5	ACCLR (0)	**Automatic Counter Clear.** When this bit is set to one, all latchable status counters are cleared automatically by the one second timer bit ONESEC (Table 106 - T1 Timer Status - R Address Y11) immediately following the counter latch operation. If zero, all latchable status counters operate normally.
0	RST (0)	**Reset**. When this bit is changed from zero to one, the selected framer (Y) will reset to its default mode. See Section 7.6 Reset Operation (RESET, TRST Pins).

Table 178 - T1 Interrupt and I/O Control - R/W Address YF1

Bit	Name	Functional Description
15-11	(#### #)	Not Used
10	ADREC (0)	**Address Recognition Enable.**When high, address recognition is enabled. This forces the receiver to recognize only those packets having the unique address as programmed in the T1 & E1 HDLC Address Recognition Control - R/W Address YF4, or if the address is an all call address providing control bit A2EN of the same register is set high. When ADREC is low, all received packets are stored in the Receive FIFO.
9	RXEN (0)	**Receiver Enable.** When high, the HDLC receiver will be immediately enabled. When low, the HDLC receiver is disabled. If a packet is received when this bit goes low, the receiver will disable after the packet is finished.
8	TXEN (0)	**Transmitter Enable.**When high, the transmitter will be immediately enabled and will begin transmitting data, if any, or go to a mark idle or interframe time fill state. When low, the HDLC transmitter is disabled. If a packet is transmitted when this bit goes low, the transmitter will disable after the packet is finished.
7	EOP (0)	**End of Packet.** When high, the next byte written to the Transmit FIFO is aborted and an EOP byte is sent to the transmitter instead, and following this byte, an FCS is transmitted. This facilitates loading of multiple packets into the Transmit FIFO. This bit is reset automatically after a write to the Transmit FIFO. See Section 12.0 HDLC.
6	FA (0)	**Frame Abort**. When high, the next byte written to the Transmit FIFO is tagged. After the write, the FA bit is cleared. When the tagged byte reaches the bottom of the FIFO, an abort sequence is sent instead of the tagged byte, see Section 12.1.4 Frame Abort.

Table 179 - T1 & E1 HDLC Control 0 - R/W Address YF2

Bit	Name	Functional Description
5	MRKID (0)	**Mark-Idle.** When high, the transmitter will be in an interframe time fill state. When low, the transmitter will be in an idle state.These two states will only occur when the Transmit FIFO is empty. See Section 12.1.5 Interframe Time Fill and Link Channel States.
4	CYCLE (0)	**Cycle.** When high, the T1 & E1 HDLC Transmit Packet Size - R/W Address YF6 will continuously cycle through a count up sequence.
3	TCRCI (0)	**Transmit CRC Inhibit.** When high, this bit will inhibit transmission of the CRC. That is, the transmitter will not insert the computed CRC onto the bit stream after seeing the EOP tag byte. This is used in V.120 terminal adaptation for synchronous protocol sensitive UI frames.
2	SEVEN (0)	**Seven.** When high, this bit will enable seven bits of address recognition in the first received address byte. The received address byte must have bit 0 equal to 1 which indicates a single address byte is being received. See Table 181 T1 & E1 HDLC Address Recognition Control - R/W Address YF4.
1	RXFRST (0)	**Receive FIFO Reset.**When high, the Receive FIFO will be reset. This causes the receiver to be disabled until the next reception of a flag. The status register will identify the FIFO as being empty. However, the actual bit values in the Receive FIFO will not be reset.
0	TXFRST (0)	**Transmit FIFO Reset.** When high, the Transmit FIFO will be reset. The Status Register will identify the FIFO as being empty. This bit will be reset when data is written to the Transmit FIFO. However, the actual bit values of data in the Transmit FIFO will not be reset. It is cleared by the next write to the Transmit FIFO.

Table 179 - T1 & E1 HDLC Control 0 - R/W Address YF2

Bit	Name	Functional Description
15-6	(#### #### ##)	Not Used
5	HRST (0)	**HDLC Reset.** When this bit is set to one, the HDLC will be reset. This bit can only be reset by writing a zero to this location or applying soft or hard reset.
4	RTLOOP (0)	**Receive to Transmit Loopback.** When this bit is high, receive to transmit HDLC loopback will be activated. Receive data, including end of packet indication, but not including flags or CRC, will be written to the Transmit FIFO as well as the Receive FIFO. When the transmitter is enabled, this data will be transmitted as though written by the microprocessor. Both good and bad packets will be looped back. Receive to transmit loopback may also be accomplished by reading the Receive FIFO using the microprocessor and writing these bytes, with appropriate tags, into the Transmit FIFO.
3	CRCTST (0)	**CRC Remainder Test.** When high, direct access to the T1 & E1 HDLC Receive CRC Data - R/W Address Y1E through the serial interface is enabled. After testing is enabled, serial data is clocked in until the data aligns with the internal comparison (16 RXCLK clock cycles) and then the clock is stopped. The expected pattern is F0B8 hex. Each bit of the CRC can be corrupted to allow more efficient testing.
2	FTST (0)	**FIFO Test.** This bit allows the writing to the Receive FIFO and reading of the Transmit FIFO through the microprocessor to allow more efficient testing of the FIFO status/interrupt functionality. This is done by making a Transmit FIFO write become a Receive FIFO write and a Receive FIFO read become a Transmit FIFO read. In addition, EOP/FA and RQ8/RQ9 are re-defined to be accessible (i.e. Receive write causes EOP/FA to go to Receive fifo input; Transmit read looks at output of Transmit fifo through RQ8/RQ9 bits).
1	ADTST (0)	**Address Recognition Test.** This bit allows direct access to the Address Recognition Registers in the receiver through the serial interface to allow more efficient testing. After address testing is enabled, serial data is clocked in until the data aligns with the internal address comparison (16 RXc clock cycles) and then clock is stopped.
0	HLOOP (0)	**TR Loopback.** When high, transmit to receive HDLC loopback will be activated. The packetized transmit data will be looped back to the receive input. RXEN and TXEN bits must also be enabled.

Table 180 - T1 & E1 HDLC Control 1 - R/W Address YF3

Bit	Name	Functional Description
15 14 13 12 11 10 9	ADR26 ADR25 ADR24 ADR23 ADR22 ADR21 ADR20	**HDLC Second Address 6-0 Comparison.** A seven bit address used for comparison with the second byte of the HDLC received address. Control bits A2EN of this register and control bit ADREC of the T1 & E1 HDLC Control 0 - R/W Address YF2 must be both set high for this address to take effect. ADR26 is the MSB.
8	A2EN	**HDLC Second Address Comparison Enable.** When high, the above HDLC Second Receive Address is used in the comparison of the HDLC received second address byte. Control bit ADREC of the T1 & E1 HDLC Control 0 - R/W Address YF2 must also be set high for this address to take effect. For a 13 or 14 bit all call address (hex 1FFF or 3FF) to take effect, both A1EN and A2EN must be set.
7 6 5 4 3 2 1	ADR16 ADR15 ADR14 ADR13 ADR12 ADR11 ADR10	**HDLC First Address 6-0 Comparison.** A seven bit address used for comparison with the first byte of the HDLC received address. Control bits A1EN of this register and control bit ADREC of the T1 & E1 HDLC Control 0 - R/W Address YF2 must be both set high for this address to take effect. Six bit address recognition is used when ADR10 is disabled by clearing control bit SEVEN of the above register. ADR16 is the MSB.
0	A1EN	**HDLC First Address Comparison Enable.** When high, the above HDLC First Receive Address is used in the comparison of the HDLC received first address byte. Control bit ADREC of the T1 & E1 HDLC Control 0 - R/W Address YF2 must also be set high for this address to take effect. For a 6 or 7 bit all call address (hex 3F or 7F) to take effect, only A1EN must be set.

Table 181 - T1 & E1 HDLC Address Recognition Control - R/W Address YF4

Bit	Name	Functional Description
15-8	(#### ####)	Not Used
7 6 5 4 3 2 1 0	TXF7 TXF6 TXF5 TXF4 TXF3 TXF2 TXF1 TXF0	**HDLC Transmit FIFO Data.** This byte is tagged with the two status bits EOP and FA from T1 & E1 HDLC Control 1 - R/W Address YF3, and the resulting 10 bit word is sent to the Transmit FIFO. The Transmit FIFO status is not changed immediately when a transmitter read or processor write occurs. It is updated after the data has settled and the transfer to the last available position has finished.

Table 182 - T1 & E1 HDLC Transmit FIFO Data - R/W Address YF5

Bit	Name	Functional Description
15-8	(#### ####)	Not Used
7 6 5 4 3 2 1 0	TPS7 TPS6 TPS5 TPS4 TPS3 TPS2 TPS1 TPS0	**Transmit Packet Size.** An eight bit register which must be loaded with the length of the packet about to be transmitted through the Transmit FIFO (T1 & E1 HDLC Transmit FIFO Data - R/W Address YF5). This value is also the start value for the counter detailed in Table 127 - T1 & E1 HDLC Test and Transmit Byte Status - R/W Address Y1C.

Table 183 - T1 & E1 HDLC Transmit Packet Size - R/W Address YF6

Bit	Name	Functional Description
15-8	(#### ####)	Not Used
7 6 5 4 3 2 1 0	TXSD7 TXSD6 TXSD5 TXSD4 TXSD3 TXSD2 TXSD1 TXSD0 (0000 0000)	**Transmit Set Delay Bits 7 - 0.** Writing to this register forces a one time setting of the delay through the transmit elastic buffer. The delay is defined as the time interval between the write of the transmit ST-BUS channel containing DS1 timeslot 1 and its subsequent read. The delay is modified by moving the position of the internally generated DS1 frame boundary. The delay (when set) will always be less than 1 frame (125 uS).

Table 184 - T1 Transmit Elastic Buffer Set Delay - R/W Address YF7

22.0 MT9071 and Network Specifications

This section compares the MT9071 with North American AT&T TR62411 specifications and European ETSI TBR 4 and ITU-T I.431 specifications. The specifications which are applicable to the clock recovery circuit including intrinsic jitter, jitter tolerance and jitter transfer are considered.

22.1 T1 Intrinsic Jitter

The MT9071 meets the AT&T TR62411 intrinsic jitter requirements for T1 (1.544MHz) frequency inputs as shown in Figure 16 - AT&T Jitter Tolerance.

Jitter Tolerance

Filter	AT&T Requirement Maximum allowed (UIpp)	MT9071 Maximum at TTIP & TRNG pins (UIpp)
10Hz-8kHz	0.020	0.005
10Hz-40kHz	0.025	0.010
8kHz-40kHz	0.025	0.010
None	0.050	0.030

Table 185 - AT&T Intrinsic Jitter

22.2 T1 Jitter Tolerance

The MT9071 meets the AT&T TR62411 jitter tolerance requirements for T1 (1.544MHz) frequency inputs as shown in Figure 16 - AT&T Jitter Tolerance.
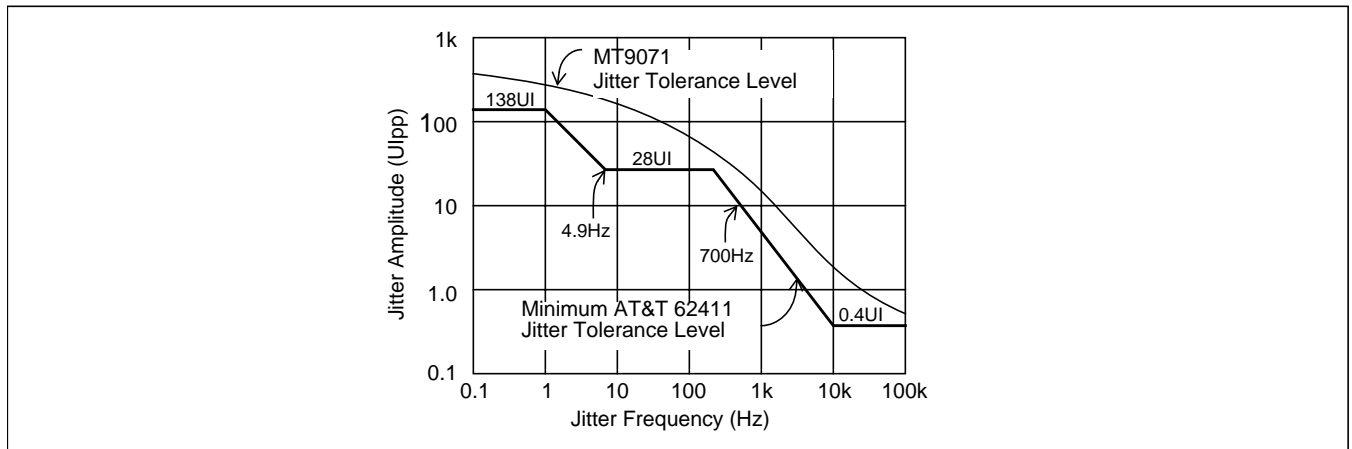
Figure 16 - AT&T Jitter Tolerance

22.3 Jitter Transfer

The MT9071 meets the AT&T TR62411 jitter transfer requirements for T1 (1.544MHz) frequency inputs as shown in Figure 17 - AT&T Jitter Transfer.
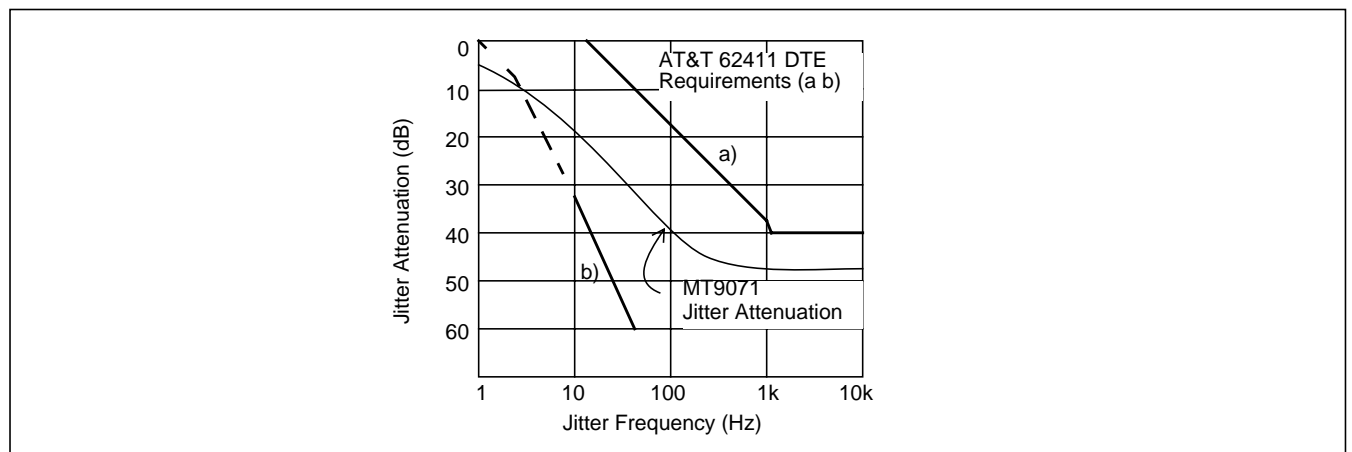
Figure 17 - AT&T Jitter Transfer

22.4 E1 Intrinsic Jitter

The MT9071 meets the ETSI TBR 4 filtered jitter transfer requirements for E1 (2.048MHz) frequency inputs thereby meeting the intrinsic jitter requirements. Note that unlike the AT&T requirement, which specifies an acceptable intrinsic jitter range, ETSI specifies a maximum allowable output jitter level, after passing through a bandpass filter for a given input signal level. See Figure 19 - ETSI Jitter Transfer.

22.5 E1 Jitter Tolerance

The MT9071 meets the ETSI TBR 4 jitter tolerance requirements for E1 (2.048MHz) frequency inputs as shown in Figure 18 - ETSI Jitter Tolerance.
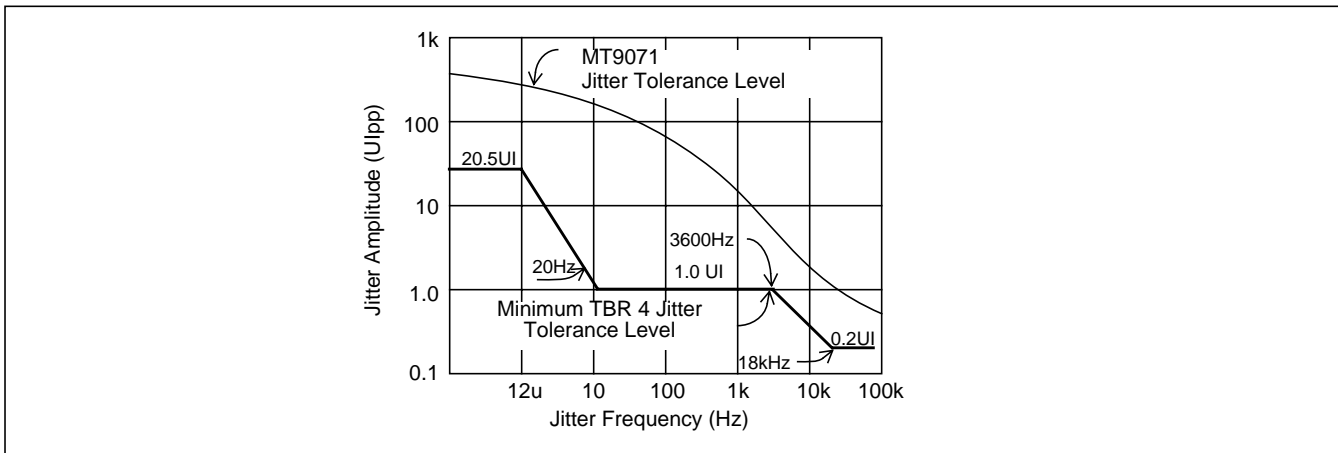
Figure 18 - ETSI Jitter Tolerance

22.6 E1 Jitter Transfer

The MT9071 meets all four of the TBR 4 filtered jitter transfer requirements for E1 (2.048MHz) frequency inputs, including the multiple access requirement. See Figure 19 - ETSI Jitter Transfer. Note that unlike the AT&T requirement, which specifies an acceptable jitter attenuation range, ETSI specifies a maximum allowable output jitter level, after passing through a bandpass filter for a given input signal level. Although ETSI specifies four different jitter transfer test conditions, the multiple access with 40Hz to 100kHz filter test condition is the most difficult to meet.
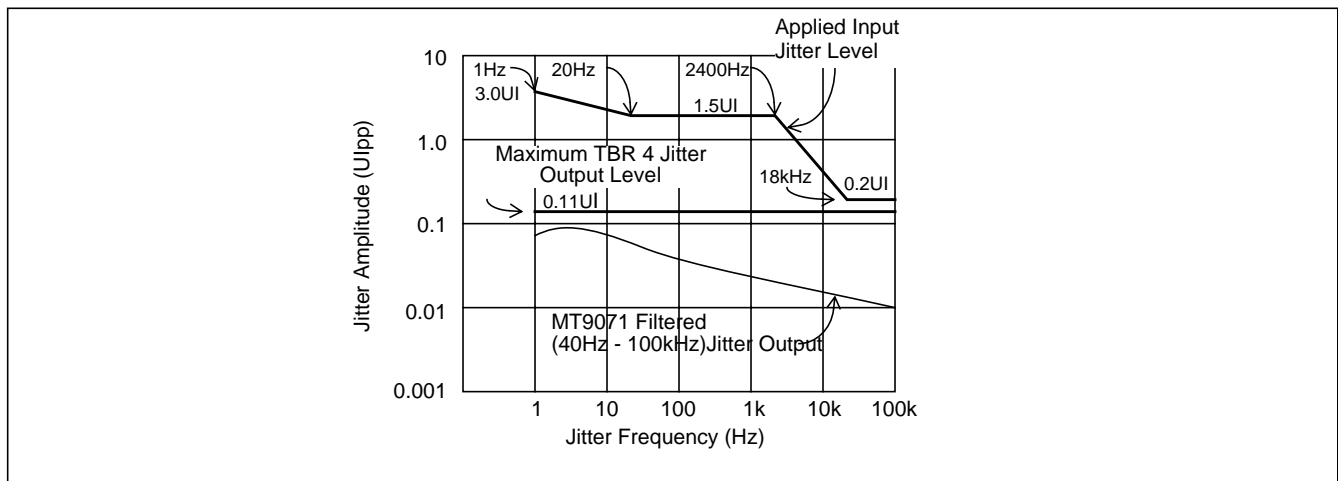
Figure 19 - ETSI Jitter Transfer

The MT9071 also meets the ITU-T I.431 jitter transfer requirements for E1 (2.048MHz) frequency inputs. See Figure 20 - ITU-T Jitter Transfer.
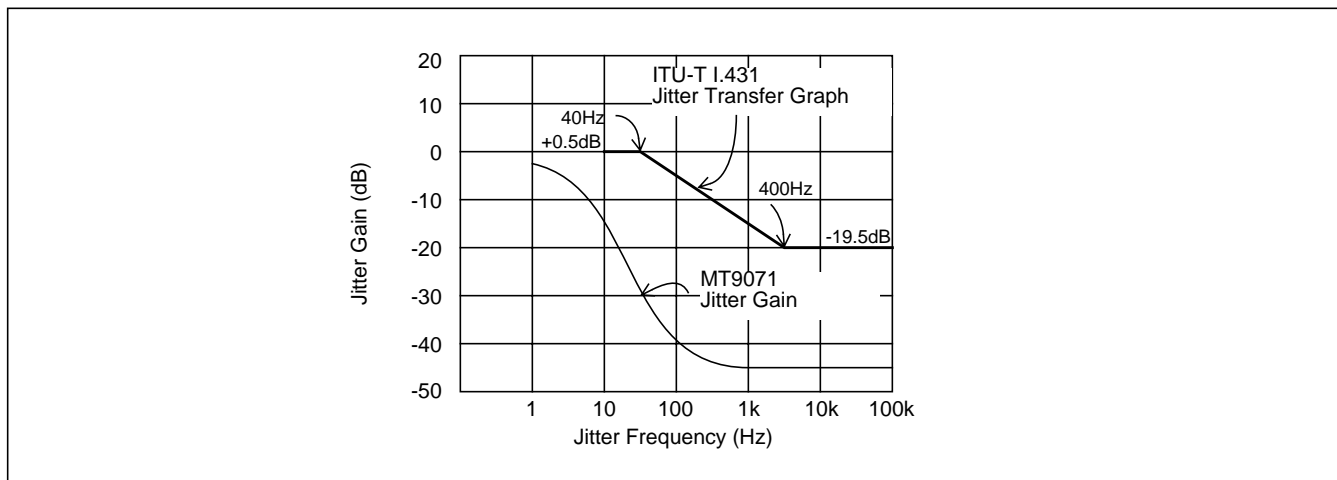
Figure 20 - ITU-T Jitter Transfer

23.0 Applications

This section contains MT9071 application specific details for clock and crystal operation, guard time usage, reset operation, power supply decoupling, Manual Control operation and Automatic Control operation.

23.1 Master Clock

The MT9071 can use either a clock or crystal as the master timing source.

In Freerun Mode, the frequency tolerance at the clock outputs is identical to the frequency tolerance of the source at the OSCi pin. For applications not requiring an accurate Freerun Mode, tolerance of the master timing source may be 100ppm. For applications requiring an accurate Freerun Mode, such as AT&T TR62411, the tolerance of the master timing source must Be no greater than 32ppm.

Another consideration in determining the accuracy of the master timing source is the desired capture range. The sum of the accuracy of the master timing source and the capture range of the MT9071 will always equal 230ppm. For example, if the master timing source is 100ppm, then the capture range will be 130ppm.

23.1.1 Clock Oscillator

When selecting a Clock Oscillator, numerous parameters must be considered. This includes absolute frequency, frequency change over temperature, output rise and fall times, output levels and duty cycle. See AC Electrical Characteristics in Section 24.0 AC and DC Electrical Characteristics.
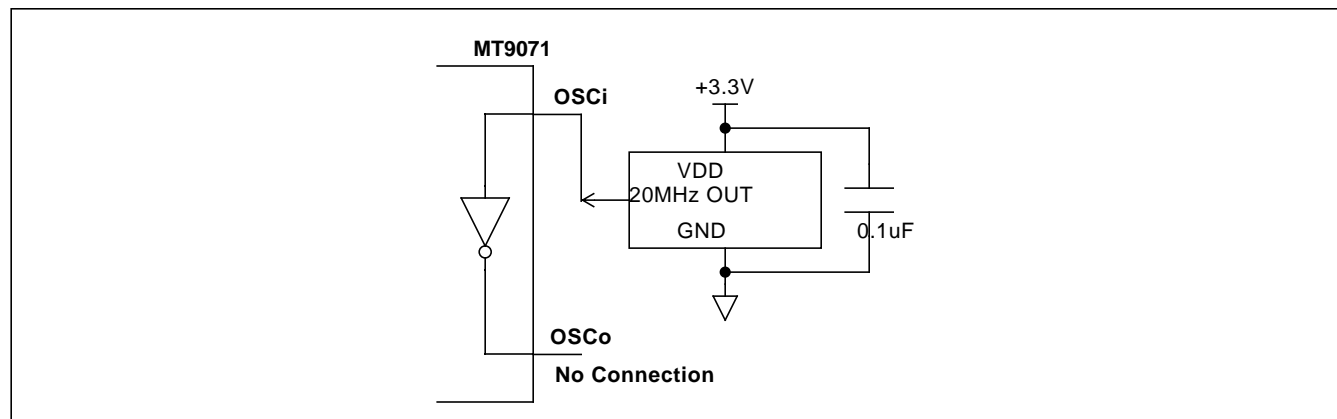
Figure 21 - Clock Oscillator Circuit

For applications requiring 32ppm clock accuracy, the following clock oscillator module may be used.

CTS CB3-LV-5C-20.00

Voltage:	3.3V
Frequency:	20MHz
Tolerance:	25ppm 0C to 70C
Rise & Fall Time:	10ns (10% 90% 50pF)
Duty Cycle:	45% to 55%

The output clock should be connected directly (not AC coupled) to the OSCi input of the MT9071, and the OSCo output should be left open as shown in Figure 21 - Clock Oscillator Circuit.

23.1.2 Crystal Oscillator

Alternatively, a Crystal Oscillator may be used. A complete oscillator circuit made up of a crystal, resistor and capacitors is shown in Figure 22 - Crystal Oscillator Circuit.
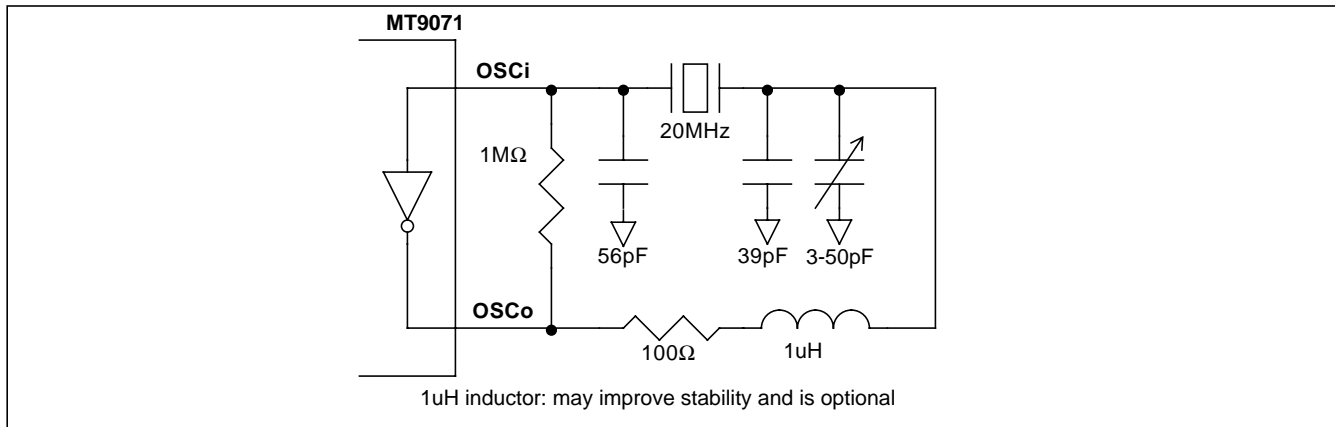
Figure 22 - Crystal Oscillator Circuit

The accuracy of a crystal oscillator depends on the crystal tolerance as well as the load capacitance tolerance. Typically, for a 20MHz crystal specified with a 32pF load capacitance, each 1pF change in load capacitance contributes approximately 9ppm to the frequency deviation. Consequently, capacitor tolerances, and stray capacitances have a major effect on the accuracy of the oscillator frequency.

The trimmer capacitor shown in Figure 22 - Crystal Oscillator Circuit may be used to compensate for capacitive effects. If accuracy is not a concern, then the trimmer may be removed, the 39pF capacitor may be increased to 56pF, and a wider tolerance crystal may be substituted.

The crystal should be a fundamental mode type - not an overtone. The fundamental mode crystal permits a simpler oscillator circuit with no additional filter components and is less likely to generate spurious responses. The crystal specification is as follows.

Frequency:	20MHz
Tolerance:	As required
Oscillation Mode:	Fundamental
Resonance Mode:	Parallel
Load Capacitance:	32pF
Maximum Series Resistance:	35Ω
Approximate Drive Level:	1mW

e.g., CTS R1027-2BB-20.0MHZ

(20ppm absolute, 6ppm 0C to 50C, 32pF, 25W)

23.2 4 Trunk T1, E1 or J1 Cross-Connect with LDX and Synchronous Backplane

A quadruple network termination switching application with the MT9071 is shown in Figure 23. Any four of a kind links (T1, E1 or J1) may be interfaced to any other four of a kind links. The MT9071 provides the line interface and the framing while the digital switch routes the signals through the synchronous 2Mb/s backplane.
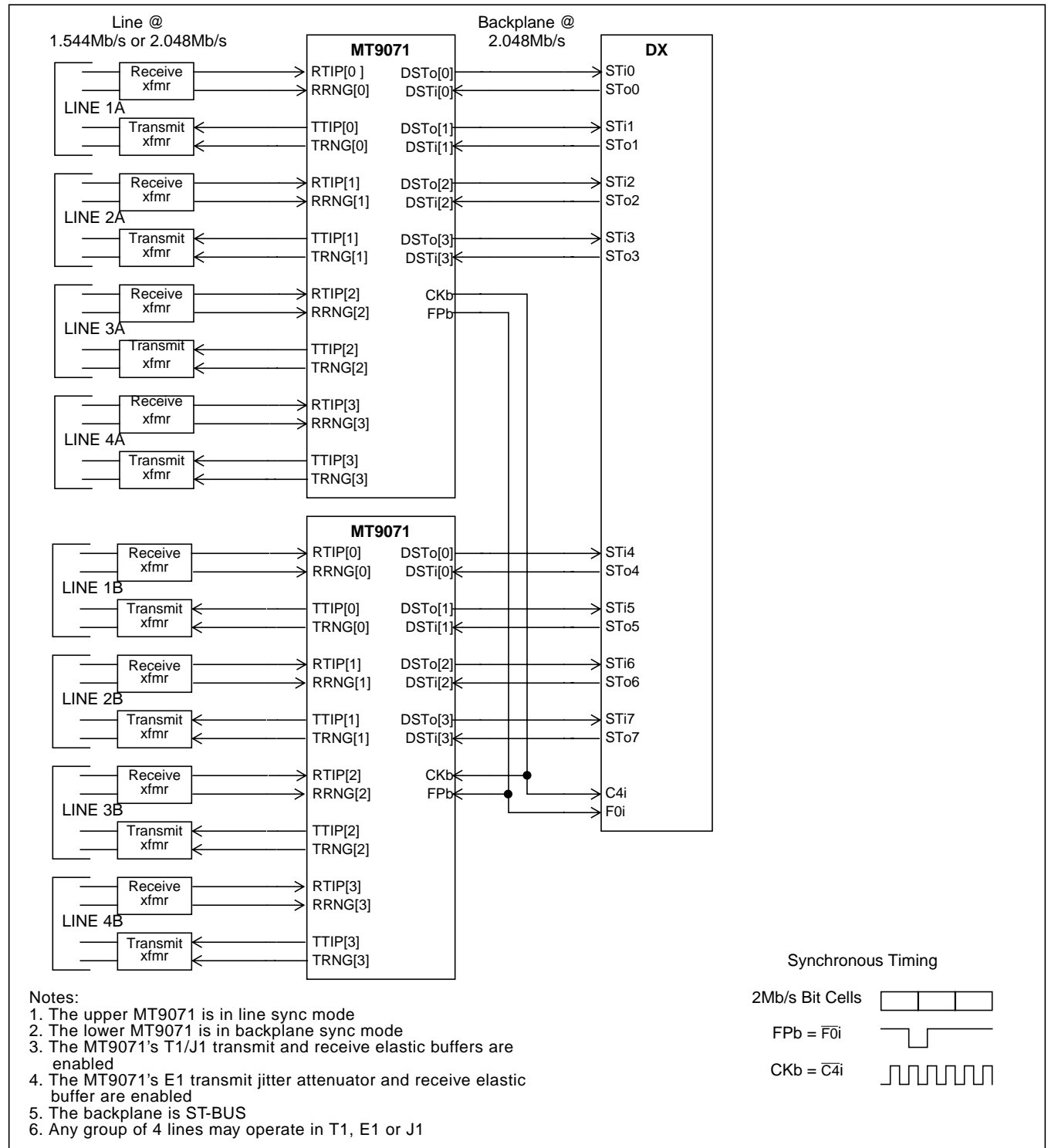
Figure 23 - 4 Trunk T1, E1 or J1 Cross-Connect with MT90820 LDX and Synchronous Backplane

Notes:
1. The upper MT9071 is in line sync mode
2. The lower MT9071 is in backplane sync mode
3. The MT9071's T1/J1 transmit and receive elastic buffers are enabled
4. The MT9071's E1 transmit jitter attenuator and receive elastic buffer are enabled
5. The backplane is ST-BUS
6. Any group of 4 lines may operate in T1, E1 or J1

23.3 8 Trunk T1, E1 or J1 Interface with LDX, Remote Timing, Internal PLL and Synchronous Backplane

An octal network termination switching application with the MT9071 is shown in Figure 24 - 8 Trunk T1, E1 or J1 Interface with MT90820 LDX, Remote Timing, Internal PLL and Synchronous Backplane. Any four of a kind links (T1, E1 or J1) may be used. The MT9071 provides the line interface and the framing while the digital switch routes the signals through the synchronous 2Mb/s backplane.
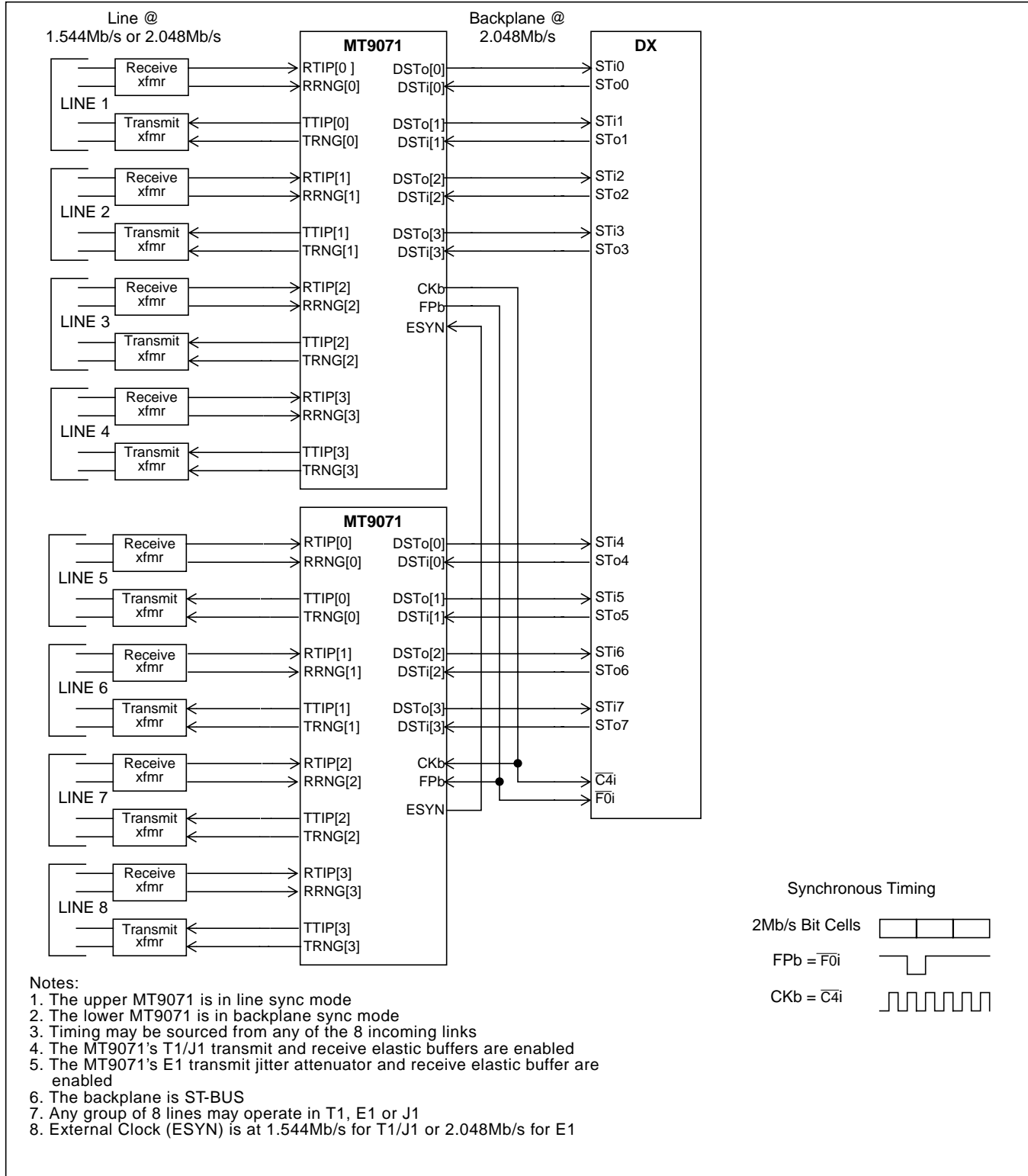
Figure 24 - 8 Trunk T1, E1 or J1 Interface with MT90820 LDX, Remote Timing, Internal PLL and Synchronous Backplane

23.4 8 T1, E1 or J1 Links with MT90220 Octal IMA/UNI and Synchronous Backplane

An ATM application with the MT9071 is shown in Figure 25 - 8 T1, E1 or J1 Links with MT90220 Octal IMA/UNI and Synchronous Backplane. Any four of a kind links (T1, E1 or J1) may be used. The MT9071 provides the line interface, framing and backplane timing while the MT90220 routes the signals to the ATM bus.
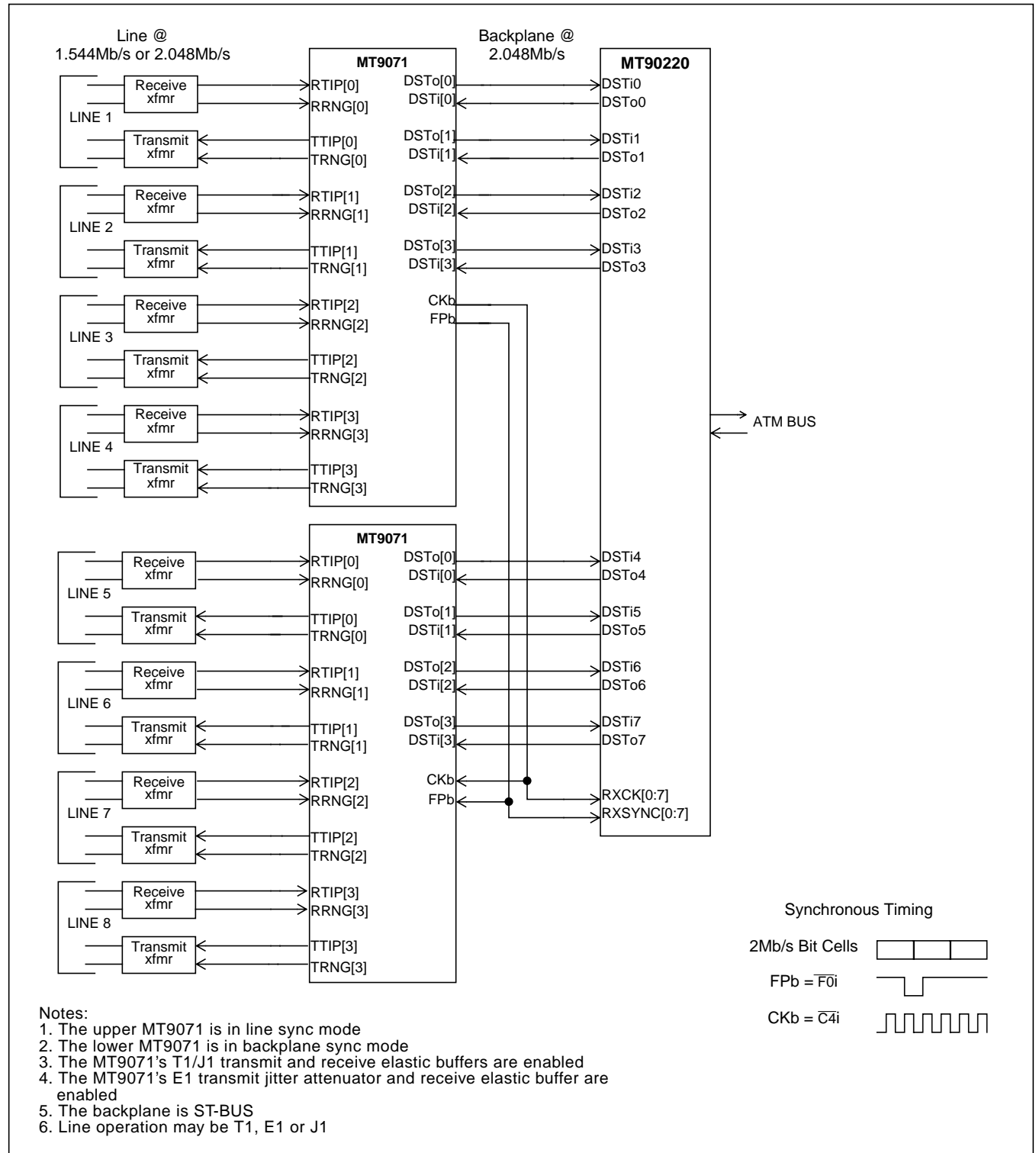
Figure 25 - 8 T1, E1 or J1 Links with MT90220 Octal IMA/UNI and Synchronous Backplane

23.5 4 T1,E1 or J1 Links with Synchronous Common Channel Signaling

A multichannel HDLC application with the MT9071 is shown in Figure 26 - 4 T1/E1/J1 Links with Synchronous Common Channel Signaling. Any four of a kind links (T1, E1 or J1) may be used. The MT9071 provides the line interface and the framing. In E1 mode, the framer routes PCM30 channels 15, 16 and 31 of each transceiver to any selected 12 TDM channels. In T1/J1 mode, the framer routes any DS0 channel of each transceiver to any selected 4 TDM channels.The HDLC formats the transmit and receive signaling data from the selected TDM channels.

Notes:
1. The MT9071 is in line sync mode
2. The MT9071's T1/J1 transmit and receive elastic buffers are enabled
3. The MT9071's E1 transmit jitter attenuator and receive elastic buffer are enabled
4. The backplane is ST-BUS
5. The HDLC is Siemens PEB20320 (32 Channel) or similar
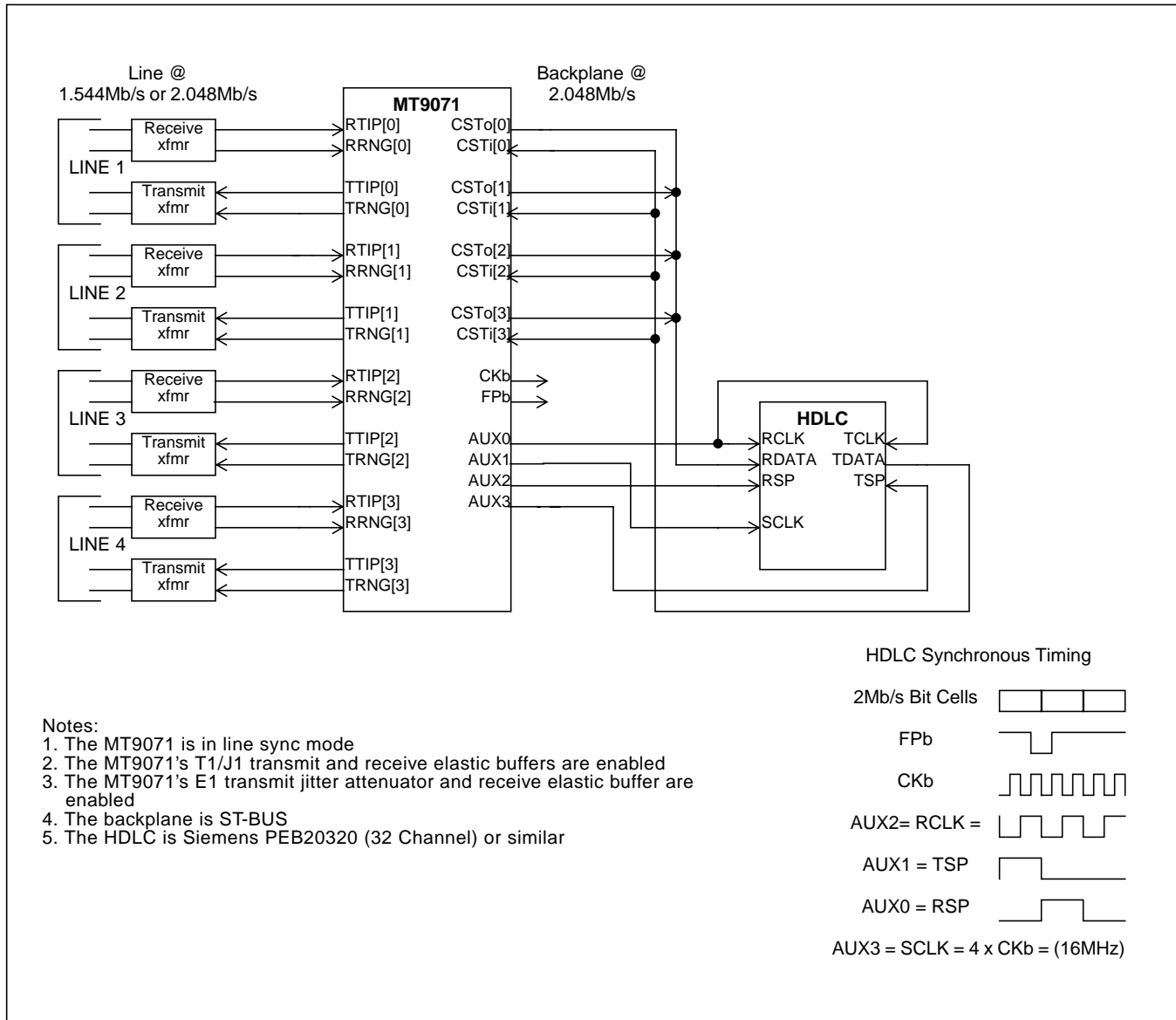
Figure 26 - 4 T1/E1/J1 Links with Synchronous Common Channel Signaling

23.6 8 Trunk T1, E1 or J1 Interface with LDX, CCS and 8.192Mb/s Synchronous Backplane

A typical high speed application is shown in Figure 27 - 8 Trunk T1, E1 or J1 Interface with MT90820 LDX, CCS and 8.192Mb/s Synchronous Backplane. Any four of a kind links (T1, E1 or J1) may be used. The MT9071 provides the line interface and the framing. In E1 mode, the framer routes PCM30 channels 15, 16 and 31 of each transceiver to any selected 24 TDM channels. In T1/J1 mode, the framer routes any DS0 channel of each transceiver to any selected 8 TDM channels.The HDLC formats the transmit and receive signaling data from the selected TDM channels. Also included is the payload transmit and receive data on a synchronous 8Mb/s backplane. The LDX switches the payload data.
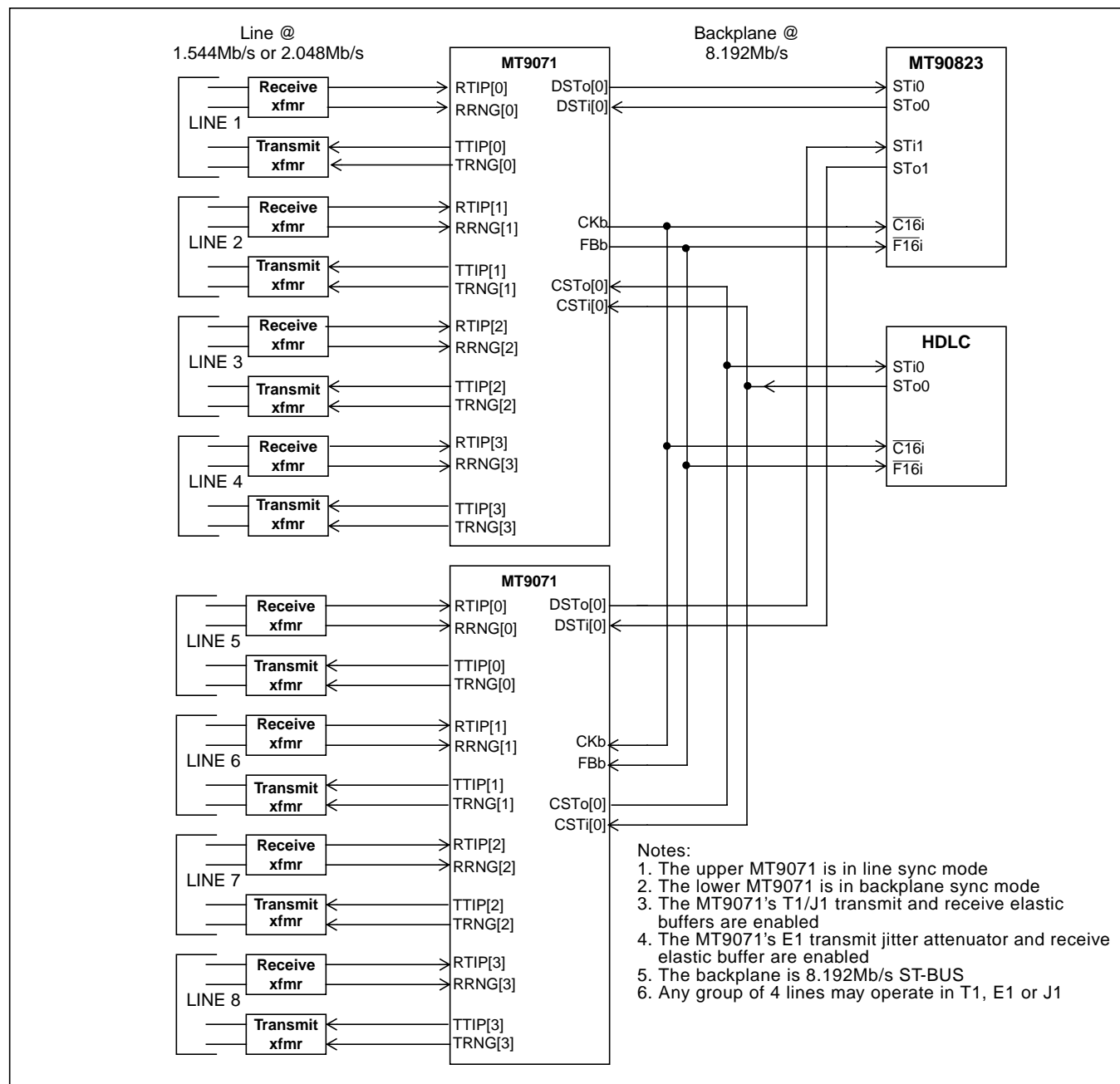
Figure 27 - 8 Trunk T1, E1 or J1 Interface with MT90820 LDX, CCS and 8.192Mb/s Synchronous Backplane

23.7 Interfacing the 3.3V MT9071 with 5V Logic Levels

A level translation application is shown in Figure 28 - Interfacing the 3.3V MT9071 with 5V Logic Levels. Note that all peripherals shown (DX, HDLC and Microprocessor) may operate at either 5V or 3.3V.
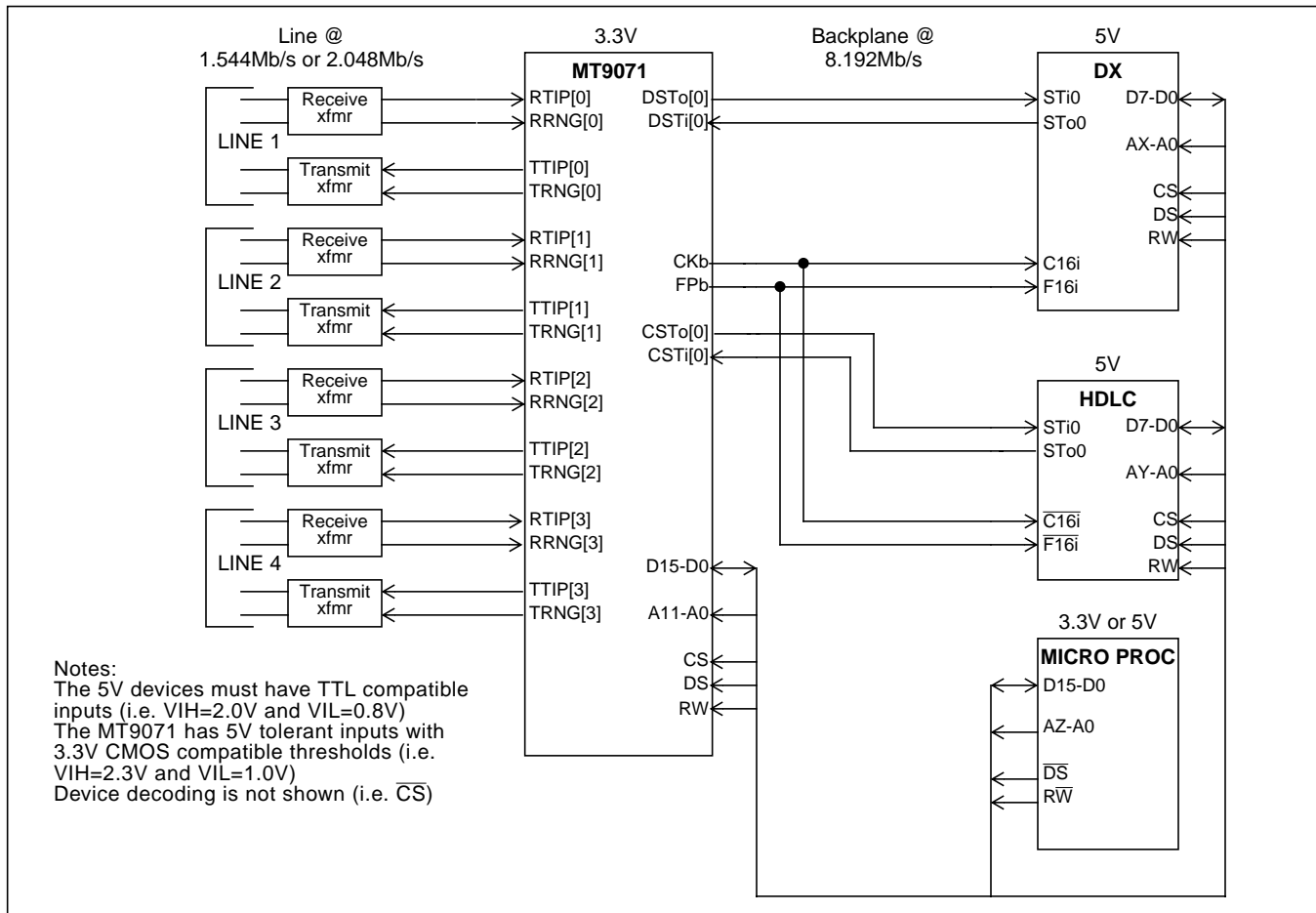
Figure 28 - Interfacing the 3.3V MT9071 with 5V Logic Levels

23.8 T1 & E1 Analog Line Interface

A 100/120 ohm T1/ E1 line driver application circuit is shown in Figure 29 - 100 ohm T1 & 120 ohm E1 Analog Line Interface; and a 75 ohm E1 line driver application is shown in Figure 30 - 75 ohm E1 Analog Line Interface.

The receiver equalization and impedance; and the transmitter pulse and amplitude are set through software control. Refer to the control bits in the following registers.

Table 173 T1 & E1 LIU Control - R/W Address YE3.
Table 174 T1 & E1 LIU Transmit Pulse Phase 1 & Phase 2 Data - R/W Address YE4.
Table 175 T1 & E1 LIU Transmit Pulse Phase 3 & Phase 4 Data - R/W Address YE5.
Table 176 T1 & E1 LIU Receive Equalizer Threshold Control - R/W Address YE6.

Notes:

1.   Protection circuitry (i.e. voltage clamps, line fuses, common mode choke etc.) depends on the
     application and is not shown. For a reference design, refer to the evaluation board schematic.
2.   The transformer shown is a Pulse Engineering T1137.
3.   For #1 mode the Rx impedance is 82.5* 1.21* 1.21 = 120 ohm.
4.   For T1 mode the Rx impedance is 68.1* 1.21* 1.21 = 100 ohm.

Figure 29 - 100 ohm T1 & 120 ohm E1 Analog Line Interface

Notes:

1.   Protection circuitry (i.e. voltage clamps, line fuses, common mode choke etc.) depends on the
     application and is not shown. For a reference design, refer to the evaluation board schematic.
2.   The transformer shown is a Pulse Engineering T1137.
3.   The Rx impedance is 51.1*1.21*1.21 = 75.0 ohm.
4.   The Tx impedance is Rout + 2*6.04*2.42*2.42 = Rout + 70.7 ohm =~75 ohms.

Figure 30 - 75 ohm E1 Analog Line Interface

Time (Nanoseconds)	-499	-149	-149	-97	0	97	149	149	298	395	603	752
Time U.I.	-.77	-.23	-.23	-.15	0	.15	.23	.23	.46	.61	.93	1.16
Normalized Amplitude	-.05	-.05	.5	.9	.95	.9	.5	-.45	-.45	-.26	-.05	-.05

Table 186 - Minimum Curve for Figure 31 - T1 Pulse Template (T1.403)

Time (Nanoseconds)	-499	-253	-175	-175	-78	0	175	220	499	752	---	---
Time U.I.	-.77	-.39	-.27	-.27	-.12	0	.27	.34	.77	1.16	---	---
Normalized Amplitude	.05	.05	.8	1.2	1.2	1.05	1.05	-.05	.05	.05	---	---

Table 187 - Maximum Curve for Figure 31 - T1 Pulse Template (T1.403)
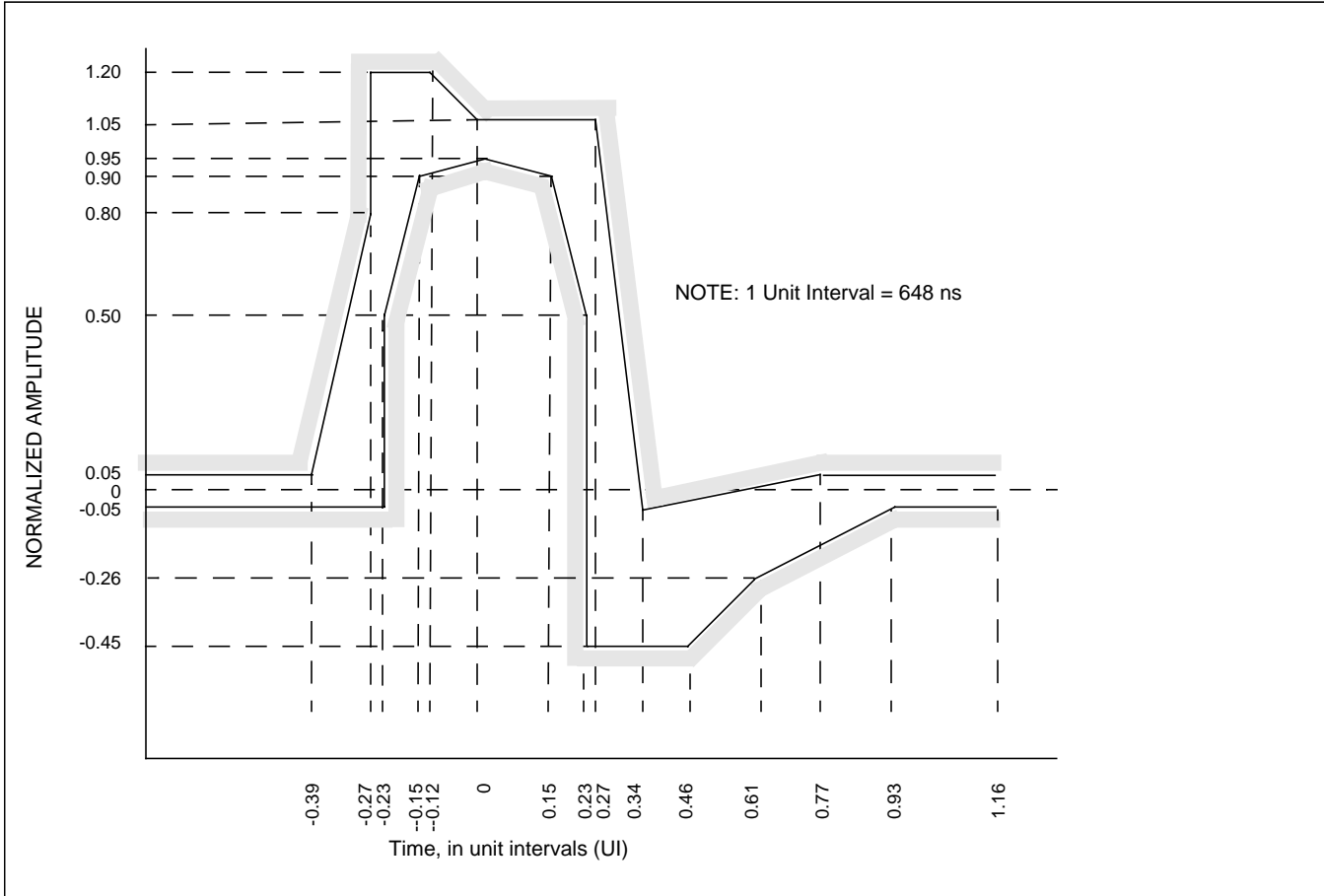
Figure 31 - T1 Pulse Template (T1.403)
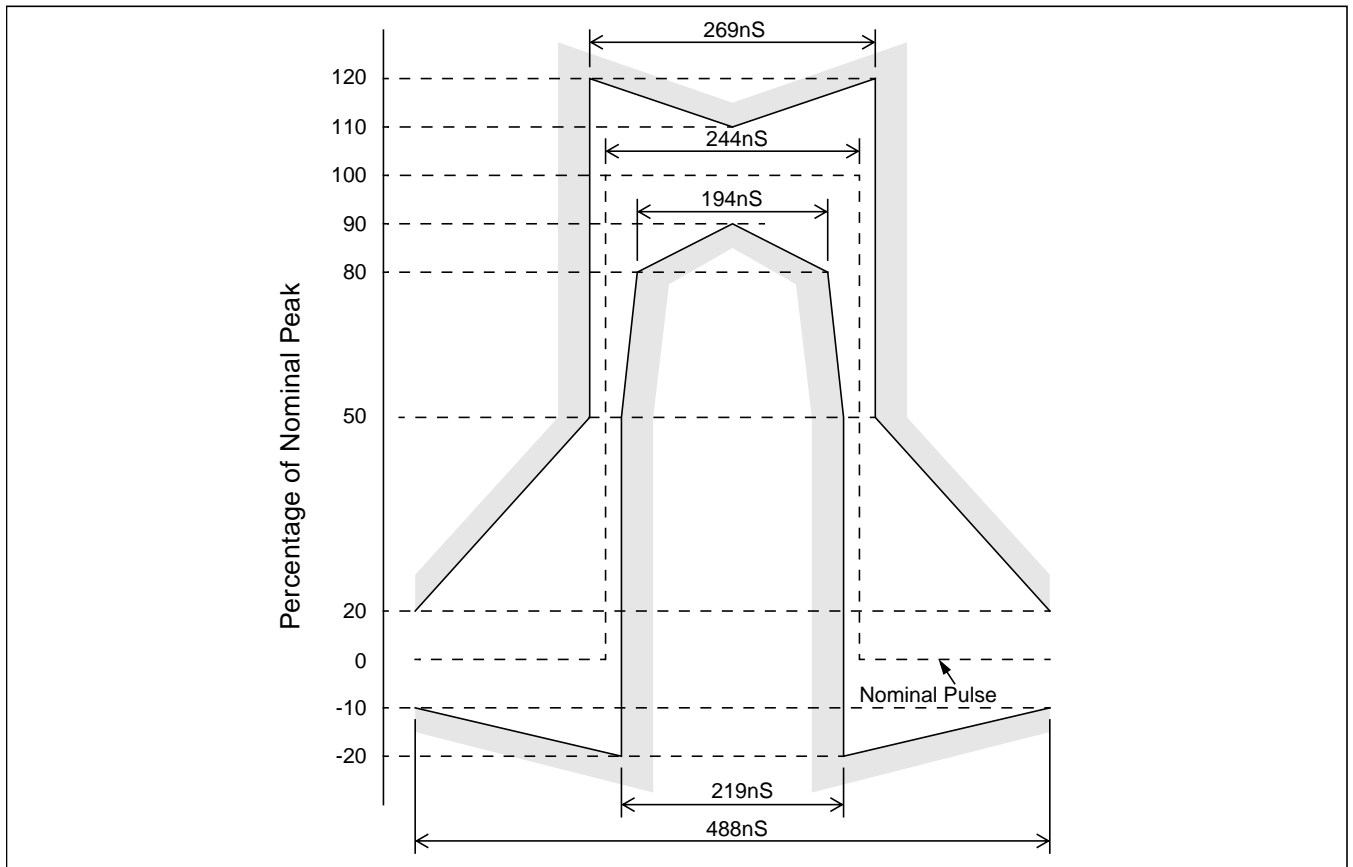
Figure 32 - E1 Pulse Template (G.703)

23.9 256 Pin LBGA to 128 Pin LQFP Mapping and 4 Layer PCB Layout

A printed circuit board layout mapping application is shown in Figure 33 - 256 Pin LBGA Package with PCB Routing Top View.

Notes:
1. LBGA is a 256 Pin LBGA 1.00mm Pitch 17mm X 17mm Package and 16 X 16 Matrix and 15mm X 15mm footprint.
2. Name below circle indicates BGA ball name.
3. 3 layers of routing are shown, 1 layer for signals and 2 layers for power.
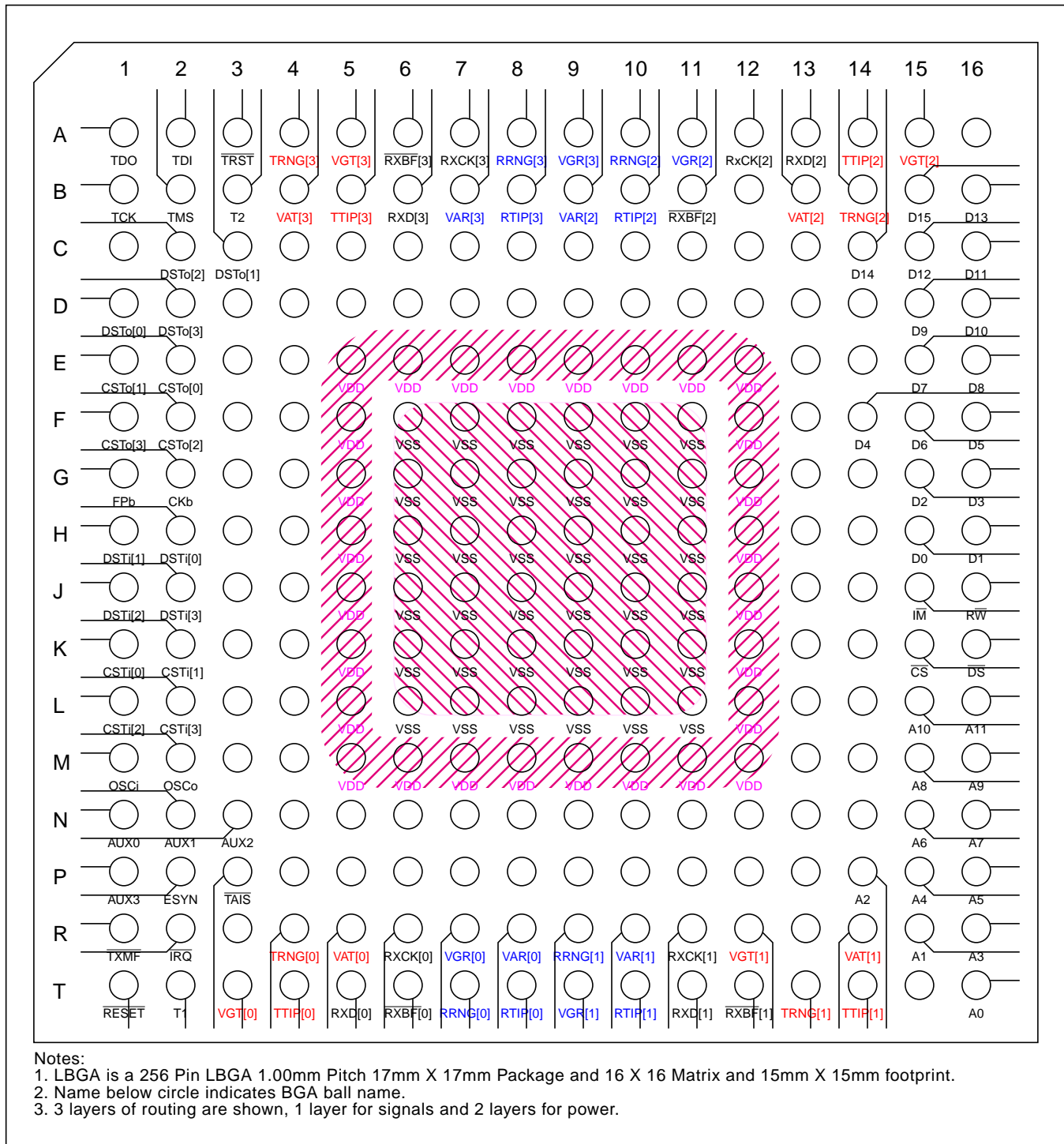
Figure 33 - 256 Pin LBGA Package with PCB Routing Top View

24.0 AC and DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
	Supply Voltage	V_{DD}	-0.5	5.0	V
	Voltage on any 5V Tolerant Input/Output	V_{IO5}	-0.5	5.5	V
	Voltage on any Non 5V Tolerant Input/Output (TDI, TDO, TMS, TCK, $\overline{TRST}$, T2, OSCi & OSCo)	V_{IO}	-0.5	V_{DD} + 0.5	V
	Current on any Input/Output	I_O		30	mA
	Storage Temperature	T_{ST}	-55	150	˚C

* Voltages are with respect to ground (VSS) unless otherwise stated.
* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions*

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
	Operating Temperature	T_{OP}	-40	25	85	˚C	
	Supply Voltage	V_{DD}	3.0	3.3	3.6	V	

* Voltages are with respect to ground (VSS) unless otherwise stated.

DC Electrical Characteristics *

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
	Input Leakage (Digital Inputs with no pullup's or pulldown's)	I_{IL}		1	10	µA	V_I = 0 to V_{DD}
	Input Leakage (Digital Inputs with pullup's or pulldown's)	I_{IL}			100	µA	V_I = 0 to V_{DD}
	High Impedance Leakage (Digital I/O)	I_{OZ}		1	10	µA	V_O = 0 to V_{DD}
	Supply Current	I_{DD}		250		mA	Outputs unloaded. Transmitting an all 1's signal.
	Input High Voltage (Digital Inputs)	V_{IH}	$0.7V_{DD}$			V	
	Input Low Voltage (Digital Inputs)	V_{IL}			$0.3V_{DD}$	V	
	Output High Voltage (Digital Outputs)	V_{OH}	$0.8V_{DD}$			V	I_{OH}=8 mA
	Output Low Voltage (Digital Outputs)	V_{OL}			0.4	V	I_{OL}=8 mA
	Pin Capacitance (Digital Inputs & Outputs)	C_P		8		pF	

* Voltages are with respect to ground (VSS) unless otherwise stated.
* Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
*Typical figures are at 25˚C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels*

	Characteristics	Sym	Level	Units	Conditions/Notes
	Threshold Voltage	V_T	1.5	V	TTL
			$0.5*V_{DD}$	V	CMOS
	Rise/Fall Threshold Voltage High	V_{HM}	2.0	V	TTL
			$0.7*V_{DD}$	V	CMOS
	Rise/Fall Threshold Voltage Low	V_{LM}	0.8	V	TTL
			$0.3*V_{DD}$	V	CMOS

* Voltages are with respect to ground (VSS) unless otherwise stated.
* Timing for output signals is based on the worst case result of the combination of TTL and CMOS thresholds.
* See Figure 34 - Timing Parameter Measurement Voltage Levels.
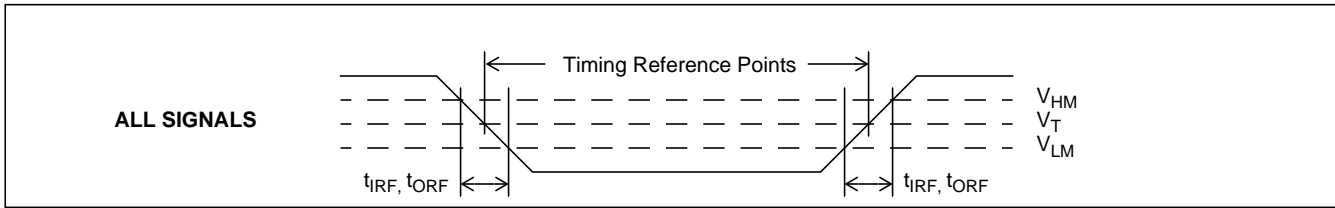
Figure 34 - Timing Parameter Measurement Voltage Levels

AC Electrical Characteristics - Output Rise and Fall Times*

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
	Output Rise/Fall Time	t_{ORF}		5		ns	C_L=150pF, R_L=1kΩ

*Typical figures are at 25˚C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics - Motorola Microprocessor Timing*

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	$\overline{DS}$ low	t_{DSL}	130			ns	
2	$\overline{DS}$ High	t_{DSH}	30			ns	
3	R/$\overline{W}$ Setup	t_{RWS}	0			ns	
4	R/$\overline{W}$ Hold	t_{RWH}	0			ns	
5	Address Setup	t_{ADS}	0			ns	
6	Address Hold	t_{ADH}	30			ns	
7	Data Setup Write	t_{DSW}	10			ns	
8	Data Hold Write	t_{DHW}	25			ns	
9	Data Delay Read	t_{DDR}			100	ns	C_L=150pF, R_L=1kΩ
10	Data Hold Read	t_{DHR}	0			ns	C_L=150pF, R_L=1kΩ
11	Data Active to High Z Delay	t_{DAZ}			20	ns	C_L=150pF, R_L=1kΩ
12	$\overline{CS}$ Setup	t_{CSS}	0			ns	
13	$\overline{CS}$ Hold	t_{CSH}	0			ns	
14	Cycle Time	t_{CYC}	160			ns	

*Typical figures are at 25˚C and are for design aid only: not guaranteed and not subject to production testing.
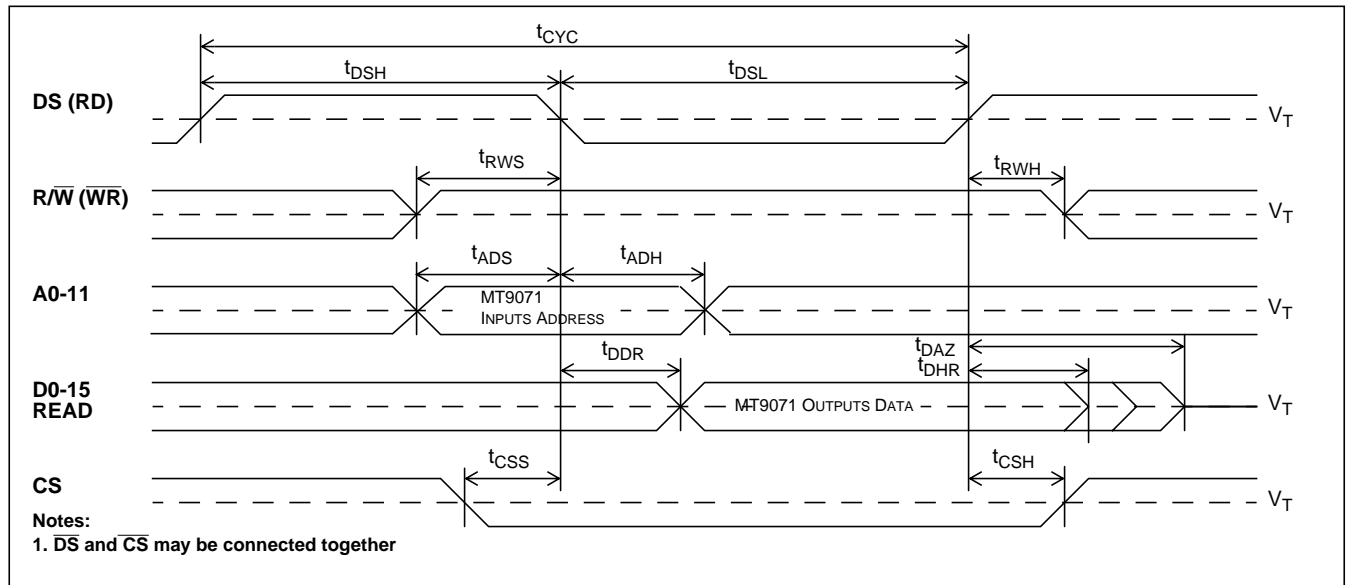
Figure 35 - Motorola Microprocessor Read Timing
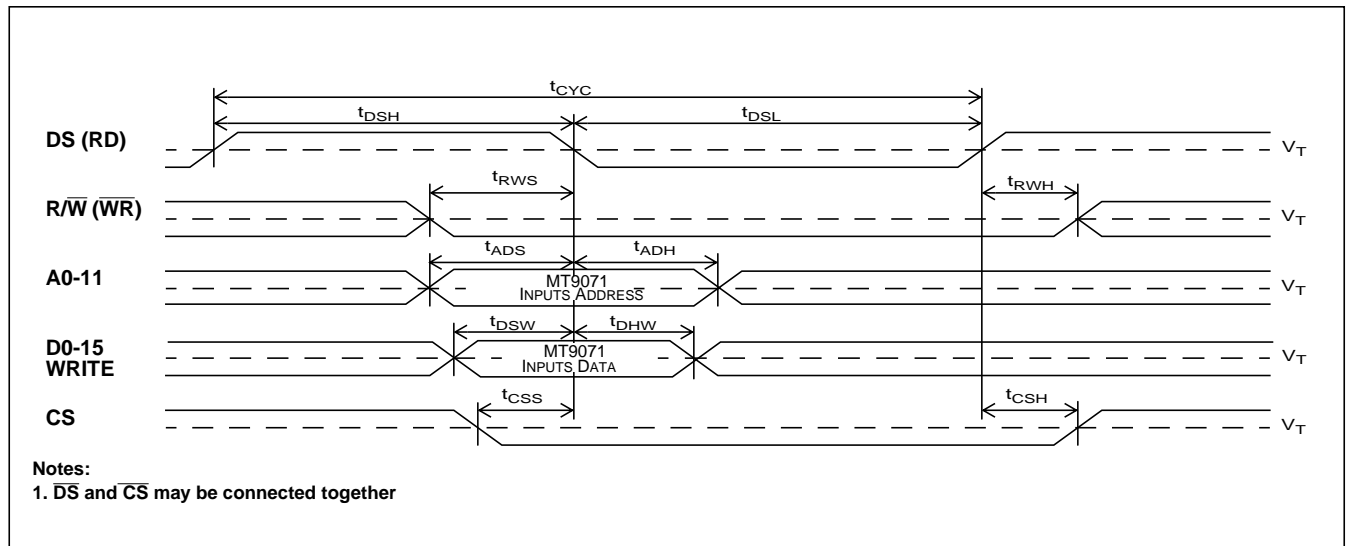
Figure 36 - Motorola Microprocessor Write Timing

AC Electrical Characteristics - Intel Microprocessor Timing*

Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
$\overline{RD}$ or $\overline{WR}$ low	t_{RWL}	130			ns	
$\overline{RD}$ or $\overline{WR}$ High	t_{RWH}	30			ns	
Address Setup	t_{ADS}	0			ns	
Address Hold	t_{ADH}	30			ns	
Data Setup Write	t_{DSW}	10			ns	
Data Hold Write	t_{DHW}	25			ns	
Data Delay Read	t_{DDR}			100	ns	$C_L=150pF$, $R_L=1k\Omega$
Data Hold Read	t_{DHR}	0			ns	$C_L=150pF$, $R_L=1k\Omega$
Data Active to High Z Delay	t_{DAZ}			20	ns	$C_L=150pF$, $R_L=1k\Omega$
$\overline{CS}$ Setup	t_{CSS}	0			ns	
$\overline{CS}$ Hold	t_{CSH}	0			ns	
Cycle Time	t_{CYC}	160				
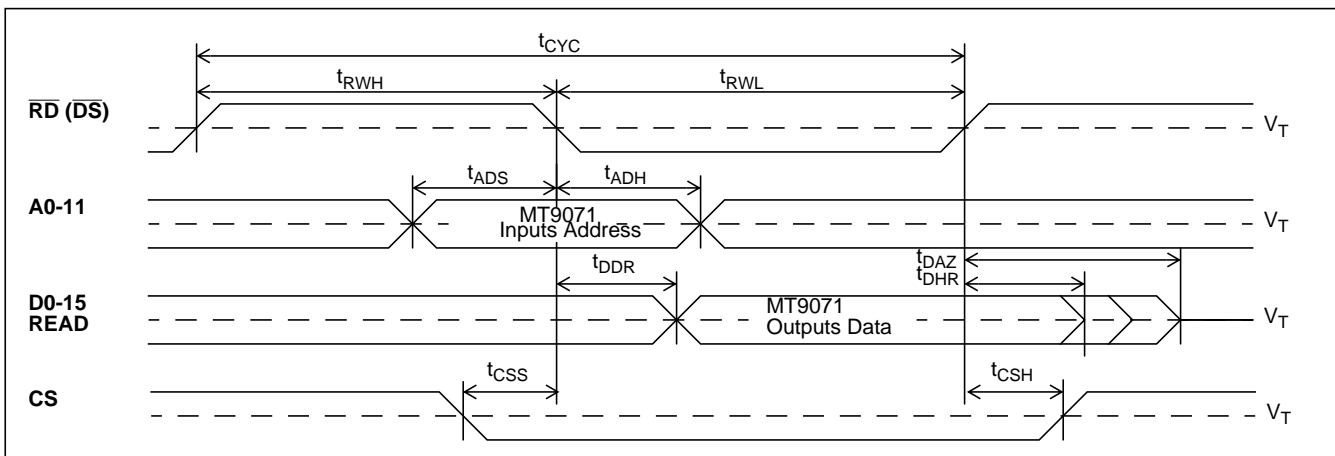
Figure 37 - Intel Microprocessor Read Timing
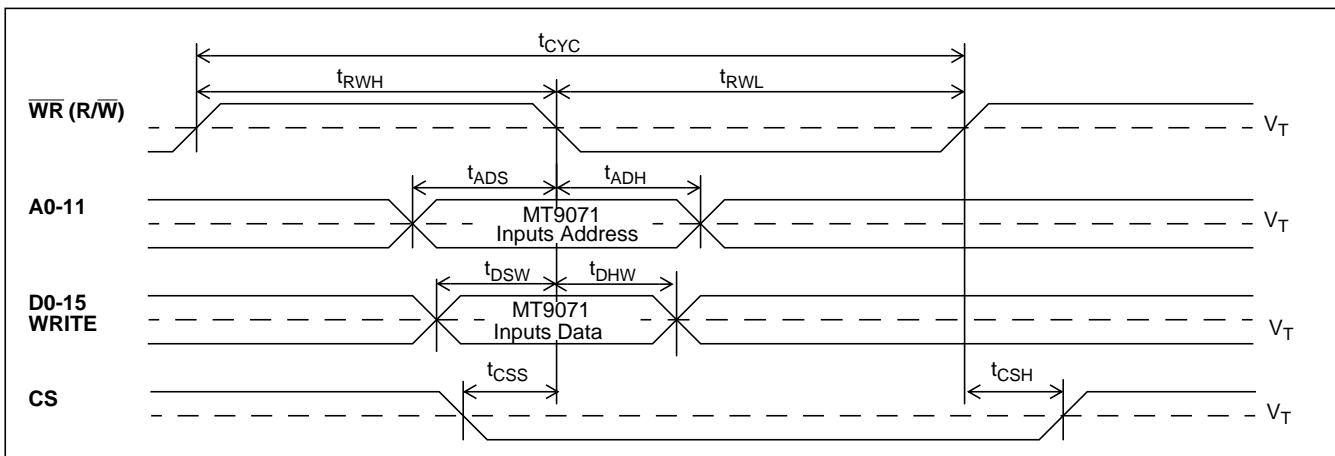
Figure 38 - Intel Microprocessor Write Timing

AC Electrical Characteristics - ST-BUS 2.048Mb/s Timing

	Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
1	Input Clock Width High or Low	t_{C4IW}	100	122	144	ns	
	Output Clock Width High or Low	t_{C4OW}	111	122	133	ns	
	Input Frame Pulse Setup	t_{F0S}	10			ns	
	Input Frame Pulse Hold	t_{F0H}	10			ns	
	Output Frame Pulse Delay	t_{F0D}	-10		10	ns	
	Serial Input Setup	t_{SIS}	15			ns	
	Serial Input Hold	t_{SIH}	15			ns	
	Serial Output Delay	t_{SOD}			55	ns	150pF load on CSTo and DSTo
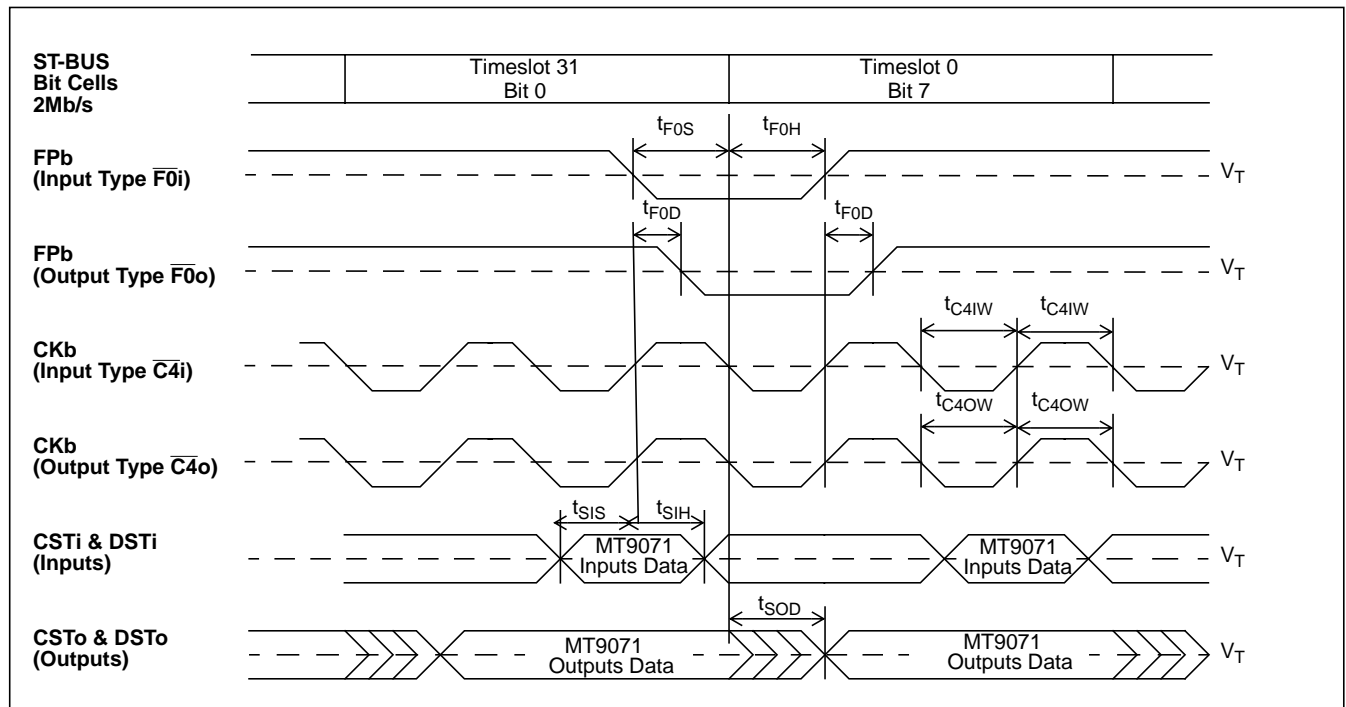
Figure 39 - ST-BUS 2.048Mb/s Timing
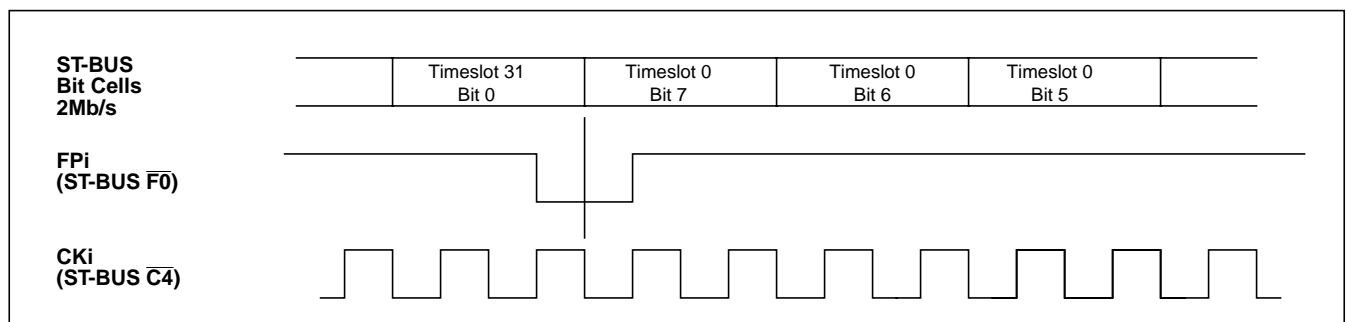
Figure 40 - ST-BUS 2.048Mb/s Functional Timing Diagram

AC Electrical Characteristics - ST-BUS 8.192Mb/s Timing

	Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
1	Input Clock Width High or Low	t_{C16IW}	25	31	35	ns	
2	Output Clock Width High or Low	t_{C16OW}	26	31	34	ns	
3	Input Frame Pulse Setup	t_{F16S}	10			ns	
4	Input Frame Pulse Hold	t_{F16H}	10			ns	
5	Output Frame Pulse Delay	t_{F16D}	-10		10	ns	
6	Serial Input Setup	t_{SIS}	15			ns	
7	Serial Input Hold	t_{SIH}	15			ns	
8	Serial Output Delay	t_{SOD}			55	ns	150pF load on CSTo and DSTo
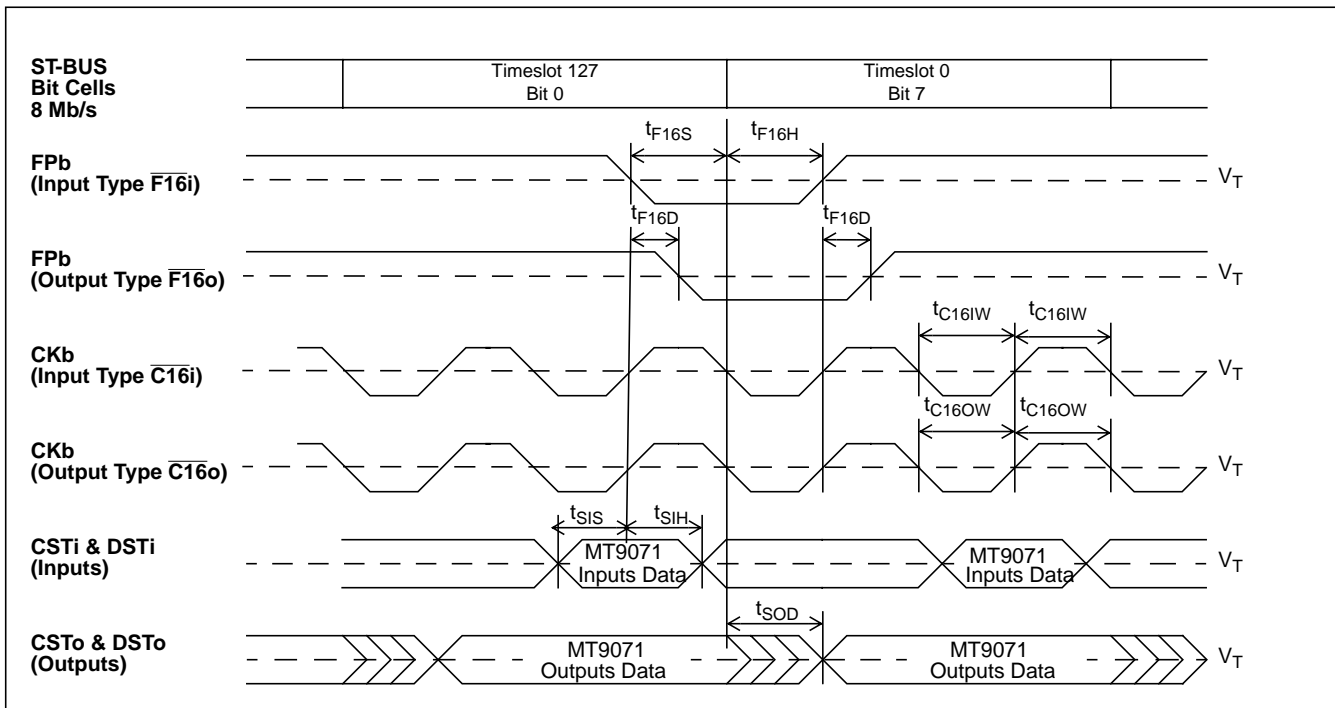
Figure 41 - ST-BUS 8.192Mb/s Timing
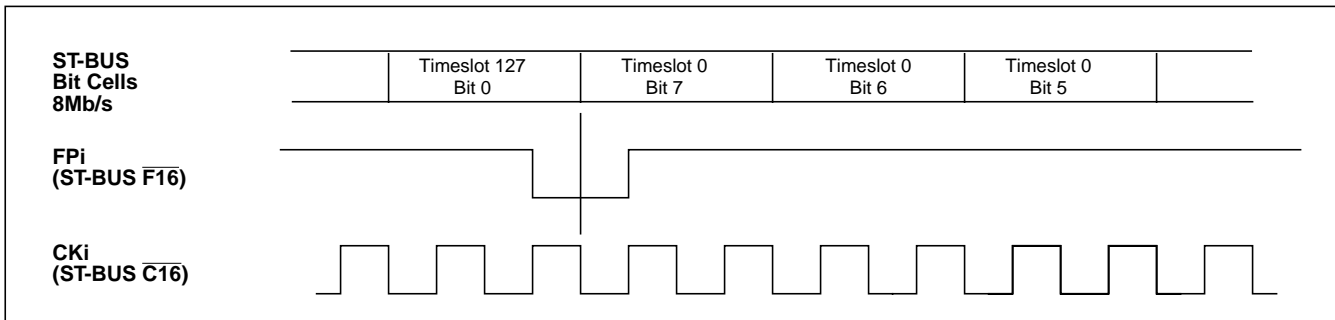
Figure 42 - ST-BUS 8.192Mb/s Functional Timing Diagram

AC Electrical Characteristics - Transmit Multiframe (CRC-4 or CAS) Timing

	Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
	Transmit Multiframe Setup	t_{MS}	50			ns	
	Transmit Multiframe Hold	t_{MH}	50		*	ns	* 255 C2 periods
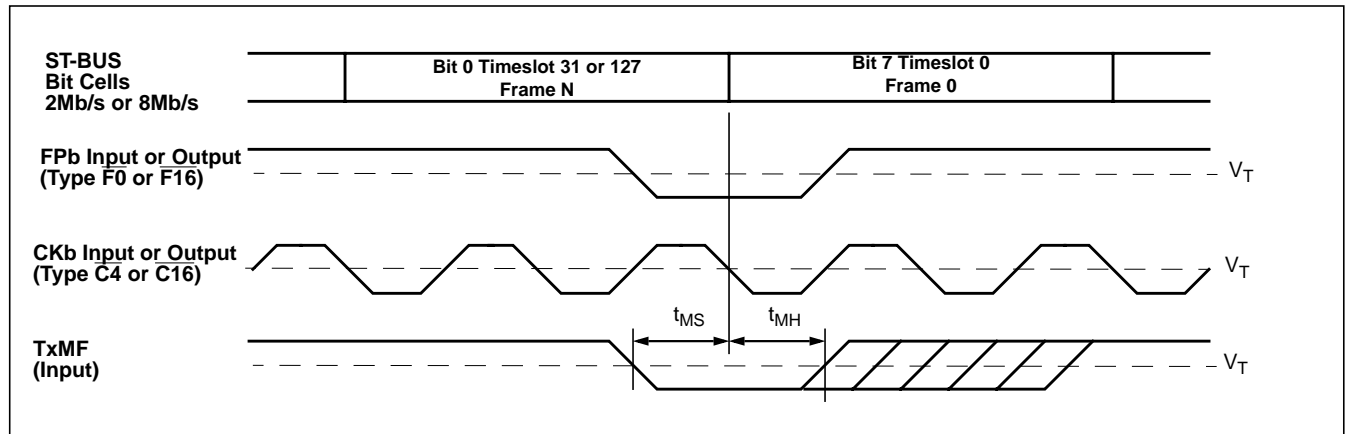
Figure 43 - Transmit Multiframe (CRC-4 or CAS) Timing
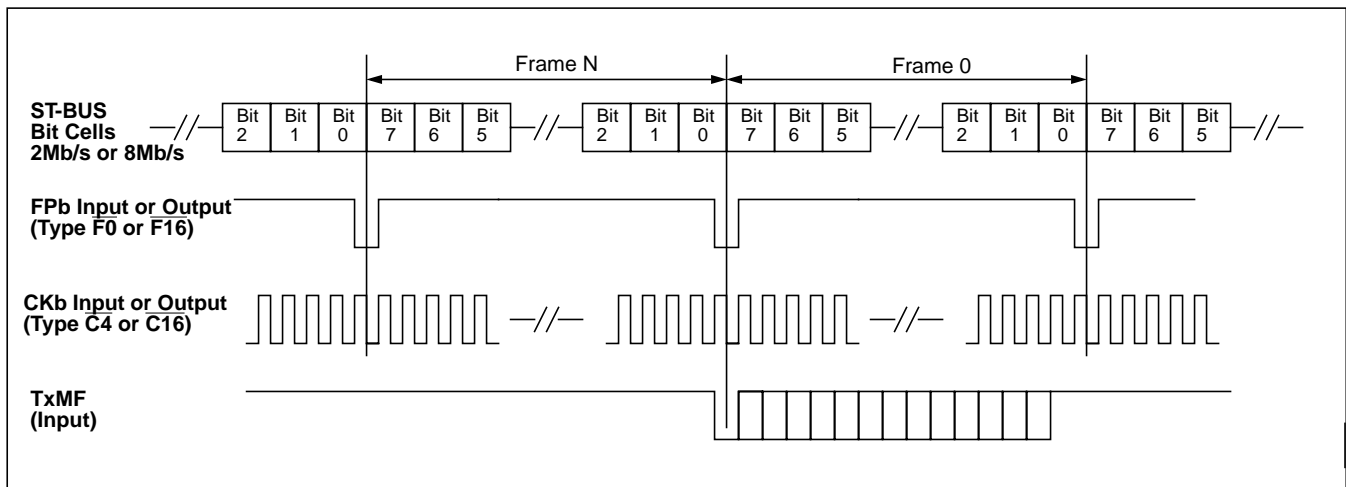
Figure 44 - Transmit Multiframe (CRC-4 or CAS) Functional Timing

AC Electrical Characteristics - Receive Multiframe (CRC-4 or CAS) 2Mb/s Timing

	Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
	Receive Multiframe Output Delay	t_{MOD}			55	ns	150pF load on $\overline{RxMF}$
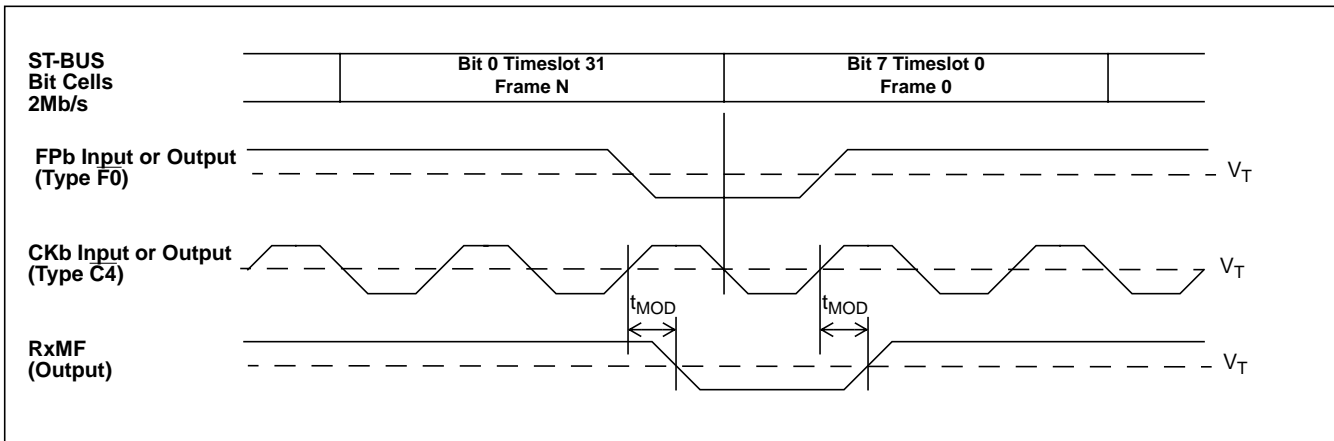
Figure 45 - Receive Multiframe (CRC-4 or CAS) 2Mb/s Timing
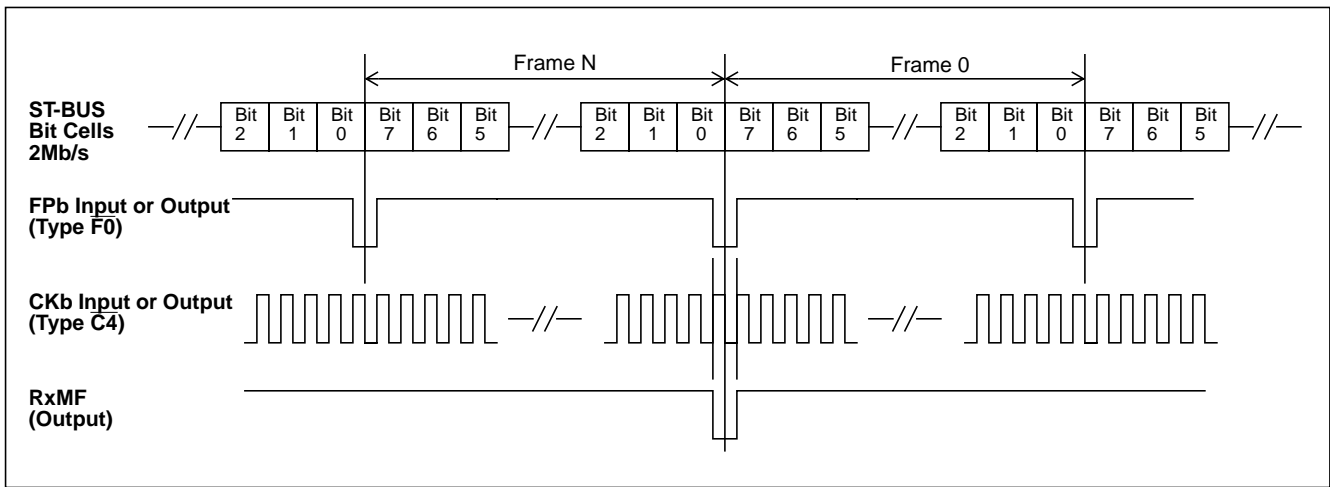
Figure 46 - Receive Multiframe (CRC-4 or CAS) Functional 2Mb/s Timing

AC Electrical Characteristics - Receive Multiframe (CRC-4 or CAS) 8Mb/s Timing

	Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
	Receive Multiframe Output Delay	t_{MOD}			55	ns	150pF load on $\overline{RxMF}$
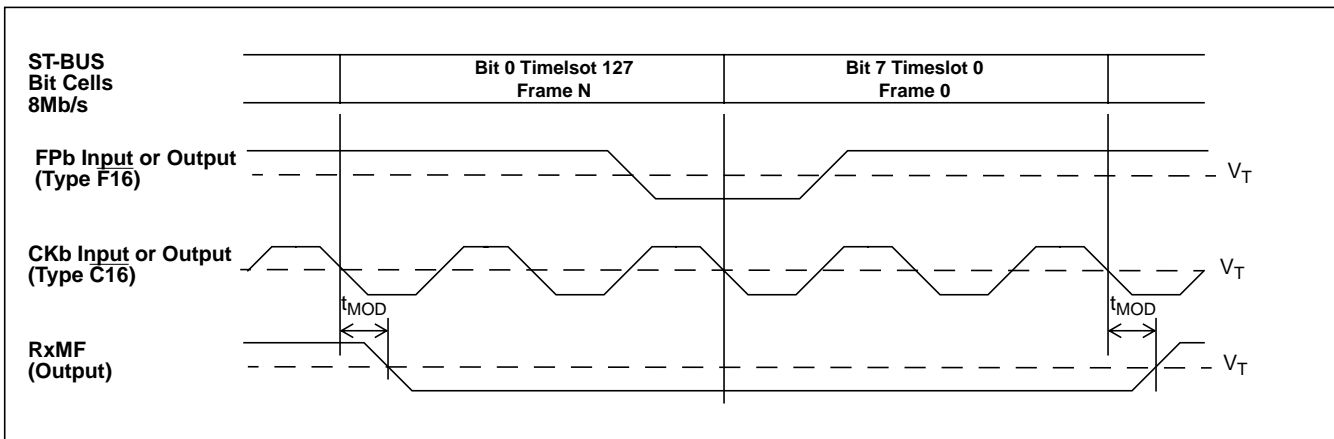
Figure 47 - Receive Multiframe (CRC-4 or CAS) 8Mb/s Timing
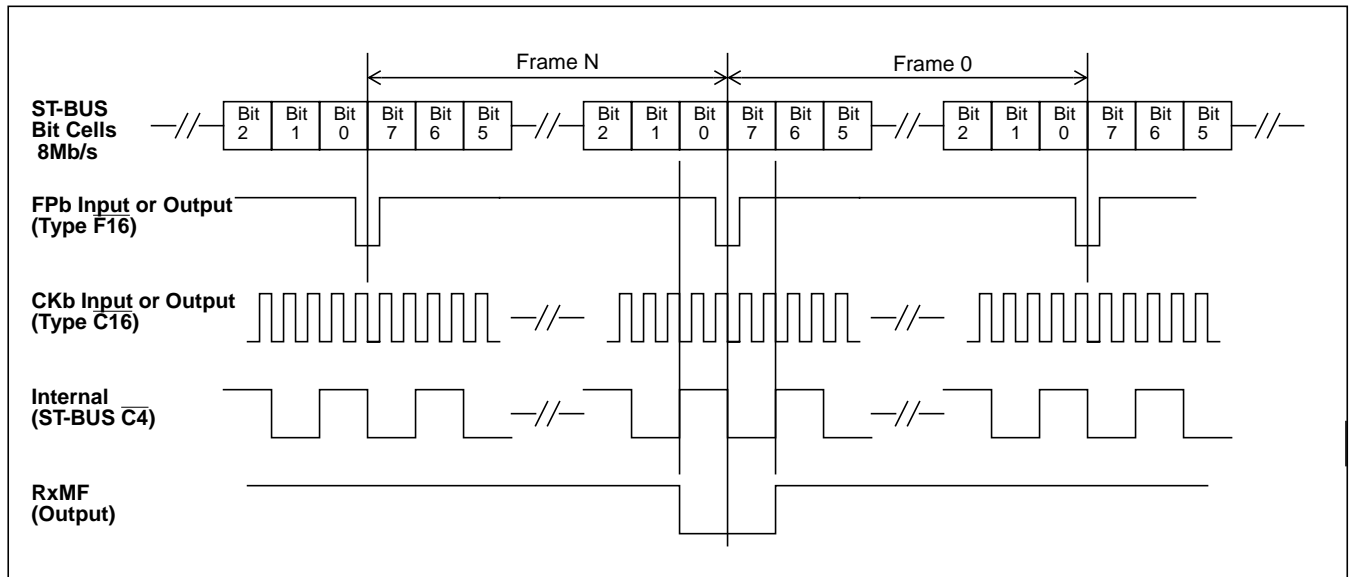
Figure 48 - Receive Multiframe (CRC-4 or CAS) Functional 8Mb/s Timing

AC Electrical Characteristics - Receive Data and Basic Frame Timing

	Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
	Basic Frame Output Delay	t_{BD}	0		160	ns	150pF load on $\overline{RxBF}$
	Data Delay Read	t_{DDR}	0		50	ns	150pF load on RxD
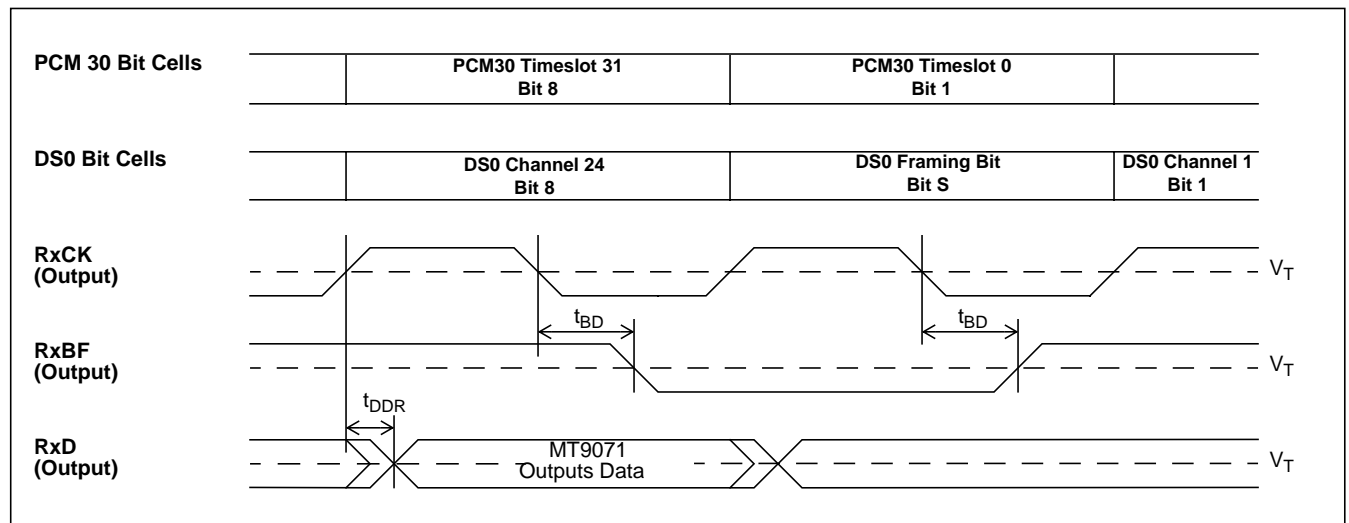
Figure 49 - Receive Data (Slip Buffer Bypass) Timing
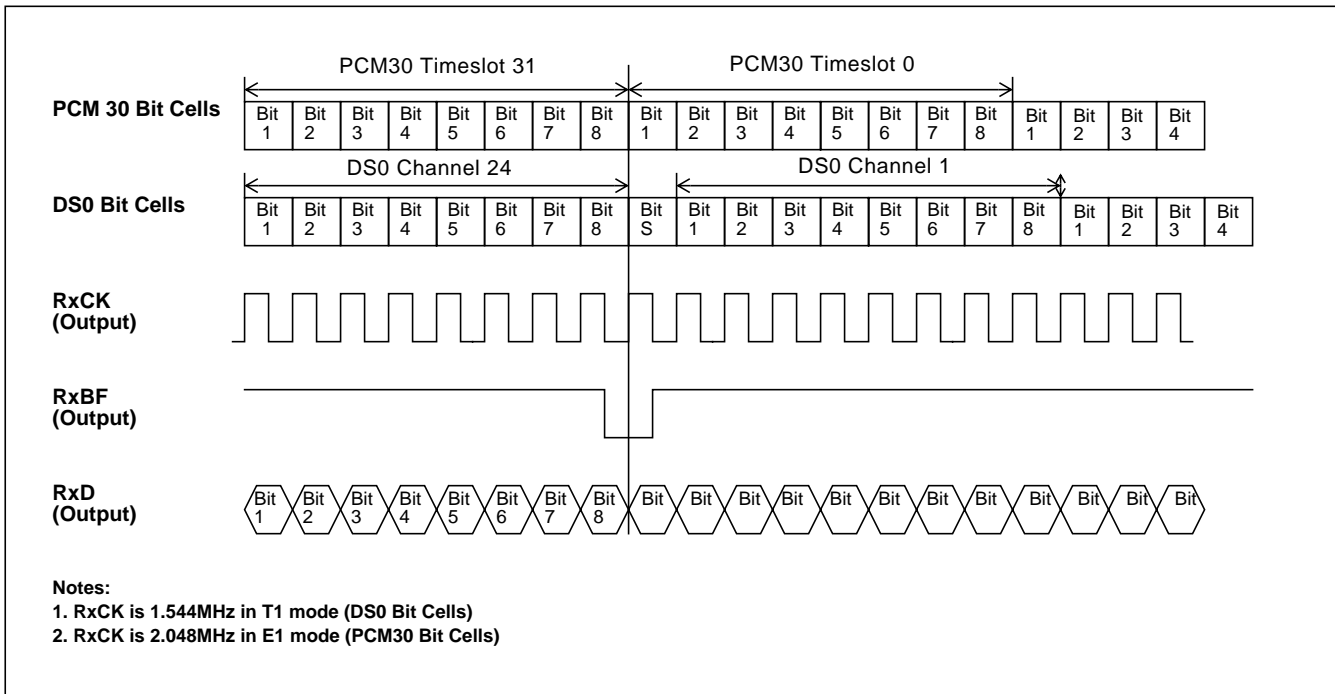
Figure 50 - Receive Data (Slip Buffer Bypass) Functional Timing

AC Electrical Characteristics - DS0, PCM30 and ST-BUS Frame Format

In both the transmit and receive directions, DS0 and PCM30 LSB map to ST-BUS LSB.
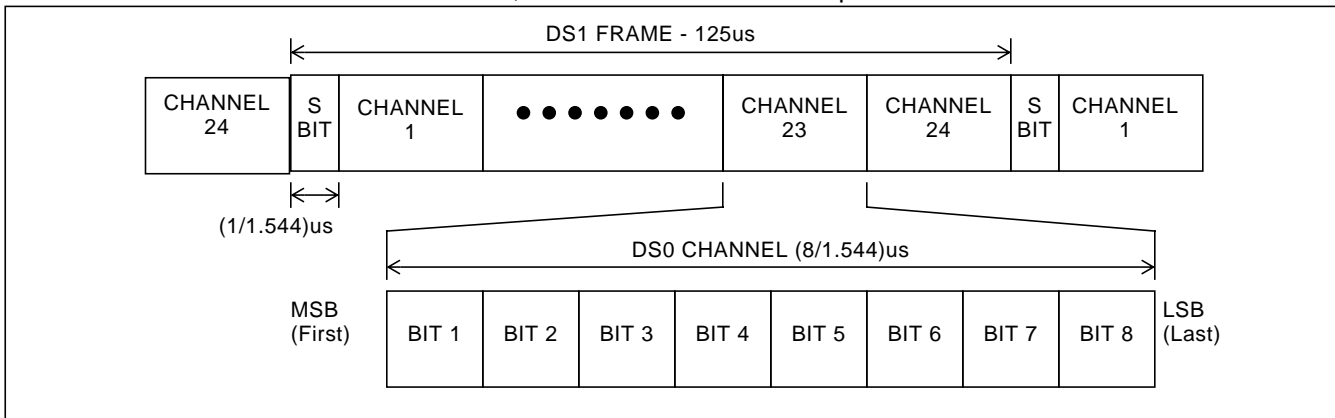
Figure 51 - DS1 Link Frame Format
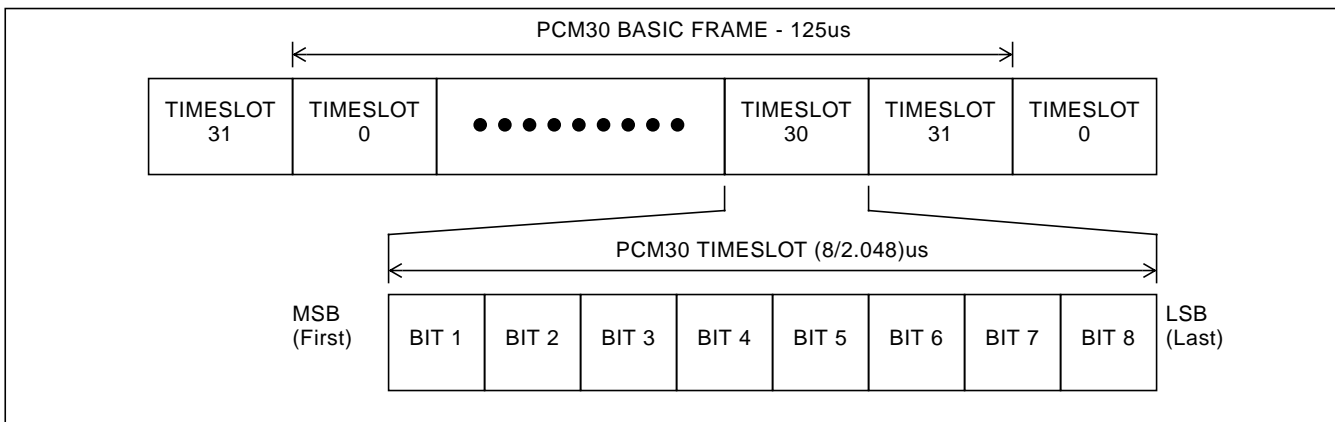
Figure 52 - PCM30 Link Frame Format
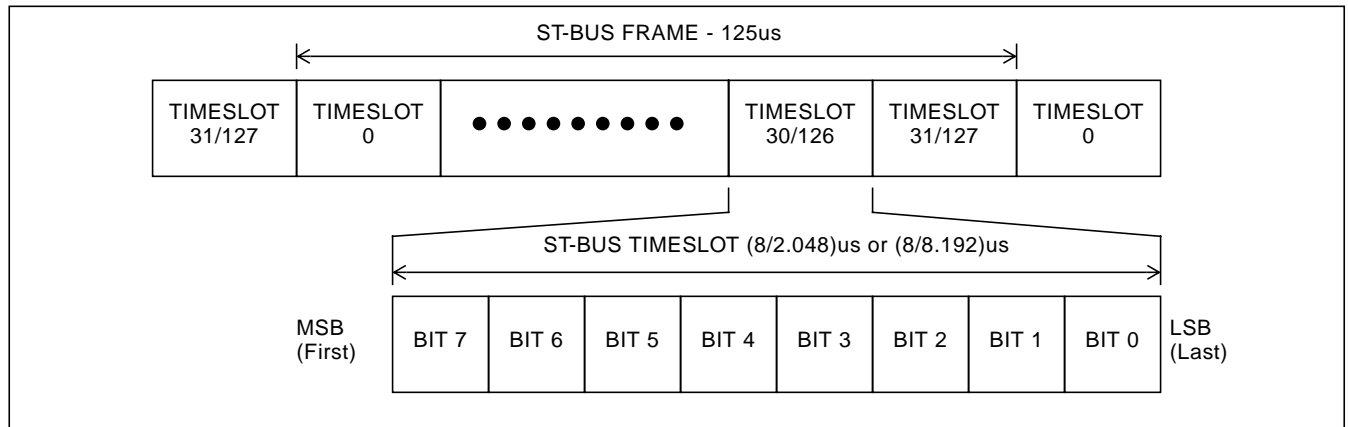
Figure 53 - ST-BUS 2.048Mb/s & 8.192Mb/s Stream Frame Format

AC Electrical Characteristics - JTAG Port Timing

	Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
	TCK Clock Period	t_{TCP}	100			ns	
	TCK Clock Width Low	t_{TCL}	40			ns	
	TCK Clock Width High	t_{TCKH}	40			ns	
	TMS Setup	t_{TMS}	10			ns	
	TMS Hold	t_{TMH}	10			ns	
	TDI Setup	t_{TDS}	10			ns	
	TDI Hold	t_{TDH}	20			ns	
	TDO Output Delay	t_{TDD}			29	ns	
	$\overline{TRST}$ Pulse Width Low	t_{TRST}	25			ns	
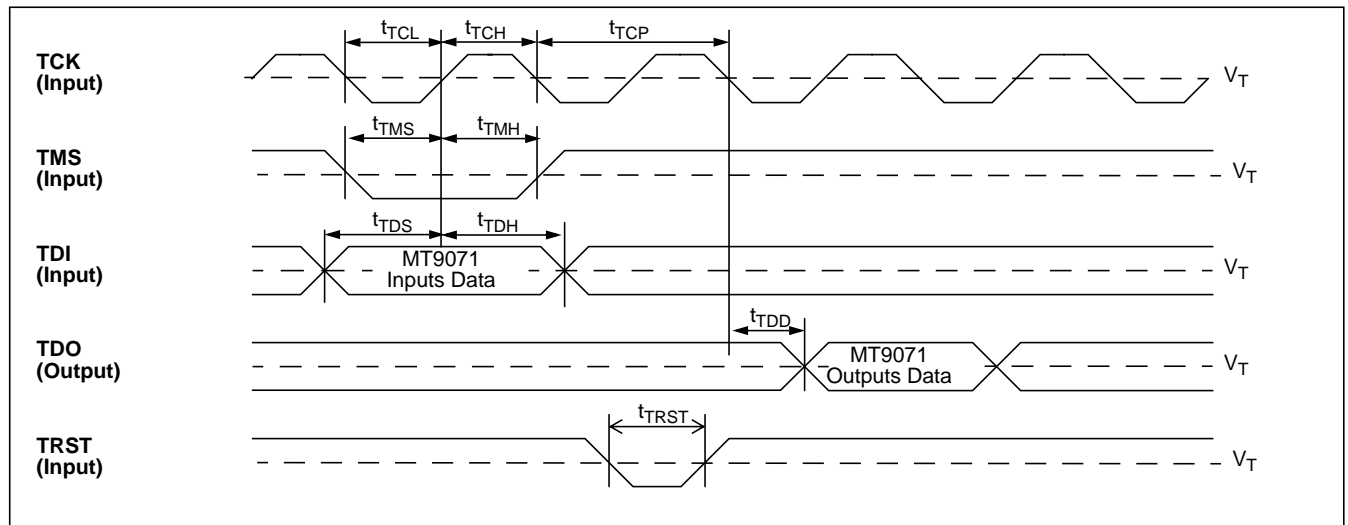
Figure 54 - JTAG Port Timing

Notes:
1) Not to scale
2) Dimensions in inches
3) (Dimensions in millimeters)
4) Ref. JEDEC Standard MS-026

Dim	80-Pin		100-Pin		128-Pin		208-Pin		256-Pin	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	-	0.063 (1.60)	-	0.063 (1.60)	-	0.063 (1.60)	-	0.063 (1.60)	-	0.063 (1.60)
A1	0.002 (0.05)	0.006 (0.15)	0.002 (0.05)	0.006 (0.15)	0.002 (0.05)	0.006 (0.15)	0.002 (0.05)	0.006 (0.15)	0.002 (0.05)	0.006 (0.15)
A2	0.053 (1.35)	0.057 (1.45)	0.053 (1.35)	0.057 (1.45)	0.053 (1.35)	0.057 (1.45)	0.053 (1.35)	0.057 (1.45)	0.053 (1.35)	0.057 (1.45)
b	0.009 (0.22)	0.015 (0.38)	0.007 (0.17)	0.011 (0.27)	0.001 (0.17)	0.011 (0.27)	0.001 (0.17)	0.011 (0.27)	0.005 (0.13)	0.009 (0.23)
D	0.630 (16.00 BSC)		0.630 (16.00 BSC)		0.866 (22.00 BSC)		1.181 (30.00 BSC)		1.181 (30.00 BSC)	
D1	0.551 (14.00 BSC)		0.551 (14.00 BSC)		0.787 (20.00 BSC)		1.102 (28.00 BSC)		1.102 (28.00 BSC)	
e	0.025 (0.65 BSC)		0.020 (0.50 BSC)		0.020 (0.50 BSC)		0.020 (0.50 BSC)		0.016 (0.40 BSC)	
E	0.630 (16.00 BSC)		0.630 (16.00 BSC)		0.630 (16.00 BSC)		1.181 (30.00 BSC)		1.181 (30.0 BSC)	
E1	0.551 (14.00 BSC)		0.551 (14.00 BSC)		0.551 (14.00 BSC)		1.102 (28.00 BSC)		1.102 (28.00 BSC)	

LQFP - B Suffix

Pin #1 Corner

Ø0.50 (3X) REF.

15.00 ± 0.20

1.215 REF

15.00 ± 0.20

Ø 0.40 ~ 0.60 (256X)

17.00 ± 0.20

15.00

1.00

1.00

15.00

17.00 ± 0.20

0.54 ± 0.05

R0.25 Typ.

30 ° X.

(0.36)

C Seating Plane

0.30 ~ 0.5

1.30 ± 0.20

*The ball diameter and stand-off different from Jedec Spec: MO-192

LBGA - 256

MITEL
SEMICONDUCTOR

http://www.mitelsemi.com

World Headquarters - Canada
Tel: +1 (613) 592 2122
Fax: +1 (613) 592 6909

North America	**Asia/Pacific**	**Europe, Middle East,**
Tel: +1 (770) 486 0194	Tel: +65 333 6193	**and Africa (EMEA)**
Fax: +1 (770) 631 8213	Fax: +65 333 6192	Tel: +44 (0) 1793 518528
		Fax: +44 (0) 1793 518581

TECHNICAL DOCUMENTATION - NOT FOR RESALE

Package Outlines

Pin #1 Corner

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

A B C D E F G H J K L M N P R T

Ø0.50 (3X) REF.

15.00 ± 0.20

1.215 REF

15.00 ± 0.20

Ø 0.40 ~ 0.60 (256X)

16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

A B C D E F G H J K L M N P R T

17.00 ± 0.20

15.00

1.00

B

A

1.00

15.00

17.00 ± 0.20

0.54 ± 0.05

R0.25 Typ.

30 ° X.

C Seating Plane

(0.36)

0.30 ~ 0.5

1.30 ± 0.20

*The ball diamter and stand-off different from Jedec Spec: : MO-192

LBGA - 256

Package Outlines

Notes:
1) Not to scale
2) Dimensions in inches
3) (Dimensions in millimeters)
4) Ref. JEDEC Standard MS-026

Dim	80-Pin		100-Pin		128-Pin		208-Pin		256-Pin	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	-	0.063 (1.60)	-	0.063 (1.60)	-	0.063 (1.60)	-	0.063 (1.60)	-	0.063 (1.60)
A1	0.002 (0.05)	0.006 (0.15)	0.002 (0.05)	0.006 (0.15)	0.002 (0.05)	0.006 (0.15)	0.002 (0.05)	0.006 (0.15)	0.002 (0.05)	0.006 (0.15)
A2	0.053 (1.35)	0.057 (1.45)	0.053 (1.35)	0.057 (1.45)	0.053 (1.35)	0.057 (1.45)	0.053 (1.35)	0.057 (1.45)	0.053 (1.35)	0.057 (1.45)
b	0.009 (0.22)	0.015 (0.38)	0.001 (0.17)	0.011 (0.27)	0.001 (0.17)	0.011 (0.27)	0.001 (0.17)	0.011 (0.27)	0.005 (0.13)	0.009 (0.23)
D	0.630 (16.00 BSC)		0.630 (16.00 BSC)		0.866 (22.00 BSC)		1.181 (30.00 BSC)		1.181 (30.00 BSC)	
D1	0.551 (14.00 BSC)		0.551 (14.00 BSC)		0.787 (20.00 BSC)		1.102 (28.00 BSC)		1.102 (28.00 BSC)	
e	0.025 (0.65 BSC)		0.020 (0.50 BSC)		0.020 (0.50 BSC)		0.020 (0.50 BSC)		0.016 (0.40 BSC)	
E	0.630 (16.00 BSC)		0.630 (16.00 BSC)		0.630 (16.00 BSC)		1.181 (30.00 BSC)		1.181 (30.0 BSC)	
E1	0.551 (14.00 BSC)		0.551 (14.00 BSC)		0.551 (14.00 BSC)		1.102 (28.00 BSC)		1.102 (28.00 BSC)	

LQFP - B Suffix

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World Headquarters - Canada
Tel: +1 (613) 592 2122
Fax: +1 (613) 592 6909

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