QUALCOMM

Q1650

k=7 MULTI-CODE RATE VITERBI DECODER

2.5, 10, 25 Mbps Data Rates

Technical Data Sheet

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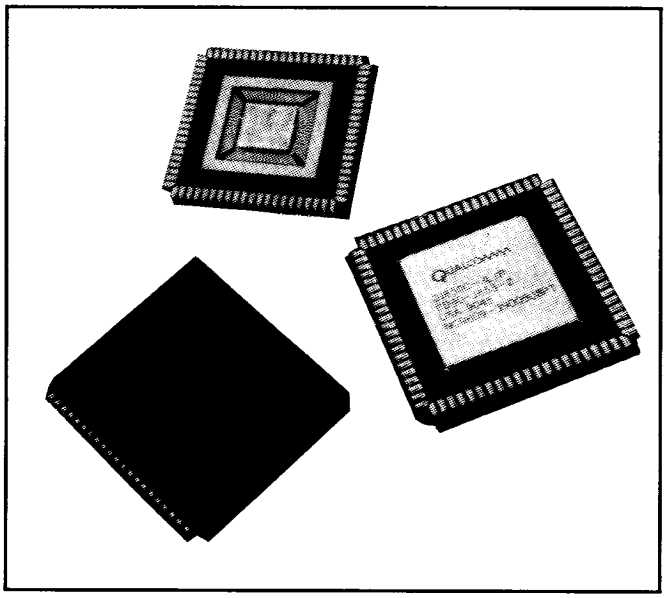
- Processor Interface Simplifies Control and Status
- 3-Bit Soft-Decision Decoder Inputs
- 5.2 dB Coding Gain (Rate 1/2), 5.5 dB Coding Gain (Rate 1/3) at 10^{-5} BER
- Easy Implementation of Additional Code Rates
- Automatic Synchronization Capability
- Parallel or Serial Decoder Data Inputs
- On-Chip V.35 Data Scrambler/Descrambler
- Low Power CMOS Implementation
- Standard 84-Pin LCC Package
- Complies with INTELSAT IESS-308 and 309
- Commercial and MIL versions available



GENERAL DESCRIPTION

Forward Error Correction (FEC) techniques provide higher throughput data rates with improved bit error rate performance for power-limited (and in some cases bandwidth-limited) digital communication channels. Convolutional encoding of data combined with Viterbi decoding at the receiving node is the industry FEC standard for digital channels, especially those concerned with errors caused by the introduction of additive white Gaussian noise (AWGN). Satellite communication channels are examples of this noise environment. Figure 1 shows a typical application of FEC techniques in a communication system.

The Q1650 decoder provides convolutional encoding and Viterbi decoding of data channels while also incorporating powerful built-in features. Its capabilities have been optimized for modern digital communication channels. Figures 2 and 3 show block diagrams of the encoder and decoder functions of the Q1650 FEC system.

The Q1650 device processes data at one of four selectable code rates ($^1/_3$, $^1/_2$, $^3/_4$, and $^7/_8$) using the industry standard constraint length (k) seven algorithms. It can operate at other code rates with minimal external circuitry. The Q1650 device provides built-in synchronization capability for standard BPSK (Binary Phase Shift Keying), QPSK (Quadrature), and OQPSK (Offset Quadrature) modems and operates with either 1-bit hard-decision data or 3-bit soft-decision encoded data.

The decoder is available in multiple speed grades with maximum data rates of 2.5, 10, and 25 Mbps to suit a variety of systems applications. All speed versions are pin-for-pin compatible; a single modem board design can be used for many of data rates.

The Q1650 device includes two powerful built-in techniques for monitoring synchronization status and for performing channel bit error rate measurements. In addition, the device includes a processor interface to facilitate control and status monitoring functions while keeping device pinout to a minimum.

The Q1650 decoder is packaged in an 84-pin plastic or ceramic LCC package and is implemented in fully static CMOS logic to reduce power consumption. The device uses fully parallel circuit architecture to negate the requirement for a higher speed computation clock as found in most Viterbi decoder implementations.

The Q1650 decoder is well suited to commercial satellite communication networks, including INTELSAT and INMARSAT, and to military and NASA communication systems. The low cost and high performance of the Q1650 product line make it ideal for FEC requirements in systems like DBS, VSAT, digital modems, and digital cellular telephone applications.

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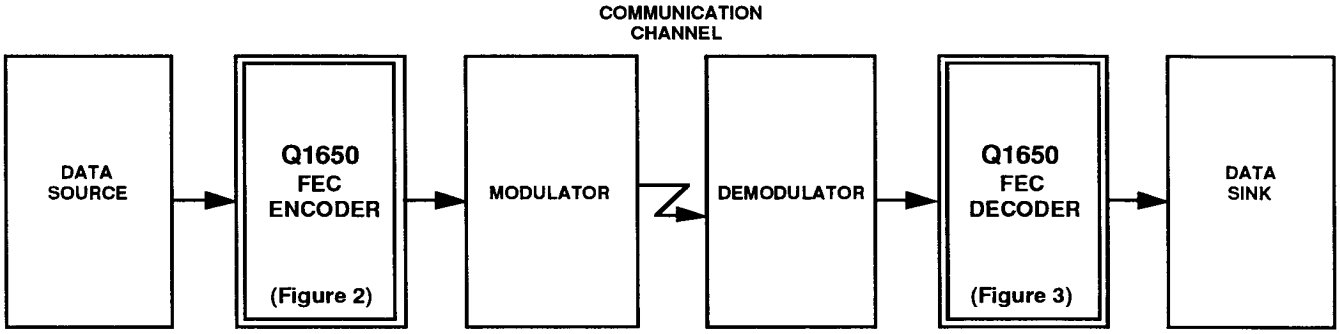


Figure 1. Typical Application of FEC in a Communication System

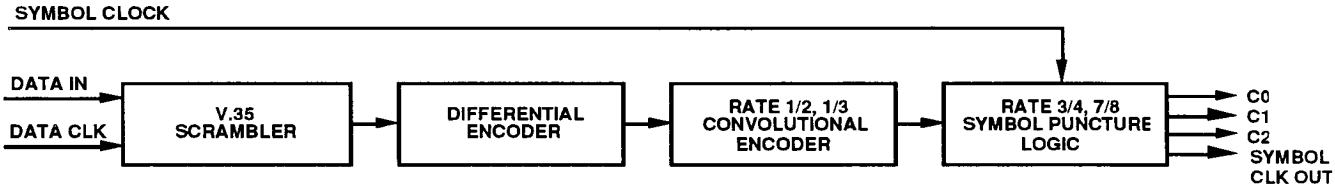


Figure 2. Q1650 Encoder Block Diagram

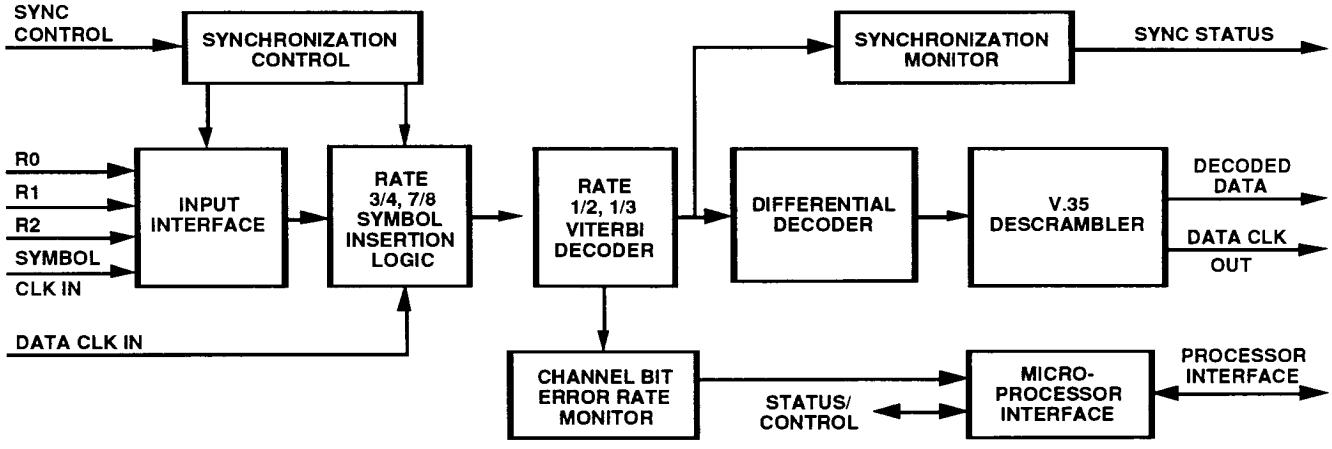


Figure 3. Q1650 Decoder Block Diagram

THEORY OF OPERATION

Convolutional Encoder

Convolutional codes have been studied and used for forward error correction (FEC) in digital communication systems since the 1950s. A convolutional code maps a number (n) of information bits into a number (m) of single-bit "code words" to be transmitted over the channel, where m>n. The ratio of $^{n}/_{m}$ is referred to the code rate. For instance, a commonly used convolutional code transforms each information bit (i.e., n=1) to two code words (i.e., m=2) prior to transmission over the noisy channel. This is a rate $^{1}/_{2}$ code.

The transformation from information bits to code words for transmission is accomplished by a time convolution of the information data with a finite-memory windowing function commonly referred to as a generating function. In the case of the rate $^{1}/_{2}$ code previously described, two generating functions (G0 and G1) are convolved with the information data stream such that each time a new information data bit is considered, the G0 and G1 generating functions each create one output bit or code word (C0, C1, respectively).

The length of the finite memory of the convolutional generating function is the "constraint length" of the code. Figure 4 shows the generating functions of the rate $^{1}/_{2}$ and $^{1}/_{3}$ codes implemented by the Q1650 convolutional encoder. As the diagram shows, the memory length of the encoder is six previous bits plus the current input bit; thus, this is a constraint length seven code (commonly denoted as k=7). The generating functions of the convolutional code are identified by denoting the "taps" of each convoluting function. For the rate $^{1}/_{2}$, k=7 code shown in Figure 4, the generating functions are denoted as G0=1111001 (binary) or 171 (octal) and G1=1011011 (binary) or 133 (octal). This algorithm provides the best error correcting performance of all rate $^{1}/_{2}$, k=7 codes.

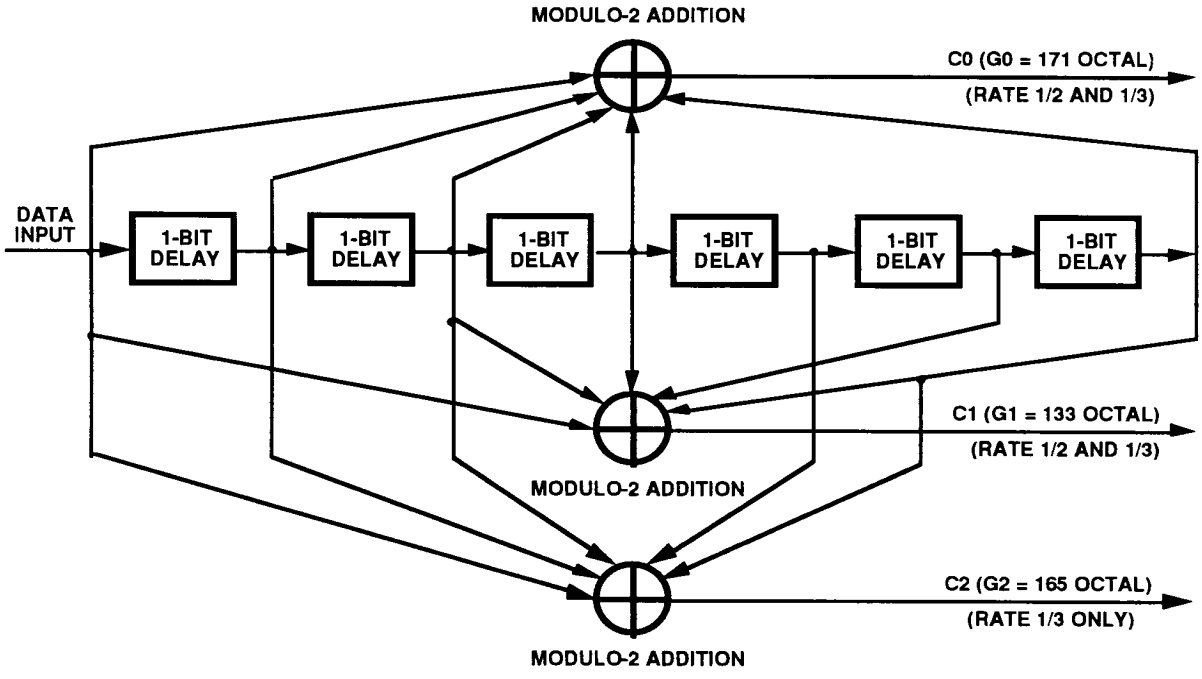


Figure 4. Constraint Length Seven (k=7) Convolutional Encoder

The Q1650 device implements two fundamental convolutional codes. Specifically, these codes are the rate 1/2 code previously described and a second code which is also k=7, but with a code rate of 1/3. The rate 1/3 algorithm involves three generating functions which are applied each time a new information bit is input to the encoder as shown in Figure 4. Two of these three generating functions (specifically G0 and G1) have the same values, i.e., 171 and 133 (octal), respectively, as the rate 1/2. The third generating function (G2) for the rate 1/3 code is 165 (octal).

In addition to these two fundamental codes, the Q1650 decoder can implement higher code rates through "punctured coding." This technique is described below. Higher code rates, such as rate 3/4 or 7/8, reduce the coding gain of the FEC system. However, these higher code rates increase the bandwidth efficiency of the communication system when compared to a rate 1/2 or 1/3 code.

Viterbi Decoder

While the implementation of a convolutional encoder is quite straightforward and simple as shown in the previous section, the decoding of such a coded data stream at the receiving node is quite complex. In the late 1960s, Dr. A. J. Viterbi described a maximum likelihood decoding technique which greatly reduced the circuit sophistication of previous approaches. In spite of this advance, the circuit complexity of such a decoder prevented high-speed single-chip implementations of the Viterbi algorithm until the mid-1980s when QUALCOMM introduced the Q1401 Viterbi decoder. Now, the Q1650 decoder offers the most efficient and powerful single-chip implementation of the Viterbi decoder algorithm.

Viterbi decoding consists fundamentally of three processes. The first step in the decoder process is to generate a set of correlation measurements, known as "branch metrics", for each "m" grouping of code words input from the communication channel (where "m" is 2 for rate 1/2 codes, 3 for rate 1/3 codes, etc.). These branch metric values indicate the correlation between the received code words and the 2^m possible code word combinations.

The Viterbi decoder determines the state of the 7-bit memory at the encoder using a maximum likelihood technique. Once the value of the encoder memory is determined, the original information is known, since the encoder memory is simply the information that has been stored in the memory. To determine the encoder state, the second step in the Viterbi algorithm generates a set of 2^{k-1} (remember that "k" is the constraint length, i.e., k=7 for the Q1650 algorithms) "state metrics" which are measurements of the occurrence probability for each of the 2^{k-1} possible encoder memory states. As the state metrics are computed, a binary decision is formed for each of the 2^{k-1} possible states as to the probable path taken to arrive at that particular state. These binary decision are stored in a "path memory."

Step three computes the decoded output data. To do this, the "path" from the current state to some point in the finite past is traced back by "chaining" the binary decisions stored in the path memory during step 2 from state to state. The effects caused by noise to the one and only correct result are mitigated as the paths within the "chainback" memory converge after some history. The greater the "depth" of the chainback process the more likely that the final decoded result is error free. As a result, higher code rates and constraint lengths require longer chainback depth for best performance. The chainback memory in the Viterbi decoder traces the history of the previous states to arrive at the most probable state of the encoder in the past, and thus determine the transmitted data.

Puncture Coding

Punctured coding techniques allow a lower rate encoder/decoder (e.g., rate 1/2) to be used to generate a higher rate coding function (e.g., rate 3/4). The operation of a punctured code system is illustrated in Figure 5. This figure shows a system based on a rate 1/2 encoder and decoder used to generate a transmitted code rate of 3/4. This operation first consists of encoding the information (A) to be transmitted with a rate 1/2 encoder (B). However, prior to transmission certain of the symbols of the rate 1/2 encoded stream are "punctured" or deleted and not transmitted (C). In the example of Figure 5, two out of six bits from the rate 1/2 encoder are deleted in a repeating pattern. Since for every three information bits to be transmitted only four encoded bits are actually transmitted, this is a rate 3/4 code operation.

At the receiving node the punctured encoded bits are replaced with "null" symbols prior to decoding with the rate 1/2 decoder (D). These nulls symbols are indicated to the Q1650 decoder inputs by asserting the "erase" input pins as appropriate for R0, R1, or R2. The decoder treats these null symbols as a symbol which is neither a received "1" nor "0", but is exactly

between the "1" and "0"; that is, no information is conveyed by that symbol. This is, of course, reducing the amount of information available to the rate 1/2 decoder from which to make decisions about the original data stream. However, the coding performance of this "punctured" rate 3/4 code operation matches the coding performance of the best known classic rate 3/4 convolutional code.

The major advantage to this approach is that a single code rate decoder (i.e., rate 1/2 or 1/3) can implement a wide range of codes. Specifically, any code rate of the form (n-1)/n can be efficiently implemented with this structure. Of course, the best performance is achieved only with a certain pattern of the puncturing of symbols. These best puncture codes have been researched and are shown in Figure 6 for rates from 2/3 through 15/16. One important aspect of operation with punctured codes is that the chainback depth of the rate 1/2 decoder must increase as the code rate increases. Whereas a chainback memory depth of 35-40 states is adequate for rate 1/2 decoding, rate 3/4 decoders require memory depths of at least 70 states to be efficient, and rate 7/8 puncture decoders should have a minimum chainback depth of more than 90 states. The Q1650 device implements a minimum chainback memory depth of 96 states and therefore is very effective at decoding code rates up to 7/8 . Operation with code rates higher than rate 7/8 will result in a minor performance degradation in the coding gain when compared to the theoretical best.

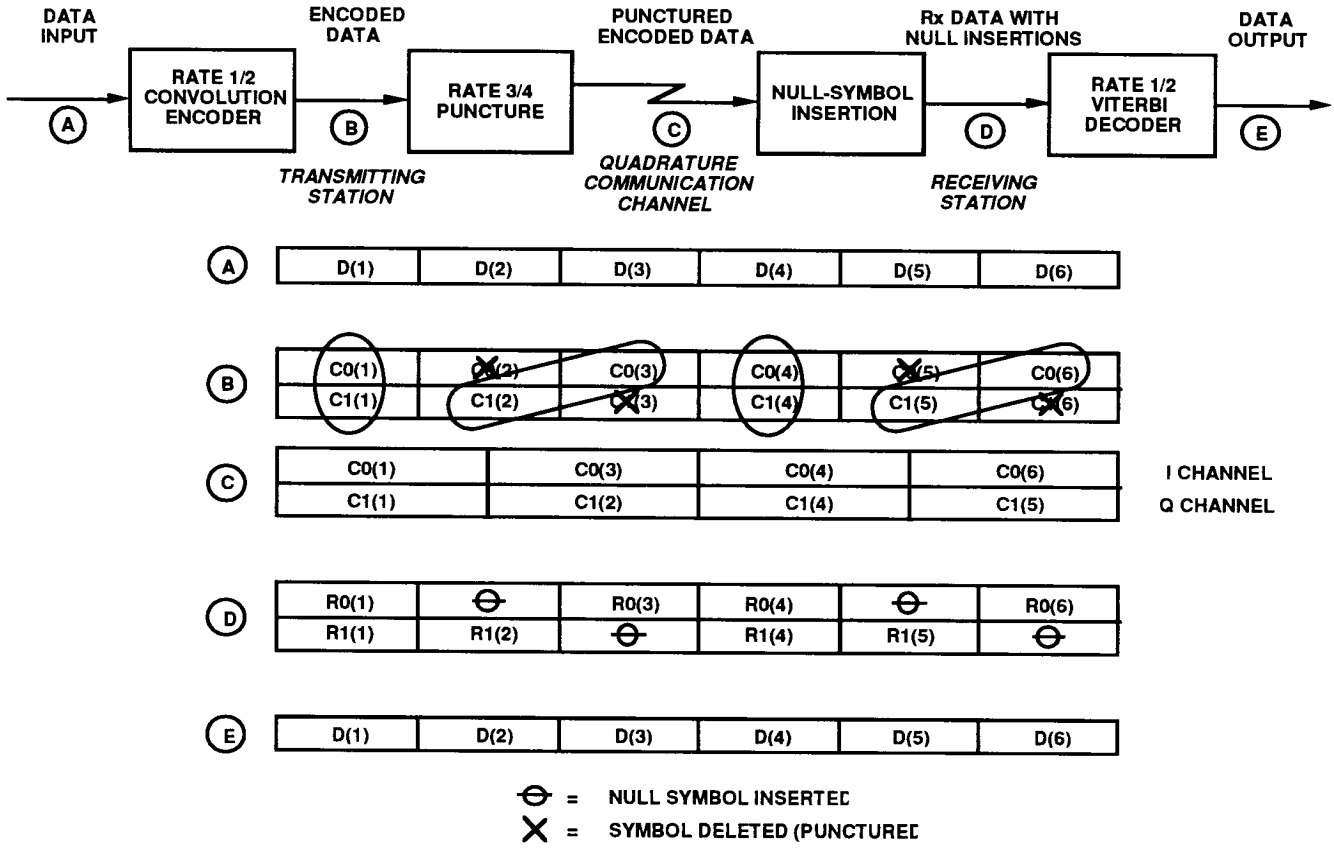


Figure 5. Punctured Coding System

One additional aspect to punctured coding operation is the requirement to synchronize the decoder "null symbol insertion" pattern to the encoder symbol puncture pattern. The Q1650 device performs all the necessary encoder symbol puncture, decoder null symbol insertion, and synchronization functions required to implement the best rate 3/4 and 7/8 patterns. In addition, the Q1650 decoder includes integral First-In-First-Out (FIFO) circuits to ease the frequent requirement of punctured code systems to re-align the punctured encoded stream to a channel clock which is a non-integer multiple of the information data rate.

The Q1650 decoder also provides "symbol erasure" input pins for the R0, R1 and R2 decoder inputs. These pins allow the designer to implement punctured code rates other than the rate 3/4 and 7/8 patterns implemented internally on the device.

CODE RATE	SYMBOL PUNCTURE PATTERN (0 = DELETED CODEWORD)	
1/2	C0:	1
	C1:	1
2/3	C0:	1 0
	C1:	1 1
3/4*	C0:	1 0 1
	C1:	1 1 0
4/5	C0:	1 0 0 0
	C1:	1 1 1 1
5/6	C0:	1 0 1 0 1
	C1:	1 1 0 1 0
6/7	C0:	1 0 0 1 0 1
	C1:	1 1 1 0 1 0
7/8*	C0:	1 0 0 0 1 0 1
	C1:	1 1 1 1 0 1 0
11/12	C0:	1 0 0 0 1 0 0 0 0 0 1
	C1:	1 1 1 1 0 1 1 1 1 1 0
12/13	C0:	1 0 0 0 0 0 0 0 1 0 1 0
	C1:	1 1 1 1 1 1 1 1 0 1 0 1
15/16	C0:	1 0 0 1 1 0 1 0 0 1 0 1 1 0 1
	C1:	1 1 1 0 0 1 0 1 1 0 1 0 0 1 0
16/17	C0:	1 0 1 0 1 0 1 1 0 1 1 1 1 1 0 1 0
	C1:	1 1 0 1 0 1 0 0 1 0 0 0 0 1 0 1

*Two-code word groupings are shown for operation with code rates 3/4 and 7/8 in parallel data mode. C0 and C1 code words are output on the C0 and C1 signals, respectively, except for the second symbol in rate 7/8 pattern. In that case, the second of the two C1 code words is output on the C0 signal.

Figure 6. Best Punctured Code Patterns

FUNCTIONAL OVERVIEW

Interfacing

Interfacing with the Q1650 decoder is straightforward. All data inputs are provided to the device synchronously with externally sourced clocks. Data signals are clocked into the device on the rising edge of the encoder and decoder clock inputs. Data outputs change on the rising edge of the encoder and decoder clock outputs. To provide varying code rates, the Q1650 device requires two externally generated clock inputs for operation of the encoder and decoder, specifically a data rate clock and a channel rate clock. The frequency relationship of these two clocks varies according to code rate and data input format.

Most control and status information is provided to and from the Q1650 device through a bus-oriented processor interface. This interface uses an 8-bit data bus and a 5-bit address bus along with read, write, and chip select signals to read from status ports and write to control ports. In addition, the encoder and decoder input and output data can be written and read directly using the processor interface. In this mode, the Q1650 device acts as a peripheral for forward error correcting of data processed by a host processor.

Clocking Scheme

Multiple code rate operation of the Q1650 encoder and decoder functions requires special timing circuits to provide for the various modes of operation. For each code rate R, the Q1650 encoder function outputs $1/R$ encoded bits for each input information bit. For instance, two encoded output bits are generated for each information bit when operating with code rate $1/2$. As described below, these encoded bits can be output in either "parallel" or "serial" fashion.

When encoded bits are output in the parallel mode, the outputs are provided on two output signals which are clocked at the same frequency as the input information. However, if the two encoded bits are output in the serial manner, all outputs are provided on the same pin and the data on this pin changes at twice the rate of the input information bits. Thus, two clocks must be provided to the encoder functions: the first clock is used for the input of information bits on the ENCDATIN pin and the second clock is used to output the serial format data on the C0 output pin.

The decoder allows for this condition by clocking the input information data on a completely independent clock from that used to output encoded data from the encoder. The input information is clocked into the device relative to the ENCINCLK signal, while output data is clocked relative to the ENCOUTCLK. The information sourced to the encoder function is re-synchronized to the output clock within the decoder with an asynchronous first-in first-out (FIFO) circuit. This asynchronous buffer capability is especially useful when operating with a code rate in which the output-to-input bit rate is not an integer (e.g., rate $3/4$ or $7/8$). Figure 7 shows the general clocking scheme for the Q1650 encoder and decoder functions. Note that the output clock input to the encoder is also provided as an output from the encoder. The Q1650 decoder function also makes use of two different clock signals to provide for changing code rates.

The ratio between the frequency of the input information clock and output encoded bit clock changes with changing code rate. When operating at code rate $1/3$ and serial output mode, the ratio of the encoder input clock to encoder output clock frequency is $1/3$. When operating with rate $1/3$ coding and parallel data mode the frequency of the input and output clock is the same. In fact, the decoder clock scheme is symmetrical to the encoder clock scheme.

Operation with rates $3/4$ and $7/8$ involves a more sophisticated relationship between the input information clock to the encoder or decoder and the output bit clock. Specifically, when operating with rate $3/4$ coding and parallel outputs, the ratio of ENCINCLK frequency to ENCOUTCLK frequency is $3/2$. This is because for every three input information bits two outputs of two bits each are formed (refer to the section on rate $3/4$ encoding operation below). These two clock frequencies must be provided by external circuitry. In a typical communication system only one of the two clocks is explicitly provided by the system, usually the channel clock signal. In this kind of system the information clock signal may be generated using various synthesis techniques such as phase-locked loop (PLL) circuits. The FIFO buffer allows for phase jitter in the relationship of the two clocks in that the FIFO is eight words deep. Upon reset the FIFO is set to operate in a half-full condition. This allows up to four input clock periods or output clock periods to occur without overflowing or under flowing the FIFO buffer.

The ratio between the information clock and the encoded clock frequencies is $4/7$ when operating with rate $7/8$ coding and parallel mode.

Coding Performance

The Q1650 decoder provides coding performance very near the theoretical limits for the optimal k=7 rate 1/3, 1/2 and 3/4 Viterbi decoder algorithm and very good performance for rate 7/8 decoding as shown in Figure 8. Coding gain of 5.5 dB is achieved when operating at a code rate of 1/3 and decoded bit error rate of 10^{-5} with a BPSK or QPSK optimal soft-decision modem. Coding gain is 5.2 dB for the same conditions when operating with rate 1/2 coding.

Performance Monitoring

The Q1650 decoder provides two powerful means of monitoring the Viterbi decoder function performance. The first technique monitors the rate at which the internal state metrics of the Viterbi algorithm increase in value. Rapidly increasing state metric values indicate that the decoder may be out of synchronization to the phase or symbol grouping associated with the input symbols. When all state metrics in the Viterbi decoder reach a certain numeric value, a normalization circuit reduces the value of all metrics by a fixed amount to prevent metric overflow.

The Q1650 device monitors the rate that these normalizations occur while decoding data. The system designer determines an acceptable normalization rate threshold and programs this threshold into the device. The designer controls both the period of time in which the metric normalization is monitored as well as the number of normalizations allowed during that time. These two numbers, which provide for more than 65,000 possible settings, are programmed into the device using the microprocessor interface. If the threshold is exceeded during any test period, a signal (OUTOFSYNC) indicates the detected loss of synchronization. In many cases, this signal can be connected to a synchronization control input pin (SYNCCHNG). In this configuration, the Q1650 decoder will try to correct the synchronization by changing the synchronization state of the decoder input and perform a retest. This technique provides a complete self-synchronizing Viterbi decoder function for a variety of communication systems with no external logic required.

The second performance monitor built into the Q1650 decoder is a channel bit error rate monitor. This

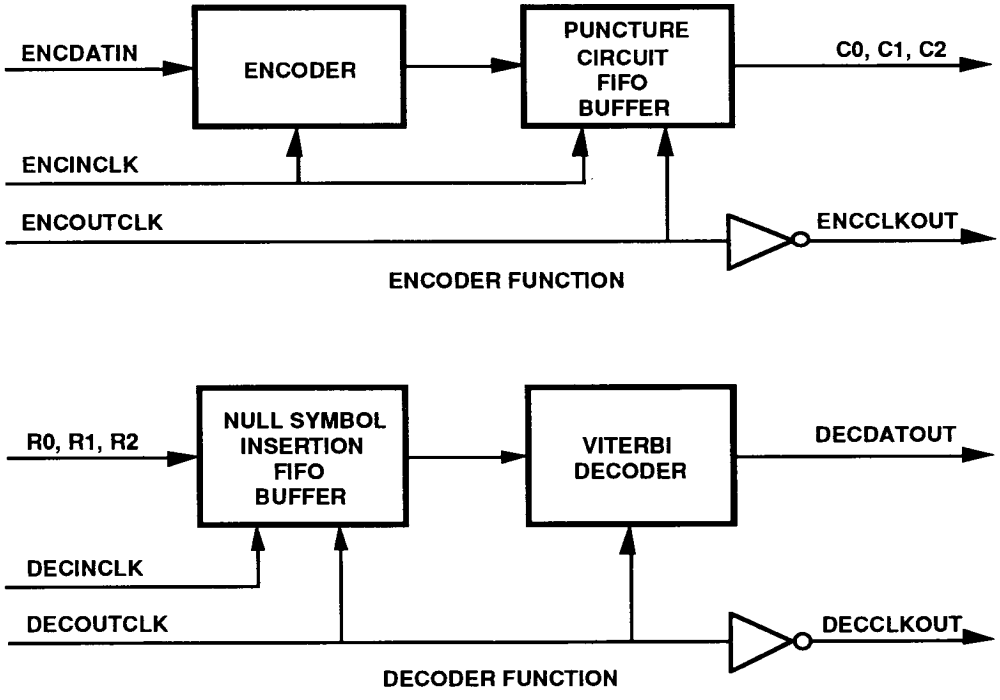


Figure 7. Q1650 Clocking Scheme

monitor works on a re-encode and compare principle as shown in Figure 9. Specifically, if a data stream {A} is first convolutionally encoded to be a data stream {A'} and then Viterbi decoded without errors injected by the transmission channel, the resulting data stream will be the original {A}. If the output data stream of the decoder were to be re-encoded with the same convolutional encoder algorithm as the original stream, then the encoded stream {A'} is again generated. Delaying the input data stream to the decoder by the exact delay associated with the Viterbi decoder and re-encoder and then comparing this delayed input with the re-encoded stream on a bit-by-bit basis will result in a constant equal comparison if the channel introduces no errors. However, if the channel introduces bit errors to the received data stream {A'}, this bit-by-bit comparison will indicate a miss whenever these channel bit errors occur. The monitor tracks the errors to generate a highly accurate estimate of the channel bit error rate (BER) . Of course, the BER monitor will also indicate errors when the decoder fails to correct an information bit error. However, the probability of an error occurring in a decoder output bit is at least two orders of magnitude below the probability of a channel error during normal operating conditions. Therefore, the effect of decoder errors on the accuracy of the BER measurement is minimal.

Synchronization

The Q1650 decoder can automatically synchronize incoming data streams to the Viterbi decoder circuit. Synchronization may require on-chip offsetting for bit, phase, and puncture pattern alignment depending on the particular mode of operation of the decoder. The synchronization technique is a two-step process. First, the decoder quality state is constantly monitored using the "state metric normalization rate" circuit described above. The user programs an "in-sync/out-of-sync" threshold for this internal circuit. The success or failure of this test for each test period is indicated on Q1650 output pins 53 (INSYNC) and 52

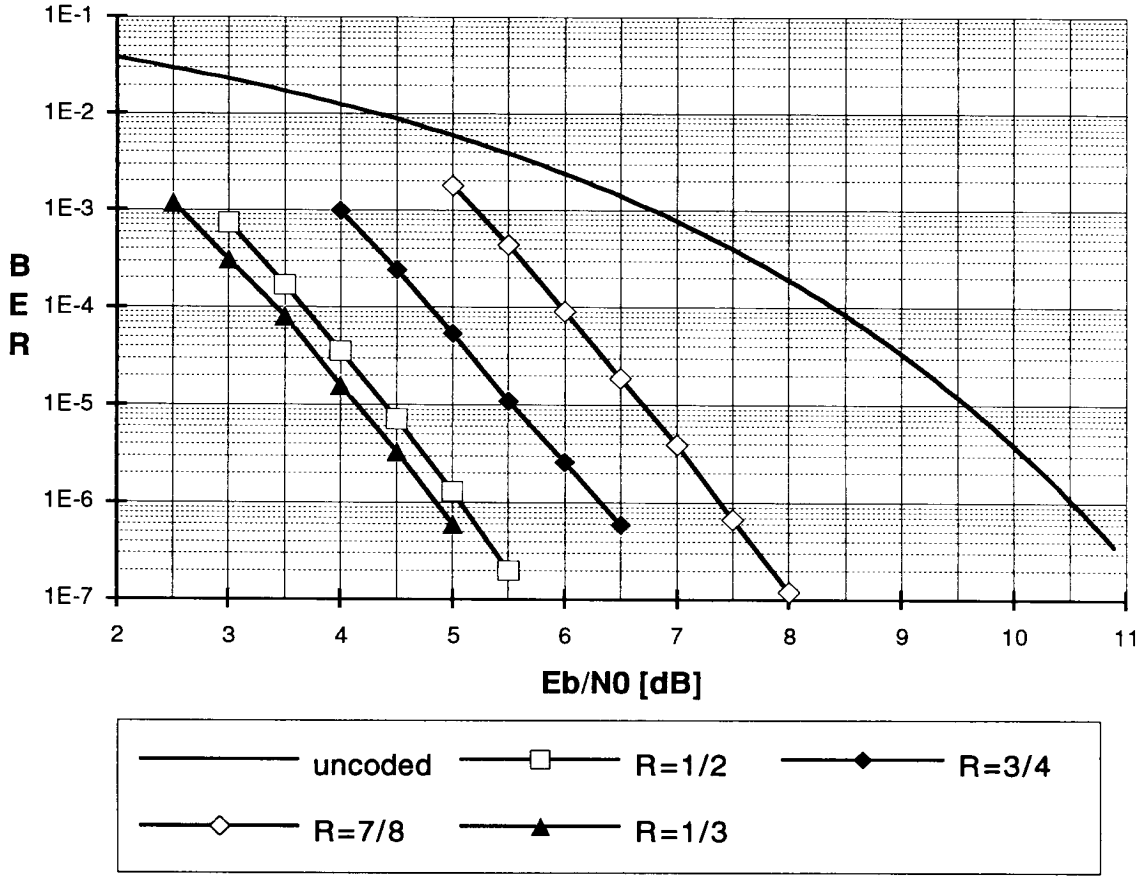


Figure 8. Q1650 Coding Performance

(OUTOFSYNC). This synchronization monitor function is operational whenever the Q1650 decoder function is processing data.

The second step of the automatic synchronization process attempts to correct an indicated out-of-sync condition by offsetting the data input to the decoder just prior to the actual decoding process. The particular offsetting technique depends on the specific mode of operation selected. In all cases, the effects of the out-of-sync condition can be compensated for either by a timing re-alignment or by permutation of the decoder input data. Wiring the OUTOFSYNC output pin (pin 52) directly to the SYNCCHNG input pin (pin 14) on the Q1650 device provides a feedback path between the synchronization monitor and the synchronization correction circuit. When an out-of-sync condition is indicated, the input processor switches synchronization state. The synchronization monitor test continues and will indicate whether the offsetting action taken by the decoder input processor has corrected the out-of-sync condition.

Some operating modes allow more than two synchronization states. If, in such cases, an out-of-sync condition is again indicated by the synchronization monitor circuit, the input processor will continue to step through all possible synchronization states. If an out-of-sync condition continues to be indicated after all possible synchronization states have been attempted, the decoder repeats the process of stepping through all the possible states until the out-of-sync indications are no longer received (i.e., an in-sync condition exists).

Descriptions of the particular synchronization states attempted for each mode of operation follow.

Decoder Input Data Formats

As seen in Figure 10, the Viterbi decoder provides the highest coding gain performance when processing multiple bit "soft-decision" values for the R0, R1, and R2 (if applicable) code words. The optimal soft-decision values are linearly quantized 3-bit values for each code word. (See QUALCOMM Application Note AN1650-2 "Setting Soft-Decision Thresholds for Viterbi Decoder Code Words from PSK Modems" for techniques on optimizing the soft decision for demodulator output samples.) The 3-bit soft-decision values can be input to the Q1650 decoder inputs (R0, R1, and R2) in either sign-magnitude or offset-binary notation. The encoding of soft-decision values for each format is given in Table 5, Q1650 Write Registers, Decoder Control Register 2. Input format selection is made via the microprocessor interface.

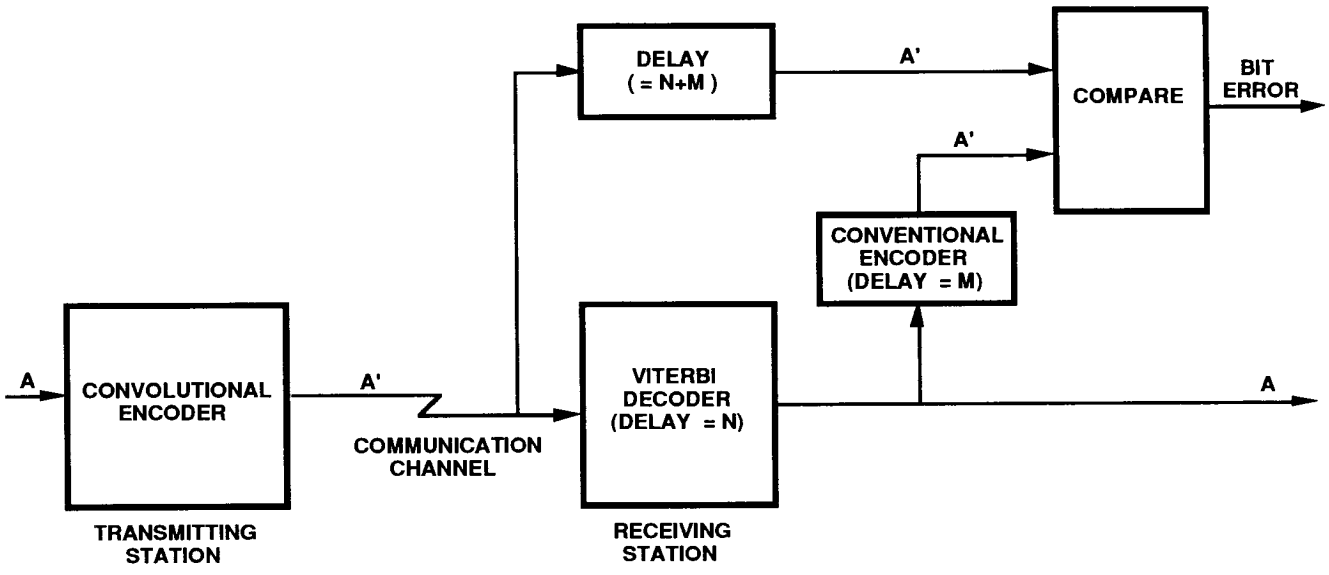


Figure 9. Re-Encode and Compare Circuit

When using the Q1650 Viterbi decoder with hard-decision (single-bit) values for R0, R1, and R2, the decoder input format should be set to sign-magnitude notation. The Rx[0] "magnitude" bits (R0[0], R1[0], and R2[0]) should be set to logic "1" (logic high). The Rx[1] "magnitude" bits (R0[1], R1[1], and R2[1]) should be set to logic "0" (logic low). The hard decision code word should be input on the "sign" signal pins (R0[2], R1[2], and R2[2]) as appropriate.

Reset Circuit Operation

The Q1650 encoder and decoder functions have individual reset inputs. A reset operation should be performed when the decoder is initially configured and when a change occurs in the mode of operation.

The reset operation can be performed using either the external input pins DECRESET (pin 13) and ENCRESET (pin 37) or reset bits in control registers of the processor interface. The operation of external input pins and processor controlled bits is identical.

When an encoder or decoder reset is asserted, either by setting the input pin to logic high or setting the processor interface bit to "1," the reset is latched synchronously into the Q1650 decoder. Both input clocks of the encoder and/or decoder must be operational during reset. The reset operation is edge-triggered, and the actual reset occurs only during the first clock periods after the reset line is asserted. Continuing to hold the reset line or bit to the logic high or "1" condition does not cause a continuous reset.

A reset affects the internal state of the puncture and synchronization circuits. Resetting the encoder circuit sets all the states of the convolutional encoder to logic "0." Resetting the decoder does not set the internal states of the path memory to a fixed value.

Monitoring Channel Bit Error Rate

The technique for monitoring the channel bit error rate (i.e., the "symbol error rate") using the internal "re-encode and compare" circuit on the decoder has been previously described in this data sheet. The bit error outputs of the re-encode and compare circuit can

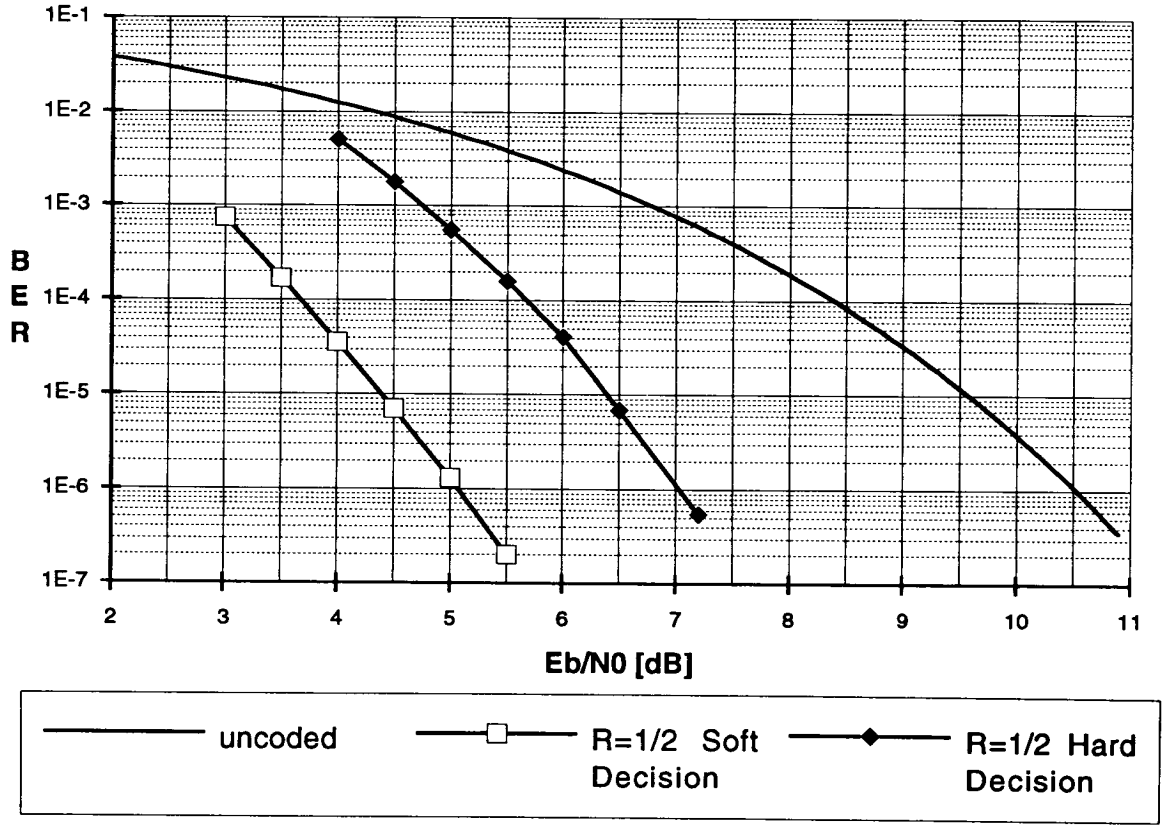


Figure 10. Hard Decision vs. Soft Decision Code Performance

be monitored either using the on-chip bit error rate (BER) monitor circuit or externally using an off-chip circuit. The on-chip BER monitor circuit is a flexible and powerful technique for determining the channel error rate. The use of an external circuit should not be required in most systems.

Figure 11 shows the functional diagram of the on-chip bit error rate measurement circuit. This circuit consists of two accumulators acting as counters. The first accumulator counts decoder input code words. The second accumulator counts code word errors detected by the re-encode and compare circuit. The period of the BER measurement is determined by the user-selectable value for the maximum count of the code word-count accumulator. This value is the two's complement 24-bit binary value entered into the Q1650 device via the processor interface. The loaded value is multiplied by 1000 to give the actual number of code words to be monitored in the BER measurement.

The BER measurement operates whenever the clock signal DECOUTCLK (pin 23) is active (i.e., toggling). During the BER measurement period, the detected errors are accumulated in the code word-error accumulator. This 16-bit binary accumulator is reset at the beginning of each BER measurement period. Once the 24-bit period of the BER measurement is entered, the loaded value is activated by writing any value to the "BER Test Value Enable" processor interface port (address 18 hex). The BER measurement is completed when the code word-count accumulator completes its count. At this point the number of detected code word errors recorded in the error-count accumulator is transferred to a parallel 16-bit buffer register.

The completion of the BER measurement period is indicated by BERDONE (pin 50), which goes to logic high for two periods of DECOUTCLK (pin 23). The BERDONE signal can be used as an interrupt or polled status bit to a controlling processor. The accumulated error value can then be read via the processor interface. The actual measured bit error count is found from the following formula: Actual Error Count = (Register Value – 1)*8, where "Register Value" is the value read from the 16-bit BER measurement register. That is, if no errors are recorded, the BER measurement register will have a value of "1" stored. If the number of errors exceeds the limit of the 16-bit register, the BER measurement will read as "0000h." The BER test continues running and stores the next test value in the 16-bit BER measurement register upon the completion of each test.

The actual symbol BER is computed by dividing the measured error quantity by the number of code words

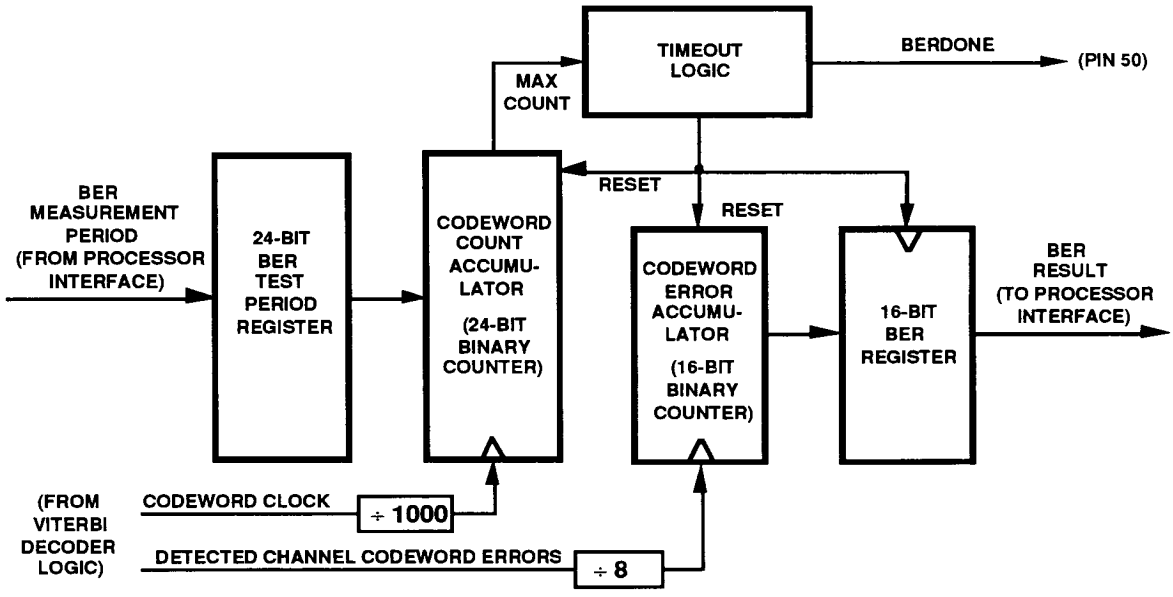


Figure 11. Bit Error Rate Measurement Circuit

in the test. This measurement division is facilitated if the measurement period is a power of 10, such as 10,000 or 100,000 code words long. In this case, the binary number recorded by the error accumulator is the mantissa of the symbol BER and the exponent of the BER value is determined by the measurement period. For example, if the test period is set to 100,000 (= 10^5) code words and 250 errors are recorded during the measurement period, the measured symbol BER is 2.5×10^{-3}.

In the event that more than 2^{19} code word errors are recorded in the measurement period, the code word error accumulator will saturate at an "all zeros" value. If this condition is indicated at the completion of a BER measurement, the period of the measurement should be reduced until a value less than saturation is recorded.

For an accurate measurement of the symbol BER, at least 100 errors should be detected within a given test period. If fewer than 100 are recorded, the statistical variance associated with such a measurement will be high. In this case, the measurement period should be increased until more than 100 code word errors are detected during the BER test.

The on-chip BER monitor can be used for measurements other than simply the symbol BER. For example, by setting the measurement period to the code word rate (i.e., code words per second), the test period becomes equal to exactly one second in time. The BER monitor therefore becomes a straightforward means for monitoring error-free seconds, which is frequently a useful error statistic. If no errors are recorded during the one second period this is an error-free second. External hardware or software can record the percentage of error-free seconds for error statistics purposes.

Data Scrambling

The Q1650 decoder includes an on-chip data scrambling circuit which can be enabled or disabled via the processor interface. Data scrambling is frequently used in conjunction with FEC techniques to guarantee minimum transition densities in the transmitted signal for purposes such as timing loop synchronization. The Q1650 device implements a specific scrambling algorithm specified in CCITT Recommendation V.35. Actually, the decoder implements two versions of the V.35 algorithm. The first version meets the letter of the CCITT specification exactly. The second version is a very slight modification of the CCITT specification which complies with a *de facto* scrambling standard used in several leading communication networks, including the INTELSAT IBS and IDR services. The details of these algorithms are described in QUALCOMM Application Note AN1650-1 "Data Scrambling Algorithms Implemented in the Q1650 Viterbi Decoder." Selection of the particular scrambling algorithm is via the microprocessor interface.

Data scrambling is performed "outside" the convolutional coding functions. That is, data scrambling, when enabled, is performed prior to differential encoding and convolutional encoding in the encoding function of the Q1650 decoder. In a symmetric manner, data descrambling is performed after data is Viterbi decoded and differentially decoded in the Q1650 decoder function.

A system consideration when designing with the data scrambling enabled is the multiplication of output bit errors from the Viterbi decoder. Error multiplication occurs because the data scrambler output bits are affected by several bits input to the descrambler. If a single bit error occurs at the output of the Viterbi decoder function the data descrambler will theoretically generate up to three output errors due to the multi-output influence of the single bit error. However, in actuality the error statistics at the output of the Viterbi decoder are such that the error multiplication is reduced to an actual factor of 1.5 to 2. This equates to a coding gain loss of only about 0.2 to 0.3 dB. This loss is an acceptable tradeoff for the advantages of the data scrambling function in many systems.

Parallel vs. Serial Data Modes

The Q1650 convolutional encoder function produces multiple encoded bits for each information input bit. This encoded data can be selected to be output in either "parallel" or "serial" data mode, as shown in Figures 12 and 13. When operating in "parallel" output mode multiple encoded bits are output during each period of the encoder output clock (ENCOUTCLK). Specifically, when operating with code rate ½ , two encoded bits are output during each period of ENCOUTCLK, when operating in either parallel or serial data mode. These two bits are the C0 and C1 encoded bits for a given information input bit. When operating in the parallel data mode these two output bits are presented at the C0 and C1 output pins during each period of ENCOUTCLK. In this case, the ENCOUTCLK frequency should be the same

as the frequency of ENCINCLK. This mode is most often used for data transmission over a channel that offers 2-bit wide transmission symbols, such as a QPSK channel. In like manner, when operating with rate 1/3 coding in the parallel mode, three encoded bits (i.e., C0, C1, and C2) are presented at the output pins C0, C1, and C2, respectively, during each period of the ENCOUTCLK signal. As with the rate 1/2 parallel operation, the frequency of ENCOUTCLK should be the same as the frequency of the ENCINCLK signal.

When operating with either of the punctured coding rates, the operation of parallel data mode differs slightly. Specifically, for operation with rate 3/4 code rate in parallel data mode, two output bits are provided during each period of the ENCOUTCLK signal at the C0 and C1 pins. These parallel outputs are two-bit symbols which have been formed from the rate 1/2 encoded bits which remain after the puncturing process. The grouping of these symbols is shown in Figure 6. Again, this mode is most commonly used when operating with transmission systems utilizing two-bit wide symbols, such as with a QPSK system. Operation with rate 7/8 coding is similar to that of rate 3/4 coding and the formation of two-bit wide symbols after the puncturing process is also shown in Figure 6. In the case of rate 3/4 parallel data mode operation the frequency of ENCOUTCLK must be set to be 2/3 the frequency of ENCINCLK.

This is because two 2-bit symbols are formed for every three input information bits. This non-integer clock multiplication must be provided with external circuitry. The frequency of the ENCOUTCLK signal must be 4/7 the frequency of ENCINCLK when operating in rate 7/8 parallel output mode.

When operating with serial output mode, all encoded bits are provided on the single output pin C0 in a bit-serial fashion at the period of the ENCOUTCLK signal. In this mode, the output data format is identical to that of the parallel mode, regardless of the code rate, except that the data is serialized before output. The first output bit for each symbol will be the C0 bit, followed by the C1 bit, and finally by the C2 bit (if operating with code rate 1/3). The Q1650 device indicates the current bit by applying a logic "1" level to output C0ACTIVE (pin 48) during output of the C0 encoded bit. Serial data mode is commonly used when operating with transmission channels that transmit a single bit during each symbol, such as with BPSK or binary optical systems.

The Q1650 decoder inputs data in either serial or parallel mode. When operating in the parallel input mode, multiple input code words are provided to the decoder during each period of the DECINCLK signal on the R0, R1, and R2 (if operating with rate 1/3 coding) inputs. The R0, R1, and R2 input values map directly to the C0, C1, and C2 output bits from the encoder. When operating in the serial mode, the decoder inputs all encoded data using only the R0 input pins. The sequence of the input code words must be the same as the sequence of the serial data output from the encoder function. The explicit location of the R0 input symbol in the input stream is indicated by setting the R0ACTIVE/signal to logic "0" during clock periods when the R0 code word is input. The relationship of the DECINCLK to DECOUTCLK frequencies is the reciprocal of the relationship of the encoder ENCINCLK to ENCOUTCLK frequencies.

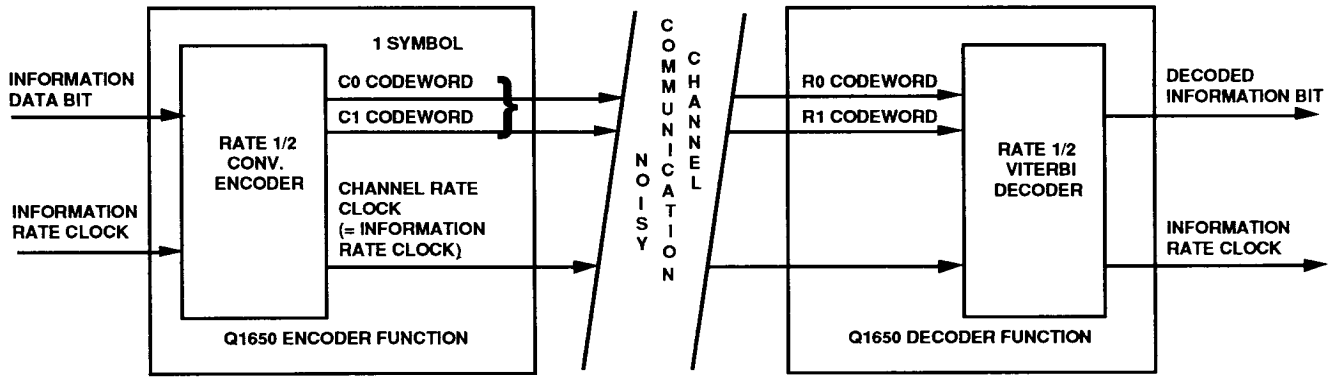


Figure 12. Parallel Data Mode

Note that when operating in the serial data input mode, all of the bits of the soft-decision decoder input code word, including the erasure bit, if used, are input during the same period of the DECINCLK signal. The "serial" mode refers to the manner by which multiple code words are input to the decoder, not to the multiple bits of the soft decision code words.

Device Throughput Delay

The input-to-output delay through the Q1650 encoder or decoder functions depends on the mode of operation selected. When operating with either rate 1/2 or 1/3 coding and parallel data input, the throughput delay of the encoder is 10 1/2 periods of the ENCINCLK clock, which is normally the same frequency as the ENCOUTCLK input signal in these modes. In these same modes the delay through the decoder is 182 1/2 periods of the DECINCLK clock, which is the same frequency as the DECOUTCLK signal, when operating in full memory mode. Operation in short memory mode reduces this decoder throughput delay to 102 1/2 clock periods. These throughput delay values are the same for operation in both direct and peripheral modes. These delays will increase by one clock each if the data scrambler or descrambler is enabled.

With serial data operation, the delay in terms of the input clocks will be approximately the same as when using parallel data mode. However, the exact relation between the input and output clock phasing will increase or decrease the throughput delay by as much as one clock period.

When operating with the built-in puncture coding modes (rate 3/4 or 7/8), the throughput delay of the encoder and decoder varies with the exact synchronization state. This uncertainty can be as much as ±4 periods of the clock due to the varying delay in the internal Q1650 FIFO buffers.

Full vs. Short Memory Chainback

The Viterbi decoder function of the Q1650 device can be selected to operate with one of two chainback path depths. "Full" chainback memory operation provides a minimum chainback depth of 96 states while "short" chainback memory operation provides a minimum chainback depth of 48 states. Operation with code rates 1/3 or 1/2 will result in near theoretical coding performance when either full or short chainback depth is selected. Operation with short chainback depth reduces the throughput delay of the decoder function. However, when operating with code rates higher than rate 1/2 (e.g., rate 3/4 or 7/8) the decoder should be operated with full chainback memory in order to provide maximum coding gain. The determination of the chainback depth is selected with bit 0 in the Decoder Control Register 3 of the processor interface.

Normalization Rate Monitor Operation (Synchronization Status Monitor)

As previously described, the Q1650 decoder includes a circuit for monitoring the rate at which state metric normalizations occur. This "normalization rate" monitoring is a useful technique for determining when the decoder is not in synchronization with the phase

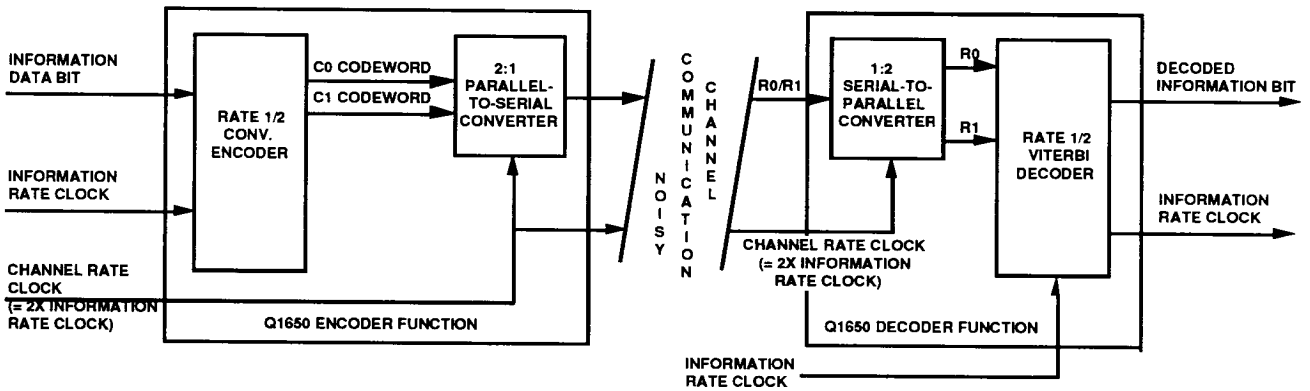


Figure 13. Serial Data Mode

ambiguity, code word grouping, or puncture pattern sequence. In fact, the outputs of the normalization rate monitor circuit are two signals, OUTOFSYNC and INSYNC. The system designer selects the allowed normalization rate (percentage) above which the decoder will indicate an out-of-sync condition.

Figure 14 shows the functional diagram of the on-chip normalization circuit. This circuit consists of two counters, similar in operation to the channel BER monitor previously described. The system designer controls the periods of these two counters. The first counter (T) measures the number of decoded bits. The second counter (N) measures the number of state metric normalizations. The normalization rate threshold is determined by taking the ratio of the count of normalizations (the N counter) and the time period (the T counter). Each of these 8-bit wide binary counters is pre-loaded using the processor interface registers. Both the N and T counters are loaded with binary values which are the two's complement of the actual count value. The count value loaded into the T counter is multiplied by 256 to determine the actual number of decoded bits in the normalization test period.

The actual count of the N counter is determined by the following formula: n=(N-1)*8+4, where "n" is the actual number of normalizations allowed, and "N" is the two's complement value of the 8-bit number loaded into the N counter. With this programming capability, the system designer selects the normalization rate threshold for determining an in-sync or out-of-sync condition as well as the period of the measurement. For example, when operating with rate $1/2$ decoding, a normalization rate threshold of about 10% will reliably detect a loss of synchronization.

To avoid false detection of synchronization loss due to a noise burst, the normalization measurement should detect at least 20-30 normalizations before declaring a loss of synchronization. As an example, the system designer may select the number of normalizations to be detected to be approximately 50. By loading the 8-bit two's complement value of seven (i.e., 0F9h) into the N counter register, the actual number of normalizations allowed in a test period without indicating a loss of synchronization would be (7-1)*8+4 = 52. The value for the T counter must be approximately ten times the value in the N counter; that is, loading the T counter with the two's complement value of 2 (i.e., 0FEh) the actual count value for T will be (2*256) = 512. Therefore, the actual normalization rate threshold will be $52/512$ = 10.2%. This is an appropriate threshold for reliable synchronization when operating with rate $1/2$ coding. The threshold should be set to approximately 1.7% for rate $3/4$ coding and 0.8% for rate $7/8$ coding. For rate 3/4, programming the N counter to 7 (i.e., 0F9h) and the T counter to 12 (i.e., 0F4h) will give the desired normalization rate of 1.7%. Likewise, for rate 7/8, programming the N counter to 8 (i.e., 0F8h) and the T counter to 29 (i.e., 0E3h) will give the desired normalization rate of 0.8%.

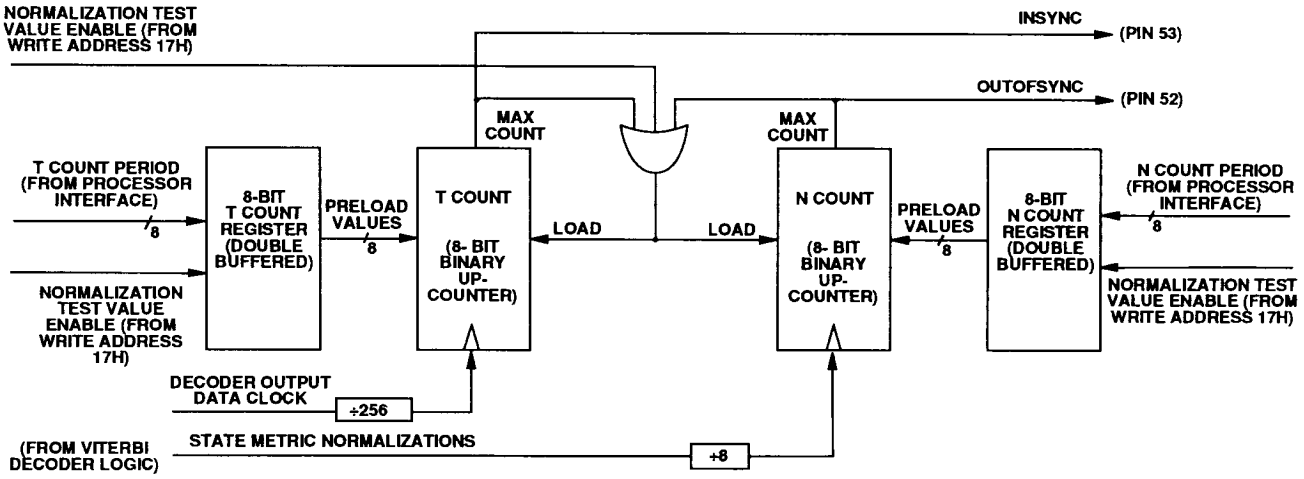


Figure 14. Normalization Rate Monitor Circuit

Direct vs. Peripheral Data Mode Operation

The Q1650 decoder interfaces data via dedicated signal pins or via the processor interface. The Direct Data mode interfaces all data via the dedicated pins and is most commonly used with synchronous data channels. The Peripheral Data mode interfaces all data signals, including the R0, R1, and R2 inputs and the C0, C1, and C2 outputs, via processor interface registers. This mode is used when the Q1650 device is used as an error control peripheral to the processor system. When operating in Peripheral Data mode the functions of the ENCDATIN (pin 33), ENCINCLK (pin 36), ENCOUTCLK (pin 44), ENCRESET (pin 37), R0 (pins 29, 26, 18), R1 (pins 28, 22, 17), R2 (pins 27, 19, 16), R0ERASE (pin 32), R1ERASE (pin 31), R2ERASE (pin 30), DECINCLK (pin 11), and DECOUTCLK (pin 23), and DECRESET (pin 13) signals are provided by writing to port addresses. In this mode all the above pins should be connected to logic "0." The selection of the Direct or Peripheral Data mode is made by setting bit 3 in both Encoder Control Register 2 and Decoder Control Register 2 of the processor interface. (1 = Peripheral, 0 = Direct).

When the Q1650 device operates in the peripheral mode, each data bit handled by either the encoder or the decoder requires four processing steps. First, the input data to the encoder or decoder is written to the appropriate register using the processor interface (see tables 2 through 5). Second, the processor controlled activation of ENCINCLK or DECINCLK is performed by writing to the appropriate processor interface address. Third, processor controlled activation of ENCOUTCLK or DECOUTCLK is performed by writing to the appropriate processor interface address. Finally, the output data is read from the appropriate register. This cycle repeats for each bit processed by the Q1650 decoder.

MODES OF OPERATION

The Q1650 device can operate in one of four internally generated code rates without external circuitry other than that required to generate the clock signals for the particular mode selected. The code rate of the on-chip encoder function can be selected to be different than that of the decoder function. In addition to the basic code rate selection, the Q1650 device supports various user-selected additional operational functions and modes. The selection of the mode of operation is made using the control registers of the processor interface as described below. The following paragraphs described the functions performed and the design considerations associated with each mode. Table 1 shows all possible combinations of the various modes and identifies the synchronization parameters adjusted by the decoder's internal synchronization circuit (when enabled).

Code Rate ½ Mode Operation

When operating with code rate ½ , two encoded bits (C0 and C1) are generated by the encoder for every information bit. Likewise, two encoded symbols are input to the decoder for every information bit output from the decoder. The encoded bits from the encoder can be output on two signal pins (C0 and C1) at the same clock frequency as the input data when operating in the parallel data mode. Alternatively, both the C0 and C1 encoded bits can be output from the same signal pin (specifically the C0 pin) at two times the frequency of the input information when in serial data mode.

The decoder's operation is similar to that of the encoder, in that the input code words can be input in a parallel fashion with both code words (R0 and R1) input during one period of the DECINCLK clock or serially in two periods of DECINCLK.

The synchronization states differ between the parallel and serial input modes of rate ½ operation. When operating with parallel input data the synchronization states of the decoder function assume operation with a QPSK demodulation system. In these types of systems the C0 code word of the rate ½ encoded output is commonly transmitted on the in-phase or quadrature channel of the QPSK modulator, while the C1 code word is transmitted on the remaining channel. In this case, the synchronization state machine on the Q1650 decoder must resolve one of two possible values. The initial synchronization state, upon device reset, connects the R0 code word inputs to the internal R0 data lines and the R1 code word inputs to the R1 data lines. This is referred to as the "normal" synchronization state. When the synchronization state of the Q1650 decoder changes due to the assertion of the SYNCCHNG signal the "alternate" synchronization state occurs in which the R0 code word input is used internally as the R1 code word and *vice versa*. In addition, this mode inverts the R0 value.

The alternate synchronization state offsets the effects of a 90 degree phase ambiguity associated

with QPSK demodulators. A QPSK demodulator actually can synchronize in one of four phase states. However, two of the four states are related to the other two in that they are inversions of both the R0 and R1 values. The effects of this data inversion can be offset by enabling the on-chip differential encoder and decoder circuits on the Q1650 decoder.

Thus, the Q1650 device need only differentiate between the "normal" and the "alternate" synchronization states in order to provide synchronization to QPSK demodulators as long as the differential decoder function is enabled, or some other means is provide by the system to offset the effects of the inversion of the data. When operating in rate 1/2 parallel data mode and Offset QPSK (OQPSK) modulation systems an additional step is required when in the alternate synchronization state. In this case, the R1 input data is delayed by a single period of the DECINCLK signal prior to the "swap and invert" of the alternate synchronization state described for QPSK demodulators. This delay is useful for correcting the time offset of the in-phase (I) and quadrature (Q) channels of the OQPSK system.

When operating with rate 1/2 coding and serial input data mode, the Q1650 decoder does not adjust for the phase ambiguity, but simply the symbol grouping of the input serial code words. That is, since the two code words for the rate 1/2 encoded symbol are input one at a time the Q1650 decoder must group these inputs prior to the actual decoding process. The input symbols can be grouped (paired) in one of two ways. Only one pairing sequence is correct, that is pairing the R0 input code word with the next input, which would be the associated R1 code word. However, if the Q1650 decoder is not provided with explicit information as to which input is the R0 code word (i.e., if the signal R0ACTIVE is not used), the code word pairings may incorrectly group the R1 input of an encoded symbol with the next input, which would be the R0 code word from the next symbol. In this case, the automatic synchronization circuit will detect the incorrect alignment and the assertion of the SYNCCHNG signal will adjust the input symbol stream by stopping the input grouping circuit for a single period of the DECINCLK signal, resulting in the correct pairing of code words. This technique requires that the C0 code word for a given encoded symbol always be transmitted immediately prior to the C1 code word of the same symbol. When operating the Q1650 encoder function in serial data mode this is the sequence in which code words are output on the C0 signal.

Code Rate 1/3 Mode Operation

Operation with code rate 1/3 is similar in function to the rate 1/2 operation just described, except that three code words are generated by the encoder for each input information bit. When operating with code rate 1/3 and parallel data input mode at the decoder, the synchronization circuit does not affect the data. Data input to the decoder in this mode must be in the correct sequence and input on the correct R0, R1, and R2 inputs. However, the on-chip differential decoder can be enabled to offset the inversion of the data which may occur in such systems as a BPSK transmission network. When operating with rate 1/3 coding in serial data mode the decoder will group the input code words in a triplet grouping. If the SYNCCHNG signal is used to correct this code word grouping the decoder will adjust the grouping by stopping the serial-to-parallel conversion process internally for a single period of DECINCLK. In this mode there are three possible synchronization states. It is required that the input sequence to the decoder be the R0, R1, and finally the R2 input code word for each given symbol. This is the order in which the serialized code words C0, C1, and C2 are output from the encoder when operating in serial data mode.

Code Rate 3/4 or 7/8 Mode Operation (Internal Puncture Mode)

Operation with the internal puncture code rates is similar to rate 1/2 operation except that the possible synchronization states increase due to the ambiguity with the pattern of the puncture process. When operating with either code rate 3/4 or 7/8 with automatic synchronization enabled, the decoder first performs either the phase ambiguity resolution process (when operating in parallel data mode) or the code word pairing process (when operating in serial input data mode). Next, the paired code words are processed by a "null"-symbol insertion circuit that must correctly insert the null symbols in the place where code words were erased at the encoder. When operating with code rate 3/4 this additional synchronization process adds a factor of two to the number of possibly correct synchronization states for a total of four possibly correct states. When operating with code rate 7/8, the puncture pattern can have one of four possible states; thus eight synchronization states are possible. The Q1650 decoder synchronization circuit attempts each possible state

Table 1. Q1650 Modes of Operation

			Control Register Bits								See Notes Next Pg	
Code Rate	Data Mode	Modu-lation	R 1/2	R 1/3	R 3/4	R 7/8	SERIAL ENABLE	OQPSK	PHASE SYNC	SWAP ERASE	Int Sync Method	Erase Bit Sync
1/2	Ser	BPSK	1	0	0	0	1	–	–	0	1	N/A
1/2	Par	QPSK	1	0	0	0	0	0	0	0	2	A
			1	0	0	0	0	0	0	1	2	B
			1	0	0	0	0	0	1	0	3	A
			1	0	0	0	0	0	1	1	3	B
1/2	Par	OQPSK	1	0	0	0	0	1	0	0	4	A
			1	0	0	0	0	1	0	1	4	C
			1	0	0	0	0	1	1	0	5	A
			1	0	0	0	0	1	1	1	5	C
1/3	Ser	BPSK	0	1	0	0	1	–	–	0	1	N/A
	Par	–	0	1	0	0	0	–	–	0	6	N/A
3/4	Par	QPSK	0	0	1	0	0	0	0	0	7	A
			0	0	1	0	0	0	0	1	7	B
			0	0	1	0	0	0	1	0	3	A
			0	0	1	0	0	0	1	1	3	B
3/4	Par	OQPSK	0	0	1	0	0	1	0	0	8	A
			0	0	1	0	0	1	0	1	8	C
			0	0	1	0	0	1	1	0	5	A
			0	0	1	0	0	1	1	1	5	C
7/8	Par	QPSK	0	0	0	1	0	0	0	0	7	A
			0	0	0	1	0	0	0	1	7	B
			0	0	0	1	0	0	1	0	3	A
			0	0	0	1	0	0	1	1	3	B
7/8	Par	OQPSK	0	0	0	1	0	1	0	0	8	A
			0	0	0	1	0	1	0	1	8	C
			0	0	0	1	0	1	1	0	5	A
			0	0	0	1	0	1	1	1	5	C

NOTES

Internal Synchronization Methods

1. Shifts input grouping pattern by one code word.
2. Edge actuation of SYNCCHNG signal toggles between alternate decoder input mapping states:
   State 1: $R0_N$ -->$R0_N$, $R1_N$--> $R1_N$
   State 2: $R0_N$ -->$R1_N$/, $R1_N$--> $R0_N$
3. Level activation of SYNCCHNG signal forces one of two decoder input mapping states:
   State 1 (SYNCCHNG = 0): $R0_N$ -->$R0_N$, $R1_N$--> $R1_N$
   State 2 (SYNCCHNG = 1): $R0_N$ -->$R1_N$/, $R1_N$--> $R0_N$
4. Edge actuation of SYNCCHNG signal toggles one of two decoder input mapping states:
   State 1: $R0_N$ -->$R0_N$, $R1_N$--> $R1_N$
   State 2: $R0_N$ -->$R1_N$/, $R1_{N-1}$--> $R0_N$
5. Level actuation of SYNCCHNG signal forces one of two decoder input mapping states:
   State 1 (SYNCCHNG = 0): $R0_N$ -->$R0_N$, $R1_N$--> $R1_N$
   State 2 (SYNCCHNG = 1): $R0_N$ -->$R1_N$/, $R1_{N-1}$--> $R0_N$
6. No internal synchronization control is provided; SYNCCHNG signal should be tied to logic 0.
7. Edge actuation of SYNCCHNG performs the same operation as synchronization method 2. In addition, the puncture code pattern is shifted by one state every other activation of SYNCCHNG.
8. Edge actuation of SYNCCHNG performs the same operation as synchronization method 4. In addition, the puncture code pattern is shifted by one state every other activation of SYNCCHNG.

Erase Bit Synchronization

A. R0ERASE and R1ERASE inputs follow R0 and R1 data signal synchronization methods.
B. R0ERASE and R1ERASE inputs do not follow R0 and R1 data signal synchronization methods.
C. R0ERASE input is not affected by synchronization methods. R1ERASE is delayed by one input code word when in synchronization state 2.

in sequence. The synchronization state changes each time the SYNCCHNG input is asserted. Synchronization of the puncture pattern sequence can be explicitly controlled while in parallel data input mode. Automatic synchronization mode should be disabled by connecting SYNCCHNG (pin 14) to logic "0." The R2ERASE signal (pin 30) indicates the clock period just prior to the first code word pair of the rate 3/4 or 7/8 puncture pattern. With either code rate, the first code word pair of the sequence is the pair in which the C0 and C1 bits are from the same rate 1/2 code word pair as shown in Figure 6. The R2ERASE signal should be set to logic "1" just once after chip reset during the period of DECINCLK prior to input of the first code word pair. R2ERASE should be set to logic "0" after this initial synchronization. The first symbol pair output from the encoder is indicated by an active high state at the C2 (pin 42) output when operating in rate 3/4 or 7/8 mode.

Higher Code Rate Operation Using External Puncturing Mode

The Q1650 encoder and decoder can encode and decode punctured code rates other than the rate 3/4 and 7/8 code implemented internally. Operation with these other codes requires the use of external puncture and null-symbol insertion circuits. The Q1650 decoder function includes symbol erasure inputs for the R0, R1, and R2 code words which are used to indicate a null-symbol to the decoder. When operating with an external puncture code synchronization for both phase ambiguity effects and the puncture pattern are typically performed using external circuitry.

TECHNICAL SPECIFICATIONS

Processor Interface

The on-chip processor interface of the Q1650 device allows a processor to set the operational mode and monitor the internal status of the device. The interface includes an 8-bit wide data bus, a 5-bit wide address bus, and read enable, write enable, and chip select lines. This interface will operate with most major microprocessor and signal processor families without wait state logic. It can also be used to write and read data to and from the encoder and decoder functions. In this mode, the Q1650 decoder operates as a single-chip FEC peripheral to the processor system.

The Q1650 processor interface has four read registers and 21 write registers. Not all registers are required in every operational mode.

Tables 2 and 3 show the memory maps of the read and write registers, while Tables 4 and 5 describe the functions of each register and bit in detail.

Table 2. Q1650 Read Registers Memory Map

ADDRESS DEC	ADDRESS HEX	DATA BITS D7	D6	D5	D4	D3	D2	D1	D0
		Decoder Data Output Register							
00	00	Rsvd	Rsvd	R0EOUT/ EOUT	Rsvd	R2ERR/ R1EOUT	R1ERR	R0ERR	DECDAT-OUT
		Encoder Data Output Register							
02	02	Rsvd	Rsvd	Rsvd	Rsvd	C0ACTIVE	C2	C1	C0
		BER Measurement LS Byte Output Register							
03	03	Bit 7 (MS)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LS)
		BER Measurement MS Byte Output Register							
04	04	Bit 7 (MS)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LS)

Table 3. Q1650 Write Registers Memory Map

ADDRESS DEC	ADDRESS HEX	D7	D6	D5	D4	D3	D2	D1	D0
		Decoder Data Input Register 1							
00	00	R0-ERASE	R0[2]	R0[1]	R0[0]	R1-ERASE	R1[2]	R1[1]	R1[0]
		Decoder Data Input Register 2							
01	01	R2-ERASE	R2[2]	R2[1]	R2[0]	Set to 0	Set to 0	Set to 0	Set to 0
		Decoder Control Register 1							
02	02	Set to 0	Set to 0	RATE 7/8	RATE 1/3	RATE 3/4	RATE 1/2	OQPSK	MODE SELECT
		Decoder Control Register 2							
03	03	Set to 0	DESCR MODE	DESCR ENABLE	DIFF DEC ENABLE	PERIPR/ DIRECT	SWAP ERASE	PHASE SYNC	SMG/OBN
		Decoder Control Register 3							
04	04	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	S/W DEC RESET	Set to 0	FUL/SHT MEM
		Encoder Data Input Register							
05	05	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	ENCDATIN
		Encoder Control Register 1							
06	06	Set to 0	Set to 0	RATE 7/8	RATE 1/3	RATE 3/4	RATE 1/2	S/W ENC RESET	SER/PAR MODE
		Encoder Control Register 2							
07	07	Set to 0	SCRAMB MODE	SCRAMB ENABLE	DIFF ENC ENABLE	BUS/PIN MODE	Set to 0	Set to 0	Set to 0
		Normalization Test Bit Count Input Register							
08	08	TCOUNT Bit 7 (MS)	TCOUNT Bit 6	TCOUNT Bit 5	TCOUNT Bit 4	TCOUNT Bit 3	TCOUNT Bit 2	TCOUNT Bit 1	TCOUNT Bit 0 (LS)
		Normalization Test Normalize Count Input Register							
09	09	NCOUNT Bit 7 (MS)	NCOUNT Bit 6	NCOUNT Bit 5	NCOUNT Bit 4	NCOUNT Bit 3	NCOUNT Bit 2	NCOUNT Bit 1	NCOUNT Bit 0 (LS)

Table 3. Q1650 Write Registers Memory Map (continued)

ADDRESS DEC	ADDRESS HEX	D7	D6	D5	D4	D3	D2	D1	D0
		BER Period Input Register LS Byte							
10	0A	BERPER Bit 7	BERPER Bit 6	BERPER Bit 5	BERPER Bit 4	BERPER Bit 3	BERPER Bit 2	BERPER Bit 1	BERPER Bit 0 (LS)
		BER Period Input Register CS Byte							
11	0B	BERPER Bit 15	BERPER Bit 14	BERPER Bit 13	BERPER Bit 12	BERPER Bit 11	BERPER Bit 10	BERPER Bit 9	BERPER Bit 8
		BER Period Input Register MS Byte							
12	0C	BERPER Bit 23 (MS)	BERPER Bit 22	BERPER Bit 21	BERPER Bit 20	BERPER Bit 19	BERPER Bit 18	BERPER Bit 17	BERPER Bit 16
		Processor Decoder Input Clock Register							
14	0E	DECINCLK Bit 7	DECINCLK Bit 6	DECINCLK Bit 5	DECINCLK Bit 4	DECINCLK Bit 3	DECINCLK Bit 2	DECINCLK Bit 1	DECINCLK Bit 0
		Processor Decoder Output Clock Register							
15	0F	DECOUT-CLK Bit 7	DECOUT-CLK Bit 6	DECOUT-CLK Bit 5	DECOUT-CLK Bit 4	DECOUT-CLK Bit 3	DECOUT-CLK Bit 2	DECOUT-CLK Bit 1	DECOUT-CLK Bit 0
		Processor Encoder Input Clock Register							
17	11	ENCINCLK Bit 7	ENCINCLK Bit 6	ENCINCLK Bit 5	ENCINCLK Bit 4	ENCINCLK Bit 3	ENCINCLK Bit 2	ENCINCLK Bit 1	ENCINCLK Bit 0
		Processor Encoder Output Clock Register							
18	12	ENCOUT-CLK Bit 7	ENCOUT-CLK Bit 6	ENCOUT-CLK Bit 5	ENCOUT-CLK Bit 4	ENCOUT-CLK Bit 3	ENCOUT-CLK Bit 2	ENCOUT-CLK Bit 1	ENCOUT-CLK Bit 0
		Reserved Registers							
21	15	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0
22	16	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0
		Normalization Test Value Enable Register							
23	17	NTVE Bit 7	NTVE Bit 6	NTVE Bit 5	NTVE Bit 4	NTVE Bit 3	NTVE Bit 2	NTVE Bit 1	NTVE Bit 0
		BER Test Value Enable Register							
24	18	BERTVE Bit 7	BERTVE Bit 6	BERTVE Bit 5	BERTVE Bit 4	BERTVE Bit 3	BERTVE Bit 2	BERTVE Bit 1	BERTVE Bit 0

NOTES
1. Write registers 0Dh, 10h, 13h, and 14h are not used.
2. All bits that are specified as "Set to 0" or "Set to 1" must be set to 0 or 1 for proper operation.
3. **Reserved write registers 15h and 16h must be set to 0 for correct operation.**

Table 4. Q1650 Read Registers

READ ADDRESS 00H: DECODER DATA OUTPUT REGISTER

BIT	NAME	FUNCTION	Same Function as Input Pin
0	DECDATOUT	Decoder data output	56
1	R0ERR	Bit-by-bit indication of detected channel bit errors for R0	70
2	R1ERR	Bit-by-bit indication of detected channel bit errors for R1	69
3	R2ERR/R1EOUT	If: Code rate set to 1/3 Then: Provides bit-by-bit indication of detected channel bit errors for R2. If: Code rate not set to 1/3 Then: Provides R1ERASE delayed to align with R1ERR.	68
4	–	Reserved	–
5	R0EOUT/EOUT	If: Code rate set to 1/3 Then: Provides logic OR of R0ERASE, R1ERASE, and R2ERASE delayed to align with R0ERR, R1ERR, and R2ERR outputs. If: Code rate not set to 1/3 Then: Provides R0ERASE delayed to align with R0ERR.	63
6-7	–	Reserved	–

READ ADDRESS 02H: ENCODER DATA OUTPUT REGISTER

BIT	NAME	FUNCTION	Same Function as Input Pin
0	C0	Encoder symbol C0	40
1	C1	Encoder symbol C1	41
2	C2	Encoder symbol C2 for code rate 1/3 – OR – "1" indicates output of first symbol of puncture pattern for code rates 3/4 and 7/8	
3	C0ACTIVE	In serial data mode, indicates C0 code word is active.	48
4-7	–	Reserved	–

READ ADDRESS 03H: BER MEASUREMENT LS BYTE OUTPUT REGISTER

BIT	NAME	FUNCTION
0-7	BER LS BYTE	Least significant eight bits of the 16-bit result of the internal bit error rate measurement. Bit 0 is LSB.

READ ADDRESS 04H: BER MEASUREMENT MS BYTE OUTPUT REGISTER

BIT	NAME	FUNCTION
0-7	BER MS BYTE	Most significant eight bits of the 16-bit result of the internal bit error rate measurement. Bit 0 is LSB.

Table 5. Q1650 Write Registers

WRITE ADDRESS 00H: DECODER DATA INPUT REGISTER 1

BIT	NAME	CONTROL/INPUT	Same Function as Input Pin
0	R1[0]	LSB of decoder R1 input symbol	28
1	R1[1]	CSB of decoder R1 input symbol	22
2	R1[2]	MSB of decoder R1 input symbol	17
3	R1ERASE	1 erases the R1 symbol	31
4	R0[0]	LSB of decoder R0 input symbol	29
5	R0[1]	CSB of decoder R0 input symbol	26
6	R0[2]	MSB of decoder R0 input symbol	18
7	R0ERASE	1 erases the R0 symbol	32

WRITE ADDRESS 01H: DECODER DATA INPUT REGISTER 2

BIT	NAME	ACCEPTS	Same Function as Input Pin
0-3	–	Set to 0	–
4	R2[0]	LSB of decoder R2 input symbol	27
5	R2[1]	CSB of decoder R2 input symbol	19
6	R2[2]	MSB of decoder R2 input symbol	16
7	R2ERASE	If: Code rate set to 1/3 Then: 1 erases the R2 symbol If: Code rate set to 3/4 or 7/8 Then: 1 directly synchronizes decoder puncture pattern	30

WRITE ADDRESS 02H: DECODER CONTROL REGISTER 1

BIT	NAME	FUNCTION
0	Decoder Input Mode Selection	1 puts decoder in serial data input mode. 0 puts decoder in parallel data input mode. See *Parallel vs. Serial Data Modes* for more information.
1	OQPSK	If: Decoder set to parallel data mode Code rate set to 1/2, 3/4, or 7/8 Phase sync enabled Then: 1 makes sync circuit adjust for phase ambiguities of OQPSK demodulators 0 makes sync circuit adjust for phase ambiguities of QPSK demodulators
2	Decoder Rate 1/2 Enable	1 makes decoder operate with code rate 1/2.
3	Decoder Rate 3/4 Enable	1 makes decoder operate with code rate 3/4. For rate 3/4 mode, connect the unused R0ERASE and R1ERASE input pins to logic 0.
4	Decoder Rate 1/3 Enable	1 makes decoder operate with code rate 1/3.
5	Decoder Rate 7/8 Enable	1 makes decoder operate with code rate 7/8. For rate 7/8 mode, connect the unused R0ERASE and R1ERASE input pins to logic 0.
6-7	–	Set to 0

Table 5. Q1650 Write Registers (continued)

WRITE ADDRESS 03H: DECODER CONTROL REGISTER 2

BIT	NAME	FUNCTION
0	SMG/OBN	0 makes decoder accept offset-binary notation soft-decision inputs at R0, R1, R2. 1 makes decoder accept sign-magnitude notation soft-decision inputs at R0, R1, R2. The following table describes the offset-binary and sign-magnitude data input encoding formats for the soft decision decoder.
1	PHASE SYNC ENA	If: The decoder is set to parallel mode, code rate 1/2, 3/4, or 7/8 Then: A "0" causes the decoder sync state to toggle on every rising edge of SYNCCHNG. A "1" causes the sync state to toggle depending on the input to SYNCCHNG (level triggered). If SYNCCHNG is "0", the decoder will be in the "Normal" state. When SYNCCHNG is "1" , the decoder will be in the "Swap & Invert" state. (Phase ambiguity automatic synchronization makes the decoder's automatic synchronization circuits perform symbol "swap-and-invert" operations to synchronize to the PSK phase ambiguities.)
2	SWAP ERASE ENA	If: PHASE SYNC ENA enabled, parallel data input, code rate 1/2, and external symbol erasure. Then: 1 internally "swaps" R0ERASE and R1ERASE with the R0 and R1 data. 0 disables "swapping" input signals R0ERASE and R1ERASE with the data.
3	DECODER PERIPHERAL/ DIRECT DATA MODE	1 makes decoder use processor bus interface for data input/output (peripheral mode). See *Processor Bus Interface* section of *Q1650 Pin Functions* table. 0 makes decoder use dedicated I/O pins for data input/output (direct data mode). See *Decoder I/O Pins* in *Q1650 Pin Functions* table. Signals affected: R0[0-2], R1[0-2], R2[0-2], R[0-2]ERASE, DECDATOUT.
4	DIFF DEC ENA	1 enables the differential decoder; 0 disables the differential decoder. (The setting of this bit does not affect the operation of the differential encoder.)
5	DESCRAMB ENA	1 enables the V.35 data descrambler; 0 disables the V.35 data descrambler. (The setting of this bit does not affect the operation of the V.35 data scrambler .)
6	DESCRAMB MODE	If: V.35 data descrambler enabled Then: 1 makes the data descrambler use the exact algorithm specified by CCITT V.35. 0 makes the data descrambler use a slightly modified CCITT algorithm preferred by most systems, including INTELSAT. (See QUALCOMM application note AN1650-1.)
7	–	Set to 0

	Encoding Format					
	Offset Binary			Sign-Magnitude		
R0[x], R1[x], or R2[x] Bit:	[2]	[1]	[0]	[2]	[1]	[0]
Strongest 1:	1	1	1	1	1	1
	1	1	0	1	1	0
	1	0	1	1	0	1
Weakest 1:	1	0	0	1	0	0
Weakest 0:	0	1	1	0	0	0
	0	1	0	0	0	1
	0	0	1	0	1	0
Strongest 0:	0	0	0	0	1	1

Table 5. Q1650 Write Registers (continued)

WRITE ADDRESS 04H: DECODER CONTROL REGISTER 3

0	FULL/SHORT MEMORY	1 makes the Viterbi decoder algorithm use a minimum chainback path depth of 96 states. 0 makes the Viterbi decoder algorithm use a minimum chainback path depth of 48 states.
1	–	Set to 0
2	S/W DECODER RESET	A transition from "0" to "1" resets decoder functions (similar to pin 13). Connect pin 13 to logic "0" when using this software-controlled reset. Bit 2 should be set to "0" when using the DECRESET pin.
3-7	–	Set to 0

WRITE ADDRESS 05H: ENCODER DATA INPUT REGISTER

BIT	NAME	FUNCTION
0	ENCDATIN	If: Encoder peripheral mode enabled Then: Accepts encoder data (same function as pin 33)
1-7	–	Set to 0

WRITE ADDRESS 06H: ENCODER CONTROL REGISTER 1

BIT	NAME	FUNCTION
0	Encoder Output Mode Selection	1 puts encoder in serial data output mode; 0 puts encoder in parallel data output mode. See *Parallel vs. Serial Data Modes* for more information.
1	S/W ENCODER RESET	A transition from "0" to "1" resets decoder functions (similar to pin 37). Connect pin 37 to logic "0" when using this software-controlled reset. Bit 1 should be set to "0" when using the ENCRESET pin.
2	Encoder Rate 1/2 Enable	1 makes encoder operate with code rate 1/2.
3	Encoder Rate 3/4 Enable	1 makes encoder operate with code rate 3/4.
4	Encoder Rate 1/3 Enable	1 makes encoder operate with code rate 1/3.
5	Encoder Rate 7/8 Enable	1 makes encoder operate with code rate 7/8.
6-7	–	Set to 0

Table 5. Q1650 Write Registers (continued)

WRITE ADDRESS 07H: ENCODER CONTROL REGISTER 2

BIT	NAME	FUNCTION
0-2	–	Set to 0
3	ENCODER PERIPHERAL/ DIRECT DATA MODE	1 makes encoder use processor bus interface for data input/output (peripheral mode). See *Processor Bus Interface* section of *Q1650 Pin Functions* table. 0 makes encoder use I/O pins for data input/output (direct data mode). See *Encoder I/O Pins* in *Q1650 Pin Functions* table. Signals affected: ENCDATAIN, C0, C1, C2.
4	DIFF ENC ENA	1 enables differential encoder; 0 disables differential encoder. (The setting of this bit does not affect the operation of the differential decoder.)
5	SCRAMB ENA	1 enables the V.35 data scrambler; 0 disables the V.35 data scrambler. (The setting of this bit does not affect the operation of the V.35 data descrambler.)
6	SCRAMB MODE	If: V.35 data scrambler enabled Then: 1 makes the data scrambler use the exact algorithm specified by CCITT V.35. 0 makes the data scrambler use a slightly modified CCITT algorithm preferred by most systems, including INTELSAT. (See QUALCOMM application note AN1650-1.)
7	–	Set to 0

WRITE ADDRESS 08H: NORMALIZATION TEST BIT COUNT INPUT REGISTER

BIT	NAME	FUNCTION
0-7	T COUNT (Bit 0 is LSB)	Determines the length of the synchronization monitor test; requires an eight-bit value. See *Normalization Rate Monitor Operation* for more information.

WRITE ADDRESS 09H: NORMALIZATION TEST NORMALIZE COUNT INPUT REGISTER

BIT	NAME	FUNCTION
0-7	N COUNT (Bit 0 is LSB)	Determines the normalization threshold level for the synchronization monitor test; requires an eight-bit value. See *Normalization Rate Monitor Operation* for more information.

WRITE ADDRESS 0AH: BER PERIOD INPUT REGISTER LS BYTE

BIT	NAME	FUNCTION: Determines BER Period
0-7	BER PERIOD LS Byte (Bit 0 is LSB.)	LS byte of 24-bit (three byte) value of period of on-chip bit error rate monitor. See *Monitoring Channel Bit Error Rate* for more information.

WRITE ADDRESS 0BH: BER PERIOD INPUT REGISTER CS BYTE

BIT	NAME	FUNCTION: Determines BER Period
0-7	BER PERIOD CS Byte (Bit 0 is LSB.)	CS byte of 24-bit (three byte) value of period of on-chip bit error rate monitor. See *Monitoring Channel Bit Error Rate* for more information.

Table 5. Q1650 Write Registers (continued)

WRITE ADDRESS 0CH: BER PERIOD INPUT REGISTER MS BYTE

BIT	NAME	FUNCTION: Determines BER Period
0-7	BER PERIOD MS Byte (Bit 0 is LSB.)	MS byte of 24-bit (three byte) value of period of on-chip bit error rate monitor. See *Monitoring Channel Bit Error Rate* for more information.

WRITE ADDRESS 0EH: PROCESSOR DECODER INPUT CLOCK REGISTER

BIT	NAME	FUNCTION
0-7	DECINCLK (software-controlled)	Generates (when given any value) a single DECINCLK clock cycle. Connect pin 11 (DECINCLK) to logic 0 when using this software-controlled clock.

WRITE ADDRESS 0FH: PROCESSOR DECODER OUTPUT CLOCK REGISTER

BIT	NAME	FUNCTION
0-7	DECOUTCLK (software-controlled)	Generates (when given any value) a single DECOUTCLK clock cycle. Connect pin 23 (DECOUTCLK) to logic 0 when using this software-controlled clock.

WRITE ADDRESS 11H: PROCESSOR ENCODER INPUT CLOCK REGISTER

BIT	NAME	FUNCTION
0-7	ENCINCLK (software-controlled)	Generates (when given any value) a single ENCINCLK clock cycle. Connect pin 36 (ENCINCLK) to logic 0 when using this software-controlled clock.

WRITE ADDRESS 12H: PROCESSOR ENCODER OUTPUT CLOCK REGISTER

BIT	NAME	FUNCTION
0-7	ENCOUTCLK (software-controlled)	Generates (when given any value) a single ENCOUTCLK clock cycle. Connect pin 44 (ENCOUTCLK) to logic 0 when using this software-controlled clock.

WRITE ADDRESS 17H: NORMALIZATION TEST VALUE ENABLE REGISTER

BIT	NAME	FUNCTION
0-7	Norm Test Values Enable (software-controlled)	Performs two functions (when given any value): 1) Enables the values previously loaded into these registers: Normalization Test Bit Count Register (write address 08H) Normalization Test Normalize Count Register (write address 09H) . 2) Restarts the normalization rate test.

WRITE ADDRESS 18H: BER TEST VALUE ENABLE REGISTER

BIT	NAME	FUNCTION
0-7	BER Test Values Enable (software-controlled)	Performs two functions (when given any value): 1) Enables the value previously loaded into the BER Period Register (three bytes–write addresses 0Ah, 0Bh 0Ch). 2) Restarts the BER test.

NOTES
1. Write registers 0Dh, 10h, 13h, and 14h are not used.
2. All bits that are specified as "Set to 0" or "Set to 1" must be set to 0 or 1 for proper operation.
3. **Reserved write registers 15h and 16h must be set to 0 for correct operation.**

Pin Descriptions

The following describes the functions and operation of the input and output pins of the Q1650. Figure 15 shows the locations of the pins; Table 6 describes the function of each pin.

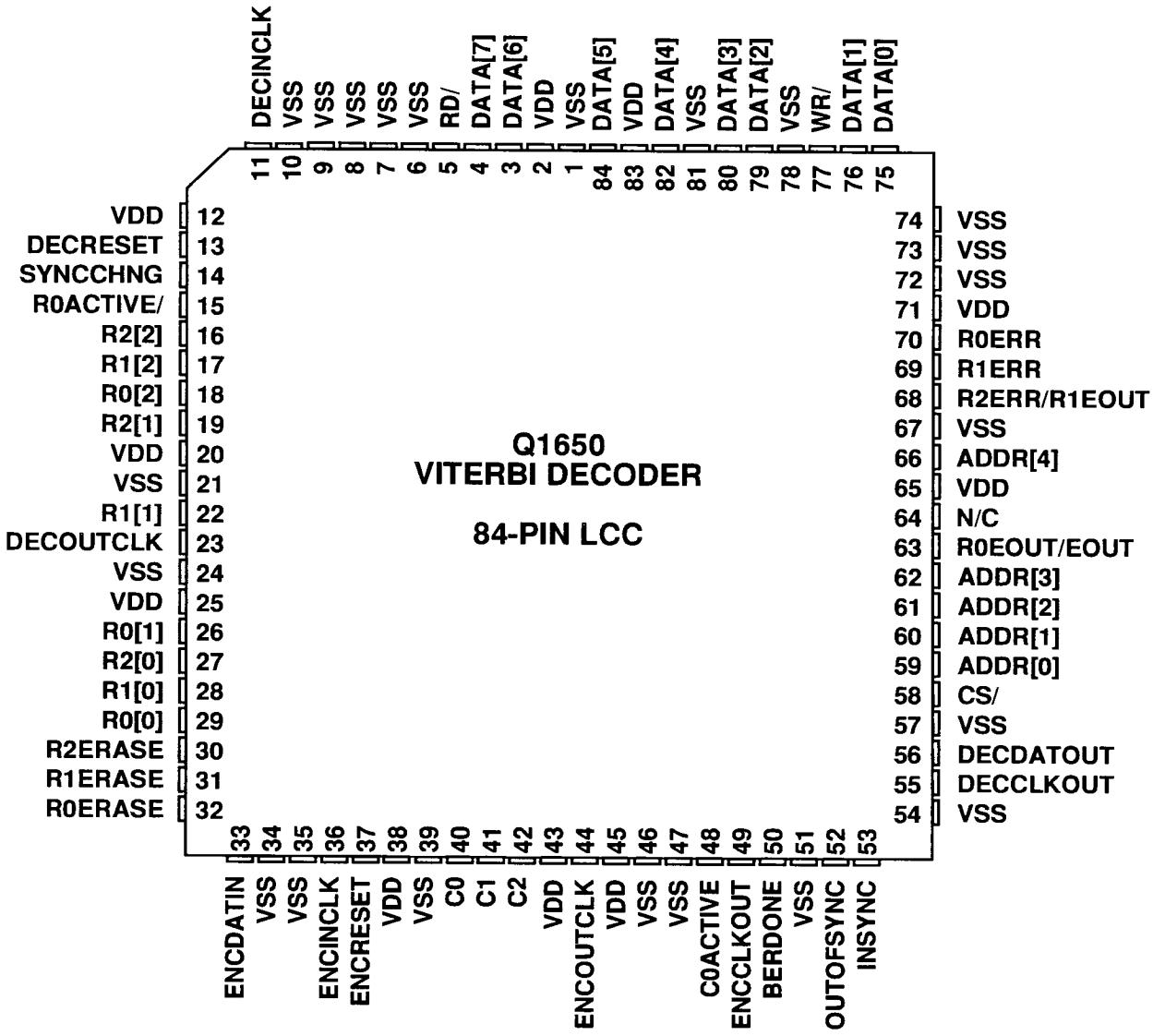


Figure 15. Q1650 Pinout Diagram

Table 6. Q1650 Pin Functions

	Name	Pins	Type	Function (Notes on following page)
Encoder I/O Pins	ENCDATIN	33	Input	Encoder data input
	ENCINCLK	36	Input	Encoder data input clock
	ENCOUTCLK	44	Input	Encoder symbol output clock
	ENCCLKOUT	49	Output	Encoder symbol clock output
	C0ACTIVE	48	Output	Indicates output of C0 bit (Note 1)
	C0	40	Output	Encoder symbol C0 (Note 2)
	C1	41	Output	Encoder symbol C1
	C2	42	Output	Encoder symbol C2 (Note 3)
	ENCRESET	37	Input	Master encoder reset (active high)
Decoder I/O Pins	R0[0], R0[1], R0[2]	29 (LSB), 26, 18	Input	Decoder R0 input symbol (Note 4)
	R1[0], R1[1], R1[2]	28 (LSB), 22, 17	Input	Decoder R1 input symbol
	R2[0], R2[1], R2[2]	27 (LSB), 19, 16	Input	Decoder R2 input symbol (Note 5)
	R0ACTIVE/	15	Input	Low selects R0 as input (Note 6)
	R0ERASE	32	Input	High erases R0 symbol (Note 13)
	R1ERASE	31	Input	High erases R1 symbol (Note 13)
	R2ERASE	30	Input	High erases R2 symbol (Notes 13 and 14)
	DECINCLK	11	Input	Decoder symbol input clock
	DECOUTCLK	23	Input	Decoder data output clock
	DECCLKOUT	55	Output	Decoder data clock output
	DECRESET	13	Input	High master resets decoder circuitry
	SYNCCHNG	14	Input	Decoder sync change control (active high)
	OUTOFSYNC	52	Output	Sync monitor test failure (Note 7)
	INSYNC	53	Output	Sync monitor test pass (Note 8)
	DECDATOUT	56	Output	Decoder data output
	R0ERR	70	Output	Indicates channel bit errors of R0 (Note 9)
	R1ERR	69	Output	Indicates channel bit errors of R1 (Note 9)
	R2ERR/R1EOUT	68	Output	Indicates channel bit errors (Notes 9 and 10)
	R0EOUT/EOUT	63	Output	Indicates error signal timing (Note 11)
Processor Bus Interface Pins	DATA[0]–DATA[7]	75, 76,79, 80, 82, 84, 3, 4	I/O	Processor interface data bus (DATA[0] is LSB)
	ADDR[0]–ADDR[4]	59 (LSB) , 60, 61, 62, 66	Input	Processor interface address bus
	WR/	77	Input	Processor interface write strobe (active low)
	RD/	5	Input	Processor interface read strobe (active low)
	CS/	58	Input	Processor interface chip select (active low)
	BERDONE	50	Output	BER test indicator (Note 12)
Voltage Supply Pins	VDD (+5V)	2, 12, 20, 25, 38, 43, 45, 65, 71, 83	Power	
	VSS	1, 6–10, 21, 24, 34, 35, 39, 46, 47, 51, 54, 57, 67, 72, 73, 74, 78, 81	Ground	
	N/C	64	Unused	Make no connection to this pin.

NOTES (for table 6)

1. In serial mode, pin 48 is active high during the period of ENCCLKOUT when the C0 encoded bit is output.
2. In serial mode, pin 40 serves as the encoder output for all output symbols.
3. In rate 3/4 or 7/8, pin 42 is active high during output of first symbol of puncture pattern.
4. In serial mode, pins 29, 26, and 18 serve as the decoder input for all input symbols.
5. Decoder R2 (input pins 27, 19, 16) is used only for rate 1/3 parallel operation.
6. In serial mode, a low on pin 15 indicates the symbol at R0 is the current decoder input symbol.
7. Pin 52 pulses high for two periods of DECCLKOUT when the internal synchronization monitor test fails.
8. Pin 53 pulses high for two periods of DECCLKOUT when the internal synchronization monitor test passes.
9. Pins 70, 69, and 68 indicate channel bit errors bit-by-bit for R0, R1, and R2, respectively (active high for one period of DECCLKOUT).
10. Rate 1/3: Pin 68 indicates channel bit errors. Rate 1/2: Pin 68 indicates R1ERASE delayed to align to R1ERR output.
11. Rate 1/3: Pin 63 indicates logic OR of R0ERASE/R1ERASE/R2ERASE delayed to align with R0ERR/R1ERR/R2ERR. Rate 1/2: Pin 63 indicates R0ERASE delayed to align with R0ERR.
12. Pin 50 indicates completion of internal bit error rate measurement test (active high).
13. The R0ERASE (pin 32), R1ERASE (pin 31), and R2ERASE (pin 30) erase inputs must be connected to logic "0" when symbol erasures are not being used. Symbol erasure inputs are used to implement punctured code rates other than the rate 3/4 and 7/8 patterns implemented internally on the device.
14. When operating the decoder in rate 3/4 or 7/8, the R2ERASE input (pin 30) can be used to synchronize the puncture pattern. Refer to Code Rate 3/4 or 7/8 Operation on page 23 of the Technical Data Sheet.

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Storage Temperature	T_S	-65	+150	°C
Operating Temperature (Comm)	T_A	0	+70	°C
Operating Temperature (Mil)	T_A	-55	+125	°C
Junction Temperature	T_J		+150	°C
Voltage on any Input Pin		-0.3	Vdd+0.3	V
Voltage on Vdd and on any Output Pin		-0.3	+7.0	V
DC Input Current	I_{IN}	-10	+10	µA

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	4.75	5.25	V	
High-Level Input Voltage	V_{IH}	2.0	Vdd+0.3	V	
Low-Level Input Voltage	V_{IL}	-0.3	0.8	V	
Input Leakage Current	I_{IL}	-1.0	-	µA	V_{IN} = 0V, V_{DD} = $V_{DD(MAX)}$
Input Leakage Current	I_{IH}	-	1.0	µA	V_{IN} = V_{DD} = $V_{DD(MAX)}$
High-Level Output Voltage (1)	V_{OH}	V_{DD} -1.0	–	V	I_{OH} = -16 mA
Low-Level Output Voltage (1)	V_{OL}	–	0.4	V	I_{OL} = 16 mA
High-Level Output Voltage (2)	V_{OH}	V_{DD} -1.0	-	V	I_{OH} = -8 mA
Low-Level Output Voltage (2)	V_{OL}	–	0.4	V	I_{OL} = 8 mA
High-Level Output Voltage (3)	V_{OH}	V_{DD} -1.0	-	V	I_{OH} = -1.6 mA
Low-Level Output Voltage (3)	V_{OL}	–	0.4	V	I_{OL} = 1.6 mA
Output Short Circuit Current (4)	I_{OS}	-	300	mA	
Output Capacitance	C_{OUT}	-	10	pF	
Power Dissipation (Quiescent)	P_D	–	0.1	W	
Power Dissipation (@10 MHz)	P_D	–	0.8	W	

NOTES
1. For DECCLKOUT, DECDATOUT, R0ERR, R1ERR, and DATA[0-7] outputs
2. For BERDONE, INSYNC, and OUTOFSYNC outputs
3. For all other outputs
4. Not more than one output shorted at a time for less than one second

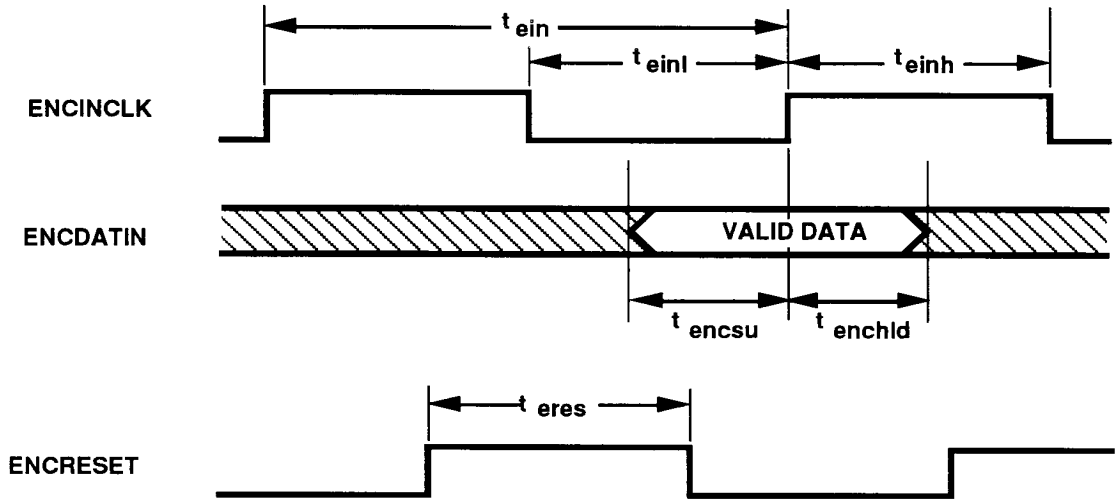
Timing

The following figures provide the timing specifications for all versions of the Q1650 device. These specifications are valid only for the recommended operating conditions:

Commercial: $0^oC \le T_A \le +70^oC$, $4.75V \le V_{DD} \le 5.25V$

Mil Screened (Q1650M-2L): $-55^oC \le T_A \le +125^oC$, $4.5V \le V_{DD} \le 5.5V$

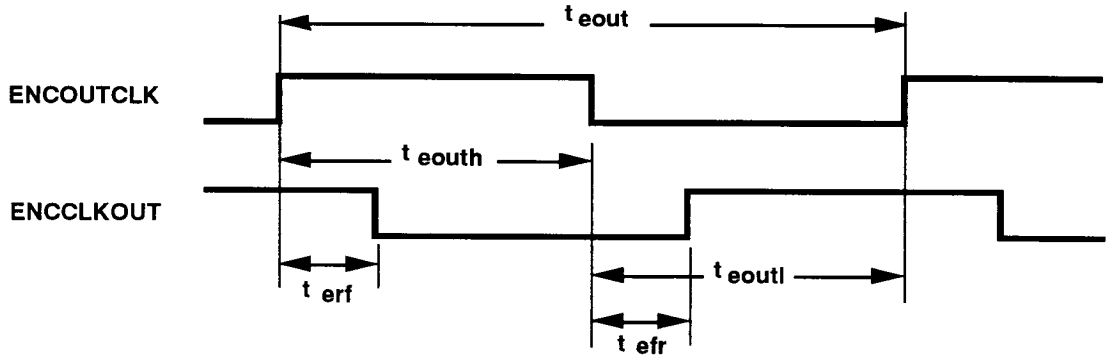
Encoder Data Input Timing



		Q1650C-1N		Q1650C-2N		Q1650M-2L		Q1650C-3N		
Signal	Description	Min	Max	Min	Max	Min	Max	Min	Max	Units
ENCINCLK	Max Frequency (=1/tein)	–	2.5	–	10	–	10	–	25	MHz
tein	ENCINCLK period	400	–	100	–	100	–	40	–	ns
tencsu	ENCDATIN setup to ENCINCLK rise	10	–	10	–	10	–	10	–	ns
tenchld	ENCDATIN hold after ENCINCLK rise	5	–	5	–	5	–	5	–	ns
teinl	ENCINCLK low period	160	–	40	–	40	–	16	–	ns
teinh	ENCINCLK high period	160	–	40	–	40	–	16	–	ns
teres	Minimum reset period	*	–	*	–	*	–	*	–	ns

*The minimum value is $2 \bullet ECLK_{MAX}$, where $ECLK_{MAX}$ = the period of ENCINCLK or ENOUTCLK, whichever is greater.

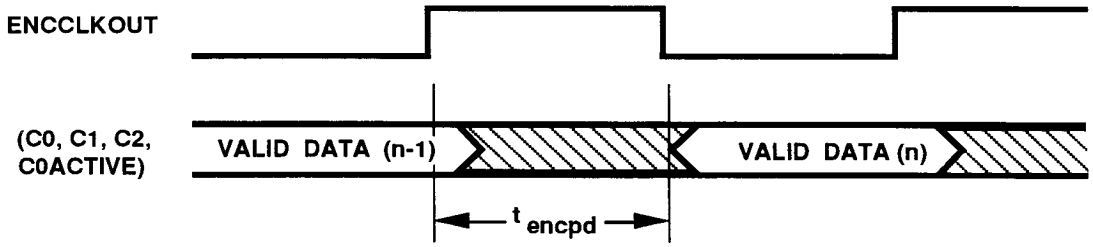
Encoder Clock Timing



		Q1650C-1N		Q1650C-2N		Q1650M-2L		Q1650C-3L		
Signal	Description	Min	Max	Min	Max	Min	Max	Min	Max	Units
ENCOUTCLK	Max Frequency (=1/teout)	–	7.5*	–	30*	–	30*	–	25**	MHz
teout	ENCOUTCLK minimum period	133	–	33	–	33	–	40	–	ns
teoutl	ENCOUTCLK low period	53	–	15	–	15	–	16	–	ns
teouth	ENCOUTCLK high period	53	–	15	–	15	–	16	–	ns
terf***	ENCOUTCLK rise to ENCCLKOUT fall	0	12	0	12	0	15	0	12	ns
tefr***	ENCOUTCLK fall to ENCCLKOUT rise	0	12	0	12	0	15	0	12	ns

* Maximum frequency for rate 1/3 serial mode.
** Maximum frequency for rate 1/3 serial mode TBD.
*** Values assume a 25 pF load on the output pin.

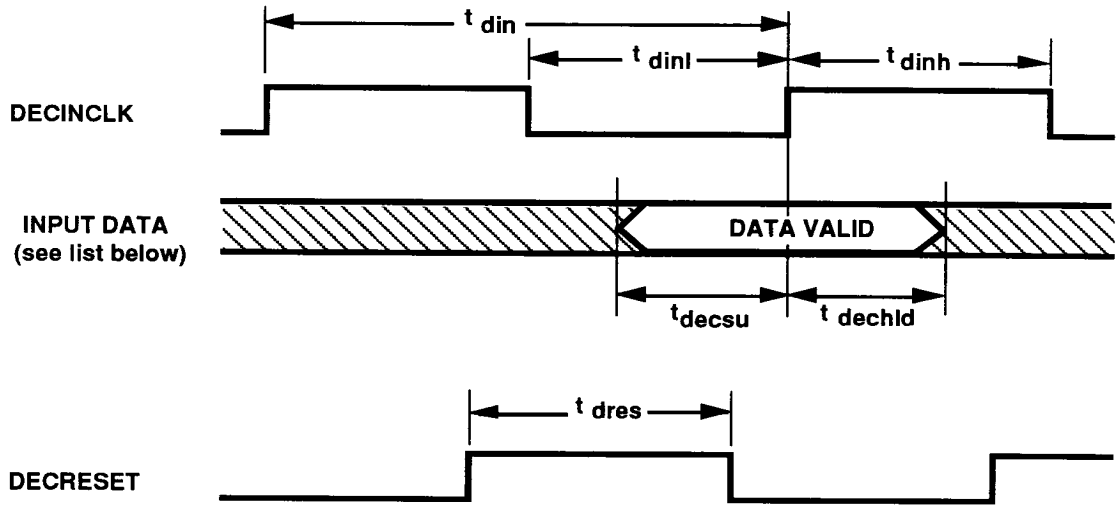
Encoder Data Output Timing



		Q1650C-1N		Q1650C-2N		Q1650M-2L		Q1650C-3L		
Signal	Description	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{encpd}	Data valid after clock output rising	1	18	1	18	1	18	1	18	ns

NOTE: Values assume a 25 pF load on the output data pin.

Decoder Data Input Timing

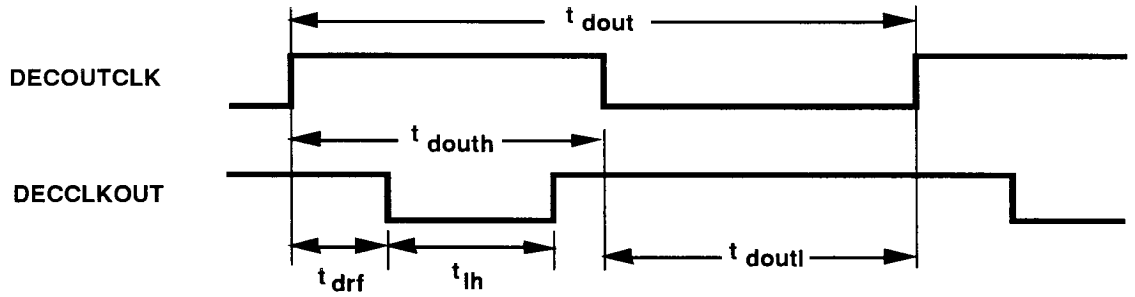


Input data includes: R0[0] R0[1] R0[2] R0ERASE R0ACTIVE/
R1[0] R1[1] R1[2] R1ERASE SYNCCHNG
R2[0] R2[1] R2[2] R2ERASE

		Q1650C-1N		Q1650C-2N		Q1650M-2L		Q1650C-3L		
Signal	Description	Min	Max	Min	Max	Min	Max	Min	Max	Units
DECINCLK	Max Frequency (=1/tdin)	–	7.5*	–	30*	–	30*	–	25**	MHz
tdin	Minimum period	133	–	33	–	33	–	40	–	ns
tdecsu	Data setup to DECINCLK rise	10	–	10	–	10	–	10	–	ns
tdechld	Data hold after DECINCLK rise	5	–	5	–	5	–	5	–	ns
tdinl	DECINCLK low period	53	–	15	–	15	–	16	–	ns
tdinh	DECINCLK high period	53	–	15	–	15	–	16	–	ns
tdres	Minimum reset period	***	–	***	–	***	–	***	–	ns

* Maximum frequency for rate 1/3 serial mode
** Maximum frequency for rate 1/3 serial mode TBD
*** The minimum value is 2•$DCLK_{MAX}$, where $DCLK_{MAX}$ = the period of DECINCLK or DECOUTCLK, whichever is greater.

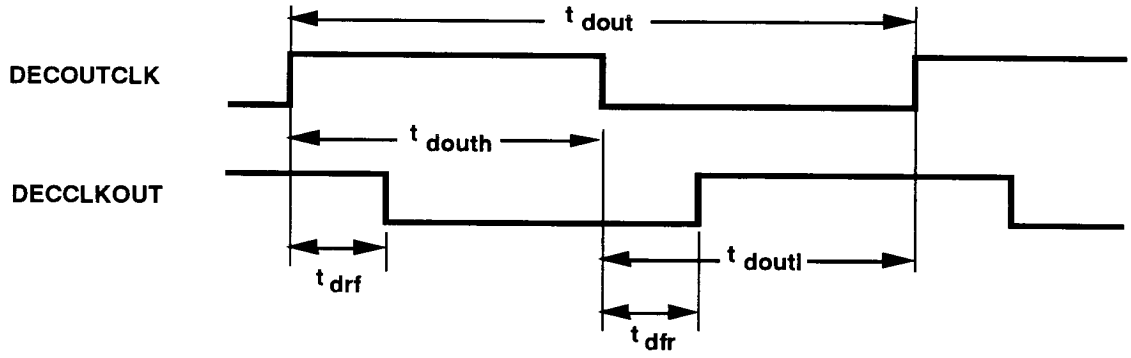
Decoder Clock Timing (Q1650-1)



		Q1650C-1N		
Signal	Description	Min	Max	Units
DECOUTCLK	Max Frequency (=1/tdout)	–	2.5	MHz
tdout	DECOUTCLK minimum period	400	–	ns
tdoutl	DECOUTCLK low period	160	–	ns
tdouth	DECOUTCLK high period	160	–	ns
tdrf	DECOUTCLK rise to DECCLKOUT fall*	0	35	ns
tlh	DECCLKOUT fall to DECCLKOUT rise*	10	-	ns

*Values assume a 25 pF load on the output pin.

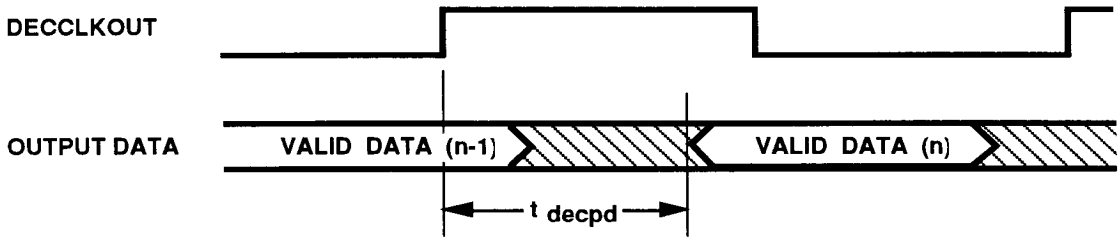
Decoder Clock Timing (Q1650-2, -3)



		Q1650C-2N		Q1650M-2L		Q1650C-3L		
Signal	Description	Min	Max	Min	Max	Min	Max	Units
DECOUTCLK	Max Frequency (=1/tdout)	–	10	–	10	–	25	MHz
tdout	DECOUTCLK minimum period	100	–	100	–	40	–	ns
tdoutl	DECOUTCLK low period	40	–	40	–	16	–	ns
tdouth	DECOUTCLK high period	40	–	40	–	16	–	ns
tdrf	DECOUTCLK rise to DECCLKOUT fall*	0	20	0	23	0	20	ns
tdfr	DECOUTCLK fall to DECCLKOUT rise*	0	20	0	23	0	20	ns

*Values assume a 25 pF load on the output pin.

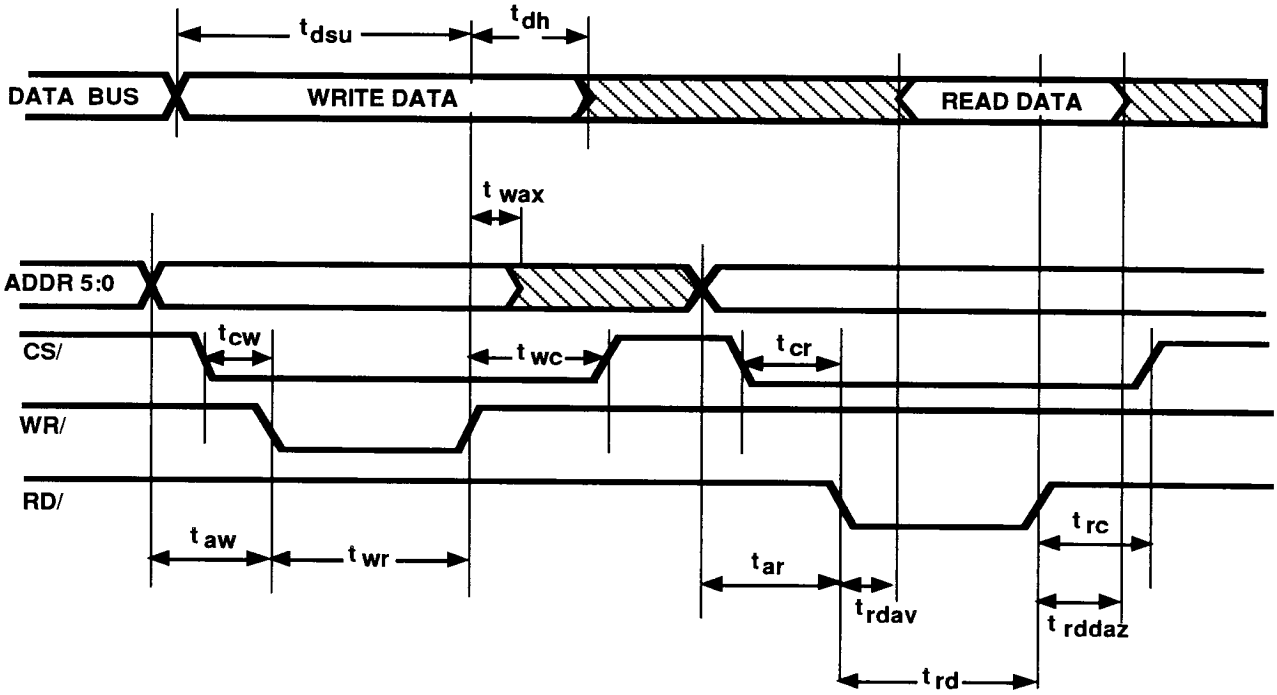
Decoder Data Output Timing



		Q1650C-1N		Q1650C-2N		Q1650M-2L		Q1650C-3L		
Signal	Description	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{decpd}	Data valid after output clock rising	-	40	1	18	1	18	1	18	ns

NOTES
1. Values assume a 25 pF load on the output data pin.
2. Output data includes R0ERR, R1ERR, R2ERR/R1EOUT, R0EOUT/EOUT, DECDATOUT, INSYNC, OUTOFSYNC, BERDONE.

Processor Interface Timing



Write Signal	Description	Q1650C-1N Min	Q1650C-1N Max	Q1650C-2N Min	Q1650C-2N Max	Q1650M-2L Min	Q1650M-2L Max	Q1650C-3L Min	Q1650C-3L Max	Units
t_{dsu}	Data setup to WR/ rising	20	–	20	–	20	–	20	–	ns
t_{dh}	Data hold after WR/ rising	5	–	5	–	5	–	5	–	ns
t_{cw}	CS/ falling to WR/ falling	15	–	15	–	15	–	15	–	ns
t_{wax}	Address hold after WR/ rising	5	–	5	–	5	–	5	–	ns
t_{wc}	CS/ hold after WR/ rising	5	–	5	–	5	–	5	–	ns
t_{aw}	Address valid to WR/ falling	20	–	20	–	20	–	20	–	ns
t_{wr}	WR/ period	80	–	80	–	80	–	80	–	ns

Read Signal	Description	Q1650C-1N Min	Q1650C-1N Max	Q1650C-2N Min	Q1650C-2N Max	Q1650M-2L Min	Q1650M-2L Max	Q1650C-3L Min	Q1650C-3L Max	Units
t_{ar}	Address valid to RD/ falling	20	–	20	–	20	–	20	–	ns
t_{rd}	RD/ period	80	–	80	–	80	–	80	–	ns
t_{cr}	CS/ falling to RD/ falling	15	–	15	–	15	–	15	–	ns
t_{rc}	CS/ hold after RD/ rising	5	–	5	–	5	–	5	–	ns
t_{rdav}	RD/ falling to DATA valid	60	–	60	–	60	–	60	–	ns
t_{rddaz}	Data hold after RD/ rising	0	–	0	–	0	–	0	–	ns

PLCC Packaging (Q1650C-1N and Q1650C-2N)

The Q1650C-1N and Q1650C-2N devices are packaged in an 84-pin plastic leaded chip carrier (PLCC) (figure 16). A suggested socket is AMP P/N 821573-1 (through-hole board mounted) or P/N 822151-5 (surface mounted). Dimensions are given in inches (mm).

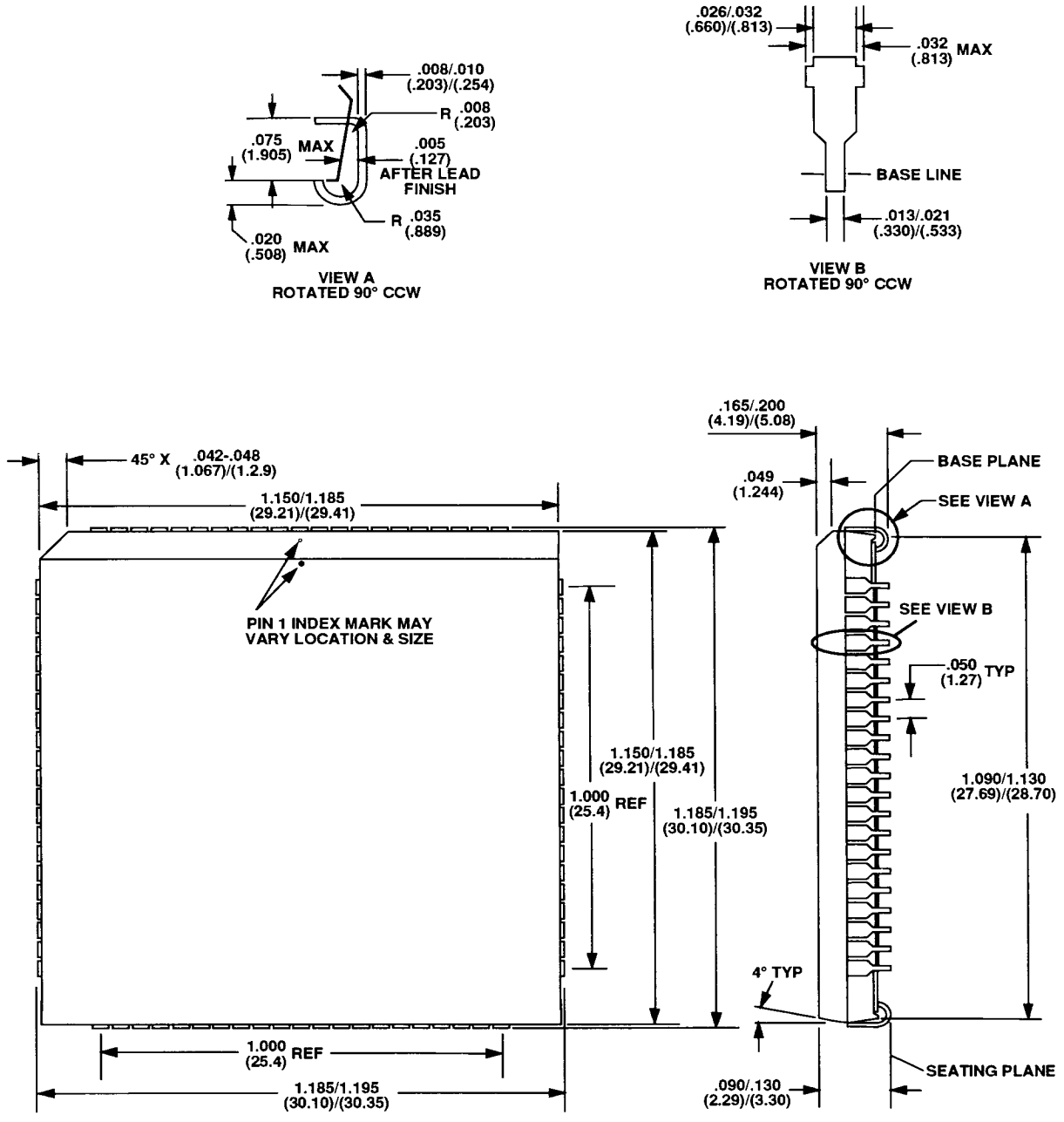


Figure 16. PLCC Packaging

CLDCC Packaging (Q1650C-3L and Q1650M-2L)

The Q1650C-3L and Q1650M-2L devices are packaged in an 84-pin ceramic leaded chip carrier (CLDCC) (figure 17). A suggested socket is AMP P/N 643066-2 (through-hole board mounted) or P/N 643151-2 (surface mounted). Dimensions are given in inches (mm).

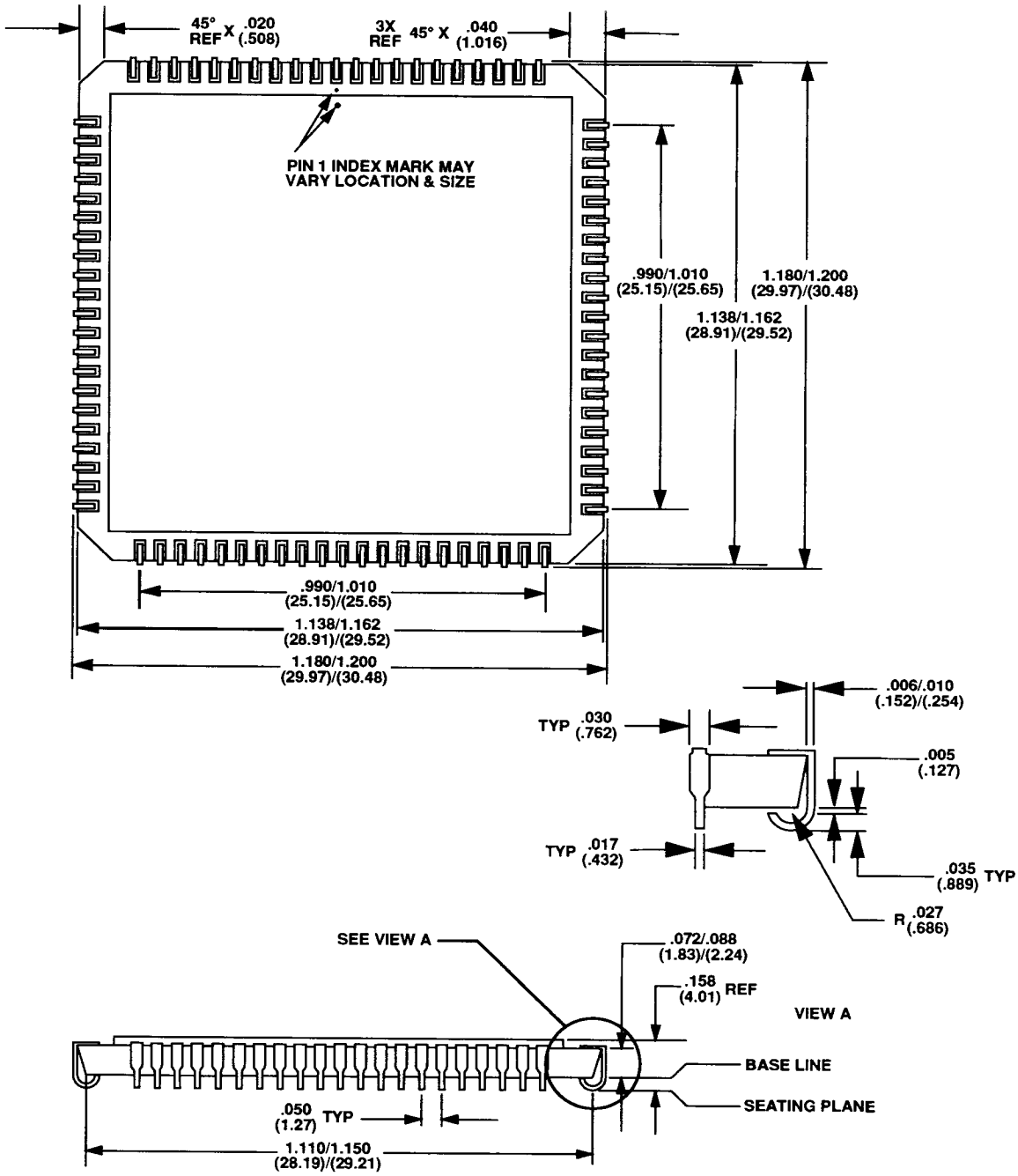


Figure 17. CLDCC Packaging

REFERENCES

Viterbi Decoding Theory

Bartee, T.C., 1986. *Data Communications, Networks, and Systems.* Indianapolis, Ind.: Howard W. Sams & Co.

Clark, G.C., Jr. and J. B. Cain, 1981. *Error Correction Coding for Digital Communications.* New York: Plenum Press.

Forney, G.D., Jr. "The Viterbi Algorithm," *IEEE Transactions on Information Theory,* vol. IT-15: 177-179.

Viterbi, A.J., 1971. "Convolutional Codes and Their Performance in Communication Systems," *IEEE Transactions on Communication Technology,* vol. COM-19: 751-772.

Punctured Code Operation

Cain, J.B., G. C. Clark, and J. M. Geist, 1979. "Punctured Convolutional Codes of Rate (n-1)/n and Simplified Maximum Likelihood Decoding," *IEEE Transactions on Information Theory,* vol. IT-25: 97-100.

Yasuda, Y., K. Kashiki, and Y. Hirata, 1984. "High-Rate Punctured Convolutional Codes for Soft Decision Viterbi Decoding," *IEEE Transactions on Communications,* vol. COM-32: 315-319.

Yasuda, Y., Y. Hirata, K. Nakamure, and S. Otani, 1983. "Development of Variable-Rate Viterbi Decoder and its Performance Characteristics," Procedures of Sixth ICDSC, Phoenix, Ariz.; XII-24-31.

Data Scrambling Algorithm

CCITT Recommendation, *Data Transmission at 48 Kilobits per Second Using 60-108 KHZ group Band Circuits,* Fascicle VIII.1, Rec. V.35, Appx. I

Related Application Notes

Morley, S.A., 1988. "Forward Error Correction Applied to INTELSAT IDR Carriers," *International Journal of Satellite Communications;* vol. 6: 445-454.

QUALCOMM Incorporated. AN1650-1, *Data Scrambling Algorithms Implemented in the Q1650 Viterbi Decoder.*

QUALCOMM Incorporated. AN1650-2, *Setting Soft-Decision Thresholds for Viterbi Decoder Code Words from PSK Modems.*

QUALCOMM Incorporated. AN1650-4, *Using the Q1650/Q0256 Viterbi Decoders with Externally Provided Branch Metrics.*

QUALCOMM Incorporated. TB0256-1, *Successful Integration of QUALCOMM VLSI Products into INMARSAT.*

Related Technical Data Sheets

QUALCOMM Incorporated, 1992. *Q0256 k=7 Multi-Code Rate Viterbi Decoder 256 and 800 Kbps Data Rates Technical Data Sheet.*

QUALCOMM Incorporated, 1992. *Q1601 10 Mbps, k=7 Viterbi Decoder Technical Dat Sheet.*

GLOSSARY

AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BPSK	Binary Phase Shift Keyed
CLDCC	Ceramic Leaded Chip Carrier
CMOS	Complementary Metallic Oxide Semiconductor
C0, C1, C2	Encoder output bits or code word
dB	Decibel
DBS	Direct Broadcast System
FEC	Forward Error Correction
FIFO	First-In First-Out
G0, G1, G2	Generating function of the convolutional encoder, described as an octal number
k	Constraint Length
LCC	Leaded Chip Carrier (either PLCC or CLDCC)
Mbps	Million Bits Per Second; refers to the encoder data input rate and the decoder data output rate.
OQPSK	Offset Quadrature Phase shift Keyed
PLCC	Plastic Leaded Chip Carrier
QPSK	Quadrature Phase Shift Keyed
R0, R1, R2	Decoder input bits or code word (C0, C1, C2 bits with AWGN added)
VSAT	Very Small Aperture Terminal

ORDERING INFORMATION

Maximum Data Rate	Plastic Package (PLCC)	Ceramic Package (CLDCC)	MIL883C Screened Version	Special Packages
2.5 Mbps	Q1650C-1N	N/A	N/A	Contact QUALCOMM
10 Mbps	Q1650C-2N	N/A	Q1650M-2L	Contact QUALCOMM
25 Mbps	N/A	Q1650C-3L	N/A	Contact QUALCOMM

For Commercial Versions
Temperature Range: 0°C to +70°C
VDD Input: 4.75 VDC to 5.25 VDC

For Military Screened Versions
Temperature Range: -55°C to +125°C
VDD Input: 4.5 VDC to 5.5 VDC

For more information or to place an order, contact your local QUALCOMM Engineering Representative or contact QUALCOMM directly:

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