497AE and 1215E Boundary-Scan Master 2 Advanced Operational Mode

Features

- The BSM2 is available in 2 versions:
  - — The 497AE is available in a 28-pin SOJ package
  - — The 1215E device is available in a 48-pin TQFP package
- The 497AE and 1215E differ in the following capabilities
  - — 497AE has an 8-bit data-bus and no user I/O signals
  - — 1215E has a 16-bit data-bus and 3 user I/O signals
- Selectable between two operational modes:
  - — 497AA compatibility
  - — Advanced Operational Mode (497AE)
- 3.3 V power supply, but fully 5 V (TTL) tolerant for all inputs and outputs
- Dedicated 8 kbits test data in (TDI) and test data out (TDO) buffers; FIFO or fully addressable
- Simple and flexible host interface options:
  - — 497AE, synchronous or asynchronous 8-bit data bus
  - — 1215E, 16-bit asynchronous data bus for maximum throughput
- Self-timing interface to a microprocessor/microcontroller
- Automatic test mode select (TMS) sequence generation
- Programmable test clock (TCK) generator with gated TCK mode
- Provides test reset (TRST*) optional TAP signal
- External pin control to 3-state test access port (TAP) signals (1215E)
- Conflict-free automatic test pattern generator (ATPG)
- 32-bit signature analysis register (SAR) with response masking for repeatable signatures
- TCK output frequency of 65 MHz
- Maskable processor interrupts; no lockup condition
- Built-in self-test for >95% fault coverage
- Support protocols for multidrop backplane test configurations, such as *TI*'s[1] addressable scan port protocol
- Provides retiming (pipeline) delays of up to 13 TCK cycles to correct skewing
- One general-purpose input, two general-purpose outputs. Outputs can be programmed for use as DMA control signals (1215E device only).

Description

The Agere Systems Inc. 497AE/1215E Boundary-Scan Master 2 (BSM2) communicates with a generic processor in parallel and controls the test and diagnosis (T&D) of a unit under test (UUT), which could be a device, board, or system, based on the ANSI/*IEEE*[2] standard 1149.1-1990 TAP and Boundary-Scan (B-S) Architecture. It serializes test vectors, delivers them to the UUT using the standard protocol, and stores the UUT response as raw data or as a signature. An ATPG generates four common test sequences for interconnect test, cluster test, etc. The device also solves the potential problems of bus conflict and nonrepeatable board-level signatures associated with the B/S architecture. Finally, the BSM2 provides support for edge-connector/backplane test and system test and diagnosis.

The BSM2 comes in two package sizes. The 497AE is a 3.3 V, 28-pin SOJ package that provides both software and hardware backward compatibility to the 497AA BSM. The 1215E is a 3.3 V, 48-pin TQFP package with a 16-bit data bus and direct register access.

Manual Description

This manual describes the advanced operational modes of the 497AE and 1215E devices. The 1215E device offers higher throughput, using a 16-bit data-bus, and 3 user I/O signals. For additional information, contact your Agere Account Manager.

* Asterisk on any pin name indicates active-low.

1. *TI* is a registered trademark of Texas Instruments Inc.
2. *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

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Introduction

Conventions

Throughout this document, an asterisk on any pin name indicates active-low.

The test and diagnostic processor interfaced to a BSM2 is simply called the controlling processor or the “rocessor.

The BSM2

The Agere 497AE/1215E Boundary-Scan Master 2 (BSM2) communicates with a generic processor in parallel and controls the test and diagnosis (T&D) of a unit-under-test (UUT)—a device, board, or system, based on the ANSI/IEEE1 Std 1149.1-1990 Test Access Port (TAP) and Boundary-Scan (B-S) Architecture and its supplements. The BSM2 serializes test vectors, delivers them to the UUT using the standard protocol, and stores UUT response as raw data or as a signature. An automatic test pattern generator (ATPG) generates four common test sequences for interconnect test, cluster test, etc. The BSM2 also solves potential problems of bus conflict and nonrepeatable board-level signatures associated with pseudorandom testing of a product through its B-S architecture. Finally, the BSM2 provides support for edge-connector/backplane test and system test and diagnosis.

The 497AE and 1215E represent a total redesign of the 5 V 497AA using 0.35 µm CMOS technology. The major differences are that both parts have a higher operating frequency: 65 MHz, only require a 3.3 V power supply, and can operate over the temperature range of –40 °C to +85 °C. The new 497AE design maintains a high degree of hardware and software compatibility with the 497AA (manual MN98-030NTNB). New features and operational modes have been added to the 497AE and 1215E. The present manual describes operation of these parts in advanced operation mode:

1. Synchronous/asynchronous-8 mode (497AE)—the interface of the 497AE can operate either synchronously or asynchronously according to user selection. In addition, one of two internal operational modes is selectable—either the 497AA Compatibility Mode or the Advanced Operational Mode.

   The Advanced Operational Mode is significantly different than the 497AA mode. There is an internal state machine that tracks the state of the TAP Controllers of the B-S devices currently in the UUT B-S chain connected to (addressed by) the BSM2. With this feature, TMS signal generation is greatly simplified, i.e., automatic. Access to the data memories is also simplified because they behave like FIFOs.

2. Asynchronous-16 interface (1215E)—this is similar to the 8-bit mode Advanced Operational Mode described above, but with a different package (48-pin TQFP) and a 16-bit data bus.

Although the 497AE supports 4 possible operational scenarios (2 different host interfaces, 2 different internal operational modes), the 1215E operates only with an asynchronous host interface and in Advanced Operational Mode. The Advanced Operational Modes are described in this document.

A systems approach was taken in defining the architecture of the BSM2. A major goal of the architecture was to minimize the housekeeping required by the processor, as well as to maximize the T&D throughput. Figure 1 depicts the architecture of the BSM2.

At the left of the figure is shown a generic microprocessor interface with address, data, and control signal connections. On the right side are shown the signals by which the BSM2 communicates with an ANSI/*IEEE* Std 1149.1-1990 TAP. Consequently, the BSM2 can be considered a protocol converter. The main subsystems of this device are listed below and will be discussed in more detail in the following sections:

- Processor Interface (PI)
- Device Controller
- BSM2 internal registers (see Appendix B)
- Test Data Memories (FIFOs)
- Automatic Test Pattern Generation (ATPG), Scan Sequence Modification, and Signature Analysis
- Automatic TMS Generator
- TAP State Tracker
- TCK Generator and Gating
- User-Definable I/O (1215E Only)
- Interrupt Control

Introduction (continued)

The BSM2 (continued)

Major functional units are given separate treatment in addition to the architectural descriptions:

- The BSM2 Scan Process
- Automatic Test Pattern Generation (ATPG), Scan Sequence Modification, and Signature Analysis
- Low Power Mode
- BIST—Self-Test of the BSM2

This document has five appendices:

- Appendix A—BSM2 Pseudocode Examples
- Appendix B—BSM2 Internal Register Descriptions
- Appendix C—BSM2 (497AE) Data Sheet
- Appendix D—BSM2 (1215E) Data Sheet
- Appendix E—BSM2 Operation as a Function of Phase Relation of TCK and TCKIN at High Speeds with Low-Valued Clock Divider

Appendix B includes description of programming the BSM2 registers. In addition, timing of actions resulting from writing to the registers is discussed.

Appendices C & D are data sheets for the two forms of the BSM2—the 497AE and the 1215E.

This manual assumes familiarity with ANSI/*IEEE* Std1149.1-1990, *IEEE* Std 1149.1a-1993, and *IEEE* Std 1149.1b-1994, obtainable from the *IEEE* Standards Office.

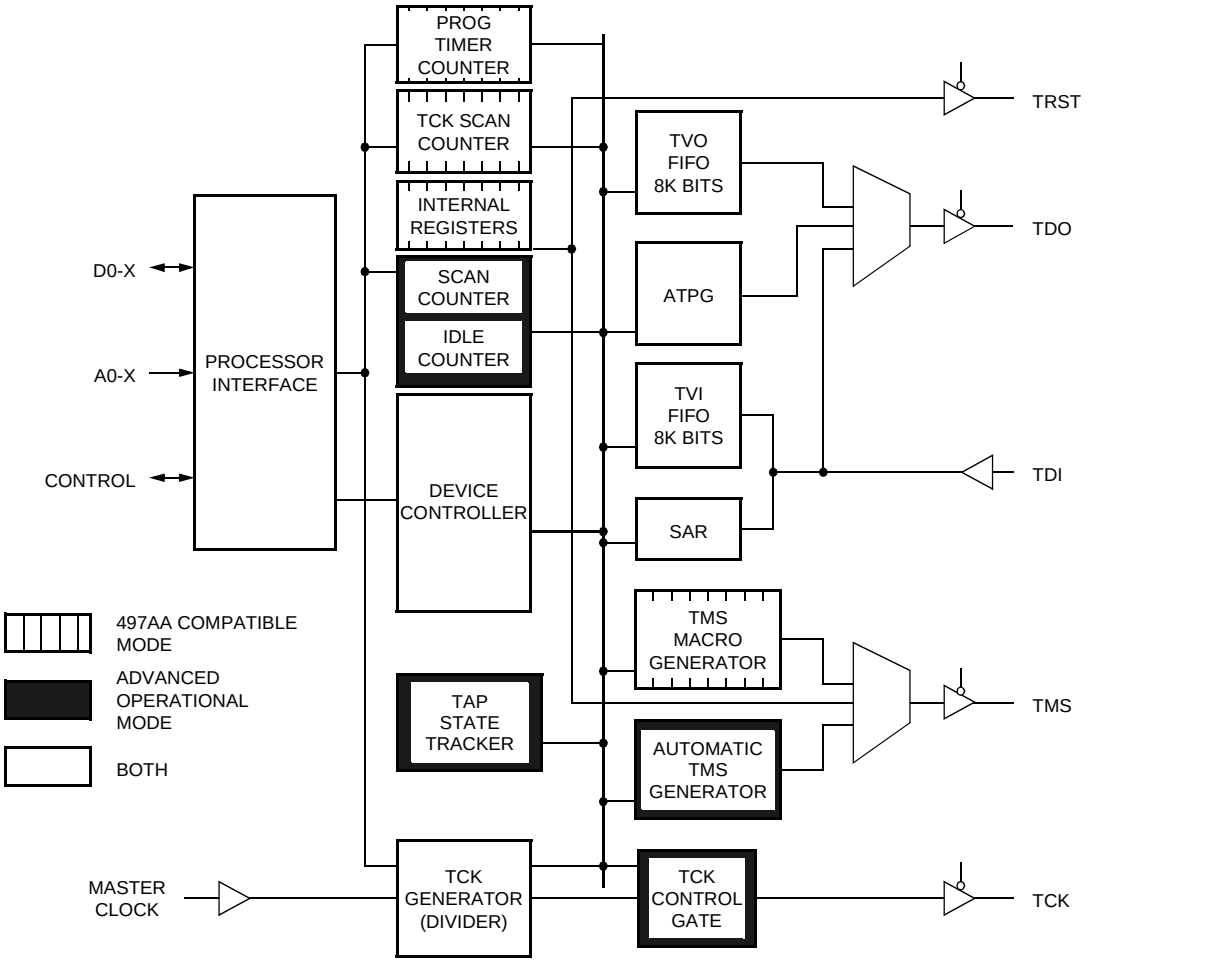


Figure 1. BSM2 Architecture

Architecture of the BSM2

TAP, Power, and Ground Pins

Both the 497AE (Table 7) and 1215E (Table 18) have a 5-pin TAP interface. Details of power and ground pinout can be found in Table 8 (497AE) and Table 19 (1215E).

BSM_MD* (497AE only)

This pin defines the operational mode of the device. It should be tied low for operation in 497AA compatible mode. If tied high or left unconnected, an internal pull-up will cause the device to operate in Advanced Operational mode. This pin should not be switched during operation of the BSM2.

SYNC_HIF*

This pin defines host interface operation. If SYNC_HIF* = 0, then the interface will operate synchronously as in 497AA mode. If SYNC_HIF* = 1 or if the pin is left unconnected, the interface will operate asynchronously (Figure 15 and Figure 16). There is an internal pull-up on this pin. This pin should not be switched during operation of the BSM2.

Processor Interface

The processor interface provides generic functionality including chip enable (CE*), read/write control (R/W*), data available/valid (DAV*), master clock input (TCKIN), interface ready handshake control (RDY), and interrupt signalling (INT*). The asterisk following a pin name indicates that the signal on that pin is active low.

Basic functional description of the pinout of the 497AE processor interface can be found in Table 6.

Basic functional description of the pinout of the 1215E processor interface can be found in Table 17.

497AE Data Bus

The data bus (D[7:0]) of the 497AE is 8 bits wide permitting writing and reading of BSM2 Internal Registers (BIRs) on a byte-at-a-time basis. Details of read/write operation are provided in Appendix B under the heading 497AE Register Size, Byte Transfer, and Synchronization of Reads and Writes.

1215E Data Bus

The data bus (D[15:0]) of the 1215E is 16 bits wide permitting writing and reading of the BIRs on a word-at-a-time basis. Details of read/write operation are provided in Appendix B under the heading 1215E Data Reads and Writes.

497AE Addressing

The 497AE preserves the indirect addressing operation of the 497AA. The RA pin is used to address a Pointer Register (PTR). Once the PTR is selected, the register address of a BIR to be accessed is placed in the PTR by writing to the 497AE data bus. Details of this indirect addressing are provided in Appendix B under the heading 497AE Register Size, Byte Transfer, and Synchronization of Reads and Writes.

One difference between the 497AA Compatibility Mode and the Advanced Operational Mode of the 497AE is that the device is *not* reset by reading from PTR in Advanced Operational Mode.

1215E Address Bus

The 1215E provides only a direct addressing method. The address bus comprises the pins RA[4:0]. Further information concerning use of the address bus is provided in Appendix B under the heading 1215E Addressing (Direct).

Device Controller

The device controller provides coordination and synchronization of the various modules depending on the selected modes of operation. All registers and memory are held in a static state until one of three command states are selected: Execute, Jump, or Reset. In the default mode, the TCK is free running, but can be set to a gated mode such that the clock is off when the device is in the nonexecuting mode.

In addition, the controller coordinates the internal self-test operations of the BSM2 (see under the heading BIST—Self-Test of the BSM2).

Architecture of the BSM2 (continued)

Test Data Memories (FIFOs)

There are two test data memories (TVI and TVO). Each consists of 8K bits organized in 512 16-bit words. They behave as FIFOs during normal load-scan-unload operation. In such a case, it is not necessary for the controlling processor to specify addresses for writing to, or reading from, the test data memories. To reset a FIFO, the relevant address pointer register (API or APO) can be loaded with the value 0.

However, in ATPG mode the test data memories do not operate as FIFOs. In such a case, these memories hold information about circuit interconnect necessary to create conflict-free ATPG. FIFO organization is not appropriate in ATPG mode. In this mode, BSM2 needs a memory pointer permitting it to loop through the circuit interconnection information—once for each vector to be generated. In ATPG mode, the words of the memories can be written and read individually using their respective address pointer registers, API and APO. (See Automatic Test Pattern Generation (ATPG), Scan Sequence Modification (SSM), and Signature Analysis.)

TVI Test Data Memory (FIFO)

This 8K-bit memory receives the output test data from the selected/attached B-S chain during normal scan operation.

During ATPG operation, the B-S chain output data stream is re-directed to a signature analysis register (SAR). The TVI test data memory is used during ATPG for a portion of a circuit map that permits the test generation function to avoid bus conflict in the application of otherwise circuit independent algorithms. More details on ATPG are found under the heading Automatic Test Pattern Generation (ATPG), Scan Sequence Modification (SSM), and Signature Analysis.

TVO Test Data Memory (FIFO)

This 8K-bit memory stores the test stimulus data to be scanned into a selected/attached B-S chain during normal scan operation.

During ATPG operation, the test stimulus is provided by the test pattern generation hardware. The TVO test data memory is used to store a portion of the circuit map mentioned above.

User-Definable I/O (1215E Only)

The 1215E provides three pins for user-definable I/O—USERIN, USEROUT1, and USEROUT2. These might be interfaced to a DMA controller, for example.

USERIN

The USERIN pin provides the capability of optionally monitoring the state of a user selected signal without adding additional parallel I/O decoding logic to a design. Because of pin limitations it is not available on the 497AE device. If it is unused in the 1215E design, it should not be left floating, but tied either high or low.

Note: The USERIN signal is not latched in the BSM2. Stability of this signal is the responsibility of the user.

USEROUT0

The USEROUT0 pin provides the means of signalling an interrupt to the controlling processor according to certain conditions of the Test Data Memories (FIFOs) (e.g., full, empty, etc.).

The pin can be considered to be the output of a 9-input OR tree as follows: The USR0 bit in the CUTO register is ORed with the STAT[15:12] and STAT [3:0] bits of the status register under control of a mask programmed in the USRC0[7:0] bits of the CMU register.

USEROUT1

The USEROUT1 pin provides the means of signalling an interrupt to the controlling processor according to certain conditions of the Test Data Memories (FIFOs) (e.g., full, empty, etc.).

The pin can be considered to be the output of a 9-input OR tree as follows: The USR1 bit in the CUTI register is ORed with the STAT[15:12] and STAT [3:0] bits of the status register under control of a mask programmed in the USRC1[7:0] bits of the CMU register.

Architecture of the BSM2 (continued)

TCK Generator and Gating

TCK Generator

The BSM2 derives the TCK signal for a selected/attached B-S TAP from the Master Clock input signal (TCKIN) via a divider called the TCK Generator (Figure 1). The TCK Generator can be programed to divide the Master Clock by 2n with $0 \leq n \leq 7$. The value of n is programed in the CDIV[2:0] bits of the CSC register.

TCK Gating

The default state of the TCK signal is free-running, with a divide by 128 of the TCKIN signal. It can be set to a gated mode, in which TCK only operates when scanning or moving from TAP state to state. TCK is gated off when the TAP State Tracker (below) is in the idle state or the scan destination state or when data overflow or underflow conditions exist.

Automatic TMS Generator

In the normal mode (nonmanual), the TMS signal pattern is provided from an internal circuit that automatically determines the pattern based on the current state, the desired scan operation (e.g., data register scan), and the destination state. In the automatic pause mode, if there is data overflow or underflow, the automatic TMS generator commands the TAP Controllers of the selected/attached B-S chain to move to the appropriate Pause-*x*R state [or, if so programmed, pause via gating the clock signal on TCK (see above)] automatically until the condition is corrected.

TAP State Tracker

This functional block controls the signals produced by the BSM2 on its TMS output pin. By doing so, at any time during scan operation, the TAP State Tracker can provide to BSM2 internals the current TAP Controller state of the TAP Controllers on the selected/attached B-S chain. When a scan operation is initiated, the then current TAP Controller state (according to the TAP State Tracker) is used as the initial state of a sequence of states passing through the desired scan state (programmed by the controlling processor) and terminating in a target state (programmed by the controlling processor).

This method of scan sequence programming differs from that implemented in the original BSM (497AA). For more about BSM2 scan operation, see the description under the heading The BSM2 Scan Process. For more about the registers used to program the BSM2 scan operation, see descriptions of the TVX, IDLE, LPC, and SDR registers.

Interrupt Control

Interrupt control is achieved by programming the interrupt mask bits OUIM and WDIM (in the CUTI register) and BIST_IE (in the CBIST register).

If any of these bits has the value 0, the interrupt signal, INT*, will not respond to the relevant interrupt-provoking stimulus. The value of one of these bits is 1, it will bring INT* low (active) according to the occurrence of the relevant stimulus.

Interrupt servicing software must scan all relevant status bits to determine the event that generated the interrupt. It is often appropriate to set the mask bits to 0 while eliminating the cause of an interrupt.

Asynchronous and Synchronous Interface Modes

Asynchronous Operation (497AE and 1215E)

The device pinout tables for the 497AE will be found in Appendix C, beginning on page 67. The device pinout tables for the 1215E will be found in Appendix D, beginning on page 78.

An asterisk following a pin name indicates that it is active-low.

In asynchronous interface mode, the CE* (chip enable) pin is the main control signal. The R/W* pin controls the direction of the data bus when CE* = 0.

On the output side of control, the RDY pin provides a handshake from the BSM2 to the controlling processor.

The defining characteristic of asynchronous interface mode is that the BSM2 protocol in this mode is independent of the BSM2 master clock signal (TCKIN). Internally, the device must synchronize with TCKIN; therefore, the RDY signal may be required to indicate whether BSM2 internal response to a previous access by the controlling processor is complete.

The RDY signal will never be active unless CE* is.

An access cycle begins with the controlling processor driving CE* = 0. The R/W* pin is driven to the logic value defining the type of access desired.

If the BSM2 is not internally synchronized for a new access, then the BSM2 will hold the RDY signal inactive (=0) until internal synchronization is achieved. When the RDY signal = 1, the controlling processor can continue the access cycle.

At the end of the access cycle, the controlling processor drives CE* = 1. Any capture of data by the BSM2 occurs on the rising edge of the CE* signal—when CE* goes inactive. In a read access cycle, any data on an output bus of the BSM2 is only correct after RDY = 1. The bus is no longer driven after the rising edge of CE*.

Note: If the BSM2 user can guarantee that accesses by the controlling processor will be separated by a minimum of 4 cycles on the TCKIN signal, then RDY pin does not need to be monitored by the controlling processor.

The Read sequence is as follows:

- The controlling processor requests an access by driving the signal on CE* low.
- R/W* is driven high. Consequently, the data bus will be driven by the BSM2 and contain data from the selected register once RDY = 1.
- After reading the data bus, the controlling processor drives the signal on CE* high, terminating the access cycle.

The Write sequence is as follows:

- The controlling processor requests an access by driving the signal on CE* low.
- R/W* is driven low. Consequently, the data bus will be driven by the controlling processor and contain data to be written to a selected register.
- The BSM2 drives the signal on RDY high.
- The controlling processor drives the CE* signal high.
- The data to be written is latched by the BSM2 on the rising edge of the CE* signal.
- Relevant timing diagrams for the 1215E begin with Figure 15 on page 80. The operation of the 497AE on the pins with common names is identical to that of the 1215E.

Synchronous Operation (497AE only)

Synchronous operation of the 497AE strongly resembles the operation of the 497AA.

Relevant timing diagrams for the 497AE begin with Figure 7 on page 69.

The BSM2 Scan Process

Introduction

Normal Scan Operation

Normal scan operation in the BSM2 involves loading test input stimulus data into the TVO FIFO and defining a sequence of states in the TAP Controllers of the selected/attached B-S chain. This sequence is the shortest path through the finite state machine implementing the TAP Controller such that it begins at a defined starting TAP Controller state, passes through a defined TAP Controller state in which scanning occurs, may pass through a defined TAP Controller state in which the operation will "idle" for a defined amount of time, and terminates in a defined TAP Controller state.

During normal scan operation, test results output data is stored in the TVI FIFO.

Normal scan operation is selected by setting the TIOM[2:0] bits of the CUTI register to 001.

Applying Stimulus While Ignoring Test Results

If it is desired to ignore test results during a scan operation, the BSM2 can be programmed to do so by setting the TIOM[2:0] bits to 000.

This mode can be used when it is desired to improve scan downloads to a target device and avoid the overhead of the extra I/O operations needed for reading output from TVI. For example, the technique can be used to download software or to establish programmable logic prior to “burn-in.”

See also the discussion of rapid upload of data under the heading Recirculation Scan.

Scanning Out Results Without Applying Test Stimulus

To scan data from a selected/attached B-S chain without scanning new test stimulus into the chain, the TIOM[2:0] bits should be set to 100. In this “response only” mode, data from the chain is directed to the TVI FIFO or the SAR (as determined by current programming of for scan sequence modifier or SSM), but no data from the TVO FIFO or the ATPG function is scanned into the chain. Instead, the chain is simply reloaded with the data it previously contained in the manner described under the heading Recirculation Scan.

Defining TAP Controller States in a Scan Sequence

The starting state is the current state of the TAP Controllers in the attached/selected B-S chain. This state is synchronized with the state known to the TAP State Tracker at power-up or by the use of TSRT* to force the attached/selected B-S chain TAP controllers to the Test-Logic-Reset TAP Controller state. Once synchronization is established, the current state of the TAP controllers of the attached/selected B-S chain can be determined by the value of the TAPS[3:0] bits in the STAT register.

The TAP Controller state in which scanning is to occur is determined by the value of the SCT[2:0] bits in the CSC register.

The destination TAP Controller state is determined by the value of the DET[1:0] bits in the CSC register.

The “Idle” TAP Controller state is determined by the Idle Type bits (IDT[1:0]) in the CSC register. Note that if an "idle" TAP Controller state is specified that does not lie on the shortest path between the starting state and the destination state running through the scanning state, then that "idle" state will never be entered in the scan operation.

The number of cycles of the TCK signal for which the operation is to remain in the "idle" TAP Controller state is written to the IDLE register.

Writing, Reading, and Operation of the Input and Output Scan Data FIFOs (TVI and TVO)

Pseudocode illustrating a normal scan process is illustrated on page 28.

The total number of bits to be scanned in a single vector is written to the TVX register.

The starting address for test stimulus data in the TVO FIFO is written to the APO register. The starting address for test results data in the TVI FIFO is written to the API register.

Establishing the type of scan operation is done by writing the TIOM[2:0] bits of the CUTI register. Execution is initiated by writing the EXEC bit of the CUTI register.

The status register allows the controlling processor to monitor the scan operation. For example, if all test result data in the TVI FIFO has been read, this will be indicated by the TVIM bit. If the TVO FIFO has not been filled with stimulus data, this will be indicated by the TVOU bit.

The BSM2 Scan Process (continued)

Writing, Reading, and Operation of the Input and Output Scan Data FIFOs (TVI and TVO) (continued)

Prior to execution, the user may program a pause during a subsequent normal scan operation by gating the signal on TCK. This is done by use of the GCLK bit in the CSC register. The gated clock function is described under the heading TCK Gating.

Overwriting TVO and Overreading TVI

If the user writes to the TVO memory when it is full, data in the FIFO will be overwritten. If the user reads the TVI memory when it is empty, the value will be unpredictable and useless. In both cases the memory pointers will become incorrect; and, consequently, the FIFOs will be corrupted. The only way to recover is to reinitialize and restart the interrupted operation. The FIFOs are reinitialized by setting the values of both the address pointers (APO for TVO and API for TVI) to zero.

Avoiding Overwriting TVO and Overreading TVI

Overwriting TVO (overreading TVI) can be avoided by checking if TVO has been filled (or TVI emptied).

When TVO is full, the TVOU bit in the status register will have the value 1. When TVI is empty, the TVIM bit in the status register will have the value 1.

Overflow and Underflow Conditions

Overflow is the condition in which more data is scanned out of the selected/attached B-S chain than can be stored in the TVI test data memory.

Underflow is the condition in which insufficient data is loaded in the TVO test data memory for the current scan operation. Underflow is not projected when the TVO memory is loaded. The condition is discovered by the BSM2 when it arises during the subsequent scan operation.

When overflow or underflow of a test data memory (FIFO) occurs, the BSM2 can be programmed to always enter the appropriate Pause-*x*R TAP Controller state or to gate the test clock (halt the signal on TCK). The programming is done by the loading the appropriate value in the GCLK bit of the CSC register prior to execution of a scan operation. When GCLK = 1, under-/overflow results in halting the test clock. When GCLK = 0, under-/overflow causes transfer of the TAP controllers in the selected/attached B-S chain to enter the nearest Pause-xR TAP Controller state.

Jump and Reset Commands

By use of the EXEC[1:0] bits of the CUTI register, the controlling processor can direct the BSM2 to drive the TAP State Tracker to specific TAP Controller states.

WARNING: The Jump and Reset commands execute whether or not there is any other ongoing process executing in the BSM2.

Jump Command

The jump command is designed to be used when a BSM2 is controlling more than one B-S chain and needs to the synchronize to the current state of the TAP Controllers in a newly selected B-S chain after having carried a sequence of operations on another.

This command is not locked out by a concurrently executing process.

The jump command results in the direct movement of the TAP State Tracker from the current TAP Controller state to any other one selected by programming. The move between states is not restricted to following an arc of the TAP Controller's finite state machine. Moreover, with the exception of a jump to/from the Test-Logic-Reset TAP Controller state, the TMS output signal is not effected; and the TAP Controllers of the formerly selected/attached B-S chain will only change state as directed by subsequent programming of the BSM2. When the jump is to/from the Test-Logic-Reset TAP Controller state, the signal on TMS must change from 0 to 1 or vice versa.

WARNING: Issuing the Jump Command while executing a scan operation, can produce undesirable results, although the results are predictable if the cycle of the TCK signal is long enough so that the controlling processor can monitor operations.

The BSM2 Scan Process (continued)

Jump and Reset Commands (continued)

Reset Command

This command overrides (halts) any current execution in any mode and internally resets the BSM2. Executing the Reset command does not activate the TRST* signal.

The TAP State Tracker will indicate that the BSM2 has driven the TAP Controllers of the selected/attached B-S chain to the Test-Logic-Reset TAP Controller state. It is necessary to synchronize the TAP State Tracker with the selected/attached B-S chain by running TCK for five cycles with the TMS signal equal to 1 or by use of the TRST* signal.

TAP Manual Mode

In the BSM2, it is possible to single step through a scan sequence in TAP Manual Mode. TAP Manual Mode is entered by writing a 1 to the MAN bit of the CUTI register.

The key to understanding TAP Manual Mode is the fact that writing the CUTO register not only supplies values to be driven on TMS, and TDO, but also produces the clock edge on TCK that causes the values to be driven. Likewise, reading the CUTO register not only is a means of capturing the value concurrently available on the TDI pin, but also produces the clock edge on TCK that cause the value in question to be captured from the output of the selected/attached B-S chain.

The CUTO register includes the bits that enable the operation of the TAP signals of the BSM2. Each TAP pin, other than TCK, is represented by a bit in the register. There is an additional bit operational in the manual mode only, TDOEM. In this mode, TDOEM controls enabling/disabling of the TDO output pin.

Control of TCK Pin

While writing (reading) the CUTO register causes an internal TAP Manual Mode TCK register to go low (high), this will not have effect on the value of the TCK pin of the BSM2 unless the pin is enabled for TAP Manual Mode by having the MAN bit of the CUTI register set. When the BSM2 is in TAP Manual Mode the normal connection of the TCK pin to the internal TCK generator (divider of the master clock) is overridden.

In this way the user can preselect the state of the TCK pin before going to the manual mode by either reading or writing to the CUTO register. In other words, once TAP Manual Mode is selected, the user does not need to worry about toggling TCK as it is done naturally by reading and writing to CUTO—with the same phase as defined in *IEEE* Std. 1149.1.

Control of TDI, TDO, TMS, and TRST* pins

In TAP Manual Mode, the next values to be driven on the TDO and TMS pins of the BSM2 are written to the TDOM and TMSM bits (respectively) of the CUTO register. Enabling/disabling of the TDO pin is controlled by the value written to the TDOEM bit (unless overridden by the state of the TOEB bit). Likewise a reset of the TAP Controllers on the selected attached B-S chain is effected by writing CUTO with the value 1 in the TRSTB bit. (The use of the TRSTB bit is not restricted to TAP Manual Mode.)

In TAP Manual Mode, when the CUTO register is read, the value output from the selected/attached B-S chain will be found in the TDIM bit of that register.

Data Modification

TDO Inversion

The value of bits from various internal sources (e.g., TVO) and driven by the BSM on its TDO output signal can be inverted before they are scanned into a selected/attached B-S chain. This is achieved by the use of the TC bit (CUTI[02]).

Signature Analysis for Deterministic Tests

The signature analysis register (SAR) can be used to compress the results of deterministic scan testing as well as in the case of ATPG. The SAR is selected through the use of the SSM function. See the description under the headings Signature Analysis for Deterministic Tests, Scan-Sequence Modifier (SSM), and Programming ATPG and SSM Functions.

Note: The retimed delay function is not applicable to scan operation in which the SAR is the target for data scanned into TDI.

The BSM2 Scan Process (continued)

Recirculation Scan

Using the TIOM[2:0] bits of the CUTI register, it is possible to program the BSM2 to directly connect its TDI input to its TDO output within the device.

There are two types of recirculating scan—recirculate mode (TIOM[2:0]=101) and recirculate mode with response only (TIOM[2:0]=111).

The Test Data Memories (FIFOs) are disconnected, and data that was in the selected/attached B-S chain when recirculating scan began is recycled through the chain for the programmed number of bits. During the recirculating scan, the BSM2 adds no delay to the scan chain—a B-S chain of *n* cells recirculates in *n* cycles of the TCK clock signal.

The recirculate mode is useful for manual debugging of B-S chains. The following approach was provided by an experienced BSM (497AA) user and is equally applicable in the case of BSM2.

First, a standard data scan is used to preload all scan flip-flops in the B-S chain. This scan operation is terminated in the Pause-DR TAP Controller state. Because of software performing I/O to the BSM2, this data scan is bursty—the host computer cannot keep the pipe flushed; TAP Controllers in the B-S chain move from Shift-DR to Pause-DR, back to Shift-DR, etc., until all of the data has been scanned in. Once the scan chain is preloaded, the recirculate mode (without storing response) is employed. By executing a scan operation in the recirculate mode, the BSM2 causes all the TAP Controllers on the selected/attached B-S chain to enter the Shift-DR TAP Controller state and remain in that TAP Controller state for the total number of scan bits. The TAP leads of individual devices can then be probed with a scope to detect and display the serial bit pattern in its entirety. The TMS signal is used to gate monitoring of the TDO/TDI data.

In the case of the recirculate mode with response only, a common application is the upload of functional data via a processor/controller with a TAP; just as applying stimulus while ignoring results (TIOM[2:0]=000) optimizes download times, recirculate mode with response only optimizes upload times.

B-S Chain Selection

The BSM2 supports a test architecture in which there are multiple B-S chains. The BSM2 can be programmed to select one of such B-S chains using the ASP protocol and interface definition (e.g., supporting *TI*'s Addressable Scan Port devices).

Retimed Delay Support

In some applications of B-S, there can be selected/attached chains that are physically distant from the BSM2. In these cases, clock skew between the signals of the TAP may become a problem. In order to alleviate the difficulty, designers may add intermediate latches (the same number for each BSM2 output signal) to deskew (retime) the signals (typically, TMS, TDO, and TDI). Each of the *n* latches in a given signal path will create one cycle of delay in the signal.

At the destination B-S chain, this is not a problem. The TMS and TDO signals will still be synchronized. The distant B-S chain will operate as if it were directly attached to TMS and TDO (after a delay of *n* cycles). The distant B-S chain will produce signals on the line driving the TDI signal of the BSM2. However, on the return path, the sequence of bits on the TDI signal will be delayed by the *m* latches in the TDI signal deskewing circuitry. The result is that the TDI signal is shifted by $n + m$ cycles, where $n + m$ is the total number of the latches in the signal path. The BSM can be programmed to take this delay into account when capturing the serial vectors scanned from the distant B-S chain.

The BSM2 can adjust to up to 13 latches in the deskewing circuitry by phase delaying the TDI signal by the value of the RTD bits. The programming of these bits is detailed in the discussion of the CSC register.

Note: The retimed delay support function applies only to scan operations when the TVI FIFO is selected as the target for input from TDI. It does not apply when the target for incoming scan data is the SAR.

Automatic Test Pattern Generation (ATPG), Scan Sequence Modification, and Signature Analysis

This section describes the BSM2 ATPG and scan sequence modification (SSM). While the description refers to interconnect test, this capability is general and can be used to test logic through a selected/attached B-S chain as well as device interconnection. It may prove useful for cluster test—testing of non-B-S devices via the B-S paths of devices that surround the non-B-S devices. It can also be used to test the internal logic of devices.

In carrying out interconnect testing, it is possible that bus conflicts could arise if multiple devices on a single bus were enabled simultaneously. The BSM2 avoids this situation by using a concise form of a wiring list to inform the ATPG function of which B-S cells are at device inputs, which are at outputs, and which must be held to a constant value (e.g., because they drive enable signals on other devices). (See the section titled Scan-Sequence Modifier (SSM).)

This section initially describes some of the BSM2 registers and memory blocks that are used for ATPG. The operation of the SSM, the subsystem that modifies the scan vectors and controls the response compression, is then described in detail. The hardware implementation of the test sequences in the ATPG mode is illustrated.

BSM2 Registers Related to ATPG

In this section, the registers used during ATPG are reviewed. Under the heading “Appendix B—BSM2 Internal Register Descriptions,” all registers are described in greater detail.

Control of ATPG, SSM, and Signature Analysis

- CUTI[09:08]—These bits, also called AMD[1:0], permit the selection of one of the four possible patterns that the BSM2 ATPG is capable of generating. The output data of an ATPG algorithm may be inverted prior to scanning into a selected/attached B-S scan path under control of the AC bit (CUTI[03]) as illustrated in the description of the CUTI register.
- The SSME bit (CUTI[04]) serves the function of enabling or disabling SSM and, with it, the signature analysis register (SAR).

ATPG-Related Registers

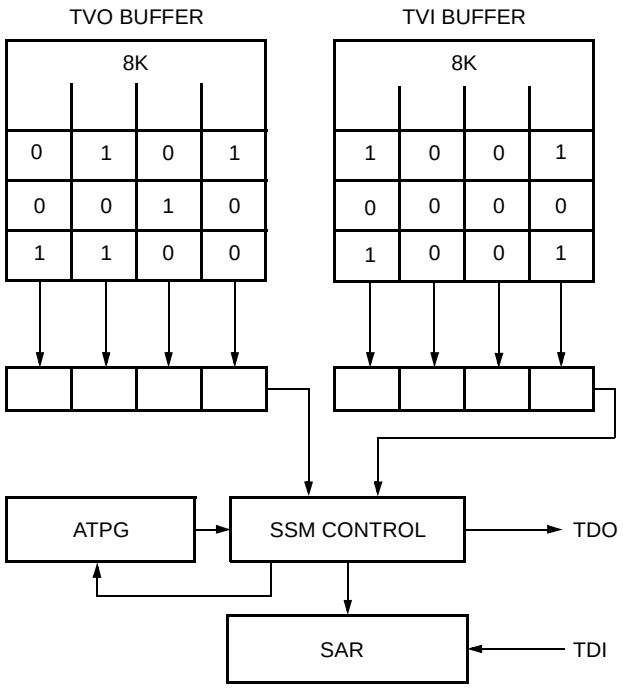
- Loop counter (LPC)—This 16-bit counter contains the number of serial tests that are to be applied to the UUT. Every time a complete vector is shifted out, this counter is decremented.
- Scan duration register (SDR)—This 16-bit register contains the length of each serial test vector to be applied to the UUT. This value is the length of the scan path—the total of the lengths of the B-S data registers in all the chips on the selected/attached B-S ring. The value from this register is loaded in a scan duration counter (SDC) which is decremented every time a vector bit is shifted out. When SDC reaches zero, a signal is sent to decrement LPC. Then, if LPC is not 0, the SDC is reloaded from the SDR. When both SDC and LPC are zero, the BSM2 stops transmitting serial test data.
- Net count register (NCR)—This 16-bit register is used by the ATPG in conjunction with the net counter (NC), to generate counting and walking sequences.
- Signature analysis register and pseudorandom pattern generator (SAR and PRPG)—These are 32-bit registers. The seed values for both of these registers are programmable in advanced operational mode. The PRPG is both readable and writable in the advanced operational mode and write-only in the 497AA mode.
- Control-Scan/Clock register (CSC)—In this register the scan type bits (SCT[2:0]) must be set for Shift-DR scan type (i.e., loaded with the pattern 010) for ATPG operation. Also, the destination state for ATPG should be set to either Test-Logic-Reset or Run-Test/Idle. This is accomplished using the destination type bits (DET[1:0]).
- IDLE counter register (IDLE)—This register should be set to zero for ATPG operation to disable the IDT bits of the CSC register.

The BSM2 has two 8K memory buffers, called the test vector out (TVO) and test vector in (TVI) buffers. For deterministic tests, these two buffers hold test vectors and the response of the UUT. In the case of ATPG, the SSM uses these to store a structure map of the scan chain, as described in the next section.

Automatic Test Pattern Generation (ATPG), Scan Sequence Modification (SSM), and Signature Analysis (continued)

Scan-Sequence Modifier (SSM)

This section describes a circuit called the SSM. It modifies a test sequence to ensure that no bus conflict will occur before the sequence is passed to the selected/attached B-S chain of the UUT. The modifier also enhances the efficiency of the test pattern generator, and controls the SAR so that only selected values are compressed. This module is used for modifying scan sequences in both ATPG and deterministic modes (see Figure 2).



5-6311 (F)

Figure 2. Scan-Sequence Modifier (SSM)

A B-S interconnect test sequence has three types of data:

- Type 1 is the test data that is to be applied to the output cells, one output cell per net. This data is determined by the test algorithm. This is the test stimulus information.
- Type 2 is output control data that determines whether a 3-state pin is active or in high impedance or the direction of a bidirectional pin. This information is determined by the board structure and does not change during application of a particular test algorithm. The control data is required to ensure that no bus conflicts occur due to the generated test. In general, this is the test information that needs to be held static. An example of this information, in the case of a cluster test, would be an enable signal that needs to be held low for meaningful tests to be applied.
- Type 3 is filler data that is scanned into the input cells at the receiving (input) sides of nets. This data is essentially don't care and is overwritten when a response is captured by these same cells. Filler data is required to permit the useful data, type 1 and type 2 data, to be scanned to the correct B-S cell positions on the B-S chain. Filler data is a placeholder for test response data.

Automatic Test Pattern Generation (ATPG), Scan Sequence Modification (SSM), and Signature Analysis (continued)

Scan-Sequence Modifier (SSM) (continued)

A test algorithm or test generator generates type 1 data. The generated data is a function of the test algorithm and number of nets, and is independent of the type of nets, their ordering, etc. Type 2 and type 3 data is typically provided by test generation software that format the test sequences. It is the critical necessity of type 2 and type 3 data that makes it difficult to automatically generate interconnect test sequences in a board- or system-level BIST environment. The technique that the BSM2 uses takes advantage of the fact that type 2 and type 3 data are static. Consequently, if the value of this data and its location is recorded once, then it can be easily inserted into the output scan sequence, and used for identifying the cells with useful test information that should be compressed by the signature analysis register (SAR).

SSM-ATPG Mode

Figure 2 shows the SSM configuration with ATPG as the TDO source and SAR as the TDI destination. To achieve this configuration SSM is enabled by setting the SSME bit.

Assume there are *L* scan cells on the currently selected/attached B-S chain. The type 2 (control) data are placed in two buffers, occupying *L* bits of each buffer. The TVO/TVI memories (each 8K) of the BSM2 serve as the buffers. There is a one-to-one mapping between the *L* locations of these buffers and the *L* scan cells on the selected/attached B-S chain. The controlling processor initializes TVI and TVO with type 2 data derived from UUT structural information. TVI identifies the control cells while TVO identifies input/output cells and supplies the data for control cells.

A 1 in location *n* in TVI identifies a control cell at position *n* in the selected/attached B-S chain. The value in TVO at the same location (*n*) contains the logic value that must be shifted into that control cell to avoid conflict during testing.

A 0 in location *m* in TVI implies that the cell in position *m* of the selected/attached B-S chain is either an input cell or output cell during the given test. A 1 in location *m* in TVO identifies the cell as an output cell and ATPG is enabled to supply test data for that cell location. A 0 in location *m* in TVI combined with a 0 in location *m* in TVO identifies the corresponding cell of the selected/attached B-S chain as an input cell. Since the data for such a cell is type 3, or filler data, any value can be applied to the scan cell at the corresponding B-S chain location. The BSM2 will always generate a 0 for filler data.

The table below defines the operation of the SSM and its interaction with SAR and the test pattern generator in the ATPG mode.

Table 1. ATPG Mode with SSM Enabled: How i^{th} Bits of TVI and TVO Encode Cell Type and Control Source of TDO and Actions of ATPG and SAR Functions

TVI(i)	TVO(i)	Cell Type	ATPG	SAR	Source of TDO
1	1 or 0	control	disable	disable	TDO(i)
0	1	output	enable	disable	ATPG(i)
0	0	input	disable	enable	constant 0

Automatic Test Pattern Generation (ATPG), Scan Sequence Modification (SSM), and Signature Analysis (continued)

Scan-Sequence Modifier (SSM) (continued)

SSM—Deterministic Mode with SAR as TDI Destination

The SSM serves a dual purpose. Not only does it select the appropriate source for data to be shifted out of the BSM2, it also has the information needed to select those bits in the stream of data being scanned into the BSM2 that correspond to bits sampled by input cells on the selected/attached B-S chain. To aid in understanding how this works, an important fact to observe is that, at any instant, when a test vector is being shifted into a selected/attached B-S chain, the B-S cell whose value is being shifted out of the BSM2 at TDO and into the B-S chain is the same B-S cell which has its previously captured response (if any) being shifted out of the B-S chain and into the BSM2, at TDI. For this reason, the TVI/TVO map that identifies the cell type and controls the value shifted into the selected/attached B-S chain, also identifies the cell type of the cell that is the origin of the bit that is being shifted out of the B-S chain and into the BSM2. Consequently, when an input cell is identified, as described above, the SAR is enabled and the bit value is taken as part of the data stream to be compressed. When the cell is identified as control or output, the SAR is disabled for that bit.

WARNING: When using ATPG, it is important to set autoincrementing on for both TVO and TVI. Otherwise, the first word of the maps in the two buffers will be used over and over as a map for the entire scan path. This may lead to undesirable changes of state in control cells along the B-S path with subsequent damage to the product.

When the BSM2 is used in normal (deterministic) scan operation with SAR as TDI destination, the output vectors, stored in TVO, are assumed to be correctly formatted so that no conflicts occur. Hence, the problem is limited to identifying the cells that have useful test information. When serial response vectors are to be compressed, TVI is used to store this information. A 1 in a location in TVI enables the SAR, and the information in the cell at the corresponding scan path location is compressed (Table 2). This feature can be used to identify the position of the input cells during interconnect test using the EXTEST instruction combined with signature analysis.

Note: The retimed delay function is not applicable to scan operation in which the SAR is the target for data scanned into TDI.

The table below defines the operation of the SSM and its interaction with SAR in this mode.

Table 2. Deterministic Mode with SSM Enabled: How i^{th} Bit of TVI Encodes Source Cell in B-S Chain and Directs Operation of SAR

Source of Test Stimulus	Receiving Test Output	TVI(i)	SAR
TVO(i)	SAR	1	enable
TVO(i)	SAR	0	disable

ATPG: Hardware Generation of Test Sequences

This section describes the hardware support provided by the BSM2 for generating a set of commonly used test vector sequences. The BSM2 provides support for generating the following sequences in ATPG mode:

- Walking-ones (walking-zeros) sequence
- Upcount (downcount) sequence
- Pseudorandom sequence (and its complement)
- Constant 1 (or 0) output

Automatic Test Pattern Generation (ATPG), Scan Sequence Modification (SSM), and Signature Analysis (continued)

Hardware Generation of Test Sequences (continued)

The complementary sequences are created by enabling ATPG with BSM2 output inversion also enabled (see under the heading TDO Inversion).

Throughout this section, *N* stands for the number of nets tested by means of a selected/attached B-S chain.

Walking Sequence ATPG

The walking-one (zero) sequence has special significance for interconnect test and is also useful for other purposes. Given *N* nets, the algorithm generates an *N* x *N* matrix with the diagonal of 1 (0). All other elements of the matrix are 0 (1). The hardware to generate this sequence is shown in Figure 3. It consists of two downcounters, NC (which is loaded via NCR) and LPC. Both NCR and LPC must be initialized to *N* by the user. After NC downcounts to zero, it is reloaded with the contents of NCR, and LPC is decremented. (SDR, as always, contains the length of the selected/attached B-S path.) NC and LPC are input to a comparator that outputs a 1 only when the two counters are equal. The sequence of bits produced from this output is the serialized test pattern.

The operation is as follows: The controlling processor initializes both NCR (and implicitly NC) and LPC to *N*. Since initially NC = LPC, a 1 is output and this is the first bit output from the test generator. After that, each time the ATPG is enabled by the SSM, the NC is decremented and the comparator output is shifted out as a bit of the test vector. After the test vector is generated (identified by SDC = NC = 0), LPC is decremented to *N* – 1, and NC is reinitialized to *N* by NCR. The operation repeats, except that now a 1 is output when NC = *N* – 1. This operation repeats until both counters are zero. This algorithm will generate *N* patterns, each of length *N* and the i^{th} pattern has a 1 in location i, and 0 in all other locations. The SSM ensures that the test vector bits are correctly positioned in each serial test vector. This is the walking-one sequence. Note that the complementary sequence, walking zeros, can be trivially constructed by complementing the output.

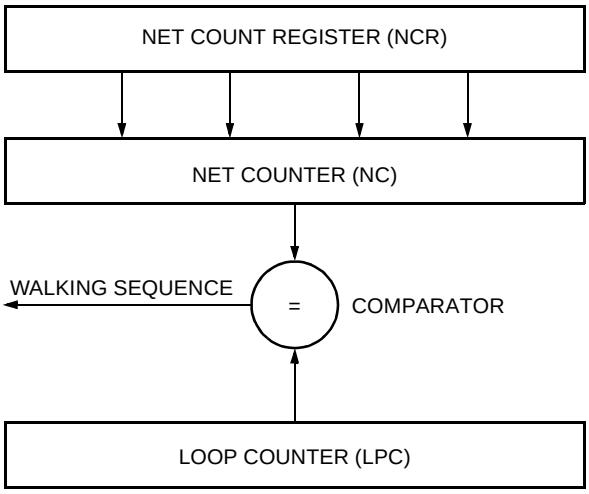


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Figure 3. Walking Sequence Test Generator

Automatic Test Pattern Generation (ATPG), Scan Sequence Modification (SSM), and Signature Analysis (continued)

Hardware Generation of Test Sequences (continued)

Counting Sequence ATPG

Application of an ATPG counting sequence is done by assigning a unique sequential (serial) test vector (STV) to each net such that the set of STVs follows a counting sequence. The counting sequence test has a short test length *O* (log *N*), where *N* is the number of nets. It should be noted that there is no "zeroth" net.

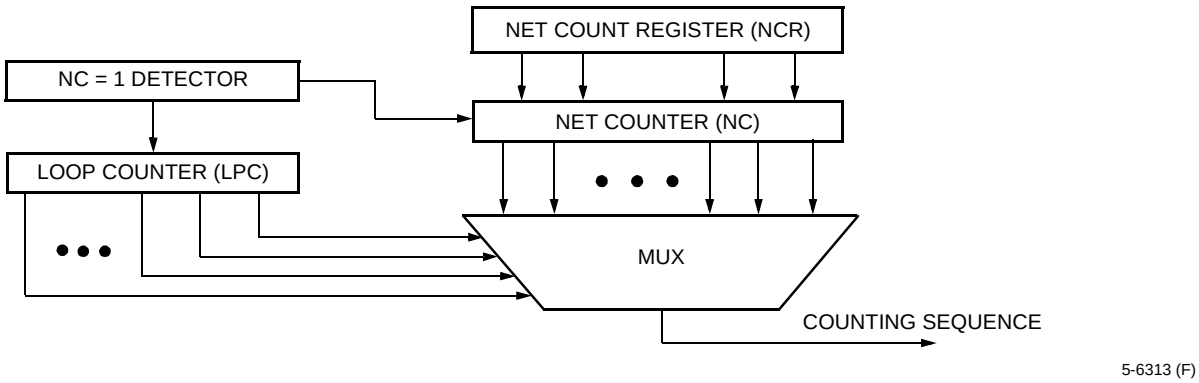


Figure 4. Counting Sequence Test Generator

Figure 4 shows the structure of the test generator. It uses the same counters as the walking sequence, NC (with the NCR) and LPC, but in a different configuration. The NCR is initialized to N, and the LPC is initialized to

$\lceil \log (N + 2) \rceil$.

The outputs of NC are fed to a multiplexor. The outputs of LPC

($\lceil \log \log (N + 2) \rceil$ bits)

are the control inputs of the multiplexor which selects one of the

$\lceil \log (N + 2) \rceil$

outputs of NC as the test output. Since the all-zero STV is prohibited, an additional logic block (NC = 1 detector) is included to detect the state when NC = 1. When NC=1, NC is reinitialized to the initial count value from NCR, and LPC is decremented.

The operation is as follows: The test master initializes NC to *N* and LPC to

$\lceil \log (N + 2) \rceil$.

The least significant bit of NC is chosen by the multiplexor as the test vector source and, on demand from the SSM, NC is decremented and the column is shifted out as the serial test vector. When NC counts down to one, it is reinitialized to *N*, and LPC is decremented. Now the multiplexor selects the second least significant bit of NC to shift out as the test vector. This sequence repeats till both NC and LPC downcount to zero. During this operation, NC counts down from *N* to 1,

$\lceil \log (N + 2) \rceil$

times and each time one of the

$\lceil \log (N + 2) \rceil$

Automatic Test Pattern Generation (ATPG), Scan Sequence Modification (SSM), and Signature Analysis (continued)

Hardware Generation of Test Sequences (continued)

lines input to the multiplexor are selected as the test output. This generates the set of *N*-bit serial test vectors comprising the serialized counting sequence. As before, the complementary sequence can be constructed by inverting the output.

Pseudorandom ATPG

The third sequence that the SSM facilitates is the pseudorandom sequence. This can be applied to the interconnect and the response compressed to a signature to give a pass/fail indication. The techniques for designing a pseudorandom test generator are well known and are not described in this document. The BSM2 has a 32-bit PRPG, the seed of which can be programmed. This generator can prove especially useful for cluster test and for testing the internal logic of some devices that do not have BIST.

Constant Output

Another useful mode of the ATPG is that in which a constant 1 or constant 0 is shifted out via TDO. This would be used when the BYPASS (all 1) or EXTEST (all 0) instruction is being scanned into the IR of all the devices in a selected/attached B-S chain.

Note: While constant output ATPG is selected, the SSM function must be disabled.

Programming ATPG and SSM Functions

The selection of the source of test vectors and the destination of the test response is programmed in the CUTI register, bits TIOM[2:0]. The ATPG type that is to be selected is programmed in the configuration registers, bits AMD[1:0]. Enabling/disabling of the SSM is also controlled by the CUTI register, bit SSME. Finally, bit AC in CUTI controls whether or not the output of the ATPG is complemented. More details concerning these registers are provided in Appendix B—BSM2 Internal Register Descriptions.

The operation of the ATPG is synchronized with the TAP State Tracker. When the TAP State Tracker indicates that all the TAP controllers on the selected/attached B-S chain have entered the Shift-DR TAP controller state, and the TDO source has been set as ATPG, the ATPG starts generating serialized algorithmic or pseudorandom test vectors. The response to the test sequences generated by the ATPG is compressed to a signature. The SAR is enabled only after the first test vector is scanned out of the selected/attached B-S chain. This is important in ensuring that the unknown values that are scanned out when the first vector is scanned in do not corrupt the signature. Also, after the last ATPG vector is scanned in, another vector needs to be shifted in to scan out the last response. This housekeeping is performed automatically in the BSM2 and is transparent to the user. For the last vector, a constant value is scanned into the B-S chain to allow access to the last response. In the BSM2, this value is 1.

Low Power Mode

To minimize power dissipation from the BSM2 several approaches can be taken.

CMOS power dissipation is strongly dependent on input voltage levels. Maintaining logic levels within 0.5 V of V_{DD} and V_{SS} will minimize power dissipation in any mode of operation.

The output loads, particularly the TAP signals, are a large factor determining the power dissipation of the device. 3-stating or disabling these signals when they are not used will minimize power consumption.

To reduce power dissipation below 43 mW, four complimentary approaches can be used when the device is not executing a scan operation. To reduce power dissipation to <5 mW, the external master clock for the BSM2 should be disabled.

To achieve low (<43 mW) power dissipation,

- All TAP output signals should be 3-stated. (This is accomplished using the TOE* pin and the TOEB bit in the 1215E and the TOEB bit alone in the 497AE.)
- CE* should not become active.
- No internal registers should change state.
- TCK generator (clock divider) circuitry (the only internal registers changing state when the BSM2 is not executing a scan operation) should be disabled by setting the value of the CDIV[2] bit of the CSC register to 1.

When these four actions have been taken, the power dissipation of the BSM2 will be less than 43 mW. This is mainly from the internal clock drivers switching the capacitive load of the clock tree.

BIST—Self-Test of the BSM2

Introduction

Definition and Classification of BIST in the BSM2

BIST for the BSM2 device must be clearly distinguished from system- or board-level BIST that can be carried out (e.g., using ATPG) or initiated through a B-S chain (e.g., by scanning a RUNBIST instruction into a device on a B-S chain) using the capabilities of the BSM2.

Since the BSM2 is designed to enhance board and system testability, it follows that the quality of the BSM2 itself must be very high. As in the previous design (497AA), both the memories (here the TVO and TVI FIFOs) and the random logic are designed to include Agere state-of-the-art BIST.

Memory BIST ensures 100% fault coverage over an extended fault model (well beyond the stuck-at fault model). The patented methodology used involves automatic insertion of BIST in regular structures. This BIST combines the characteristics of low overhead and complete absence of BIST signature aliasing (i.e., presence of a modeled fault will always cause a test failure).

The core portions of the random logic include partial-scan BIST (PSBIST) techniques giving 96% stuck-at fault coverage. Moreover, non-BIST scan techniques are used to raise fault coverage for manufacturing test.

All latches, flip-flops, etc. in the noncore logic are included in two full-scan paths used in manufacturing test.

95% of the circuitry in the BSM2 contains BIST features used in manufacturing test that can also be invoked by a controlling processor when the BSM2 is an assembled component in a board or system. The remaining 5% comprises sections of the processor interface and the CBIST register. Failure in either of these parts of the BSM2 can be rapidly detected by application software.

This section addresses the hardware self-test features built into the BSM2.

Three of the BSM2 self-test algorithms can be accessed by the user when the BSM2 is embedded in product. These algorithms are the memory self test, the random logic self-test, and memory retention tests. The last type is beyond the scope of this manual, and users desiring further information about it should contact Agere.

Impact on Connected Devices

When random logic BIST is activated in the BSM2, all of the TAP outputs and the USEROUTx signals are disabled (3-stated). This is not necessary (and not done) during memory BIST.

Memory BIST in the BSM2

Following memory BIST, memory in the BSM2 will have been corrupted; however, address pointers, etc. will retain their original values.

Random Logic BIST in the BSM2

Random logic BIST tests only the core combinational and registered logic of the design. Some of the peripheral I/O logic for communicating with the controlling processor operates in normal (nontest) mode throughout random logic BIST in order to allow communication of BIST status, etc.

When random logic BIST is running, the only register of the BSM2 that can be accessed by the controlling processor is the CBIST register. The other registers are locked and not unlocked until random logic BIST ends.

Random logic BIST o” is defined by the XECBIST bit having the value 1 and the RLSKP bit’s having the value 0. Random logic BIST off is defined by the XECBIST bit’s having the value 0 or the RLSKP bit’s having the value 1. Random logic BIST must be off in order read the correct result signature.

BUG (August, 1988): The RDY signal is disabled (3-stated) during random logic BIST and is not available for use in handshake with the controlling processor.

BIST—Self-Test of the BSM2 (continued)

Programming BIST in the BSM2

Initiating and Terminating BIST

In the BSM2, BIST is initiated by writing a 1 to the XECBIST bit in the CBIST register.

Writing a 0 to the XECBIST bit not only terminates a BIST operation, but also clears the DONE bits and initializes miscellaneous internal BIST control registers. Execution of BIST may be shut off at any time by writing a 0 to the XECBIST bit. After normal BIST termination, the XECBIST bit also should be set to 0.

Parameters Controlling BIST Execution

The parameters for running BSM2 self-test are programmed using the MEMSKIP, RLSKIP, and MEMRETE bits of the CBIST register.

If the value of the MEMSKIP bit is 1, the memory BIST operation will be skipped when BIST is executed. If the value of this bit is 0, then memory BIST will be activated when BIST is executed.

Similarly, if the value of the RLSKIP bit is 1, the random logic BIST operation will be skipped when BIST is executed. If the value of this bit is 0, then random logic BIST will be activated when BIST is executed.

If the value of the MEMRETE bit is 1, the memory BIST retention test will be included in the BIST execution. Otherwise, the retention test is skipped. Retention testing is normally done only during manufacture. This test checks for leakage paths that check the volatility of the memory. In order to carry out this test in the field, the master clock (TCKIN) must be stopped at particular intervals into the memory test. Contact Agere for further details regarding implementation of this test.

A pseudocode example of programming, executing, and terminating BSM2 BIST is included in Appendix A under the heading Programming Self-Test of the BSM2.

Appendix A—BSM2 Pseudocode Examples

Definitions of Terms

The following tables provide definition of terms used in the pseudocode examples of this appendix and descriptions of registers read and written in the pseudocode.

Table 3. Descriptions of Registers Accessed in the Pseudocode Examples

Register Abbreviation	Address (Decimal)	Size (Bits)	Register
CSC	00	16	Control-Scan/Clock register
CUTI	01	16	Control-USEROUT1/Test Data/Interrupt register
CUTO	02	16	Control-USEROUT0/TAP Function/Output Enable register
STAT	03	16	Status register
API	06	16	TVI Address pointer
APO	07	16	TVO Address pointer
TVX	13—12	32	TVX Counter register
IDLE	15—14	32	Idle Counter register
SAR	27—26	32	Signature Analysis register4

Table 4. Description of Operations Used in Pseudocode

Operation	Device	Description
Write to <register>	497AE	Write register address (8 bits) to BSM address 0. Write register data in 8-bit bytes (low order bits first) to BSM address 1 until entire value has been written.
	1215E	Write data directly to BSM register in 16-bit words.
Read from <register>	497AE	Write register address (8 bits) to BSM address 0. Read register data in 8-bit bytes (low order bits first) from BSM address 1 until entire value has been read.
	1215E	Write data directly to BSM register in 16-bit words.

Appendix A—BSM2 Pseudocode Examples (continued)

Initialize Device

```
Reset BSM2.
Write 0x1800 to CUTI
                                    /*Set EXEC bits to Reset [ bits 12-11 ]*/
Read STAT until DONE bit = 1.
                                    /*Wait for completion*/
Read SAR register.
                                    /*Check for valid signature*/
If signature = 0x0DAAD03B,
  then write 0x08 to CUTO
  else handle initialization failure
                                    /*Set TOEB bit to 1—enabling BSM2 output
                                    signals*/
                                    /*---------------------------------------*/
                                    /*Next, force all devices in TAP chain to
                                    Test-Logic-Reset by holding TMS high for 5
                                    TCK cycles.*/
Write 0 to TVX
                                    /*Clear scan counter*/
Write 5 to IDLE
                                    /*Set Idle count to 5 cycles*/
Write 0x1000 to CSC
                                    /*Set Idle/Scan/Destination Types to
                                    Test-Logic-Reset*/
Write 0x0820 to CUTI
                                    /*Set EXEC and TIOM bits for normal scan
                                    operation*/
Read STAT until DONE bit = 1
                                    /*Wait for completion*/
```

Appendix A—BSM2 Pseudocode Examples (continued)

Move to Stable State

```
                                    /*Cause TAP Controllers on selected/attached
                                    B-S chain to go to a specific Stable State
                                    (with or without delay). If a delay of x is
                                    specified, the processor will remain in the
                                    specified state for x TCK cycles before the
                                    DONE bit is set.*/
                                    /*---------------------------------------*/
                                    /*Specify state and delay value*/
Write 0 to TVX
                                    /*Clear scan counter*/
Write <x> to IDLE
                                    /*Set Idle count to x cycles*/
Write 0x<n>00 to CSC
                                    /*Set IDT, SCT, and DET bits:
                                       n=10, 0x1000 -Test-Logic-Reset
                                       n=35, 0x3500 -Run-Test/Idle
                                       n=46, 0x4600 -Pause-IR
                                       n=6f, 0x6f00 -Pause-DR*/
Write 0x0820 to CUTI
                                    /*Set EXEC and TIOM bits for normal scan
                                    operation */
Read STAT until DONE bit = 1
                                    /*Wait for completion*/
```

Appendix A—BSM2 Pseudocode Examples (continued)

Instruction Scan—Load Data in TVO, Unloaded from TVI

```
                                /*Scan data into Instruction Registers in
                                selected/attached B-S chain. Assume concate-
                                nated Instruction Registers have overall
                                length of 36 bits. Scan 36 bits—all 1's*/
                                /*--------------------------------------*/
                                Specify TAP Controller state in which scan is
                                to occur and TAP Controller state to be
                                stable state entered after scan*/
Write 0x0100 to CSC
                                /*Scan state is Scan-IR, Destination is
                                Run-Test/Idle*/
                                /*--------------------------------------*/
                                /*Specify number of bits to scan*/
Write 0x24 to TVX
                                /*Scan 36 bits*/
                                /*--------------------------------------*/
                                /*Specify start addresses in TVO and TVI*/
Write <x> to APO
                                /*Can use any address 0 - 511*/
Write <y> to API
                                /*Can use any address 0 - 511*/
                                /*--------------------------------------*/
                                /*Write instruction data to TVO FIFO*/
Write 0xFFFF to TVO FIFO
                                /*Write first 16 bits*/
Write 0xFFFF to TVO FIFO
                                /*Write second 16 bits*/
Write 0x000F to TVO FIFO
                                /*Write last 4 bits. Note: low order bits
                                scanned first*/
                                /*--------------------------------------*/
                                /*Start Scan*/
Write 0x0820 to CUTI
                                /*Set EXEC and TIOM bits for normal scan
                                operation*/
Read STAT until DONE bit = 1.
                                /*Wait for completion*/
                                /*--------------------------------------*/
                                /*Read output data from TVI FIFO*/
Read 16 bits from TVI FIFO
                                /*Read first 16 bits*/
Read 16 bits from TVI FIFO
                                /*Read second 16 bits*/
Read 16 bits from TVI FIFO
                                /*Read last 4 bits. Low order bits are
                                scanned data. Other 12 bits are junk*/
```

Appendix A—BSM2 Pseudocode Examples (continued)

Data Scan—Data Loaded/Unloaded in Loop

```
                                    /*Scan data into Data Registers of devices in
                                    selected/attached B-S Chain. Maximum amount
                                    of data that can be scanned by this method is
                                    2**32 - 1 bits*/
                                    /*-------------------------------------*/
                                    /*Specify state in which scan is to occur and
                                    stable state to enter after scan*/
  Write 0x8900 to CSC
                                    /*Gate TCK on FIFO under-/overflow. Scan
                                    state is Scan-DR, Destination is
                                    Run-Test/Idle*/
                                    /*-------------------------------------*/
                                    /*Specify number of bits to scan*/
  Write <n> to TVX
                                    /*Scan n bits*/
  Copy <n> to local_counter         /*User must keep track of amount of data
                                    written to TVO buffer*/
                                    /*-------------------------------------*/
                                    /*Specify starting addresses to use in TVO
                                    and TVI buffers*/
  Write x to APO
                                    /*Can use any address 0 - 511*/
  Write y to API
                                    /*Can use any address 0 - 511*/
                                    /*-------------------------------------*/
                                    /*Start Scan*/
  Write 0x0820 to CUTI
                                    /*Set EXEC and TIOM bits for normal scan
                                    operation*/
                                    /*-------------------------------------*/
                                    /*Loop until scan complete*/
  Begin loop
    Read STAT.
    If DONE bit = 1 and TVIM bit = 1,
      exit loop.
                                    /*Exit if scan completed and TVO FIFO empty*/
    If local_counter > 0 and TVOU bit = 0,
      then write word of data to TVO FIFO
                                    /*Write 16 bits of data to TVO FIFO if it is
                                    not yet full.*/
    If TVIM bit = 0,
      then read next word of output data from TVI FIFO
                                    /*Read 16 bits from TVI FIFO if
                                    it is not yet empty*/
    Subtract 16 from local_counter.
    Return to top of loop.
  Done
```

Appendix A—BSM2 Pseudocode Examples (continued)

Setting up and Running an ATPG Algorithm

The following pseudocode illustrates the selection of an ATPG algorithm, the writing of seeds values to the pseudo-random pattern generating register (PRPG) and to the signature analysis register (SAR), and the initiation of the ATPG algorithm, and the reading of the resulting signature from the SAR.

The pseudocode is for the test of a board with seven nets and applies a walking-ones test. Each net's inputs and outputs are described with i's and o's. The board contains two devices. Each has an instruction register length of eight bits and a boundary-scan register length of 18 bits. A description of translation of circuit net list to BSM2 ATPG control information is beyond the scope of this manual.

Other relevant data for the chip follows. A control cell that must be maintained in the logic 1 state is indicated by an h.

Sample Opcode: `00000010 - 00000010`

Extest Opcode: `11111111 - 11111111`

Safe Value: `hh xxxx xxxx xxxx xxxx - hh xxxx xxxx xxxx xxxx`

Net 1: `xx xxxx xxxo xxxi xxxx - xx xxxx xxxx xxxx xxxx`

Net 2: `xx xxxx xxox xxix xxxx - xx xxxx xxxx xxxx xxxx`

Net 3: `xx xxxx xoxx xixx xxxx - xx xxxx xxxx xxxx xxxx`

Net 4: `xx xxxx oxxx ixxx xxxx - xx xxxx xxxx xxxx xxxx`

Net 5: `xx xxxx xxxx xxxx xxxx - xh xxxo xxxo xxix xxxx`

Net 6: `xx xxxx xxxx xxxx xxxx - xh xxox xxox xixx xxxx`

Net 7: `xx xxxx xxxx xxxx xxxx - xh xoxx xoxx ixxx xxxx`

```
Scan Sample Opcodes into instruction registers
Scan Safe Values into data registers
Scan Extest Opcodes into instruction registers
Preload TVO/TVI memory with code describing nets
                                /*these codes can be automatically generated
                                from the above net descriptions*/
                                /*-------------------------------------*/
                                /*Select location in TVO memory*/
Write <address> to APO
                                /*-------------------------------------*/
                                /*Write coded data to TVO memory*/
Write 0x00E0 to TVOR
Write 0x03C1 to TVOR
Write 0x0000 to TVOR
                                /*Only low order 4 bits are significant*/
                                /*-------------------------------------*/
                                /*Select same location in TVI memory*/
Write <address> to API
```

Appendix A—BSM2 Pseudocode Examples (continued)

Setting up and Running an ATPG Algorithm (continued)

```
                                    /*---------------------------------------*/
                                    /*Write coded data to TVI memory*/
    Write 0x881F to TVIR
    Write 0xC03F to TVIR
    Write 0xFFFF to TVIR
                                    /*Only low order 4 bits are significant*/
                                    /*---------------------------------------*/
                                    /*Specify number of nets to be tested (7)*/
    Write 7 to NCR
    Write 7 to LPC
                                    /*---------------------------------------*/
                                    /*Specify scan size (36)*/
    Write 0x24 to SDR
                                    /*---------------------------------------*/
                                    /*Clear Signature Analysis Register*/
    Write 0x0 to SAR
                                    /*---------------------------------------*/
                                    /*Set Control-Scan/Clock Register (Scan state
                                    Scan_DR, Terminate in Run-Test/Idle)*/
    Write 0x900 to CSC
                                    /*---------------------------------------*/
                                    /*Set Start Scan process (Normal Execute,
                                    ATPG Mode Walking-One, Source ATPG,
                                    Destination SAR, SSME on, auto-increment on
                                    TVO and TVI)
    Write 0x973 to CUTI
                                    /*---------------------------------------*/
                                    /*Wait for completion*/
    Read STAT until DONE bit is set
                                    /*---------------------------------------*/
                                    /*Read test result signature*/
    Read SAR - should be 0xBF13C204
                                    /*Value can be precalculated based on net
                                    description*/
```

Appendix A—BSM2 Pseudocode Examples (continued)

Switching Between B-S Chains

Depending on the architecture, a single BSM2 device could control several B-S chains. The design would need to allow switching between the B-S chains—enabling the TAP signals for each B-S chain as needed. The Addressable Scan Port (ASP) protocol and interface definition (e.g., supporting *TI*'s ASP devices) is one example of such an architecture. For the purpose of this example, we assume a single BSM2 is controlling two different B-S chains, A and B, via enabling circuitry EA and EB, respectively.

EA and EB could be enabled via the ASP protocol, which will not be shown here.

After reset, both chains A and B have TAP controllers in their Test-Logic-Reset TAP Controller state. The BSM2 internal TAP State Tracker is in its corresponding state. Both EA & EB are disabled.

First we perform an instruction register scan to chain A with a destination of Run-Test/Idle:

```
Enable EA
                                    /*Enable B-S chain A*/
Write 0x0100 to CSC
                                    /*Scan state is Scan-IR, Destination
                                    state is Run-Test/Idle*/
Write <n> to TVX
                                    /*Scan n bits*/
Write <data> to TVO FIFO
                                    /*Write n bits to FIFO*/
Write 0x0820 to CUTI
                                    /*Start scan*/
Read STAT until DONE bit = 1
Read <data> from TVI FIFO
                                    /*Read n bits from FIFO*/
                                    /*Now B-S chain A is at destination
                                    Run-Test/Idle*/
                                    /*---------------------------------------*/
```

Now we send an identical instruction to chain B with a destination of Run-Test/Idle.

```
Disable EA
                                    /*Disable B-S chain A*/
                                    /*Move the BSM2 TAP State Tracker to
                                    Test-Logic-Reset before enabling chain B*/
Write 0x0000 to CSC
                                    /*Destination state is Test-Logic-Reset*/
Write 0x1000 to CUTI
                                    /*Execute Jump to Destination command*/
                                    /*This command will immediately set the
                                    internal TAP State Tracker to
                                    Test-Logic-Reset so that it matches the
                                    TAP controller state of B-S chain B*/
Enable EB
                                    /*Enable B-S chain B*/
                                    /*---------------------------------------*/
                                    /*Send a Shift-IR scan to chain B with a
                                    destination of Run-Test/Idle.*/
```

Appendix A—BSM2 Pseudocode Examples (continued)

Switching Between B-S Chains (continued)

```
Write 0x0100 to CSC
                                    /*Scan state is Scan-IR, Destination
                                    state is Run-Test/Idle*/
Write <n> to TVX
                                    /*Scan n bits*/
Write <data> to TVO FIFO
                                    /*Write n bits to FIFO*/
Write 0x0820 to CUTI
                                    /*Start scan*/
Read STAT until DONE bit = 1
Read <data> from TVI FIFO
                                    /*Read n bits from FIFO*/
```

Appendix A—BSM2 Pseudocode Examples (continued)

Programming Self-Test of the BSM2

Table 5. Register Descriptions (Advanced Operational Mode/497AA Compatible Mode) Relevant to BSM2 BIST

Register Abbreviation	Address (Decimal)	Size (Bits)	Register
CBIST	5/46	16	Control BIST register
BSR	14-15/47	32	BIST Signature register

To run Memory BIST only:

```
Write to CBIST 0x001a
                                    /*interrupt enabled, execute, skip RLBIST*/
Wait for 12,500 TCKIN clock cycles or interrupt.
Read CBIST compare to 0x039a
                                    /*all done bits high, signature 0, interrupt
                                     enabled, execute bit on, skip RLBIST*/
If signature (upper 6 bits) doesn't compare to 0,
  then Memory BIST failure.
Write to CBIST 0x0000
                                    /*everything off*/
Reset device
Done
```

To run Random Logic BIST only:

```
Write to CBIST 0x0019
                                    /*interrupt enabled, execute, skip
                                     memory BIST*/
Wait for 1,050,000 TCKIN clock cycles or interrupt.
Read CBIST compare to 0x0399
                                    /*all done bits high, signature 0, interrupt
                                     enabled, execute bit on, skip memory BIST*/
Write to CBIST 0x0000
                                    /*everything off*/
Read BSR and compare to 0x000bdb3a
  if signature doesn't compare,
  then Random Logic BIST failure.
Reset device
Done
```

To run both back to back:

```
Write to CBIST 0x0018
                                    /*interrupt enabled, execute*/
Wait for 1,062,500 TCKIN clock cycles or interrupt.
```

Appendix A—BSM2 Pseudocode Examples (continued)

Programming Self-Test of the BSM2 (continued)

```
Read CBIST and compare to 0x0398
                                    /*all done bits high, signature 0,
                                     interrupt enabled, execute bit on*/
If signature (upper 6 bits) doesn't compare to 0,
  then Memory BIST failure.
Write to CBIST 0x0000
                                    /*everything off*/
Read BSR and compare to 0x000bdb3a
  if signature doesn't compare,
  then Random Logic BIST error.
Reset device
Done
```

Appendix B—BSM2 Internal Register Descriptions

General Introduction and Conventions

The BSM2 contains a number of 16-bit and 32-bit registers through which it is programmed and from which results and status of BSM2 operation can be read. The means of addressing these registers (indirectly and directly) and the details of reading and writing these registers are detailed under the heading BSM2 Register Addressing, Reading, and Writing.

In each of the subsections of the present appendix, the functionality of a BSM2 internal register (BIR) is described in detail. The main purpose and the format (bit assignments) of each BIR is also given. The address of each 16-bit word of each BIR is provided in octal notation.

Note: There is no register defined with addresses 23 and 30—40 (octal).

The default values of the registers (if any) are specified. These values correspond to the initial states of the registers immediately upon device reset or powerup, and they are presented in hexadecimal notation unless indicated otherwise.

The following conventions are used in this section:

- BIR[*a*] refers to the BSM2 register with the octal address value *a*. This applies in both the cases of direct and indirect register addressing.
- SIG_NAME, BIR[*a*, *b*] indicates that the signal SIG_NAME resides in the b^{th} bit of the BIR with address *a*. In this case, *b* is a decimal integer and *a* is octal.
- In graphical presentations of registers, the most significant bit is presented on the left.

Note: In the following register descriptions only those bits that are read-only bits will be indicated. All are other bits are both readable and writable by the controlling processor.

Note: The CMU (Control-MASK/USEROUT0(1)register—involved in control of internal connection of BSM2 register bits to the user I/O pins of the BSM2) is active only in the 48-pin package—the 1215E.

Throughout this section, an X denotes a “don’t care” bit or an undefined state. The register address space is incompletely specified so as to allow for possible future increases in the number of BIRs.

Unused Addresses

There are ten unused addresses—23 and 30—40 (octal). Writing to an illegal address will have no effect on the contents of any BIR. Reading from an illegal address will result in undefined data, and will have no effect on the contents of any BIR.

Classification of Registers

When learning the use of the BIRs, it may be helpful to remember that BIRs are of two types:

- Registers used in the programming of scanning tasks (writing to these registers does not cause an immediate effect)
- Registers that are not associated directly with a scanning task, but facilitate altering the configuration of the BSM2 (writing to these registers causes an immediate effect described in the relevant register descriptions, below).

In the 497AE, register addressing is managed through a register (PTR) that is not a BIR.

BSM2 Register Addressing, Reading, and Writing

All registers are readable in the Advanced Operational Mode.

Data Bus Widths

The 1-bit data bus width supported in the 497AA is *not supported* in the 1215E and is *not supported* in the 497AE in Advanced Operational Mode. The data bus is 8 bits wide in the 497AE (see Appendix C—BSM2 (497AE) Data Sheet) and 16 bits wide in the 1215E (see Appendix D—BSM2 (1215E) Data Sheet).

Address Bus Width

The 497AE external address bus comprises 1 bit. This entails indirect addressing of internal registers (see below). The 1215E external address bus is 5 bits wide allowing direct addressing of internal registers.

Appendix B—BSM2 Internal Register Descriptions (continued)

BSM2 Register Addressing, Reading, and Writing (continued)

497AE Addressing (Indirect)

Addressing in the 497AE is accomplished in two steps. First the PTR register must be selected by driving the RA pin of the 497AE to 0. The first subsequent write to the 8-bit data bus (D[0:7]) will be taken to be the address of the BIR to be accessed. Only the 5 low order bits of the byte written will be decoded as a BIR address.

497AE Register Size, Byte Transfer, and Synchronization of Reads and Writes

The 8-bit data bus of the 497AE can accommodate only single-byte read and write operations. A BIR can have a length of 2 or 4 bytes. As a result, access to an n-byte BIR normally takes exactly n consecutive single-byte bus cycles to complete. The order of transfer is from the lowest-order byte to the highest-order byte.

To enable the controlling processor to synchronize multibyte data transfers, all BIRs are designed such that whenever the processor writes into the PTR, the lowest-order byte of the selected BIR will always be the first byte to be transferred in a subsequent BIR read or write operation—regardless of any prior byte transfers. So if, in error, a user's microcode transfers 3 bytes to a 4-byte register, writing the PTR will always produce resynchronization and ensure that the next read or write will start with the lowest-order byte of the next register target.

Even though the user may be confident that resynchronization is easily achieved, it may be necessary to know the results when insufficient bytes have been transferred to achieve the full writing of some register. Assume that m < n. Then, the effect of an m-byte transfer to or from an n-byte BIR (occurring between any two consecutive PTR writes) varies according to the following conditions:

- If the BIR is either TVOR or TVIR, then the contents of the internal memory buffer (TVO or TVI) as well as the address pointer (APO or API) will be unchanged by the incomplete write. All TVOR and TVIR data transfers must occur in multiples of 16-bit words.
- Otherwise, the least significant m bytes of the BIR will have been written if the transfer was a write operation. The higher n-m bytes of the BIR will have retained the values they held prior to the incomplete write operation. In other words, with 8-bit bus size selected, all BIR write operations are byte-effective—they alter contents of a BIR along the byte boundaries.

A memory buffer (FIFO) example: to write into the 2-byte TVOR, a total of two single-byte write cycles are required, starting with the first byte (byte 0). The entire word in the TVOR is written into the TVO memory only after the second byte (byte 1) has been written into the TVOR. If, for some reason, the processor selected another BIR (through a PTR write) just after the transfer of the first byte (byte 0), then data transfer would restart with the first byte (byte 0) of the newly selected BIR (byte transfer is thus resynchronized). Moreover, the contents of the TVOR (partially altered) would not have been written into the TVO.

A nonmemory buffer (FIFO) example: had the BIR in question been SAR instead of TVOR, the first byte would have been written into the lowest-ordered byte (byte 0) of the SAR. The remaining 3 bytes of the SAR (byte 1—byte 3) would have retained the values they held prior to the incomplete write operation.

1215E Addressing (Direct)

The address of the register to be read or written is written to the 5-bit address bus (RA[0:4]). The address is directly decoded; and the addressed BIR, selected.

1215E Data Reads and Writes

In the 1215E, a 32-bit register is accessed via two sequential address operations on the RA[0:4] bus. Data transfer occurs on 16-bit word boundaries by reading to, or writing from, the 16-bit data bus (D[0:15]). The 1215E differs from the 497AE in that the latter latches an address and automatically indexes it as a read or write requires.

Timing of events associated with reading and writing specific registers is addressed in the following section.

Timing of Actions Resulting from Writing Registers

Actions Taken Upon Writing a Register (497AE Synchronous Operation)

An action programmed by means of writing to a BIR occurs on the second *positive* edge of TCKIN after CE* goes active (is driven to 0) following latching of the input data. See Figure 8 and Figure 16.

Actions Taken Upon Writing a Register (Asynchronous Operation—497AE and 1215E)

An action programmed by means of writing to a BIR occurs on the second *positive* clock edge after CE* goes inactive (is driven to 1).

Appendix B—BSM2 Register Descriptions (continued)

PTR: Pointer Register

Purpose

Provides the indirect addressing capability for the 497AE. There is no corresponding register in the 1215E which only supports direct addressing.

Address

The access to this register is governed by the RA pin in the 497AE. Further information will be found above, under the heading BSM2 Register Addressing, Reading, and Writing.

Format

04—00
PTR[4:0]

Default (Hex)

PTR = 0000

Read-only Bits

None

Appendix B—BSM2 Register Descriptions (continued)

CSC: Control-Scan/Clock Register

Purpose

Provides processor access to and control of various parameters of the scan operation of the BSM2 and of the low power mode of the BSM2.

Address (Octal)

00

Format

15	14—13	12—10	09—08	07—04	01	02—00
GCLK	IDT[1:0]	SCT[2:0]	DET[1:0]	RTD[2:0]	LP	CDIV[2:0]

Default (Hex)

CSC = 0000

Read-only Bits

None

Description

GCLK (Gated Clock Bit)—A 0 in this bit causes the BSM2 to bring the TAPs of devices on the selected/attached B-S chain into the Pause-IR or Pause-DR TAP Controller state automatically when the 8K bit input (output) buffers experience overflow (underflow) during an instruction or data register scanning sequence. A 1 in this bit causes the BSM2 to halt operation of the TAP Controllers of devices on the currently selected/attached B-S chain by fixing the state of (gating) the TCK signal feeding the B-S chain.

IDT[1:0] (Idle Type Bits)—These two bits encode the name of a TAP Controller state. The values of the two bits only have effect when the IDLE counter is nonzero. During a scan operation, if the IDLE counter is nonzero, the first time the TAP Controller state designated by IDT[1:0] is reached (as monitored by the state of the TAPS bits of the status (STAT) register), the IDLE counter will be activated and begin downcounting. The BSM2 will hold the TAP Controller states of all devices on the selected/attached B-S chain in the designated state until the IDLE counter contains 0. Then the scan operation programmed into the BSM2 will continue. If a scan operation is defined involving a sequence of TAP Controller states that does not include the then defined Idle TAP Controller state, there will be no effect from the setting of IDT[1:0].

Designated Idle TAP Controller State	IDT1	IDT0
Test-Logic-Reset	0	0
Run-Test/Idle	0	1
Pause-IR	1	0
Pause-DR	1	1

Note: For ATPG operation, the IDLE counter register should be set to zero, disabling the IDT bits.

Appendix B—BSM2 Register Descriptions (continued)

CSC: Control-Scan/Clock Register (continued)

SCT[2:0] (Scan Type Bits)—These three bits encode the name of a TAP Controller state. The state designated by SCT[2:0] is the one in which shifting via TDI/TDO will occur during a scan operation. (See The BSM2 Scan Process.)

Designated Scan Type	SCT2	SCT1	SCT0
Shift-IR	0	0	0
Pause-IR	0	0	1
Shift-DR	0	1	0
Pause-DR	0	1	1
Test-Logic-Reset	1	X	0
Run-Test/Idle	1	X	1

Note: These bits must be set for Shift-DR scan type (010) for ATPG operation.

DET[1:0] (Destination Type Bits)—These two bits encode the name of a TAP Controller state. The state designated by DET[1:0] is the stable state in which the current or next scan operation will terminate. The BSM2 takes advantage of the fact that TAP Controllers of a selected/attached B-S chain can remain indefinitely in stable states with the clock signal on the TCK pin of a TAP running. (See The BSM2 Scan Process or Automatic Test Pattern Generation (ATPG), Scan Sequence Modification (SSM), and Signature Analysis.) These bits determine the terminal state of a scan operation whether or not ATPG is employed.

Destination TAP Controller State	DET1	DET0
Test-Logic-Reset	0	0
Run-Test/Idle	0	1
Pause-IR	1	0
Pause-DR	1	1

Note: These bits must be set for either the Test-Logic-Reset or Run-Test/Idle destination TAP controller states (i.e., set to 00 or 01) for ATPG operation.

RTD[3:0] (Retimed Delay Control Bits)—Values written to these bits provide control of the BSM2 retimed delay control for electrically distant B-S chains. According to the decimal value of the four bits, RTD[3:0] provides for from 0 to 11 cycles of TCK delay as described in the section on Retimed Delay Support.

LP (Low Power Mode Bit)—A 0 in this bit causes the BSM2 to place itself in its normal operational mode. In this mode, its TCK divider registers are enabled even when the part is otherwise idle. A 1 in this bit causes the BSM2 to place itself in low power mode with its TCK divider registers disabled (off).

Appendix B—BSM2 Register Descriptions (continued)

CSC: Control-Scan/Clock Register (continued)

CDIV[2:0] (Clock Divider Control Bit)—Values written to these three bits provide control over the TCK generator—a divider of the Master Clock signal to the BSM2. The value of the three bits is bitwise complemented and then (converting to decimal notation) employed as the exponent of 2 to generate the value 2^n by which the Master Clock signal is to be divided.

CDIV[2:0] (binary)	Complement of CDIV[2:0] (binary)	2^n (decimal)
000	111	128
001	110	64
010	101	32
011	100	16
100	011	8
101	010	4
110	001	2
111	000	1

Appendix B—BSM2 Register Descriptions (continued)

CUTI: Control-USEROUT1/Test Data/Interrupt Register

Purpose

Provides means by which an external processor may (a) control BSM2 internal connection, BSM2 ATPG algorithm selection, and other means to effect output values on USEROUT1 and TDO and (b) enable/disable interrupts indicating data overflow or underflow conditions, and (c) place the BSM2 in single step or TAP Manual Mode. Application of elements of this register that control ATPG algorithm behavior is explained under the heading BSM2 Registers Related to ATPG. Applications related to scan sequence modification are explained under the heading Scan-Sequence Modifier (SSM). Application to TDO signal value modification is explained under the heading TDO Inversion.

Note: CUTI[7:0] has the same function as in the TVMR register of the original BSM with the exception that the TAP I/O Mode Bits (TIOM) now require three bits instead of two (as in the Test Resource Control Bits of the 497AA).

Address (Octal)

01

Format

15	14	13	12—11	10	09—08	07—05	04	03	02	01—00
USR1	OUIM	WDIM	EXEC[1:0]	MAN	AMD[1:0]	TIOM[2:0]	SSME	AC	TC	AINC[1:0]

Default (Hex)

CUTI = 0000

Read-only Bits

None

Description

USR1 (USEROUT1 Control Bit)—The value of USR1 feeds the OR tree that drives USEROUT1 in the 1215E. When the value of the USR1 bit is 1, the BSM2 USEROUT1 pin will take the value of 1. When the value of this bit is 0, the value of USEROUT1 pin is 0 unless one or more of the inputs to the OR tree is driving the value 1. When USR1 is 0, the value of USEROUT1 may be interpreted as an interrupt (active when equal to 1) accessible by a controller (e.g., a DMA controller) other than the controlling processor. The USR1 bit has no effect in the 497AE.

OUIM (Data Over/Underflow Interrupt Mask Bit)—In order for the BSM2 to issue an interrupt—in order for the INT* pin to be active—in the cases of over/underflow of the test data memories (FIFOs), this pin must be set equal to 1. If this bit is set and either of the TVOM or TVIU bits of the status register = 1, then the INT* pin will be active. See the description of the WDIM bit, below.

WDIM (When Done Interrupt Mask Bit)—In order for the BSM2 to issue an interrupt—in order for the INT* pin to be active—in the case of the DONE bit of status register being set, this bit must be set equal to 1. If the value of this bit is 1, then an interrupt is enabled when the DONE bit is 1.

Appendix B—BSM2 Register Descriptions (continued)

CUTI: Control-USEROUT1/Test Data/Interrupt Register (continued)

EXEC[1:0] (Execution Bits)—These bits provide the means by which execution of a programmed scan operation is controlled/initiated. These bits only have effect when the value of the MAN bit (below) is 0.

EXEC[1]	EXEC[0]	Meaning
0	0	Do not execute.
0	1	Initiate normal execution of scan operation.
1	0	Jump to scan operation destination state and halt execution.
1	1	Reset device.

These bits are readable; however, executing the jump or reset operations (writing either the pattern 10 or the pattern 11) immediately resets the bits back to 00. In other words, the patterns 10 and 11 can never be read from the EXEC bits. The pattern 01 (normal operation) is static—can be read when it is loaded in the EXEC bits.

MAN (TAP Manual Bit)—When the value of this bit is 1, single step scan operation (via programming of the CUT0 register) is enabled. The single step operation is called TAP Manual Mode. When operating in this mode, the gated clock bit (GCLK, register CSC) must be set to 0.

AMD[1:0] (ATPG Mode Bits)—With these two bits, one of the ATPG algorithms of the BSM2 is selected. These bits correspond to register CFGR[1:0] of the original BSM. Combined with the AC bit (CUTI[03]), the selected algorithm's output can be inverted before being scanned into the B-S chain currently selected/attached to/by the BSM2.

AMD[1]	AMD[0]	AC = 0	AC = 1
0	0	upcount sequence	downcount sequence
0	1	walking 1	walking 0
1	0	pseudorandom	inverted pseudorandom
1	1	constant 0	constant 1

TIOM[2:0] (TAP I/O Mode Bits)—With these three bits, mode of test of the selected/attached B-S chain is determined. The TIOM bits provide flexibility for deterministic scan operations (see page 11), for ATPG operation (see Scan-Sequence Modifier (SSM) and Programming ATPG and SSM Functions), and for recirculation mode—direct connection of TDI to TDO within the BSM2 device (see Recirculation Scan).

TIOM[2:0]	Type of Scan Operation	Source of TDO	Destination of TDI	TVO	TVI
000	Apply stimulus, ignore results	TVO	ignore; TDI off	→TDO	off
001	Normal scan operation	TVO	TVI	→TDO	TDI→
010	SSM mode with TVO as data source and SAR as data destination	TVO	SAR	→TDO	off
011	SSM mode with ATPG as data source and SAR as data destination	ATPG	SAR	->SSM (if enabled)	
100	Response only	no source; TDO off	TVI	off	TDI→
101	Recirculate mode (TDI -> TDO)	TDI	TDO	off	off
110	Illegal—don't use	—	—	—	—
111	Recirculate with response only	TDI	TDO & TVI	off	TDI→

WARNING: The pattern 110 is illegal in the TIOM bits. The loading of 110 in the TIOM bits will result in unpredictable operation.

Appendix B—BSM2 Register Descriptions (continued)

CUTI: Control-USEROUT1/Test Data/Interrupt Register (continued)

SSME (Scan Sequence Modifier Enable Bit)—This bit determines whether the SSM feature is to be enabled (SSME = 1) or disabled (SSME = 0). Enabling the SSM means that the values scanned out of the selected/attached B-S chain will be received by the signature analysis register. Specialized use of TVI (for ATPG or deterministic testing) and TVO (for ATPG only) is made. This is described under the headings Scan-Sequence Modifier (SSM) and Programming ATPG and SSM Functions.

AC (ATPG Complement Bit)—If the value of this bit is 1 (0), the algorithmic test vectors generated by the ATPG will (will not) be complemented before being transmitted via TDO. The AMD bits (CUTI[09:08]) select the ATPG algorithm to be applied.

TC (TVO Complement Bit)—If the value of this bit is 1 (0), the test vectors stored in the TVO will (will not) be complemented before being transmitted via TDO.

AINC[1] (TVI/TVO Address Increment Enable Bit 1)—If the value of this bit is 1, the TVI Address Pointer (API) will be autoincremented each time a complete 16-bit TVI word has been transferred. If the value of this bit is 0, then API will remain unchanged during any TVI access. Except during ATPG operation of the BSM2, this bit is ignored.

WARNING: This bit must be set during execution of an ATPG-based test. Otherwise the first word in the TVI buffer will be used repeatedly producing an incorrect B-S chain map and possibly causing undesirable or damaging states to appear in control cells along the B-S chain during the test.

AINC[0] (TVI/TVO Address Increment Enable Bit 0)—If the value of this bit is 1, the TVO Address Pointer (APO) will be autoincremented every time a complete 16-bit TVO word has been transferred. If the value of this bit is 0, APO will remain unchanged during any TVO access. Except during ATPG operation of the BSM2, this bit is ignored.

WARNING: This bit must be set during execution of an ATPG-based test. Otherwise the first word in the TVO buffer will be used repeatedly producing an incorrect B-S chain map and possibly causing undesirable or damaging states to appear in control cells along the B-S chain during the test.

Appendix B—BSM2 Register Descriptions (continued)

CUTO: Control-USEROUT0/TAP Function/Output Enable Register

Purpose

Provides means by which a selected/attached B-S chain can be operated in TAP Manual Mode. (TAP Manual Mode is entered by writing a 1 to the MAN bit of the CUTI register.) Provides means of control for the TRST* and USEROUT0 pins (1215E only). Provides means of overriding enabling/disabling of TDO output pin.

Address (Octal)

02

Format

15—08	07	06	05	04	03	02	01	00
unused	TDIM	unused	USR0	TRSTB	TOEB	TDOM	TMSM	TDOEM

Default (Binary)

CUTO = 000000000*t*0000000, where *t* is the value on the TDI pin. If the BSM2 is not in TAP Manual Mode, then the values of the TDOM, TMSM, and TDOEM bits have no effect, although such values will have significance when the TAP Manual Mode is selected.

Read-only Bits

CUTO[7] is read-only.

Description

TDIM (TDI Manual Mode Bit)—In TAP Manual Mode, the value read from this bit is the last value of the TDI signal received by the BSM2. The TDI signal is not latched, but feeds the TDIM bit directly. The value is captured when a read of the CUTO register occurs according to the section titled Control of TDI, TDO, TMS, and TRST* pins.

USR0 (USEROUT0 Control Bit)—The value of USR0 feeds the OR tree that drives USEROUT0 in the 1215E. When the value of the USR0 bit is 1, the BSM2 USEROUT0 pin will take the value of 1. When the value of this bit is 0, the value of USEROUT0 pin is 0 unless one or more of the inputs to the OR tree is driving the value 1. When USR0 is 0, the value of USEROUT0 may be interpreted as an interrupt (active when equal to 1) accessible by a controller (e.g., a DMA controller) other than the controlling processor. The USR1 bit has no effect in the 497AE.

TRSTB (TAP Reset Control Bit)—When the value of this bit is 1, all TAP Controllers in a selected/attached B-S chain will be reset. The internal TAP State Tracker is also reset. The use of this bit is not restricted to TAP Manual Mode. This bit may be used judiciously to halt execution of a scan operation.

Appendix B—BSM2 Register Descriptions (continued)

CUTO: Control-USEROUT0/TAP Function/Output Enable Register (continued)

TOEB (TDO Output Enable Control Bit)—In applications in which the TAP output signals must be 3-stated, a user has the option of selecting this function either through hardware (TOE* pin in 1215E) or software (using the TOEB bit). The value of the TOEB bit is ORed with the inverted value of the BSM2 TOE* pin (in the 1215E) and with a constant 0 (in the 497AE). When the resulting value (TOEB_internal) is 1, all TAP output pins of the BSM2 except TDO are enabled. TDO is enabled in two ways:

1. In the TAP Manual Mode, both TOEB_internal and TDOEM must be in their active states (1 in both cases).
2. When not in the TAP Manual Mode, the automatic enable/disable of TDO described in the Standard is in effect when TOEB_internal has the value 1.

The TOEB bit in the 1215E gives the user the option of either software or hardware control over the TAP output enable/disable function. This function may be especially useful if the user plans to switch or share TAP buses.

Note: In the 497AE, the TAP outputs will never be enabled (not in any mode) unless the TOEB bit is set. This is because there is no TOE* pin on the 497AE to give a hardware option for TAP output enable control. There is no BSM2 internal sanity check for this item. It is the user's responsibility.

TDOM (TDO Control Bit for TAP Manual Mode)—In TAP Manual Mode, the value of this bit is the next value of the signal to be driven on the BSM2 TDO pin. The value is driven following a write of the CUT0 register according to the section titled Control of TDI, TDO, TMS, and TRST* pins.

TMSM (TMS Control Bit for TAP Manual Mode)—In TAP Manual Mode, the value of this bit is the next value of the signal to be driven on the BSM2 TMS pin. The value is driven following a write of the CUT0 register according to the section titled Control of TDI, TDO, TMS, and TRST* pins.

TDOEM (TAP Output Enable Control Bit for TDO in TAP Manual Mode)—This bit is only active in TAP Manual Mode. When the value of this bit is 1, the TDO signal is enabled if the TOEB bit is also active (above). The BSM2 does not check for sanity in TAP Manual Mode. The user is responsible for enabling TDO only at desired/appropriate times.

Appendix B—BSM2 Register Descriptions (continued)

STAT: Status Register

Note: In the case of the 28-pin package (479AE), the masking function (see CMU description register below and the topic Masking USEROUTX in the part description above) has no function.

Purpose

Provides status information concerning whether the Test Data Memories (FIFOs) are full or empty (with masking capability for these bits in the 1215E), the state currently recorded by the TAP State Tracker, the status (zero or not) of the TVX counter and IDLE counter registers, the status of the most recently executed scan test (done or not), and the current value of the USERIN signal (1215E only).

Address (Octal)

03

Format

15	14	13	12	11—08	07	06	05	04	03	02	01	00
TVOU–1	TVOM+1	TVIU–1	TVIM+1	TAPS[03:00]	USRN	IDL0	TVX0	DONE	TVOU	TVOM	TVIU	TVIM

Default (Binary)

STAT = 00000000*u*1110101, where *u* is the value on the USERIN pin (1215E) or 1 (497AE).

Read-only Bits

All

Description

TVOU-1 (TVO Full - 1 Bit)—The value of this bit is 1 if and only if the TVO FIFO is exactly one word of data short of full.

TVOM+1 (TVO Empty + 1 Bit)—The value of this bit is 1 if and only if the TVO FIFO contains exactly one word of data.

TVIU-1 (TVI Full - 1 Bit)—The value of this bit is 1 if and only if the TVI FIFO is exactly one word of data short of full.

TVIM+1 (TVI Empty + 1 Bit)—The value of this bit is 1 if and only if the TVO FIFO contains exactly one word of data.

Appendix B—BSM2 Register Descriptions (continued)

STAT: Status Register (continued)

TAPS[3:0] (TAP State Bits)—These four bits encode the current state of the TAP controllers of devices on the currently selected/attached B-S chain. The STAT register is read-only. The only way these bits will be altered is by the TAP State Tracker, or by executing the Jump Command or the Reset Command (see description of the Execution Bits in the CUTI register). In response to the Jump Command (page 12), the TAPS bits immediately record the destination TAP Controller state. The encoding used is as follows:

TAPS[3:0] Value	Current TAP Controller State
0000	Test-Logic-Reset
0001	Select-DR-Scan
0010	Capture-DR
0011	Shift-DR
0100	Exit1-DR
0101	Pause-DR
0110	Exit2-DR
0111	Update-DR
1000	Run-Test/Idle
1001	Select-IR-Scan
1010	Capture-IR
1011	Shift-IR
1100	Exit1-IR
1101	Pause-IR
1110	Exit2-IR
1111	Update-IR

USRN (USERIN Signal Value Bit)—This bit contains the current value from the USERIN pin. The value of the signal on USERIN is not latched by the BSM2. Stability of this signal (as required) is the responsibility of the user. This bit is only functional in the 1215E. In the 497AE, this bit always has the value 1.

IDL0 (Idle Counter State Bit)—When the value of this bit is 0, the IDLE counter register has not yet counted down to zero. When the IDLE counter register has counted down to zero, this bit has the value 1. (See description of the IDT[1:0] bits, above.)

TVX0 (TVX Counter State Bit)—When the value of this bit is 0, the TVX counter register has not yet counted down to zero. When the TVX counter has counted down to zero, this bit has the value 1.

DONE (Scan Done Bit)—The value of this bit is 1 if and only if the most recently initiated scan process has terminated. Otherwise, the value of this bit is 0. The conditions under which the value of the bit will be 1 are as follows:

If the last scan operation was in normal (non-ATPG) mode, then the TVX and IDLE counter registers are at zero.

If the last scan operation was via ATPG and the ATPG mode is 011, then the SDC and LPC registers are at zero.

If the last scan operation was via ATPG and the ATPG mode is *not* 011, then the LPC register is at zero.

In all three cases, the TAP state bits (above) will indicate that the destination TAP Controller state has been entered.

Appendix B—BSM2 Register Descriptions (continued)

STAT: Status Register (continued)

TVOU (TVO Full Bit)—If the value of this bit is 1, data is loaded in all 512 words of the TVO Test Data Memory (FIFO) (buffer). If the value of this bit is 0, data is loaded in less than 512 words of the TVO FIFO (including the possibility that it is empty).

TVOM (TVO Empty Bit)—If the value of this bit is 1, data is loaded in none of the words of the TVO Test Data Memory (FIFO) (buffer). If the value of this bit is 0, data is loaded in some of the 512 words of the TVO FIFO (including the possibility that it is full).

TVIU (TVI Full Bit)—If the value of this bit is 1, data is loaded in all 512 words of the TVI Test Data Memory (FIFO) (buffer). If the value of this bit is 0, data is loaded in less than 512 words of the TVI FIFO (including the possibility that it is empty).

TVIM (TVI Empty Bit)—If the value of this bit is 1, data is loaded in none of the words of the TVI Test Data Memory (FIFO) (buffer). If the value of this bit is 0, data is loaded in some of the 512 words of the TVI FIFO (including the possibility that it is full).

Appendix B—BSM2 Register Descriptions (continued)

CMU: Control-MASK/USEROUT0(1) Register

NOTE: The register is present in the 1215E (48-pin package) BSM2 only.

Purpose

Provides ability to mask the use of USEROUT0 and USEROUT1 pins with each bit of the CMU register acting as a mask for a status signal that is in an 8-input OR cone feeding either USEROUT0 or USEROUT1. Bits 15—8 are dedicated to USEROUT1. Bits 7—0 are dedicated to USEROUT0.

Address (Octal)

04

Format

15—08	07—00
USRC1[7:0]	USRC0[7:0]

Default (Hex)

CMU = 0000

Read-only Bits

None

Description

USRC1[7] When the value of this bit is 1, the TVOU-1 bit is added to the OR cone feeding USEROUT1.

USRC1[6] When the value of this bit is 1, the TVOM+1 bit is added to the OR cone feeding USEROUT1.

USRC1[5] When the value of this bit is 1, the TVIU-1 bit is added to the OR cone feeding USEROUT1.

USRC1[4] When the value of this bit is 1, the TVIM+1 bit is added to the OR cone feeding USEROUT1.

USRC1[3] When the value of this bit is 1, the TVOU bit is added to the OR cone feeding USEROUT1.

USRC1[2] When the value of this bit is 1, the TVOM bit is added to the OR cone feeding USEROUT1.

USRC1[1] When the value of this bit is 1, the TVIU bit is added to the OR cone feeding USEROUT1.

USRC1[0] When the value of this bit is 1, the TVIM bit is added to the OR cone feeding USEROUT1.

USRC0[7] When the value of this bit is 1, the TVOU-1 bit is added to the OR cone feeding USEROUT0.

USRC0[6] When the value of this bit is 1, the TVOM+1 bit is added to the OR cone feeding USEROUT0.

USRC0[5] When the value of this bit is 1, the TVIU-1 bit is added to the OR cone feeding USEROUT0.

USRC0[4] When the value of this bit is 1, the TVIM+1 bit is added to the OR cone feeding USEROUT0.

USRC0[3] When the value of this bit is 1, the TVOU bit is added to the OR cone feeding USEROUT0.

USRC0[2] When the value of this bit is 1, the TVOM bit is added to the OR cone feeding USEROUT0.

USRC0[1] When the value of this bit is 1, the TVIU bit is added to the OR cone feeding USEROUT0.

USRC0[0] When the value of this bit is 1, the TVIM bit is added to the OR cone feeding USEROUT0.

Appendix B—BSM2 Register Descriptions (continued)

CBIST: Control-BIST Register

Purpose

Provides facility for selection and execution of BSM2 BIST functions (memory, random logic, memory retention) provides memory BIST result signature.

Address (Octal)

05

Format

15—10	09	08	07
MEMSIG[5:0]	RL_DONE	MEMDONE	SYSDONE

06-05	04	03	02	01	00
unused	BIST_IE	XECBIST	MEMRETE	RLSKIP	MEMSKIP

Default (Hex)

CBIST = 0000

Read-only Bits

Bits CBIST[15:07] are read-only.

Passing Signatures

Memory BIST: MEMSIG[5:0] = 00000 (binary)

Random Logic BIST: BSR = 000BDB3A (hex)

Description

MEMSKIP (Memory BIST Skip Bit)—If the value of this bit is 1, the memory BIST operation will be skipped when the XECBIST bit (below) is set and BIST is executed. If the value of this bit is 0, then memory BIST will be activated when BIST is executed.

RLSKIP (Random Logic BIST Skip Bit)—If the value of this bit is 1, the random logic BIST operation will be skipped when the XECBIST bit (below) is set and BIST is executed. If the value of this bit is 0, then random logic BIST will be activated when BIST is executed.

MEMRETE (Memory BIST Retention Test Enable Bit)—If the value of this bit is 1, the memory BIST retention test will occur. Otherwise, the retention test is skipped. Retention testing is normally done only during manufacture. This test checks for leakage paths that check the volatility of the memory. In order to carry out this test in the field, the master clock (TCKIN) must be stopped at particular intervals into the memory test. Contact Agere for further details regarding implementation of this test.

Appendix B—BSM2 Register Descriptions (continued)

CBIST: Control-BIST Register (continued)

XECBIST (Execute BIST Bit)—When a 1 is written to this bit, execution of BIST will occur. When the value of the bit is 0, execution is not initiated. This bit may be written simultaneously with or after the writing of the bits that establish the BIST control parameters—MEMSKIP, RLSKIP, MEMRETE, and BIST_IE.

Execution of BIST may be shut off at any time by writing a 0 to the XECBIST bit. After normal BIST termination, the XECBIST bit also should be set to 0. Writing a 0 to the XECBIST bit not only terminates a BIST operation, but also clears the DONE bits and initializes miscellaneous internal BIST control registers.

A reset (through hardware or software) should be applied after BIST operations to initialize all registers. Operation of memory BIST will naturally destroy any information in the TVI and TVO memories.

BIST_IE (BIST Interrupt Enable Bit)—When the value of this bit is 1 and execution of BIST is initiated, the BSM2 will generate an interrupt via the interrupt pin (INT*) when the selected BIST operation(s) is/are done (see SYSDONE, below).

SYSDONE (All BIST Done Bit)—When the value of this bit is 1, all BIST operations are complete. BIST result signatures can be read. When the value of this bit is 0, BIST is running (not finished) or the CBIST register has been cleared to its default value. Since the SYSDONE bit is read-only, the only means of clearing it is setting the XECBIST bit to 0.

MEMDONE (Memory BIST Done Bit)—When the value of this bit is 1, memory BIST execution is complete. The signature produced by memory BIST can be read in MEMSIG[5:0] (below). The passing signature consists of all zeros. When the value of the MEMDONE bit is 0, then memory BIST is running (not finished) or the CBIST register has been cleared to its default value. Since the MEMDONE bit is read-only, the only means of clearing it is setting the XECBIST bit to 0.

RL_DONE (Random Logic BIST Done Bit)—When the value of this bit is 1, random logic BIST execution is complete. The signature produced by random logic BIST can be read in the BIST signature register (BSR) register. The passing signature (hex) is 000BDB3A. When the value of the RL_DONE bit is 0, then random logic BIST is running (not finished) or the CBIST register has been cleared to its default value. Since the RL_DONE bit is read-only, the only means of clearing it is setting the XECBIST bit to 0.

MEMSIG[5:0] (Memory BIST Signature Bits)—At the completion of memory BIST (see MEMDONE, above), a BSM2 that has passed memory BIST will contain 00000 (binary) in the MEMSIG bits. All other values indicate failure of memory BIST. Since the MEMSIG bits are read-only, they are only cleared if memory BIST completes without detecting a fault. Otherwise, the values of these bits are undefined.

Appendix B—BSM2 Register Descriptions (continued)

API: TVI Address Pointer Register

Purpose

Provides a pointer to currently addressed word of the TVI Test Data Memory (FIFO) (buffer). The currently addressed word during a scan operation is the word currently being written with test data from the output of the selected/attached B-S chain. Autoincrementing of this pointer is turned on and off by the use of the AINC[1] bit.

Address (Octal)

06

Format

15—09	08—00
unused	API[8:0]

Default (Hex)

API = 0000

Read-only Bits

None

Description

API[8:0] (TVI Address Pointer)—In normal scan operation, this register field contains the address [0—777 (octal), 0—511 (decimal)] of the word of the TVI data memory currently being written from the output of the currently selected/attached B-S chain. The only instance in which a controlling processor would write to this register during normal scan operation would be to reset it to 0 if that were necessary because TVI operates as a FIFO in normal scan operation—no addressing action by the controlling processor is necessary.

In ATPG mode, the TVI data memory is combined with the TVO data memory to create an interconnect map of the circuit sensed and driven by the selected/attached B-S chain [(see under the heading Scan-Sequence Modifier (SSM)]. The interconnect map is written by the controlling processor prior to starting ATPG. The TVI address pointer (API) is then used to address the words of TVI to be written with the necessary information. (See also, description of the TVIR register and the AINC[1] bit.) After writing data to the TVI data memory for these ATPG modes, the TVI address pointer register must be reset to its initial value.

Appendix B—BSM2 Register Descriptions (continued)

APO: TVO Address Pointer Register

Purpose

Provides a pointer to currently addressed word of the TVO Test Data Memory (FIFO) (buffer). The currently addressed word during a scan operation is the word currently being read to supply test data to be scanned into the selected/attached B-S chain. Autoincrementing of this pointer is turned on and off by the use of the AINC[0] bit.

Address (Octal)

07

Format

15—09	08—00
unused	APO[8:0]

Default (Hex)

APO = 0000

Read-only Bits

None

Description

APO[8:0] (TVO Address Pointer)—In normal scan operation, this register field contains the address [0—777 (octal), 0—511 (decimal)] of the word of the TVO data memory currently being scanned into the currently selected/attached B-S chain. The only instance in which a controlling processor would write to this register during normal scan operation would be to reset it to 0 if that were necessary because TVO operates as a FIFO in normal scan operation—no addressing action by the controlling processor is necessary.

In ATPG mode the TVO data memory is combined with the TVI data memory to create an interconnect map of the circuit sensed and driven by the selected/attached B-S chain (see under the heading Scan-Sequence Modifier (SSM)). The interconnect map is written by the controlling processor prior to starting ATPG. The TVO address pointer (APO) is then used to address the words of TVO to be written with the necessary information. (See also, description of the TVOR register and the AINC[0] bit.) Unlike the TVI address pointer register, after writing data to the TVO data memory, the TVO address pointer register should not be reset to its initial value.

Appendix B—BSM2 Register Descriptions (continued)

TVIR: TVI Memory Register

Purpose

Provides ability for the controlling processor to read (one word at a time) the serial test response data stored in the TVI Test Data Memory (FIFO) and to load (one word at a time) test-related data into the TVI FIFO.

Address (Octal)

10

Format

15—00
TVIR[15:0]

Default (Hex)

TVIR = uninitialized

Read-only Bits

None

Description

This 16-bit register enables the controlling processor to read test response data that has been stored in the 16 x 512 TVI FIFO. It takes two consecutive, 1-byte read cycles (in the 497AE) or one 1-word read cycle (in the 1215E) to read a complete 16-bit word from the TVI FIFO. Note that the lower-order byte in a word is transferred before the higher-ordered byte in the same word.

The TVIR can be written by the user. In writing using the 8 bit data bus, the lower-order byte of TVIR is transferred first; and the word is not written to the TVI FIFO until both bytes have been written to TVIR.

Appendix B—BSM2 Register Descriptions (continued)

TVOR: TVO Memory Register

Purpose

Provides ability for the controlling processor to write (one word at a time) the serial test response data stored in the TVO Test Data Memory (FIFO) and to read (one word at a time) test-related data into the TVO FIFO.

Address (Octal)

11

Format

15—00
TVOR[15:0]

Default (Hex)

TVOR = uninitialized

Read-only Bits

None

Description

This 16-bit register enables the controlling processor to write test-related data to the 16 x 512 TVO FIFO. It takes two consecutive, 1-byte write cycles (in the 497AE) or one 1-word write cycle (in the 1215E) to write a complete 16-bit word to the TVO FIFO. Note that the lower-order byte in a word is transferred before the higher-ordered byte in the same word; and the word is not written to the TVO FIFO until both bytes have been written to TVOR.

The TVOR can be read by the user. In reading using the 8-bit data bus, the lower-order byte of TVOR is transferred first.

Appendix B—BSM2 Register Descriptions (continued)

TVX: TVX Counter Register

Purpose

Provides a downcounter for the purpose of controlling the number of bits scanned into a selected/attached B-S chain during a normal scan operation.

Addresses (Octal)

13—12

Format

31—00
TVX[31:0]

Default (Hex)

TVX = 00000000

Read-only Bits

None

Description

At the start of a normal scan operation, the value written to this register is the total number of bits to be scanned during the scan operation—the number of bits in the selected/attached B-S chain times the number of serial vectors to be scanned into the chain. When TVX has counted down to zero, the scan operation is complete unless the retimed delay function is being used. See details under the heading The BSM2 Scan Process—especially, under the heading Writing, Reading, and Operation of the Input and Output Scan Data FIFOs (TVI and TVO).

Appendix B—BSM2 Register Descriptions (continued)

IDLE: IDLE Counter Register

Purpose

Provides capability to fix a period for the TAP Controllers of the selected/attached B-S chain to be held in a defined Idle TAP Controller state. Used in normal scan operation. See under the heading Defining TAP Controller States in a Scan Sequence.

Addresses (Octal)

15—14

Format

31—00
IDLE[31:0]

Default (Hex)

IDLE = 00000000

Read-only Bits

None

Description

The IDLE counter specifies the number of cycles of the clock signal on TCK in which the TAP Controllers of a selected/attached B-S chain will remain in a predetermined idle state. The period is determined by a downcount to 0 from the value written to the IDLE counter register. The precise count in the idle state is n + 1, where n is the value programmed in this register. (Note: a programmed count of 1 will result in an operational idle count of 2. An operational idle count of 1 is not allowed as a programmed count of 0 implies no idle state.)

The TAP Controller state in which the downcount will occur is encoded by the value of the IDT[1:0] bits in the CSC register. If the programmed scan operation involves a sequence of TAP Controller states not including the Idle TAP Controller state defined in the IDT[1:0] bits, no downcount will occur regardless of the value in the IDLE counter register.

A common use of the IDLE counter is to specify the amount of time the BSM2 should wait in the Run-Test/Idle TAP Controller state while some BIST activated via the B-S chain runs to completion. Another application occurs during the programming of devices via the B-S chain. For example, a device may be designed such that the burn-in time must occur when the device's TAP Controller is in its Pause-IR TAP Controller state. The IDLE counter would be used to maintain the TAP Controller state for a time ≥ the burn-in time.

If an operational mode is selected where the scan type and idle type are the same, both counters run simultaneously. The state is exited when the maximum count reaches zero.

Appendix B—BSM2 Register Descriptions (continued)

BSR: BIST Signature Register

Purpose

Provides the signature analysis resource for random logic BIST.

Addresses (Octal)

17—16

Note: The address for this register in the 497AA Compatibility Mode is octal 57 (binary 1X1111).

Format

31—20	19—00
unused	RLSIG[19:0]

Default (Hex)

BSR = uninitialized

Read-only Bits

BSR[31:00]

Description

RLSIG[19:0] (Random Logic BIST Signature Bits)—At the conclusion of execution of random logic BIST, RLSIG contains the resulting test signature. When random logic BIST is initiated, RLSIG[19:0] is automatically initialized.

If the random logic BIST passes, the value in the BSR will be 000BDB3A (hex). The presence of any other value in the BSR at the termination of random logic BIST indicates a logic failure in the BSM2.

Control of execution of random logic BIST and detection of the completion of execution are managed through the BIST_IE, RL_DONE, RLSKIP, and XECBIST bits in the CBIST register.

Appendix B—BSM2 Register Descriptions (continued)

LPC: Loop Counter Register

Purpose

Provides the ability for the controlling processor to program the number of algorithmic patterns to be generated when the ATPG capability of the BSM2 is enabled.

Addresses (Octal)

20

Format

15—00
LPC[15:00]

Default (Hex)

LPC = 0000

Read-only Bits

None

Description

The LPC is used only during ATPG. This 16-bit counter provides the means whereby the controlling processor can program the BSM2 with the number of serial test patterns to be applied to the currently selected/attached B-S chain. When the BSM2 is in the execution mode, the value in LPC is decremented by one every time the scan duration counter (SDC) reaches zero (indicating a complete test pattern has been delivered). The BSM2 stops transmitting serial test data when LPC and SDC have both reached zero. LPC can be read and written by user programs.

Appendix B—BSM2 Register Descriptions (continued)

SDR: Scan Duration Register

Purpose

Provides the means by which the controlling processor can program the number of bits in, or the length of, a serial test pattern to be generated during ATPG operation. See Automatic Test Pattern Generation (ATPG), Scan Sequence Modification (SSM), and Signature Analysis.)

Addresses (Octal)

21

Format

15—00
SDR[15:00]

Default (Hex)

SDR = 0000

Read-only Bits

None

Description

This 16-bit register is to be loaded with the number of serial test data bits to be shifted out to the selected/attached B-S chain via TDO during ATPG operation. Typically, the number equals the length of the B-S ring. The contents of the SDR are loaded into the scan duration counter (SDC) prior to shifting each newly generated serial test vector (see under the heading BSM2 Registers Related to ATPG). The SDC is decremented by one in each TCK cycle beginning as soon as the TAP Controller(s) targeted by the BSM2 has (have) entered a **Shift-DR** controller state during ATPG execution. When SDC reaches zero, the shifting process of a single serial vector has been completed.

Appendix B—BSM2 Register Descriptions (continued)

NCR: Net Count Register

Purpose

Provides capability for the controlling processor to program the number of B-S accessible nets driven/sensed by the selected/attached B-S chain; is used by the ATPG for generating interconnect test patterns.

Address (Octal)

22

Format

15—00
NCR[15:00]

Default (Hex)

NCR = 0000

Read-only Bits

None

Description

This 16-bit register is used by the ATPG function of the BSM2 in conjunction with the net counter (NC) for generating counting and walking sequences. Typically, the NCR is loaded with the number of B-S accessible nets driving (driven by) the selected/attached B-S chain. When a counting or walking sequence is to be generated, the contents of the NCR are loaded into the NC when the BSM2 enters the execution mode. Then, the NC is decremented by one for every bit of the algorithmic test vector that is shifted out to an active B-S output cell (i.e., whenever the serial output of the TVI Test Data Memory (FIFO) is low). Otherwise, the counter is inhibited. Note that there are as many active B-S output cells as there are B-S accessible nets. After the NC has reached zero, it is reloaded with the contents of the NCR before counting down again. This process is repeated until a specified number (contained in the loop counter, LPC) of algorithmic patterns has been delivered to the B-S ring.

Appendix B—BSM2 Register Descriptions (continued)

PRPG: ATPG Pseudorandom Pattern Generation Register

Purpose

Provides the pseudorandom test patterns for board interconnect testing as well as device scan testing. A user-defined seed value may be loaded into PRPG prior to execution of ATPG.

Addresses (Octal)

25—24

Format

31—00
PRPG[31:0]

Default (Hex)

PRPG = 00000000

Read-only Bits

None.

Description

The PRPG starts generating serial test patterns whenever it is selected as the TDO source and the TAP State Tracker indicates that the TAP Controllers on the selected/attached B-S ring are in the Shift-DR TAP Controller state. The feedback polynomial of the PRPG is $x^{32} + x^{22} + x^2 + x + 1$.

Appendix B—BSM2 Register Descriptions (continued)

SAR: ATPG Signature Analysis Register

Purpose

Provides the resource for computing and retaining the output signature in the case the signature analysis option is selected for the output of an automatically generated test pattern or to compress any other pattern scanned from a selected/attached B-S chain (see Table 1 and Table 2).

Addresses (Octal)

27—26

Format

31—00
SAR[31:0]

Default (Hex)

SAR = 0DAAD03B

Read-only Bits

None

Description

The signature is computed as the remainder obtained as the result of performing binary division of the test data output stream by the polynomial $x^{32} + x^{22} + x^2 + x + 1$. The polynomial is not alterable by the user. The register may be loaded with a user-selected seed value prior to execution of ATPG.

Appendix B—BSM2 Register Descriptions (continued)

BIR Quick Reference

PTR	unused 7—5	RP[4:0] 4—0

Note: PTR is used only in the 497AE (for indirect addressing).

CSC/BIR[00]	GCLK 15	IDT[1:0] 14—13	SCT[2:0] 12—10	DET[1:0] 9—8	RTD[2:0] 7—4	LP 1	CDIV[2:0] 2—0

CUTI/BIR[01]	USR1 15	OUIM 14	WDIM 13	TMC[1:0] 12—10	MAN 10	AMD[1:0] 9—8	TIOM[2:0] 7—-5	SSME 4	AC 3	TC 2	AINC[01:00] 1—0

CUT0/BIR[02]	unused 15—8	TDIM 7	unused 6	USR0 5	TRSTB 4	TOEB 3	TDOM 2	TMSM 1	TDOEM 0

STAT/BIR[03]	TVOU-1 15	TVOM+1 14	TVIU-1 13	TVIM+1 12	TAPS[03:00] 11-8	USRN 7	IDL0 6	TVX0 5	DONE 4	TVOU 3	TVOM 2	TVIU 1	TVIM 0

CMU/BIR[04]	USRC1[7:0] 15—8	USCR0[7:0] 7—0

CBIST/BIR[05]	MEMSIG[5:0] 15—10	RL_DONE 9	MEMDONE 8	SYSDONE 7	unused 6—5	BIST_IE 4	XECBIST 3	MEMRETE 2	RLSKIP 1	MEMSKIP 0

API/BIR[06]	unused 15—9	API[8:0] 8—0

APO/BIR[07]	unused 15—9	APO[8:0] 8—0

TVIR/BIR[10]	TVIR[15:0] 15—0

TVOR/BIR[11]	TVOR[15:0] 15—0

TVX/BIR[13:12]	TVX[31:0] 31—0

IDLE/BIR[15:14]	IDLE[31:0] 31—0

Notes:

In “BIR[a],” “a” is an octal number.

There are no BIRs at any of the following octal addresses: 23, 30—40.

Figure 5. BIR Quick Reference

Appendix B—BSM2 Register Descriptions (continued)

BIR Quick Reference (continued)

BSR/BIR[17:16]	unused 31—20	RLSIG[19:0] 19—0

LPC/BIR[20]	LPC[15:00] 15—0

SDR/BIR[21]	SDR[15:00] 15—0

NCR/BIR[22]	NCR[15:00] 15—0

PRPG/ BIR[25:24]	PRPG[31:00] 31—0

SAR/BIR[27:26]	SAR[31:00] 31—0

Notes:

In “BIR[a],” “a” is an octal number.

There are no BIRs at any of the following octal addresses: 23, 30—40.

Figure 5. BIR Quick Reference (continued)

Appendix C—BSM2 (497AE) Data Sheet

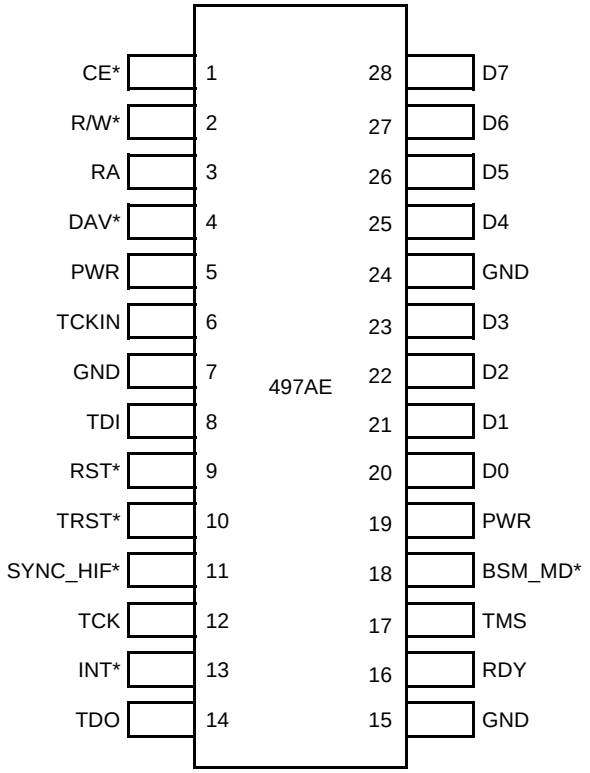
Introduction

The BSM2 (497AE) is a 28-pin, 50-mil (1.27 mm) pitched, surface-mount, plastic, SOJ device with TTL-compatible inputs and outputs. The device is designed using the Agere 0.35 µm, 3 V design enhanced CMOS technology. The primary function of the BSM2 is to interface the serial ANSI/*IEEE* Std. 1149.1-1990 test access port (TAP) with the parallel bus of either a test and diagnostic (T&D) processor (controlling processor) or conventional automatic test equipment (ATE). With this device, B-S based board and system testing can be improved in terms of both efficiency and effectiveness. Specifically, the BSM2 enables a system T&D master to easily access and control a number of slave boards over a parallel T&D bus.

The 497AE conforms to JEDEC solid-state product outlines standard MO-088, details AA through AF for the small-outline J-lead 300 mil (7.62 mm) body family. The footprint is JEDEC standard compatible and the leads are the same shape, pitch, and distance from the bottom of the package as required by the standard.

Pin Descriptions

The BSM2 has 23 functional pins. Two of the five remaining pins are used for power, and the other three for ground. Pin names are shown in Figure 6.



5-6318a (F)

Notes:

Package: 28-pin SOJ.

Device Code: 497AE.

Dimensions: 18.03 mm x 7.62 mm.

Pin Spacing: 1.27 mm.

Figure 6. BSM2 Pin Diagram (Package: 28-pin SOJ; Device Code: 497AE)

Appendix C—BSM2 (497AE) Data Sheet (continued)

Pin Descriptions (continued)

Table 6. 497AE Processor Interface Pins

The following pins are used to provide the parallel interface between the BSM2 and a generic processor or an ATE.

Pin	Symbol	Name/Description
1	CE*	**Chip Enable (Active-Low)**. This input pin is active-low. When CE* = 0, the BSM2 is enabled or selected. The BSM2 data bus D[7:0] becomes active, and the BSM2 internal registers can be accessed by the controlling processor.
2	R/W*	**Read/Write Control (Active-Low).** When the BSM2 is enabled (CE* = 0), this input pin controls the direction of data transfer. When R/W* = 1, D[7:0] become outputs, indicating a BSM2 internal register is to be read. When R/W* = 0, D[7:0] become inputs, indicating a BSM2 internal register is to be written.
3	RA	**Register Address.** When the BSM2 is enabled, this input pin is used to select a BSM2 internal register. When RA = 0, the pointer register (PTR) is addressed; when RA = 1, the internal register, whose address is in the pointer field of the PTR, is selected (see under the heading 497AE Addressing (Indirect) on page 36).
4	DAV*	**Data Available/Valid (Active-Low).** This active-low input pin indicates when the data placed on the data bus is valid and ready to be strobed. DAV* is operational only in the synchronous interface mode; and the value on the DAV* input has an effect on the BSM2 only when the BSM2 is enabled (CE* = 0).
6	TCKIN	**Test Clock Input.** This is a 50% duty cycle clock input with a maximum frequency of 65 MHz. The TCK clock output is derived from this input clock. All internal BSM2 operations are synchronous with respect to TCKIN.
9	RST*	**Reset (Active-Low).** This active-low input pin can be used to synchronously reset the entire device. A low pulse applied to RST* on the rising edge of the signal on TCKIN is sufficient to initiate the BSM2 internal reset operation. All of the output and bidirectional signals are set to a high-impedance state when RST* = 0.
11	SYNC_HIF*	**Synchronous Host Interface (Active-Low).** This pin defines host interface operation. If SYNC_HIF* = 0, then the interface will operate synchronously as in 497AA mode. If SYNC_HIF* = 1 or if the pin is left unconnected, the interface will operate asynchronously (Figure 15 and Figure 16). There is an internal pull-up on this pin. This pin should not be switched during operation of the BSM2.
13	INT*	**Interrupt (Active-Low).** This is an active-low, open drain (open collector) output pin. It generates processor interrupts (e.g., for FIFO over-/underflow or completion of BIST). (See discussion under Interrupt Control.) For proper operation, this pin should be terminated with a pull-up resistor.
16	RDY	**Ready.** This pin is only used in asynchronous operation of the host interface. This output pin provides the handshake signal to the controlling processor. The pin has no function when the device is operating in 497AA Compatibility Mode.
18	BSM_MD*	**BSM Mode (Active-Low).** This pin defines the operational mode of the device. It should be tied to logic 0 for operation in 497AA Compatibility Mode. If tied to logic 1 or left unconnected, an internal pull-up will cause the device to operate in Advanced Operational mode. This pin should not be switched during operation of the BSM2.
28—25, 23—20	D[7:0]	**Data Bus.** These eight pins are bidirectional, with D0 being the least significant bit (LSB) and D7 the most significant bit (MSB). The data bus is active if the device is enabled, and the direction of the data bus (input or output) is controlled by the R/W* pin. The controlling processor accesses the BSM2 internal registers through these pins.

Appendix C—BSM2 (497AE) Data Sheet (continued)

Pin Descriptions (continued)

Table 7. 497AE Board-Level TAP Interface Pins

Pin	Symbol	Name/Description
8	TDI	**Test Data Input.** This is a standard TAP serial test data input pin with an internal pull-up resistor. It receives serial test response from the local board B-S ring. All values arriving at TDI are latched on the rising edge of TCKIN defined with respect to TCK. The test response can be stored in an on-chip memory buffer or compressed into a 32-bit signature.
10	TRST*	**Test Reset (Active-Low).** This output is a standard TAP test reset signal. When TRST* = 0, the TAP controllers in any selected/attached B-S chain are asynchronously placed in their Test-Logic-Reset TAP Controller state.
12	TCK	**Test Clock.** This is a 50% duty cycle, standard TAP test clock output pin. This programmable clock output is derived from the TCKIN clock input. It is broadcast to all the B-S devices supported by the BSM2. Its maximum frequency is 65 MHz. Upon device reset, the default speed of the signal on TCK is 1/128 of the speed of TCKIN.
14	TDO	**Test Data Output.** This is a 3-state, standard TAP serial test data output pin which drives the local board B-S ring. All changes at TDO occur on the falling edge of TCK, referenced by TCKIN. This pin can deliver prestored, deterministic test vectors, or algorithmic patterns generated by the ATPG (see Appendix A).
17	TMS	**Test Mode Select.** All changes at TMS occur on the falling edge of TCK, referenced by TCKIN. Upon device reset, this pin outputs a constant value of 1.

Notes:
The BSM2 interfaces with the board-level B-S ring, of which the BSM2 is master, through these five pins.

Careful timing and skew analysis of the signals on TDI, TDO, and TMS are required when operating with a clock divider of 1 or 2 at high frequencies (see Appendix E—BSM2 Operation as a Function of Phase Relation of TCK and TCKIN at High Speeds with Low-Valued Clock Divider).

Table 8. 497AE Power and Ground Pins

Pin	Symbol	Name/Description
5, 19	PWR/VDD	**Power Supply.** Two 3 Vdc power input pins are used to minimize potential noise in the power supply.
7, 15, 24	GND/VSS	**Ground.** Three ground pins (all at 0 Vdc) are used to minimize potential ground bounces caused by high frequency and, potentially, high fanout pins such as TCK.

5 V Tolerant Buffers

All I/Os are 5 V tolerant. For the input signals, they can be driven with standard TTL logic. The output and bidirectional signals will drive only to a 3 V level (>high-level threshold TTL input voltage). When used in bused applications, the outputs and bidirectional signals can be driven to 5 V when in the high impedance state.

If the 3 V power supply fails during normal operations, no current will be drawn from pins supplying 5 V. However, to minimize long-term degradation, these conditions should not last for long periods of time.

Appendix C—BSM2 (497AE) Data Sheet (continued)

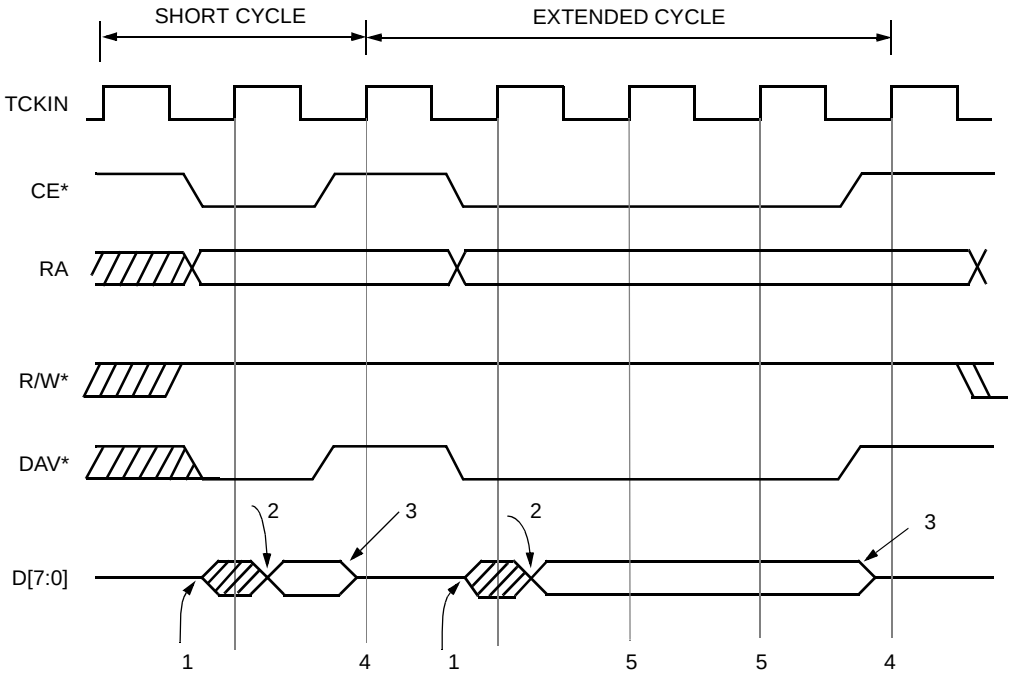
Read/Write Cycle Timing—Synchronous Operation

During a read or write operation, if RA = 0, then the PTR (pointer register) is addressed; otherwise, the internal register pointed to by the PTR is selected.

A read cycle starts when the BSM2 is enabled and R/W* = 1. The D[7:0] output buffers are enabled during a read cycle. Also, the D[7:0] outputs become valid on the first rising edge of TCKIN after DAV* goes to logic 0. The read cycle terminates when the BSM2 has detected a logic 1 at DAV* on a subsequent TCKIN rising edge. This implies that every read cycle consumes at least two TCKIN cycles (see Figure 7).

D[7:0] output buffers are controlled asynchronously by CE* and R/W*. When a BSM2 register is to be read after a series of writes, D[7:0] change from inputs to outputs; this takes a maximum of 15 ns.

Note: R/W* should be stable before or at the same time as CE* goes to logic 0. Otherwise, there is the potential for bus conflict (see Figure 7).



5-6319 (F)

Notes:

1. D[7:0] output buffers are turned on after CE* goes to logic 0; DAV* going to logic 0 while R/W* = 1 initiates the read cycle.
2. Valid data are placed on the data bus by the BSM2 after the rising edge of TCKIN.
3. D[7:0] output buffers are disabled after CE* goes to logic 1.
4. DAV* = 1 at the rising edge of TCKIN causes the BSM2 to terminate the read cycle.
5. No further read operations will occur (i.e., no new data will be read from the BSM2) while DAV* = 0.

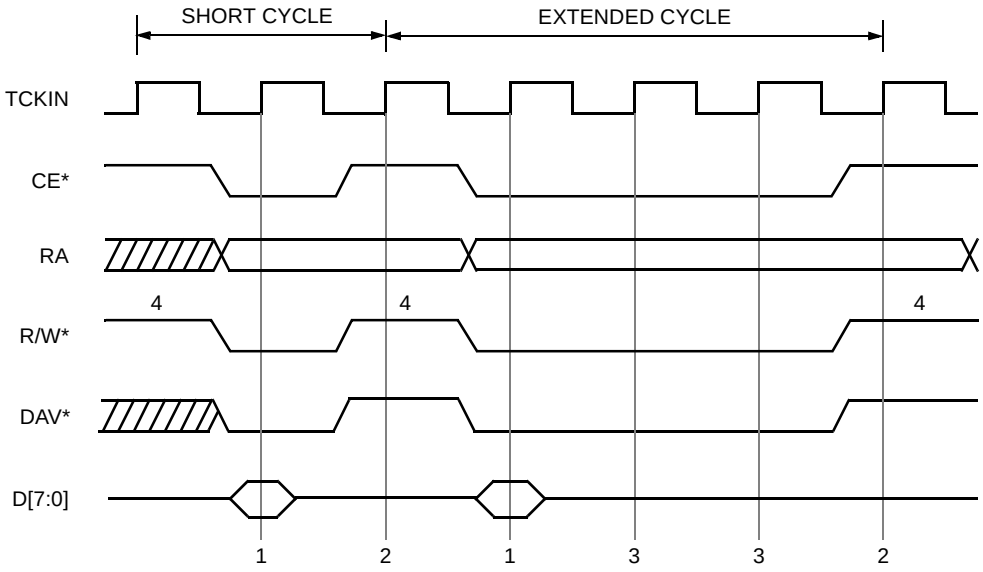
Figure 7. 497AE Read Cycle Timing Diagram

Appendix C—BSM2 (497AE) Data Sheet (continued)

Read/Write Cycle Timing—Synchronous Operation (continued)

A write cycle begins when the BSM2 is enabled and R/W* = 0 (see Figure 8). The D[7:0] output buffers are disabled during a write cycle. Also, the input data on the D[7:0] data bus are internally latched on the first rising edge of TCKIN after DAV* goes to logic 0. The write cycle terminates when the BSM2 has detected a logic 1 at DAV* on a subsequent TCKIN rising edge. This implies that every write cycle consumes at least two TCKIN cycles.

D[7:0] output buffers are controlled asynchronously by CE* and R/W*. When a BSM2 register is to be written after a series of read operations, D[7:0] change from outputs to inputs; this takes a maximum of 15 ns (see Figure 11).



5-6320 (F)

Notes:

1. DAV* going to logic 0 while CE* and R/W* are held = 0 signifies the start of a write cycle; the BSM2 latches the input data D[7:0] on the rising edge of TCKIN.
2. DAV* = 1 on the rising edge of TCKIN causes the BSM2 to terminate the write cycle.
3. No further write operations will occur (i.e., no additional data will be written into the BSM2) while DAV* is still = 0.
4. Successive write cycles must be terminated/delimited by a logic-1 value of R/W* which lasts for at least one TCKIN cycle.

Figure 8. 497AE Write Cycle Timing Diagram

Appendix C—BSM2 (497AE) Data Sheet (continued)

Read/Write Cycle Timing—Synchronous Operation (continued)

It is important to notice that the BSM2 processor interface logic adopts a pipelined design to maximize the rate of data transfer to and from the BSM2. As a result, following a write operation, the processor must wait for a period of at least one TCKIN cycle before initiating a read cycle (see Figure 9).

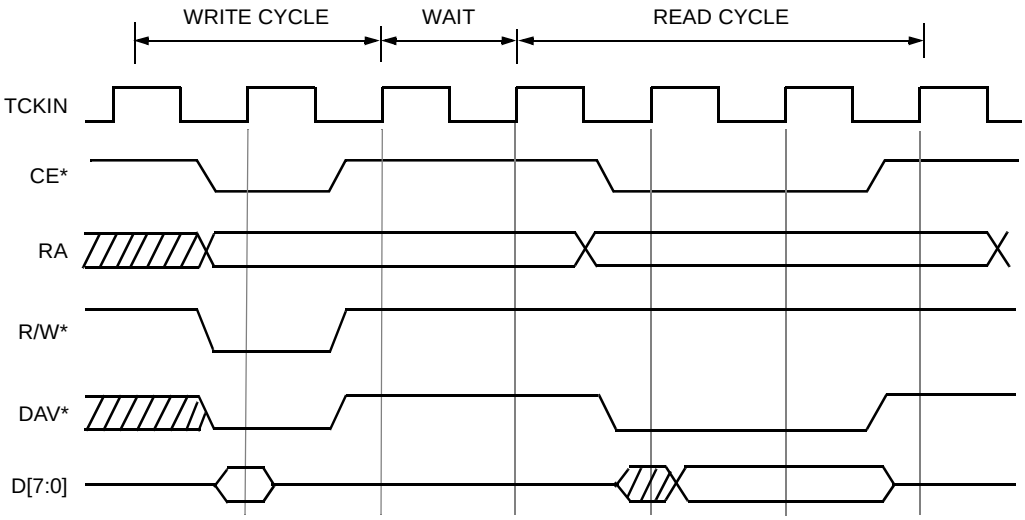


Figure 9. 497AE Write-then-Read Cycle Timing Diagram

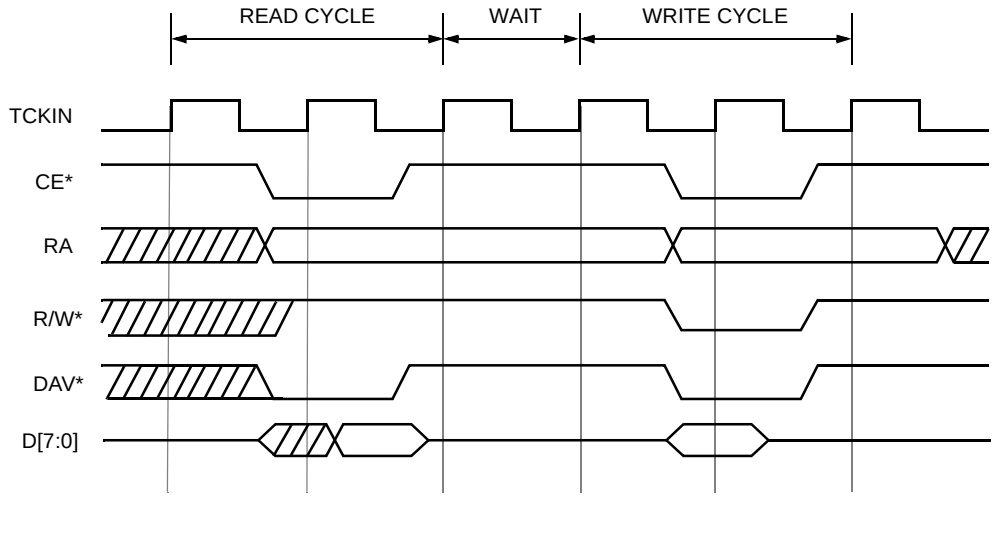
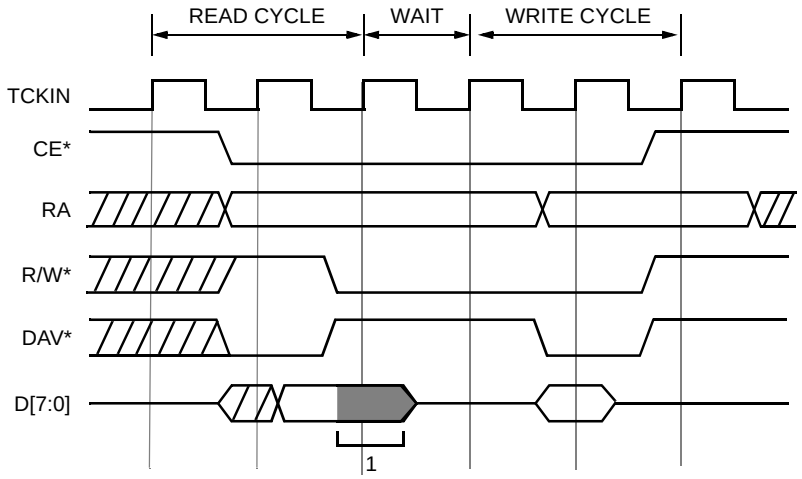


Figure 10. 497AE Read-then-Write Cycle with CE* Deasserted Between Cycles

Appendix C—BSM2 (497AE) Data Sheet (continued)

Read/Write Cycle Timing—Synchronous Operation (continued)



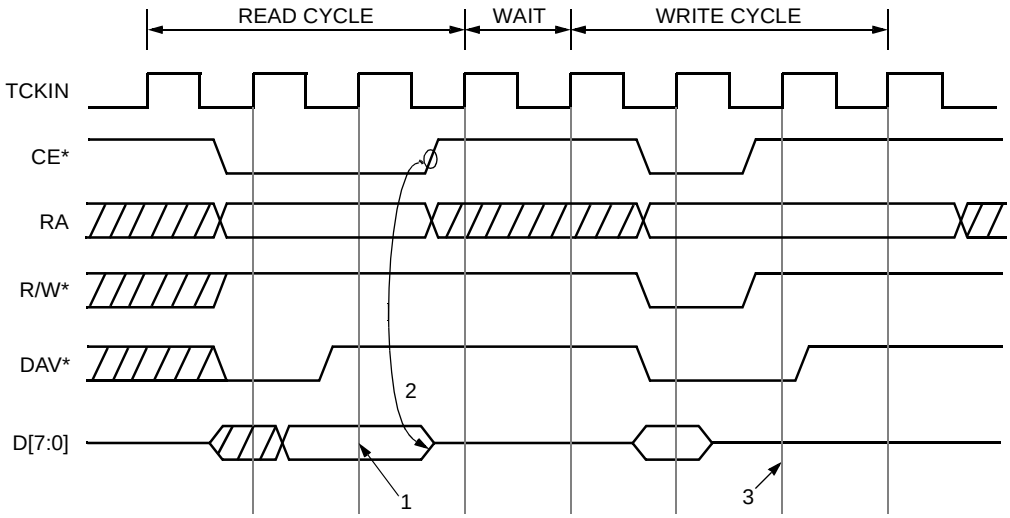
5-6323 (F)

Note:With CE* asserted, when R/W* goes to logic 0, D[7:0] buffers will change direction from outputs to inputs. It takes a maximum of 15 ns for D[7:0] buffers to change direction. Therefore, the BSM2 might still control and put out valid data on the data bus during that time. A wait cycle prevents possible data bus conflict.

Figure 11. 497AE Read-then-Write Cycle with CE* Asserted Through Cycles

Appendix C—BSM2 (497AE) Data Sheet (continued)

Read/Write Cycle Timing—Synchronous Operation (continued)



5-6324 (F)

Notes:

1. DAV* is deasserted. But CE* is still asserted so BSM2 maintains valid data on the data bus.
2. D[7:0] output buffers are disabled asynchronously after CE* goes to logic 1.
3. CE* is deasserted, but DAV* is still asserted. The write cycle is terminated by either CE* going inactive or DAV* going inactive. At that point, the write cycle is terminated.

Figure 12. 497AE Cycle with CE* and DAV* Deasserted Separately

The length of a BSM2 internal register ranges from 8 bits to 32 bits. Although the preceding timing diagrams are valid for all modes of read/write operations, it is useful to keep the following points in mind while accessing any of the BSM2 internal registers:

To write data into an m-byte register, a total of m consecutive write operations must be performed starting with the least significant byte. Reading the register before m write operations have been completed may produce undesirable effects. Similarly, to read an m-byte register, a total of m consecutive read operations must be performed starting with the least significant byte. Writing the register before m read operations have been completed may produce undesirable effects.

Appendix C—BSM2 (497AE) Data Sheet (continued)

Operating Conditions

Table 9. 497AE Power Considerations

Parameter	Min	Typ	Max	Unit
Absolute Maximum Power Supply Voltage (V_{DD} – V_{SS})	—	—	3.6	V
Recommended Power Supply Voltage (V_{DD} – V_{SS})	3.0	3.3	3.6	V
Signal Input Voltage Level	V_{SS} – 0.3	—	V_{DD} + 0.3	V
Total Power Dissipation (ac + dc)	3	—	540	mW

Note: Maximum power—V_{DD} = 3.6 V, worst-case output drivers, TCKIN = 65 MHz. For minimum power see section titled Low Power Mode.

Table 10. 497AE Input/Output Characteristics

Parameter	Min	Typ	Max	Unit
Input Logic Low Voltage (V_{IL})	—	—	1.3	V
Input Logic High Voltage (V_{IH})	1.7	—	—	V
Output Logic Low Voltage (V_{OL})	—	—	0.5	V
Output Logic High Voltage (V_{OH})	V_{DD} – 0.5	—	—	V
RDY Output Source Current	—	—	8	mA
RDY, INT* Output Sink Current	—	—	10	mA
TDO Output Source Current	—	—	16	mA
TDO Output Sink Current	—	—	20	mA
TCK, TMS, TRST* Output Source Current	—	—	32	mA
TCK, TMS, TRST* Output Sink Current	—	—	40	mA
Input Leakage Current	—	—	0.9	µA
Output/Bidirectional Leakage Current	—	—	9	µA

Table 11. 497AE Ambient and Storage Temperatures

Parameter	Min	Typ	Max	Unit
Ambient Temperature	–40	—	85	°C
Storage Temperature	–40	—	125	°C

Appendix C—BSM2 (497AE) Data Sheet (continued)

ac Timing Characteristics—Synchronous Operation

The ac timing parameters shown in this section are measured under the following worst-case-slow testing conditions:

- Ambient temperature: 85 °C
- Power supply voltage: 3.0 V
- Output capacitive load: 70 pF

Table 12. 497AE Input Clock

Parameter	Min	Typ	Max	Unit
TCKIN Frequency	—	—	40	MHz
Rise Time	—	—	2	ns
Fall Time	—	—	2	ns
Low Pulse Width	7	—	—	ns
High Pulse Width	7	—	—	ns
Period	25	—	—	ns

Table 13. 497AE Input Signals

Input Signal	Max Rise	Max Fall	Clock Edge	Min Setup	Min Hold	Typ Int Pull-Up
CE*	2 ns	2 ns	TCKIN↑	10 ns	5 ns	none
RA	2 ns	2 ns	TCKIN↑	8 ns	5 ns	none
R/W*	2 ns	2 ns	TCKIN↑	10 ns	5 ns	none
DAV*	2 ns	2 ns	TCKIN↑	10 ns	5 ns	none
D[7:0]	2 ns	2 ns	TCKIN↑	8 ns	5 ns	none
RST*	2 ns	2 ns	TCKIN↑	10 ns	5 ns	none
TDI	2 ns	2 ns	TCKIN↑	10 ns	5 ns	20 kΩ

Table 14. 497AE Output Signals

Output	Ref Signal	Max Prop Delay
INT*	TCKIN↑	15 ns
D[7:0]	TCKIN↑	0 ns
TCK	TCKIN↑	15 ns
TDO	TCKIN↑	16 ns
TMS	TCKIN↑	16 ns

Notes:

NT* is an open-collector output.

All outputs are disabled (3-stated) during chip reset and self-test operations.

Table 15. 497AE Bidirectional Signals

Parameter	Min	Typ	Max	Unit
D[7:0] State Transition Time (input to output)	—	—	15	ns
D[7:0] State Transition Time (output to input)	—	—	15	ns

Appendix C—BSM2 (497AE) Data Sheet (continued)

ac Timing Characteristics—Asynchronous Operation

In asynchronous interface mode, input and output signals of the 497AE having the same names as signals of the 1215E (Appendix D) have the same ac timing characteristics given in Appendix D. See Table 23 through Table 26. The SYNC_HIF* signal will be hardwired for asynchronous operation.

In the 497AE, Advanced Operational Mode is selected with the BSM_MD* pin. The 1215E device only operates in asynchronous interface mode and the Advanced Operational Mode. Alternative modes are not selectable as in the 497AE. The 1215E also provides additional I/O. Otherwise, in the asynchronous interface mode, the 497AE and 1215E operate identically.

Outline Diagram

Dimensions are in millimeters.

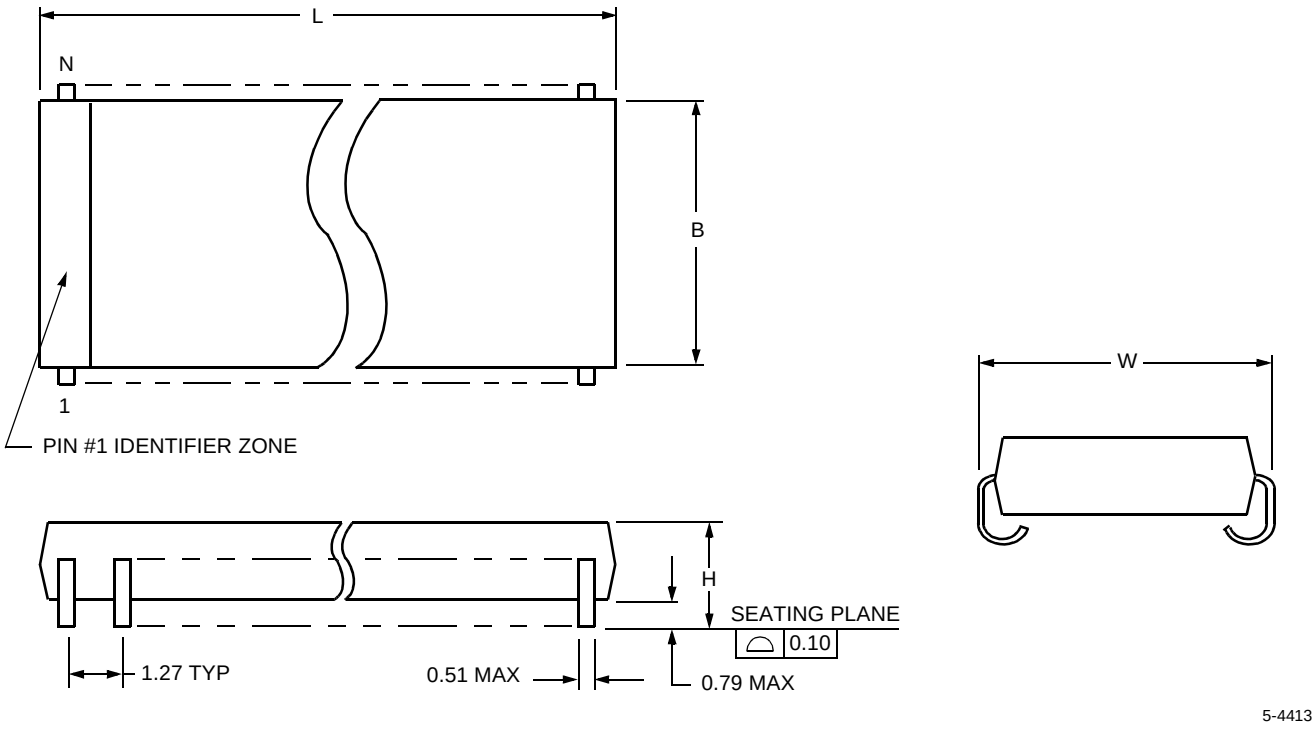


Figure 13. Outline Diagram of 28-pin SOJ Package

Table 16. Summary of Outline Data for 28-pin SOJ Package

Package Description	Number of Pins	Package Dimensions			
		Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
SOJ (Small-Outline, J-Lead)	28	18.03	7.62	8.81	3.18

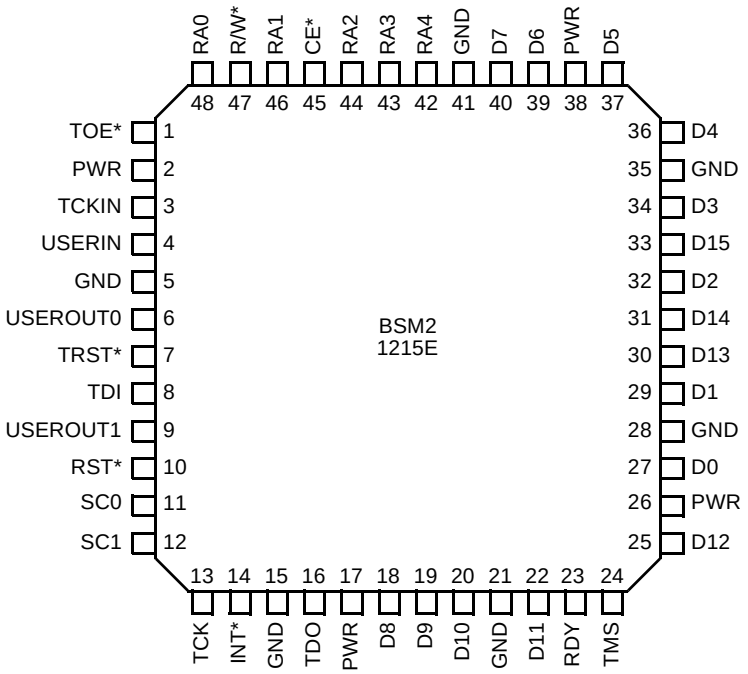
Appendix D—BSM2 (1215E) Data Sheet

Introduction

The BSM2 (1215E) is a 48-pin, 0.5 mm (0.50 mm) pitched, surface-mount, plastic, TQFP device with TTL-compatible inputs and outputs. The device is designed using the Agere 0.35 µm, 3 V design enhanced CMOS technology. The primary function of the BSM2 is to interface the serial ANSI/*IEEE* Std. 1149.1-1990 test access port (TAP) with the parallel bus of either a controlling processor or conventional automatic test equipment (ATE). With the BSM2, B-S based board and system testing can be improved in both efficiency and effectiveness. Specifically, the BSM2 enables a system test and diagnostics (T&D) master to access and control a number of slave boards over a parallel T&D bus.

Pin Descriptions

The 1215 has 38 functional pins. Four of the ten remaining pins are used for power, and the other six for ground. Pin names are shown in Figure 14.



5-7258F

Notes:

Package: 48-pin TQFP.

Device Code: 1215E.

Dimensions without leads: 7.0 mm x 7.0 mm.

Dimensions with leads: 9.0 mm x 9.0 mm.

Pin Spacing: 0.50 mm.

Figure 14. BSM2 Pin Diagram (Package: 48-pin TQFP; Device Code: 1215E)

Appendix D—BSM2 (1215E) Data Sheet (continued)

Pin Descriptions (continued)

The pins listed in Table 17 are used to provide the parallel interface between the BSM2 and a generic processor or an ATE. An asterisk after a pin name indicates that that pin is active low.

Table 17. 1215E Processor Interface Pins

Pin	Symbol	Name/Description
1	TOE*	**TAP Output Enable**. This active-low input is inverted and logically ORed with the TDO Output Enable Control (TOEB) bit of the CUTO register. This pin provides the hardware mode of control of the 3-stating of TAP outputs. A detailed explanation of operation is to be found in the description of the TOEB bit.
3	TCKIN	**Test Clock Input.** This is a 50% duty cycle clock input with a maximum frequency of 65 MHz. The TCK clock output is derived from this input clock. All internal BSM2 operations are synchronous with respect to TCKIN.
4	USERIN	**User Input.** This pin provides the capability of optionally monitoring the state of a user selected signal without adding additional parallel I/O decoding logic to a design. Because of pin limitations it is not available on the 497AE device. If it is unused in the 1215E design, it should not be left floating, but tied either high or low.
6	USEROUT0	**User Output 0.**This pin provides the means of signalling an interrupt to the controlling processor according to certain conditions of the Test Data Memories (FIFOs) (e.g., full, empty, etc.). The pin can be considered to be the output of a 9-input OR tree as follows: The USR0 bit in the CUTO register is ORed with the STAT[15:12] and STAT [3:0] bits of the status register under control of a mask programmed in the USRC0[7:0] bits of the CMU register.
9	USEROUT1	**User Output 1.** This pin provides the means of signalling an interrupt to the controlling processor according to certain conditions of the Test Data Memories (FIFOs) (e.g., full, empty, etc.). The pin can be considered to be the output of a 9-input OR tree as follows: The USR1 bit in the CUTI register is ORed with the STAT[15:12] and STAT [3:0] bits of the status register under control of a mask programmed in the USRC1[7:0] bits of the CMU register.
10	RST*	**Reset (Active-Low).** This active-low input pin can be used to synchronously reset the entire device. A low pulse applied to RST* on the rising edge of the signal on TCKIN is sufficient to initiate the BSM2 internal reset operation. All of the output and bidirectional signals are set to a high-impedance state when RST* = 0.
11, 12	SC[0:1] (AMODE_SW, ATEST_EN)	**Scan Control.** These pins are used for signals that run a scan-test of the 1215E. For normal operation, both signals should be tied to logic 1 or (because they have internal pull-ups) left disconnected. For information on specific operation of the scan-test, contact Agere.
14	INT*	**Interrupt (Active-Low).** This is an active-low, open drain (open collector) output pin. It generates processor interrupts (e.g., for FIFO over-/underflow or completion of BIST). (See discussion under Interrupt Control. Compare to USEROUT0 and USEROUT1, above.) For proper operation, this pin should be terminated with a pull-up resistor.
23	RDY	**READY.** This is only used in asynchronous operation of the host interface. This output pin provides the handshake signal to the controlling processor. The pin has no function when the device is operating in 497AA compatible mode.

Appendix D—BSM2 (1215E) Data Sheet (continued)

Pin Descriptions (continued)

Table 17. 1215E Processor Interface Pins (continued)

Pin	Symbol	Name/Description
33, 31—30, 25, 22, 20—18, 40—39, 37—36, 34, 32, 29, 27	D[15:0]	**Data Bus.** These 16 pins are bidirectional, with D0 being the least significant bit (LSB) and D15 the most significant bit (MSB). The data bus is active if the device is enabled, and the direction of the data bus (input or output) is controlled by the R/W* pin.
45	CE*	**Chip Enable (Active-Low)**. This input pin is active-low. When CE* = 0, the BSM2 is enabled or selected. The BSM2 data bus D[7:0] becomes active, and the BSM2 internal registers can be accessed by the controlling processor.
47	R/W*	**Read/Write Control (Active-Low).** When the BSM2 is enabled (CE* = 0), this input pin controls the direction of data transfer. When R/W* = 1, D[7:0] become outputs, indicating a BSM2 internal register is to be read. When R/W* = 0, D[7:0] become inputs, indicating a BSM2 internal register is to be written.
42—44, 46, 48	RA[4:0]	**Address Bus**. These five input pins drive the address bus of the 1215E. When CE* = 0, the signals on these five lines define the register to be accessed for the current operation.

The BSM2 interfaces with the board-level B-S ring, of which the BSM2 is master, through the five pins described in the following table.

Table 18. 1215E Board-Level TAP Interface Pins

Pin	Symbol	Name/Description
7	TRST*	**Test Reset (Active-Low).** This output is a standard TAP test reset signal. When TRST* = 0, the TAP controllers in any selected/attached B-S chain are asynchronously placed in their Test-Logic-Reset TAP Controller state.
8	TDI	**Test Data Input.** This is a standard TAP serial test data input pin with an internal pull-up resistor. It receives serial test response from the local board B-S ring. All values arriving at TDI are latched on the rising edge of TCKIN defined with respect to TCK. The test response can be stored in an on-chip memory buffer or compressed into a 32-bit signature.
13	TCK	**Test Clock.** This is a 50% duty cycle, standard TAP test clock output pin. This programmable clock output is derived from the TCKIN clock input. It is broadcast to all the B-S devices supported by the BSM2. Its maximum frequency is 65 MHz. Upon device reset, the default speed of the signal on TCK is 1/128 of the speed of TCKIN.
16	TDO	**Test Data Output.** This is a 3-state, standard TAP serial test data output pin which drives the local board B-S ring. All changes at TDO occur on the falling edge of TCK, referenced by TCKIN. This pin can deliver prestored, deterministic test vectors, or algorithmic patterns generated by the ATPG (see Appendix A).
24	TMS	**Test Mode Select.** All changes at TMS occur on the falling edge of TCK, referenced by TCKIN. Upon device reset, this pin outputs a constant value of 1.

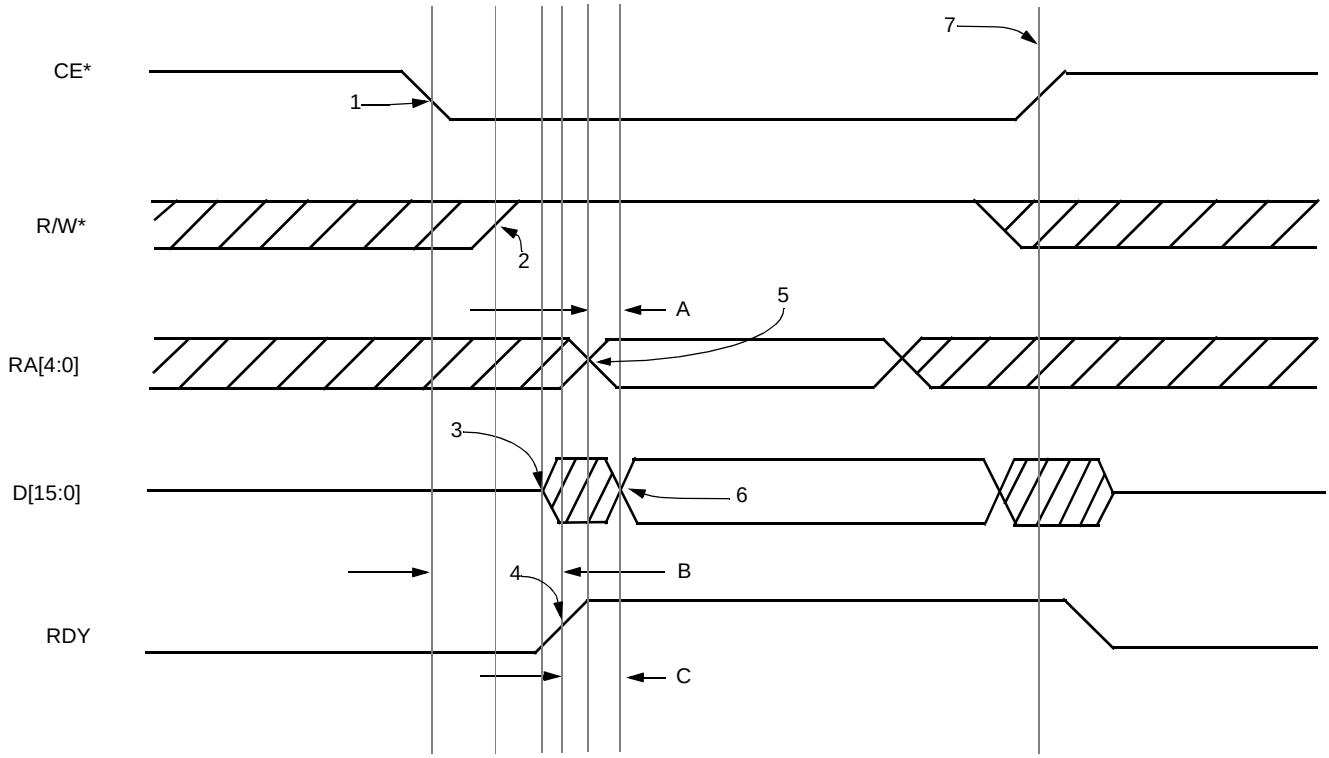
Table 19. 1215E Power and Ground Pins

Pin	Symbol	Name/Description
2, 17, 26, 38	PWR/VDD	**Power Supply**. Four 3 Vdc power input pins are used to minimize potential noise in the power supply.
5, 15, 21, 28, 35, 41	GND/VSS	**Ground.** Six ground pins (all at 0 Vdc) are used to minimize potential ground bounces caused by high frequency and, potentially, high fanout pins such as TCK.

Appendix D—BSM2 (1215E) Data Sheet (continued)

Read/Write Cycle Timing—Asynchronous Operation

Read and write cycle operation in asynchronous mode is described by a series of figures in this section. The figures represent asynchronous operation of both the 497AE and the 1215E.



Notes:

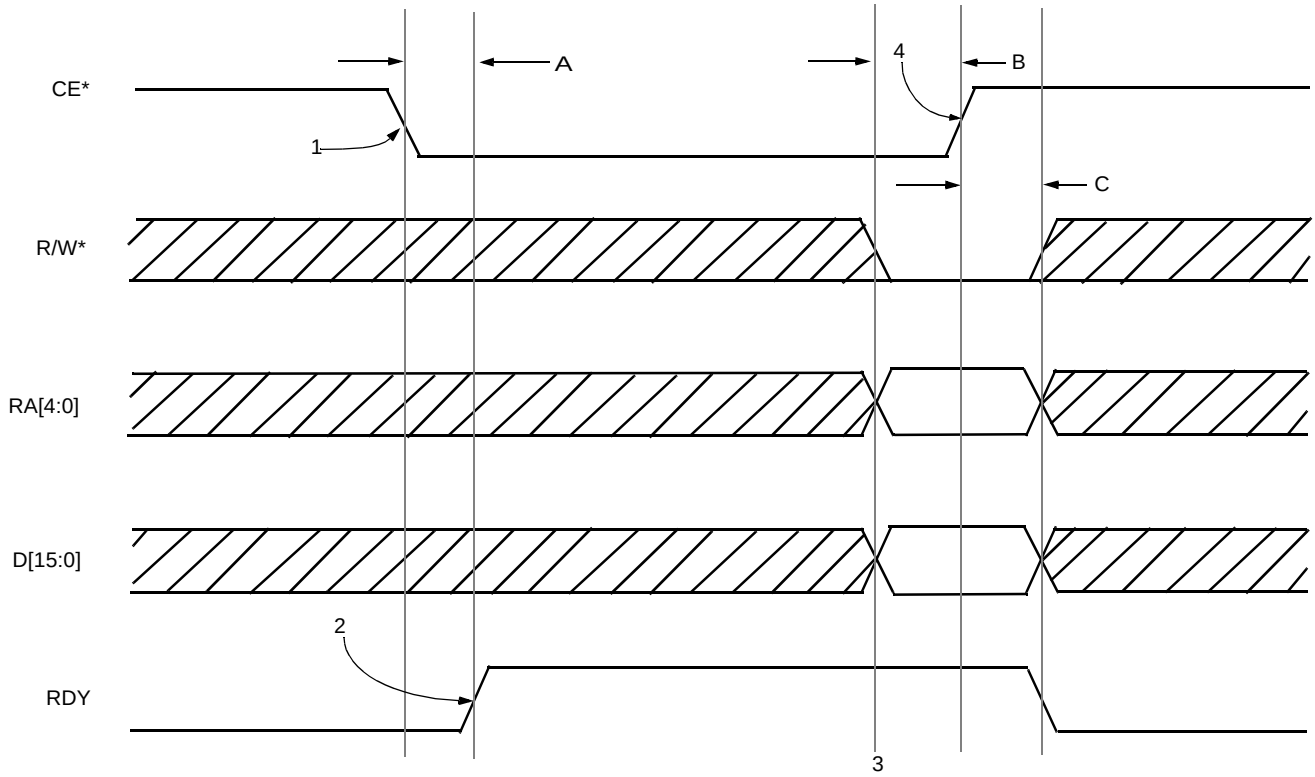
1. CE* goes to logic 0. CE* is the main control signal for the device. All other signals are valid/meaningful only if this signal is active (= 0).
2. R/W* goes to logic 1. The R/W* and RA[4:0] signals can be set up before CE* becomes active. This diagram shows worst case access time for each signal. If both signals are set up in advance of CE* becoming active, data becomes valid on D[15:0] at point 3 rather than point 6.
3. When both CE* = 0 and R/W* = 1, the D[15:0] output buffers are turned on.
4. RDY becomes valid. The interval B represents the best case timing for RDY going to logic 1 after CE* becomes active. The worst case is approximately 3 cycles of the signal on TCKIN after the previous CE* access.
5. Controlling processor drives valid address on RA[4:0].
6. Data becomes available on the data bus. The interval A is the access time of the device—time for address decoding and outputting data to the data bus.
7. CE* going to logic 1 terminates the cycle. Although R/W* is shown as don't care in this diagram, this signal should remain = 1 through this point for normal read operations. Otherwise, a write operation could occur (see Figure 16). The situation depicted in the present figure illustrates that write may follow a read operation in one CE* cycle—if the proper write cycle timing is followed. In the 1215E device, multiple non-memory reads can occur in a single CE* cycle by changing the address bus (RA[4:0]) and carefully maintaining proper data access time from RA[4:0] to D[15:0] (interval A).

C. The interval C is the delay between RDY going to logic 1 and availability of data on the data bus in the case in which the device is not ready when accessed—CE* is active, and the initial value of the signal on RDY is 0.

Figure 15. 1215E Read Cycle Timing Diagram

Appendix D—BSM2 (1215E) Data Sheet (continued)

Read/Write Cycle Timing—Asynchronous Operation (continued)



Notes:
1. CE* goes to logic 0 (becomes active).
2. RDY becomes valid. The interval A represents the best case timing for RDY going to logic 1 after CE* becomes active. The worst case is approximately 3 cycles of the clock signal on TCKIN after the previous CE* access.
3. Controlling processor drives valid address (RA[4:0]), data (D[15:0]) and control (R/W* = 0) signals. The three sets of signals are all latched on the positive going edge of CE* (end of cycle) for writing. B is the set-up time for these signals with respect to CE*.
4. CE* goes to logic (becomes inactive). C is the write cycle hold time with respect to CE*.
5. RDY goes to logic 0. Data and address bus signals are no longer detected by the device.

Figure 16. 1215E Write Cycle Timing Diagram

Appendix D—BSM2 (1215E) Data Sheet (continued)

Operating Conditions

Table 20. 1215E Power Considerations

Parameter	Min	Typ	Max	Unit
Absolute Maximum Power Supply Voltage (V_{DD} – V_{SS})	—	—	3.6	V
Recommended Power Supply Voltage (V_{DD} – V_{SS}) (3.3 V typical)	3.0	3.3	3.6	V
Signal Input Voltage Level	V_{SS} – 0.3	—	V_{DD} + 0.3	V
Total Power Dissipation (ac + dc)	5	—	540	mW

Note: Maximum power—V_{DD} = 3.6 V, worst-case output drivers, TCKIN = 65 MHz. For minimum power see section titled Low Power Mode.

Table 21. 1215E Input/Output Characteristics

Parameter	Min	Typ	Max	Unit
Input Logic Low Voltage (V_{IL})	—	—	1.3	V
Input Logic High Voltage (V_{IH})	1.7	—	—	V
Output Logic Low Voltage (V_{OL})	—	—	0.5	V
Output Logic High Voltage (V_{OH})	V_{DD} – 0.5	—	—	V
RDY, USEROUT[0:1] Output Source Current	—	—	8	mA
RDY, INT*, USEROUT[0:1] Output Sink Current	—	—	10	mA
TDO Output Source Current	—	—	16	mA
TDO Output Sink Current	—	—	20	mA
TCK, TMS Output Source Current	—	—	32	mA
TCK, TMS Output Sink Current	—	—	40	mA
Input Leakage Current	—	—	0.9	µA
Output/Bidirectional Leakage Current	—	—	9	µA

Table 22. 1215E Ambient and Storage Temperatures

Parameter	Min	Typ	Max	Unit
Ambient Temperature	–40	—	85	°C
Storage Temperature	–40	—	125	°C

Appendix D—BSM2 (1215E) Data Sheet (continued)

ac Timing Characteristics

The ac timing parameters shown in this section are measured under the following worst-case-slow testing conditions:

- Ambient temperature: 85 °C
- Power supply voltage: 3.0 V
- Output capacitive load: 70 pF

The SC[0:1] pins will be hardwired.

Table 23. 1215E Input Clock

Parameter	Min	Typ	Max	Unit
TCKIN Frequency	—	—	65	MHz
Rise Time	—	—	2	ns
Fall Time	—	—	2	ns
Low Pulse Width	7	—	—	ns
High Pulse Width	7	—	—	ns
TCKIN Period	15.4	—	—	ns

Table 24. 1215E Input Signals

Input Signal	Max Rise	Max Fall	Clock Edge	Min Setup	Min Hold	Typ Int Pull-Up
RA[4:0]	2 ns	2 ns	CE*↑	8 ns	5 ns	none
R/W*	2 ns	2 ns	CE*↑	10 ns	5 ns	none
D[15:0]	2 ns	2 ns	CE*↑	8 ns	5 ns	none
RST*	2 ns	2 ns	TCKIN↑	10 ns	5 ns	none
TDI	2 ns	2 ns	TCKIN↑	0 ns	5 ns	20 kΩ
USERIN	propagation delay to D7 when CUTI register is accessed: min = 3 ns; max = 13 ns					

Note: USERIN is not referenced to TCKIN because it is not a latched input.

Table 25. 1215E Output Signals

Output	Ref Signal	Max Prop Delay
INT*	TCKIN↑	15 ns
D[15:0]	RA[4:0]	24 ns
TCK	TCKIN↑	15 ns
TDO	TCKIN↑	16 ns
TMS	TCKIN↑	16 ns
RDY	CE*↓	10 ns
USEROUT[1:0]	TCKIN↑	15 ns

Notes:

INT* is an open-collector output.

All outputs are disabled (3-stated) during chip reset and self-test operations.

Appendix D—BSM2 (1215E) Data Sheet (continued)

ac Timing Characteristics (continued)

Table 26. 1215E Bidirectional Signals

Parameter	Min	Typ	Max	Unit
D[15:0] State Transition Time (input to output)	—	—	15	ns
D[15:0] State Transition Time (output to input)	—	—	15	ns

Outline Diagram

Dimensions are in millimeters.

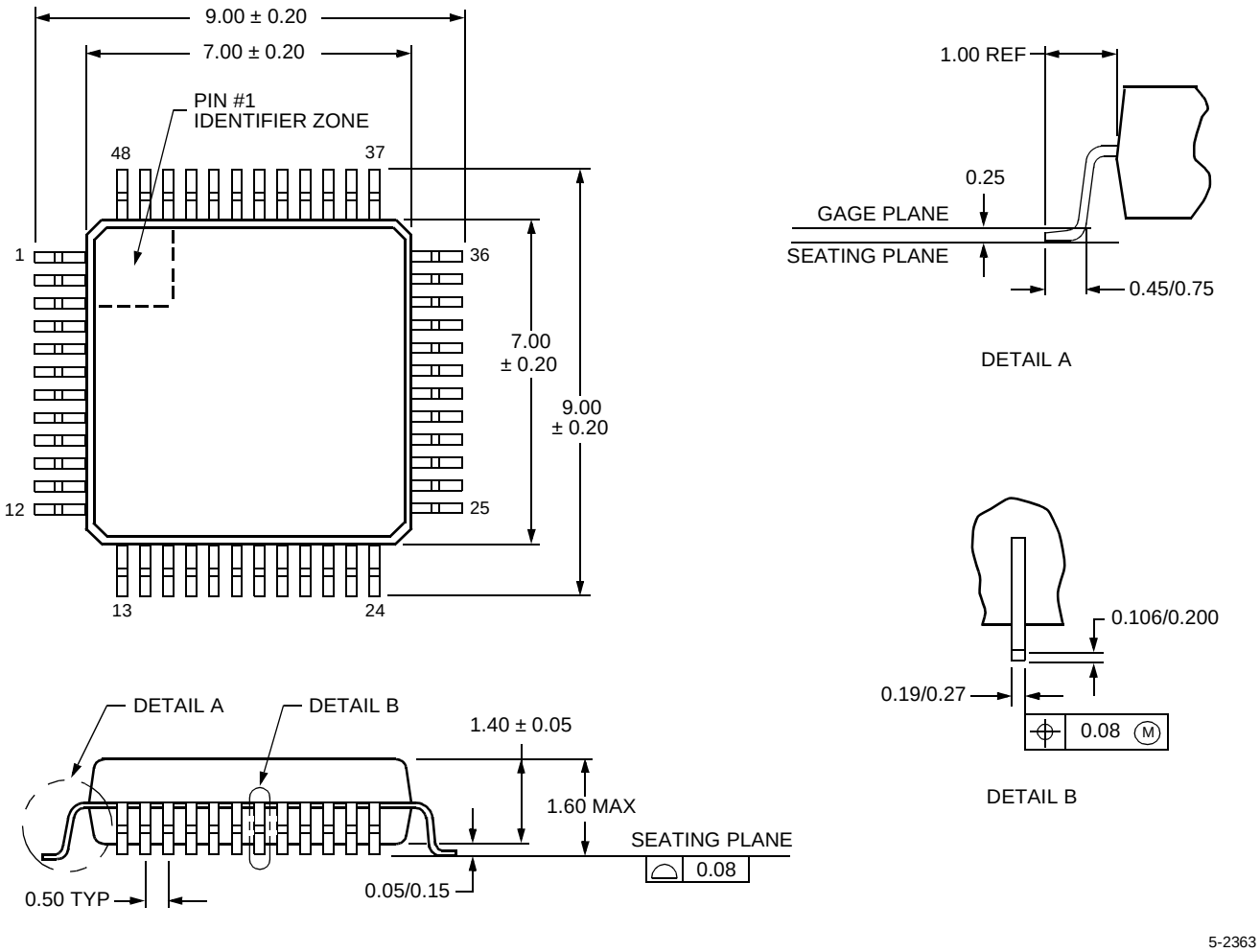


Figure 17. Outline Diagram of 48-pin TQFP Package

Appendix E—BSM2 Operation as a Function of Phase Relation of TCK and TCKIN at High Speeds with Low-Valued Clock Divider

When operating the BSM2 at high speeds, careful consideration must be given to the clock phases, in particular, the phase relationship of TCKIN to TCK and the relationship of the TAP signals, TMS, TDO and TDI. To illustrate potential problems, some examples are shown in the following figures.

Case 1: Consider the situation with TCK = TCKIN/1 and with TCKIN operating at 6.5 MHz (fmax/10—with a period of 152 ns). For this divide by 1 application, TCK is equal to the inverted TCKIN plus a delay of approximately 11 ns. At 6.5 MHz, this delay has negligible consequence as shown in Figure 18. TMS and TDO change state based on the positive edge of TCKIN which in the case of divide by 1 is the negative edge of TCK—this meets the *IEEE* Std. 1149.1 specification. In this application, TDI is captured on the positive edge of TCKIN—matching the best margin for TDI capture for this device. (The *IEEE* specification requires capture on the positive edge of TCK which is the negative edge of TCKIN. This requirement is met in this example, because of the black box argument—the behavior of the B-S chain and the values scanned in and out of it cannot be distinguished from a part operating precisely as specified by the Standard without knowledge of the internal workings of the BSM2.) Since the negative edge of the signal on TCK is where the signal on TDI can make a transition and this lags the rising edge of the signal on TCKIN, latching TDI on the positive edge of TCKIN may be late; but it's safe—it preserves proper operation. Typical propagation delays from TCKIN to TMS, TDO and TCK are 15 ns, which is approximately 10% of the period.

The dashed box (A) represents the capture range of TDI with respect to the appropriate clock edge of TCKIN in all of the figures.

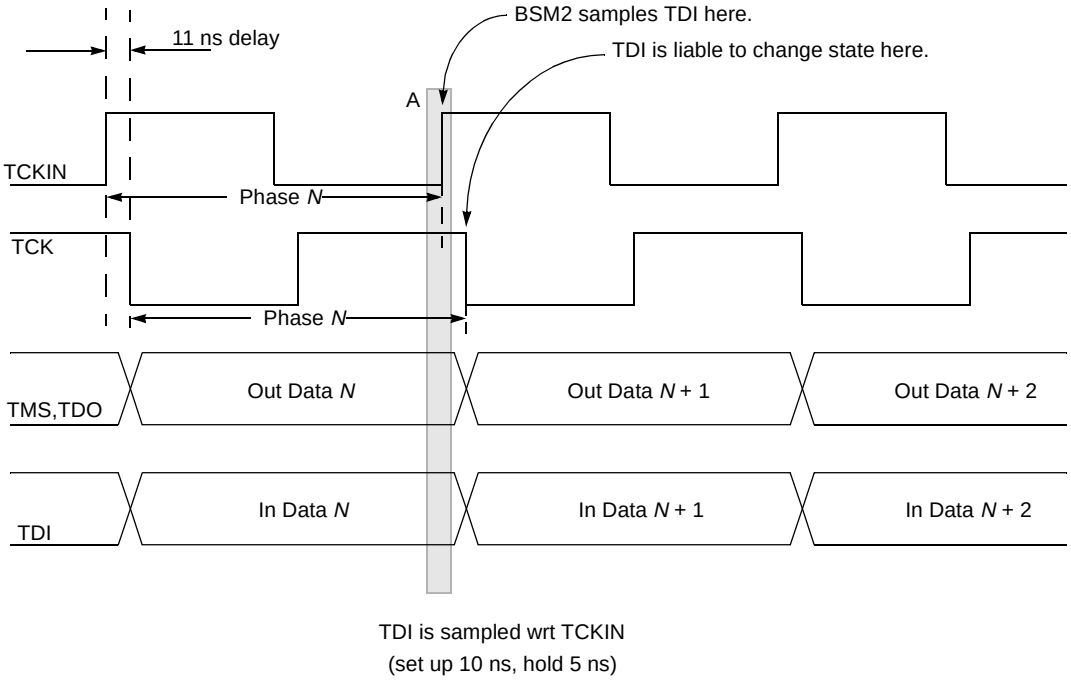


Figure 18. Relationships of TCKIN, TCK, TDI, TDO, and TMS with TCKIN Frequency of 6.5 ns and TMS Defined by Clock Divider Value of 1

Appendix E—BSM2 Operation as a Function of Phase Relation of TCK and TCKIN at High Speeds with Low-Valued Clock Divider (continued)

Case 2: Consider TCK and TCKIN with identical frequency (clock divider of 1, again) and TCKIN = 65 MHz (fmax). The timing diagram is shown in Figure 19. Now the propagation delays and set up and hold times are on the order of the period of TCKIN (15.4 ns). One may have to clean up or deskew the phases of the signals with extra latches, depending on the particular application. In this case one would have to use the retimed delay function (not available when TDI inputs to the SAR) to accommodate for the phase delay of TDI. Also, the set up and hold specifications of TDI would have to be carefully evaluated.

TCK (inverted) lags TCKIN by approximately 11 ns. TMS and TDO are delayed by 15 ns—almost one full period. So already the TDO data are one clock delayed—even if TDO was directly connected to TDI, we have lost one clock cycle. This can be corrected by using the retimed delay register.

Now the set up and hold values for TDI become much tighter with respect to the total period (box B), so some custom circuit phasing must be incorporated.

Note, in the diagram, that the data input cycle *N* is one clock behind. The TDO signal has to drive a B-S chain that returns the signal on TDI; so even in loopback mode, we've lost one clock cycle. Therefore, it is necessary to set the BSM2 for a retimed delay value of 1. Now the BSM2 will store the value sampled during data input cycle *N* + 1 as if it had been captured during data input cycle *N*. In a loopback mode, the input and output test data would be synchronized properly.

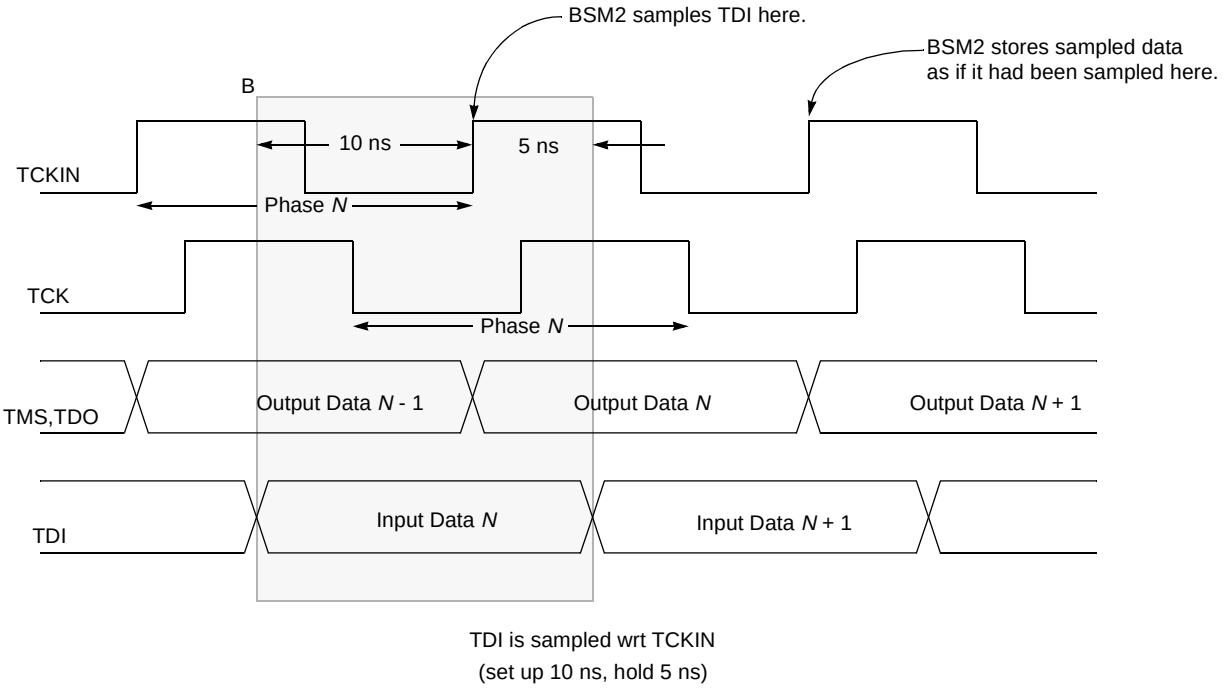


Figure 19. Relationships of TCKIN, TCK, TDI, TDO, and TMS with TCKIN Frequency of 65 ns and TMS Defined by Clock Divider Value of 1

Appendix E—BSM2 Operation as a Function of Phase Relation of TCK and TCKIN at High Speeds with Low-Valued Clock Divider (continued)

Case 3: Finally, consider the example of the signal on TCK having half the frequency of the signal on TCKIN and the latter operating at 65 MHz (fmax). (See Figure 20.) When the clock divider is not equal to 1, then the propagation delay is a little different, on the order of 15 ns—almost one full cycle of the signal on TCKIN. However, this correlates well with the 15 ns delays of TMS and TDO so that, in combination, the delays create operation satisfying *IEEE* Std 1149.1.

With regard to TDI, the BSM2 design in a situation with the clock divider value not equal to one follows the following rule: Latch TDI with the last positive edge of the clock signal on TCKIN of each TCK cycle. At low TCKIN frequencies, the 15 ns delays would be insignificant, and it would latch at the end of the cycle—close to the negative edge of the signal on TCK as in Figure 18. But, in this third instance, the latching action gets advanced into the phase somewhat. However, even in the worst case of 65 MHz, it does not create a one clock cycle delay as the divide by one did (case 2). For example, if TDO were looped back to TDI, we would still be capturing the correct phase—as is shown in the figure. However, the tolerance for delays on the TDI signal should still be considered in the external design of the TAP chain.

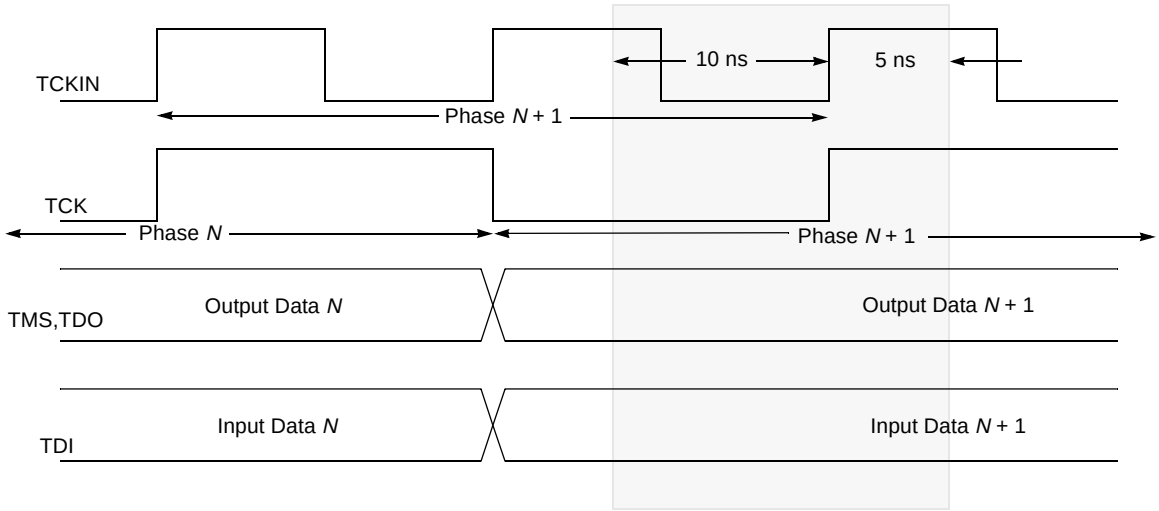


Figure 20. Relationships of TCKIN, TCK, TDI, TDO, and TMS with TCKIN Frequency of 65 ns and TMS Defined by Clock Divider Value of 2

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