# 16 Pin DIL 3 Bit Programmable ECL Delay Lines

## DELAYS AND TOLERANCES (in nS)

| PART NUMBER | MINIMUM DELAY (Inherent) | MAX IMUM DELAY (Nom) | DELAY/STEP | STEP DELAY TOLERANCE (Ref. Inherent Delay) | TRUTH TABLE (Programming Pins = CBA) 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EP9450-1 | 3.0 ± .3 | 10 | 1 ±0.3 | ±0.4 nS or ±5% | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
| EP9450-2 | 3.0 ± .3 | 17 | 2 ±0.4 | ±0.6 nS or ±5% | 3 | 5 | 7 | 9 | 11 | 13 | 15 | 17 |
| EP9450-3 | 3.0 ± .3 | 24 | 3 ±0.5 | ±0.8 nS or ±5% | 3 | 6 | 9 | 12 | 15 | 18 | 21 | 24 |
| EP9450-4 | 3.0 ± .3 | 31 | 4 ±0.5 | ±1.0 nS or ±5% | 3 | 7 | 11 | 15 | 19 | 23 | 27 | 31 |
| EP9450-5 | 3.0 ± .3 | 38 | 5 ±0.5 | ±1.0 nS or ±5% | 3 | 8 | 13 | 18 | 23 | 28 | 33 | 38 |
| EP9450-6 | 3.0 ± .3 | 45 | 6 ±0.6 | ±2.0 nS or ±5% | 3 | 9 | 15 | 21 | 27 | 33 | 39 | 45 |
| EP9450-7 | 3.0 ± .3 | 52 | 7 ±0.7 | ±2.0 nS or ±5% | 3 | 10 | 17 | 24 | 31 | 38 | 45 | 52 |
| EP9450-8 | 3.0 ± .3 | 59 | 8 ±0.8 | ±2.0 nS or ±5% | 3 | 11 | 19 | 27 | 35 | 43 | 51 | 59 |
| EP9450-9 | 3.0 ± .3 | 66 | 9 ±0.9 | ±2.0 nS or ±5% | 3 | 12 | 21 | 30 | 39 | 48 | 57 | 66 |
| EP9450-10 | 3.0 ± .3 | 73 | 10 ± 1.0 | ±2.0 nS or ±5% | 3 | 13 | 23 | 33 | 43 | 53 | 63 | 73 |
| EP9450-15 | 3.0 ± .3 | 108 | 15 ± 1.5 | ±2.0 nS or ±5% | 3 | 18 | 33 | 48 | 63 | 78 | 93 | 108 |
| EP9450-20 | 3.0 ± .3 | 143 | 20 ± 2.0 | ±2.0 nS or ±5% | 3 | 23 | 43 | 63 | 83 | 103 | 123 | 143 |
| EP9450-25 | 3.0 ± .3 | 178 | 25 ± 2.0 | ±2.0 nS or ±5% | 3 | 28 | 53 | 78 | 103 | 128 | 153 | 178 |
| EP9450-30 | 3.0 ± .3 | 213 | 30 ± 2.0 | ±2.0 nS or ±5% | 3 | 33 | 63 | 93 | 123 | 153 | 183 | 213 |
| EP9450-35 | 3.0 ± .3 | 248 | 35 ± 2.0 | ±2.0 nS or ±5% | 3 | 38 | 73 | 108 | 143 | 178 | 213 | 248 |
| EP9450-40 | 3.0 ± .3 | 283 | 40 ± 2.5 | ±2.0 nS or ±5% | 3 | 43 | 83 | 123 | 163 | 203 | 243 | 283 |
| EP9450-45 | 3.0 ± .3 | 318 | 45 ± 2.5 | ±2.0 nS or ±5% | 3 | 48 | 93 | 138 | 183 | 228 | 273 | 318 |
| EP9450-50 | 3.0 ± .3 | 353 | 50 ± 2.5 | ±2.0 nS or ±5% | 3 | 53 | 103 | 153 | 203 | 253 | 303 | 353 |

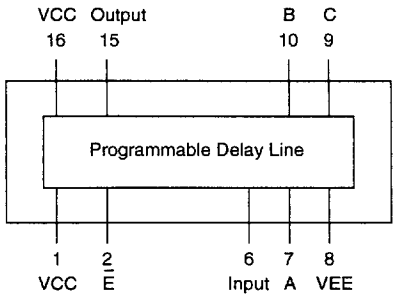
*Delay Times referenced from input to leading edges at 25°C, 5.0V.*

## DC Electrical Characterstics

($V_{CC1} = V_{CC2} = GRD$, $V_{EE} = 5.2V \pm 0.01V$
Output Loading With 50 Ohms to -2.0V±0.01V)

| | Parameter | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | High Level Ouput Voltage | $V_{IL}$ = Min | -960 | | mV |
| $V_{OHT}$ | High Level Output Threshold Voltage | | -980 | | mV |
| $V_{OLT}$ | Low Level Ouptut Threshold Voltage | | | -1630 | mV |
| $V_{OL}$ | Low Level Output Voltage | $V_{IH}$ = Max | | -1650 | |
| $I_{IH}$ | High Level Input Current | $V_{IH}$ = Max | | 15 | mA |
| $I_{IL}$ | Low Level Input Current | $V_{IL}$ = Min | 0.5 | | mA |
| $-I_{EE}$ | $V_{EE}$ Supply Current | | | 75 | mA |

## Schematic

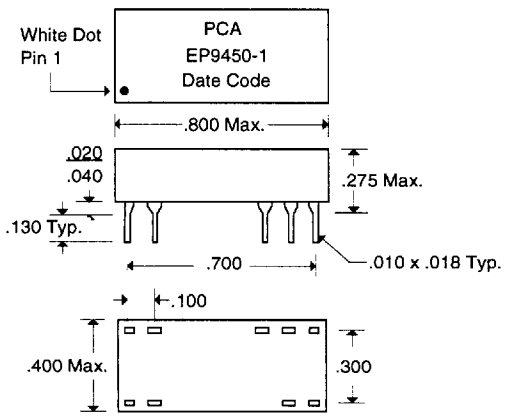



## Recommended Operating Conditions

| | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{EE}$ | Supply Voltage (Negative) | 4.94 | 5.46 | V |
| $V_{CC}$ | Circuit Ground (Pins 1 and 16) | 0 | 0 | V |
| $V_{IH}$ | High Level Input Voltage | -980 | -810 | mV |
| $V_{IHT}$ | High Level Input Threshold Voltage | -1105 | | mV |
| $V_{IL}$ | Low Level Input Voltage | -1850 | -1630 | mV |
| $V_{ILT}$ | Low Level Input Threshold Voltage | | -1475 | mV |
| $P_W$* | Pulse Width of Total Delay | 40 | | % |
| d* | Duty Cycle | | 40 | % |
| $T_A$ | Operating Free-Air Temperature | -30 | +80 | °C |

**These two values are inter-dependent.*

## Package




## Input Pulse Test Conditions @ 25° C

| | | |
|---|---|---|
| $V_{IN}$ | Pulse Input Voltage | -1.0V (-0.75 to - 1.75V) |
| $P_{IN}$ | Pulse Width of Total Delay | 3 x Max Delay |
| $T_{RI}$ | Pulse Rise Time | 2 nS |
| $P_{RR}$ | Pulse Repetition Rate | 10 x Td |
| $V_{EE}$ | Supply Voltage | -5.2V |



Unless Otherwise Noted Dimensions in Inches
Tolerances:
Fractional = ± 1/32
.XX = ± .030 .XXX = ± .010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