

4 M × 9-Bit Dynamic RAM Module

HYM 94500S/-60/-70/-80
HYM 94500L/-60/-70/-80

Advanced Information

- 4 194 304 words by 9-bit organization
- Fast access and cycle time
 - 60 ns access time
 - 110 ns cycle time (-60 version)
 - 70 ns access time
 - 130 ns cycle time (-70 version)
 - 80 ns access time
 - 150 ns cycle time (-80 version)
- Fast page mode capability with
 - 45 ns cycle time (-60/-70 version)
 - 50 ns cycle time (-80 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
 - max. 5445 mW active (-60 version)
 - max. 4950 mW active (-70 version)
 - max. 4455 mW active (-80 version)
 - CMOS – 49.5 mW standby
 - TTL – 99 mW standby
- Common $\overline{\text{CAS}}$ control for eight common data-in and data-out lines
- Separate $\overline{\text{CAS}}$ control for ninth bit
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only-refresh, Hidden refresh
- 9 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- Single in-Line Memory Module socket (HYM 94500S) and lead (HYM 94500L) version
- Pin configuration according to JEDEC standards
- Utilizes nine 4M × 1-DRAMs in 300 mil wide SOJ packages
- 1024 refresh cycles / 16 ms

The HYM 94500S/L-60/-70/-80 is a 4 Mbyte RAM module organized as 4 194 304 words by 9-bit in a 30-pin single-in-line package comprising nine HYB 514100BJ 4 M × 1 DRAMs in 300 mil wide SOJ-packages mounted together with nine 0.2 µF multilayer ceramic decoupling capacitors on a PC board.

Each HYB 514100BJ is described in the data sheet and is fully electrical tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

A common CAS controls for eight common data-in and data-out lines.

Bit nine (D8, Q8) which is generally used for parity is controlled by $\overline{\text{CAS}}$.

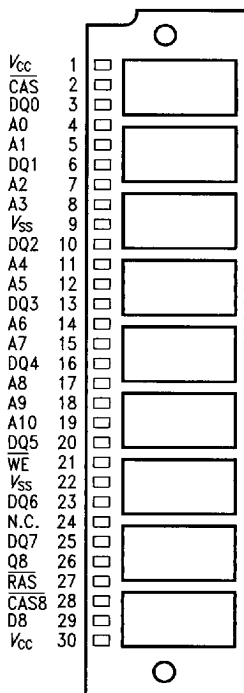
The common I/O feature on the HYM 94500S/L-60/-70/-80 dictates the use of early write cycles to prevent contention on D and Q.

Ordering Information

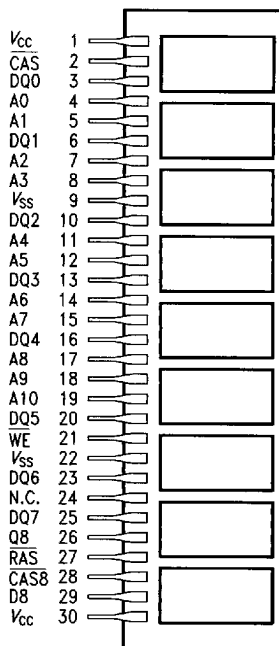
Type	Ordering Code	Package	Descriptions
HYM 94500S-60	Q67100-Q574	L-SIM-30-3	DRAM Module (access time 60 ns) ¹⁾
HYM 94500S-70	Q67100-Q582	L-SIM-30-3	DRAM Module (access time 70 ns) ¹⁾
HYM 94500S-80	Q67100-Q573	L-SIM-30-3	DRAM Module (access time 80 ns) ¹⁾
HYM 94500L-60	on request	L-SIM-30-4	DRAM Module (access time 60 ns) ²⁾
HYM 94500L-70	on request	L-SIM-30-4	DRAM Module (access time 70 ns) ²⁾
HYM 94500L-80	Q67100-Q798	L-SIM-30-4	DRAM Module (access time 80 ns) ²⁾

¹⁾ Socket type

²⁾ Pin type



HYM 94500S
(Socket type)



SPP02207

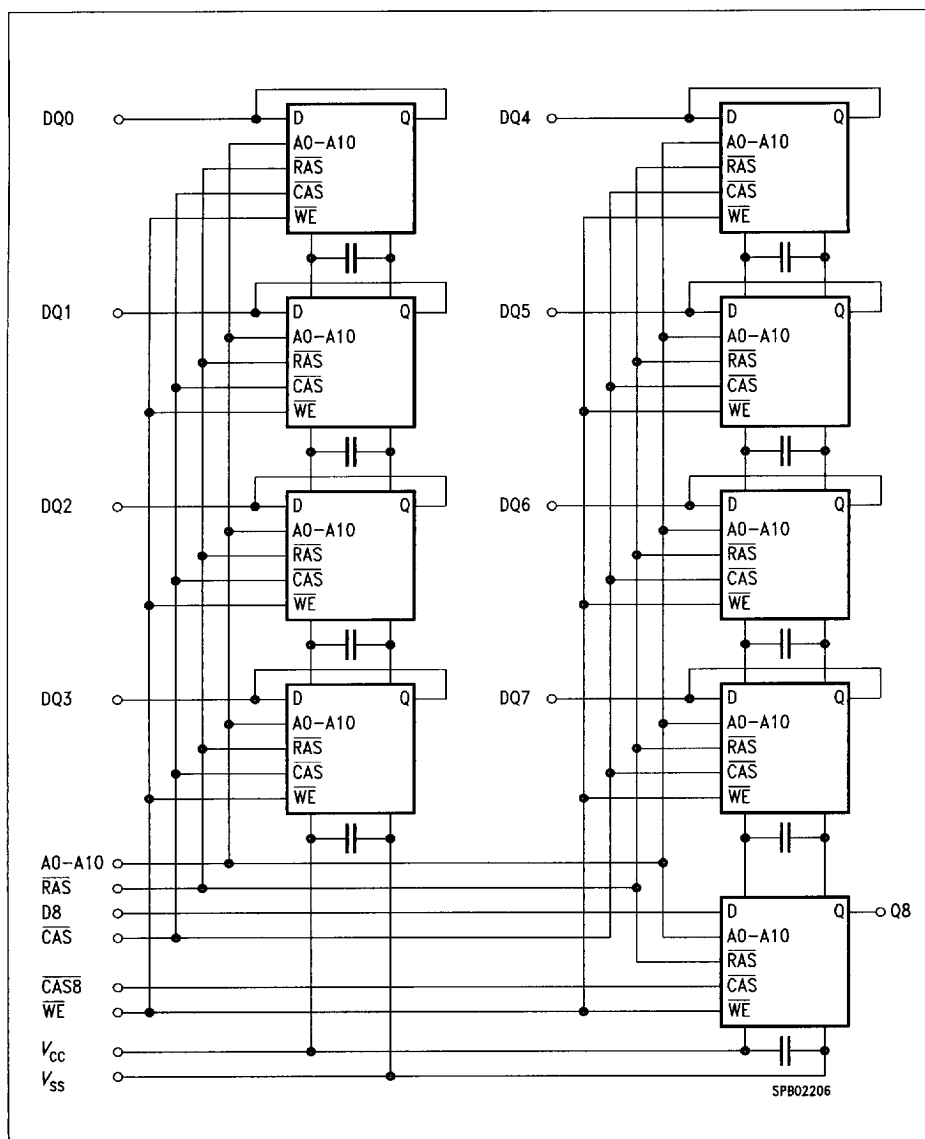
HYM 94500L
(Pin type)

Pin Names

A0-A10	Address Inputs
DQ0-DQ7	Data Input/Output
D8	Data Input
Q8	Data Output
RAS	Row Address Strobe
CAS	Column Address Strobe

CAS8	Column Address Strobe
WE	Read/Write Input
V _{cc}	Power Supply (+ 5 V)
V _{ss}	Ground (0 V)
N.C.	No Connection

Pin Configuration



Block Diagram

Absolute Maximum Ratings

Operating temperature range	0 to + 70 °C
Storage temperature range	– 55 to + 125 °C
Soldering temperature	260 °C
Soldering time	10 s
Input/output voltage	– 1 to + 7 V
Power supply voltage	– 1 to + 7 V
Power dissipation	6.93 W
Data out current (short circuit)	50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics ¹⁾

$T_A = 0$ to 70 °C; $V_{CC} = 5$ V $\pm$ 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	6.5	V	–
Input low voltage	V_{IL}	– 1.0	0.8	V	–
Output high voltage ($I_{OUT} = -5$ mA)	V_{OH}	2.4	–	V	–
Output low voltage ($I_{OUT} = 4.2$ mA)	V_{OL}	–	0.4	V	–
Input leakage current (0 V < V_{IN} < 6.5 V, all other pins = 0 V)	$I_{(L)}$	– 10	10	μ A	–
Output leakage current (DO is disabled, 0 V < V_{OUT} < 5.5 V)	$I_{O(L)}$	– 10	10	μ A	–
Average V_{CC} supply current: HYM 94500S/L-60 HYM 94500S/L-70 HYM 94500S/L-80 ($\overline{RAS}$, $\overline{CAS}$, address cycling, $t_{RC} = t_{RC\ min.}$)	I_{CC1}	– – –	990 900 810	mA mA mA	2), 3)
Standby V_{CC} supply current ($RAS = CAS = V_{IH}$)	I_{CC2}	–	18	mA	–
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles: HYM 94500S/L-60 HYM 94500S/L-70 HYM 94500S/L-80 ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC\ min.}$)	I_{CC3}	– – –	990 900 810	mA mA mA	2)

Notes see page 349.

DC Characteristics (cont'd) ¹⁾

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode: HYM 94500S/L-60 HYM 94500S/L-70 HYM 94500S/L-80 $(\overline{RAS} = V_{IL}, \overline{CAS}, \text{address cycling}; t_{PC} = t_{PC \text{ min.}})$	I_{CC4}	— — —	630 540 450	mA mA mA	2), 3)
Standby V_{CC} supply current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2 \text{ V}$)	I_{CC5}	—	9	mA	—
Average V_{CC} supply current during CAS-before-RAS refresh mode: HYM 94500S/L-60 HYM 94500S/L-70 HYM 94500S/L-80 ($\overline{RAS}, \overline{CAS}$ cycling, $t_{RC} = t_{RC \text{ min.}}$)	I_{CC6}	— — —	990 900 810	mA mA mA	2)

Notes see page 349.

Capacitance

 $T_A = 0 \text{ to } 70^\circ\text{C}; V_{CC} = 5 \text{ V} \pm 10\%; f = 1 \text{ MHz}$

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10)	C_{I1}	—	70	pF
Input capacitance ($\overline{RAS}, \overline{CAS}, \overline{WE}$)	C_{I2}	—	50	pF
Input capacitance (D8, CAS8)	C_{I3}	—	10	pF
I/O capacitance (DQ0 to DQ7)	C_{I0}	—	17	pF
Output capacitance (Q8)	C_O	—	10	pF

AC Characteristics ^{4) 5)} $T_A = 0 \text{ to } 70^\circ\text{C}$; $V_{CC} = 5 \text{ V} \pm 10\%$; $t_r = 5 \text{ ns}$

Parameter	Symbol	Limit Values						Unit
		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	—	130	—	150	—	ns
Fast page mode cycle time	t_{PC}	45	—	45	—	50	—	ns
Access time from $\overline{\text{RAS}}$ ^{6) 11) 12)}	t_{RAC}	—	60	—	70	—	80	ns
Access time from $\overline{\text{CAS}}$ ^{6) 11)}	t_{CAC}	—	20	—	20	—	20	ns
Access time from column address ^{6) 12)}	t_{AA}	—	30	—	35	—	40	ns
Access time from $\overline{\text{CAS}}$ precharge ⁶⁾	t_{CPA}	—	40	—	40	—	45	ns
$\overline{\text{CAS}}$ to output in low-Z ⁶⁾	t_{CLZ}	0	—	0	—	0	—	ns
Output buffer turn-off delay ⁷⁾	t_{OFF}	0	20	0	20	0	20	ns
Transition time (rise and fall) ⁵⁾	t_T	3	50	3	50	3	50	ns
$\overline{\text{RAS}}$ precharge time	t_{RP}	40	—	50	—	60	—	ns
$\overline{\text{RAS}}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns
$\overline{\text{RAS}}$ pulse width (fast page mode)	t_{RASP}	60	200000	70	200000	80	200000	ns
$\overline{\text{RAS}}$ hold time	t_{RSH}	20	—	20	—	20	—	ns
$\overline{\text{CAS}}$ hold time	t_{CSH}	60	—	70	—	80	—	ns
$\overline{\text{CAS}}$ pulse width	t_{CAS}	20	10000	20	10000	20	10000	ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time ¹¹⁾	t_{RCD}	20	40	20	50	20	60	ns
$\overline{\text{RAS}}$ to column address delay time ¹²⁾	t_{RAD}	15	30	15	35	15	40	ns
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	5	—	5	—	5	—	ns
$\overline{\text{CAS}}$ precharge time (fast page mode)	t_{CP}	10	—	10	—	10	—	ns
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns
Column address hold time	t_{CAH}	15	—	15	—	15	—	ns

Notes see page 349.

AC Characteristics ^{4) 5)} (cont'd) $T_A = 0 \text{ to } 70^\circ\text{C}$; $V_{CC} = 5 \text{ V} \pm 10\%$; $t_T = 5 \text{ ns}$

Parameter	Symbol	Limit Values						Unit
		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	
Column address hold time ref. to RAS	t_{AR}	50	—	55	—	60	—	ns
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	40	—	ns
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns
Read command hold time ⁸⁾	t_{RCH}	0	—	0	—	0	—	ns
Read command hold time ref. to RAS ⁸⁾	t_{RRH}	0	—	0	—	0	—	ns
Write command hold time	t_{WCH}	10	—	15	—	15	—	ns
Write command hold time ref. to RAS	t_{WCR}	45	—	55	—	60	—	ns
Write command pulse width	t_{WP}	10	—	15	—	15	—	ns
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	20	—	20	—	20	—	ns
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	20	—	20	—	20	—	ns
Data setup time ⁹⁾	t_{DS}	0	—	0	—	0	—	ns
Data hold time ⁹⁾	t_{DH}	15	—	15	—	15	—	ns
Data hold time ref. to $\overline{\text{RAS}}$	t_{DHR}	50	—	55	—	60	—	ns
Refresh period	t_{REF}	—	16	—	16	—	16	ms
Write command setup time ¹⁰⁾	t_{WCS}	0	—	0	—	0	—	ns
$\overline{\text{CAS}}$ setup time ¹³⁾	t_{CSR}	5	—	5	—	5	—	ns
$\overline{\text{CAS}}$ hold time ¹³⁾	t_{CHR}	15	—	15	—	15	—	ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t_{RPC}	0	—	0	—	0	—	ns
$\overline{\text{CAS}}$ precharge time ¹³⁾	t_{CPN}	10	—	10	—	10	—	ns
Write to $\overline{\text{RAS}}$ precharge time ¹³⁾	t_{WRP}	10	—	10	—	10	—	ns
Write hold time ref. to RAS ¹³⁾	t_{WRH}	10	—	10	—	10	—	ns

Notes see page 349.

Waveforms see page 391.

Notes for pages 345 to 348:

- 1) All voltages are referenced to V_{SS} .
- 2) I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} depend on cycle rate.
- 3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
- 4) An initial pause of 200 μ s is required after power-up followed by 8 $\overline{RAS}$ cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
- 5) $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL} .
- 6) Measured with a load equivalent of 2 TTL loads and 100 pF.
- 7) $t_{OFF}(\max)$ defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.
- 8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- 9) These parameters are referenced to the $\overline{CAS}$ leading edge.
- 10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}(\min)$, the cycles is an early write cycle and data out pin will remain open circuit (high impedance).
- 11) Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max.)$ can be met. $t_{RCD}(\max.)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled by t_{CAC} .
- 12) Operation within the $t_{RAD}(\max.)$ limit insures that $t_{RAC}(\max.)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
- 13) For $\overline{CAS}$ -before- $\overline{RAS}$ cycles only.