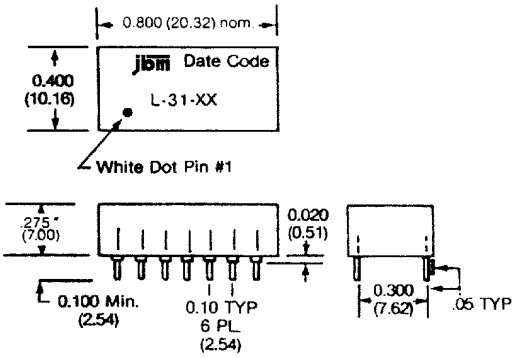
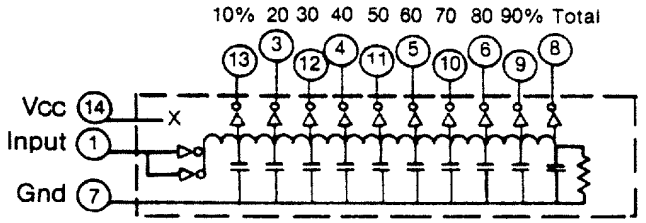
Delay Range 50 thru 1000 nsec

STYLE L-31 (14-pin DIP)

10 equally-spaced taps

TTL and DTL Compatible





Dimensions in inches (mm).

INPUT CONDITIONS

Operating Temp . . . . . 0° to + 70°C
Storage Temp . . . . . – 55°C to + 125°C
(All lines internally terminated)
I_{IH} Logic "1" Input Current . . . . . 100μA Max.
I_{IL} Logic "0" Input Current . . . . . – 4mA Max.
V_{OH} Logic "1" Voltage Out . . . . . 2.7V Min.
V_{OL} Logic "0" Voltage Out . . . . . 0.5V Max.

DRIVE CAPABILITIES
(TTL LOADS)

Logic "0" { 10 Loads / Tap Max.
20 Loads / Unit Max.

Logic "1" 20 Loads / Unit Max.

Supply Current . . . . . 150 mA Typ.
Voltage Range . . . . . 4.75V to 5.25V

TOTAL DELAY (nsec ± 5%)	TAP INTERVALS (nsec*)	RISE TIME (ns MAX) (0.8 to 2.0V)	JBM PIN L-31-XX
50	5.0 ± 3ns	2.0	L-31-50
75	7.5 ± 3ns	2.0	L-31-51
100	10.0 ± 3ns	2.0	L-31-52
125	12.5 ± 3ns	2.5	L-31-53
150	15.0 ± 3ns	2.5	L-31-54
175	17.5 ± 3ns	3.0	L-31-55
200	20.0 ± 3ns	3.0	L-31-56
250	25.0 ± 3ns	3.0	L-31-57
300	30.0 ± 5%	3.5	L-31-58
350	35.0 ± 5%	3.5	L-31-59
400	40.0 ± 5%	4.0	L-31-60
450	45.0 ± 5%	4.0	L-31-61
500	50.0 ± 5%	4.0	L-31-62
600	60.0 ± 5%	4.5	L-31-63
700	70.0 ± 5%	4.5	L-31-64
750	75.0 ± 5%	4.5	L-31-65
800	80.0 ± 5%	5.0	L-31-66
900	90.0 ± 5%	5.0	L-31-67
1000	100.0 ± 5%	5.0	L-31-68

* 50ns – 250ns TAP/TAP; 300ns – 1,000ns cumulative @ 25°C, 5.00VDC.

Delays may change 2% or 1ns for a respective 5% increase or decrease in supply voltage.

Consult factory for other delays, tolerances, and logic families.