Features

- Sixteen full-duplex, serial time-division multiplexed (TDM) highway streams
- Switching up to 2,048 incoming PCM channels to up to 2,048 outgoing PCM channels
- Accept data rates of 2.048Mb/s, 4.096Mb/s, 8.192Mb/s (Single-Rate mode) or any combination of data rates of 2.048Mb/s, 4.096Mb/s and 8.192Mb/s (Multi-Rate mode)
- 64 kbits/s granularity with optional 32 kbits/s (4-bit) and 16 kbits/s (2-bit) subrate switching
- Tristate function per-channel for further expansion
- Low-latency/frame integrity selection per-channel
- Automatic frame offset delay measurement.
- Per input stream offset programming
- Intel/Motorola microprocessor interface
- Connection memory block programming for fast device initialization
- Automatically identifies ST-BUS/GCI formats
- Internal loopback per-channel for diagnostic purposes
- IEEE-1149.1 (JTAG) boundary scan

Applications

- Medium and large switching platforms
- CTI application
- Voice/data multiplexer
- Digital cross-connect
- ST-BUS/GCI interface functions
- DM highway data rate adaptation
- LAN/WAN gateways

Introduction

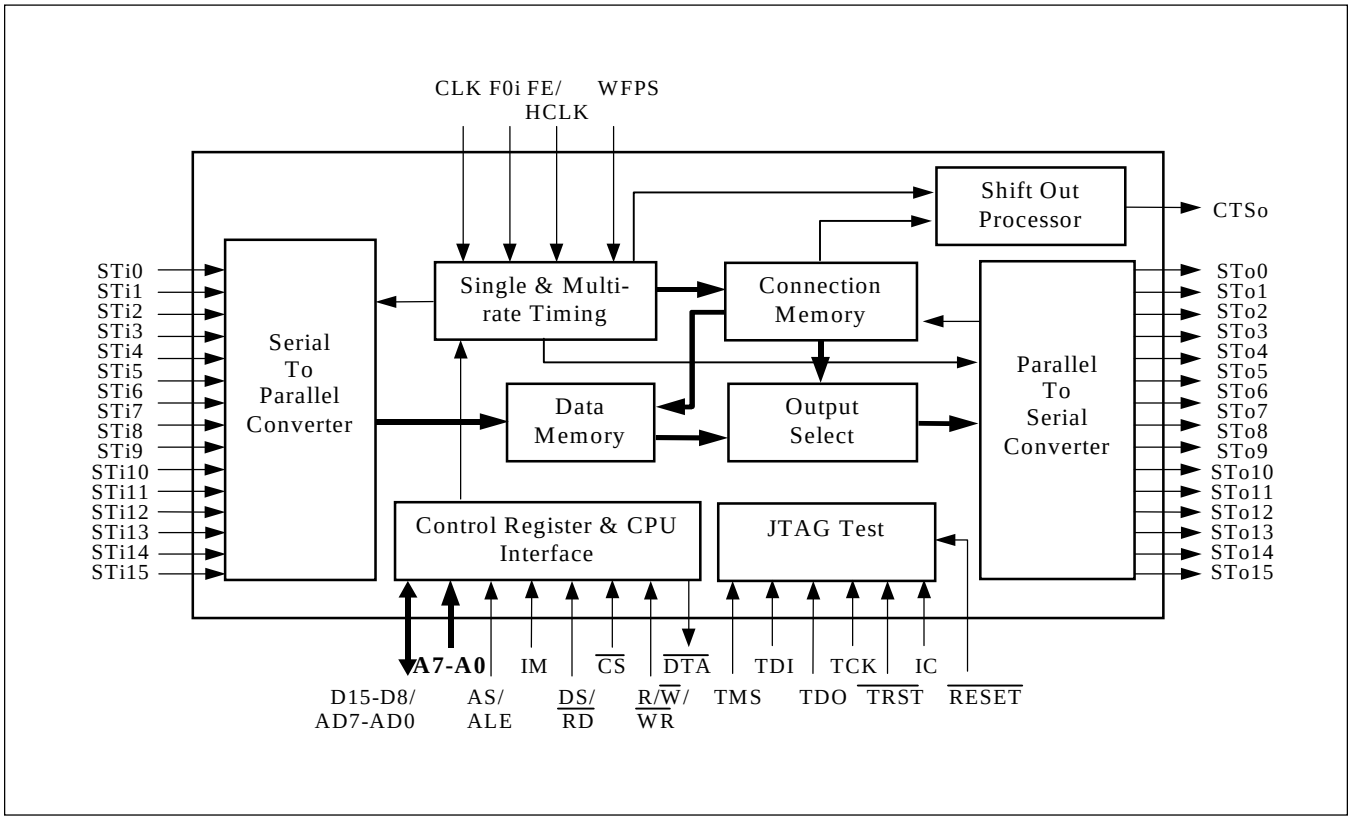
The PT7A5020 is a Multi-rate Large Digital Switch (MLDS). It provides 2,048 x 2,048 channel non-blocking switching among 16 input streams and 16 output streams at most.

This device can operate in two modes: Single-Rate mode and Multi-Rate mode. In Single-Rate mode, the all 16 input streams and 16 output streams serial bit rate must be single rate of 8.192Mb/s, 4.096Mb/s or 2.048Mb/s. In Multi-Rate mode, the 16 input streams and the 16 output streams are both divided into two parts, the serial bit rate of each one of the four parts can be 8.192Mb/s, 4.096Mb/s or 2.048Mb/s independently.

The device has many features that are programmable on stream or channel basis, including message mode, input offset delay and high impedance output control. Per steam input delay control is particularly useful for managing large multi-chip switches that transport both voice channel and concatenated data channels. In addition, input stream can be individually calibrated for input frame offset using a dedicated pin.

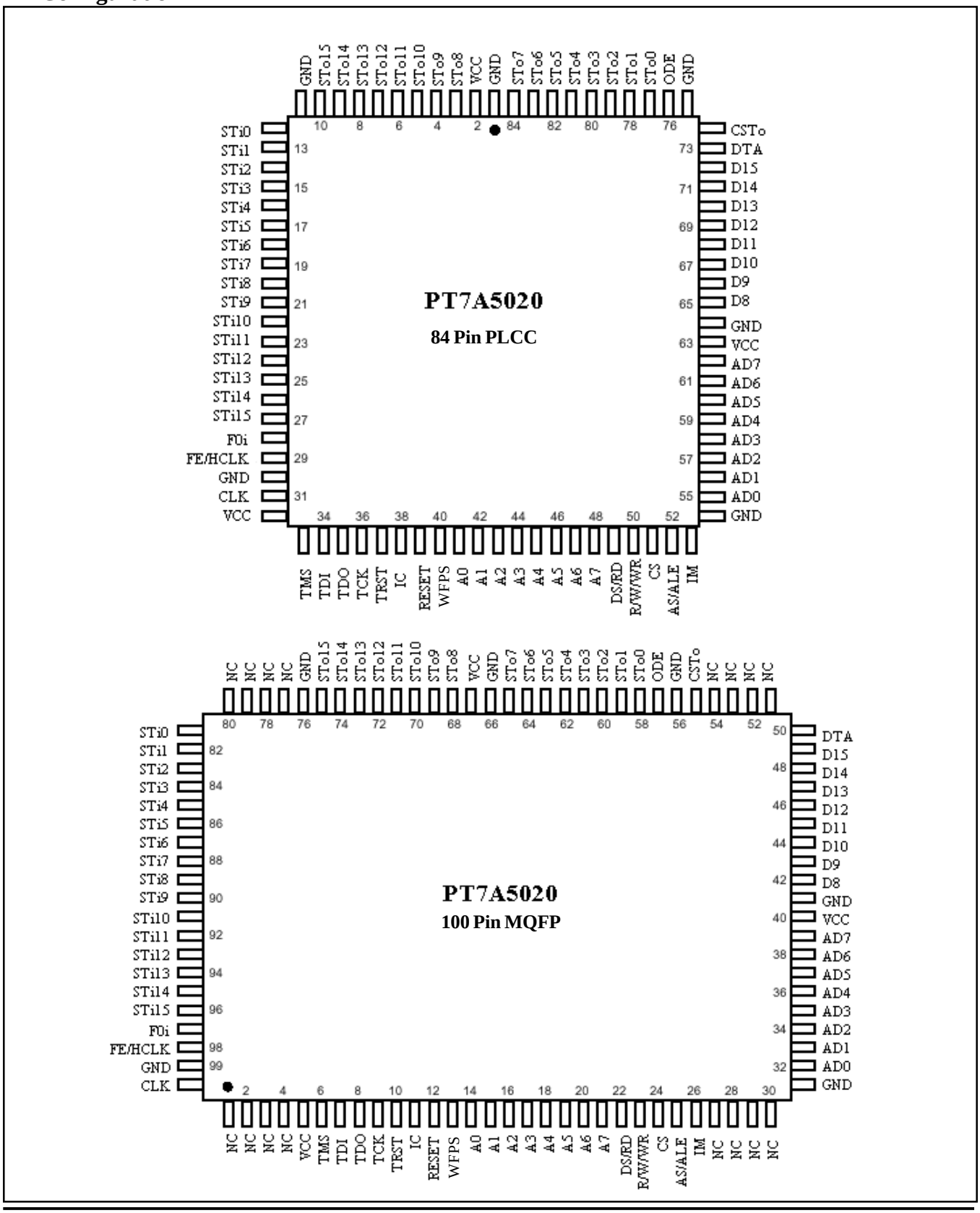
Part Number	Package
PT7A5020J	84 - Pin PLCC
PT7A5020M	100 - Pin MQFP

Block Diagram



Pin Information

Pin Configuration



Pin Description

Pin No.		Type	Name	Description
84-PL-CC	100-M-QFP			
1, 11, 30, 54 64, 75	31, 41, 56, 66, 76, 99	GND	GND	Ground.
2, 32, 63	5, 40, 67	Power	V_{CC}	+5V Power Supply.
3 - 10 77 - 84	68-75 58 - 65	O	STo8 - 15 STo0 - 7	ST-BUS Output (Three-state Outputs): Serial data Output streame, data rates of 2.048, 4.096 or 8.192 Mb/s, programmable by bits DR0 - 1 in the IMS register.
12 -27	81-96	I	STi0 - 15	ST-BUS Input: Serial data input stream, data rates of 2.048, 4.096 or 8.192 Mb/s, programmable by bits DR0 - 1 in the IMS register.
28	97	I	F0i	Frame Pulse: accepts and automatically identifies frame synchronization signals formatted according to ST-BUS and GCI specifications when WFPS=0, and accepts a negative frame pulse which conforms to WFPS formats when WFPS=1.
29	98	I	FE/HCLK	Frame Evaluation/HCLK Clock: frame measurement input when WFPS=0, when WFPS=1, the HCLK (4.096MHz clock) is required for frame alignment in the wide frame pulse (WFP) mode.
31	100	I	CLK	Clock: Serial clock for shifting data in/out on the serial streams (STi/o 0 - 15). In Single-Rate mode, this input accepts a 4.096, 8.192 or 16.384 MHz clock; in Multi-Rate mode, this pin only accepts 16.384 MHz clock..
33	6	I	TMS	Test Mode Select (Input): JTAG signal that controls the state transitions of the TAP controller. Pulled high by an internal pull-up when not driven.
34	7	I	TDI	Test Serial Data In: input for JTAG serial test instructions and data, pulled high by an internal pull-up when not driven.
35	8	O	TDO	Test Serial Data Out: output for JTAG serial data on the falling edge of TCK. It is held in high impedance state when JTAG scan is not enable.
36	9	I	TCK	Test Clock: clock to the JTAG test logic. Pulled high by an internal pull-up when not driven.
37	10	I	$\overline{\text{TRST}}$	Test Reset: Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin is pulled by an internal pull-up when not driven. This pin should be pulsed low on power-up, or held low, to ensure that the device is in the normal functional mode.
38	11	I	IC	Internal Connection: Connect to GND for normal operation. This pin must be low for normal operation and to comply with IEEE 1149 (JTAG) boundary scan requirements. It is pulled low internally when not driven.
39	12	I	$\overline{\text{RESET}}$	Device Reset (Schmitt Trigger Input): active LOW, reset the device by clearing the device internal counters, registers and setting STo0 - 15 and microport data outputs to a high impedance state. The time constant for a power up reset circuit must be a minimum of five times the rise time of the power supply. In normal operation, the RESET pin must be held low for a minimum of 100nsec to reset the device.

Pin No.		Type	Name	Description
84-PLCC	100-MQFP			
40	13	WFPS	I	Wide Frame Pulse Select: When 1, enables the WFP Frame Alignment interface. When 0, the device operates in ST-BUS/GCI mode.
41-48	14-21	A0-A7	I	Address 0 - 7: in non-multiplexed CPU bus operation, these lines provide the A0 - A7 address lines to the internal memories.
49	22	DS/$\overline{RD}$	I	Data Strobe / Read: For Motorola multiplexed bus operation, this input is DS. This active high DS input works in conjunction with CS to enable the read and write operations. For Motorola non-multiplexed CPU bus operation, this input is DS. This active low input works in conjunction with CS to enable the read and write operations. For Intel multiplexed bus operation, this input is RD. This active low input sets the data bus lines (AD0-AD7, D8-D15) as outputs.
50	23	R/$\overline{W}$ / $\overline{WR}$	I	Read/Write / Write: In the cases of Motorola non-multiplexed and multiplexed bus operations, this input is R/W. This input controls the direction of the data bus lines (AD0 - AD7, D8-D15) during a microprocessor access. For Intel multiplexed bus operation, this input is WR. This active low input is used with CS to control the data bus (AD0 - 7, D8 - D15) lines as inputs.
51	24	$\overline{CS}$	I	Chip Select: Active low input used by a processor to activate the microprocessor port of MLDS.
52	25	AS/ALE	I	Address Strobe or Latch Enable: This input is used if multiplexed bus operation is selected via the IM input pin. For Motorola non-multiplexed bus operation, connect this pin to ground. This pin is pulled low by an internal pull-down when not driven.
53	26	IM	I	CPU Interface Mode: When IM is high, the microprocessor port is in the multiplexed mode. When IM is low, the microprocessor port is in non-multiplexed mode. This pin is pulled low by an internal pull-down when not driven.
55-62	32-39	AD0-7	I/O	Address/Data Bus 0 to 7: These pins are the eight least significant data bits of the microprocessor port. In multiplexed mode, these pins are also the input address bits of the microprocessor port.
65-72	42-49	D8-15	I/O	Data Bus 8-15: These pins are the eight most significant data bits of the microprocessor port.
73	50	$\overline{DTA}$	O	Data Transfer Acknowledgement: Indicates that a data bus transfer is complete. When the bus cycle ends, this pin drives HIGH and then tri-states, allowing for faster bus cycles with a weaker pull-up resistor. A pull-up resistor is required to hold a HIGH level when the pin is tri-stated.
74	55	CSTo	O	Control Output: This is a 4.096, 8.192 or 16.384Mb/s output containing 512, 1024 or 2048 bits per frame respectively in Single-Rate mode. In Multi-Rate mode, this output rate is 16.384 Mb/s. The level of each bit is determined by the CSTo bit in the connection memory. See External Drive Control Section.
76	57	ODE	I	Output Drive Enable: This is the output enable control for the STo0 to STo15 serial outputs. When ODE input is low and the OSB bit of the IMS register is low, STo0-15 are in a high impedance state. If this input is high, the STo0-15 output drivers are enabled. However, each channel may still be put into a high impedance state by using the per channel control bit in the connection memory.
-	1-4 27-30 51-54 77-80	NC		No connection

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +125°C
Ambient Temperature with Power Applied ..... -40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc) ..... -0.3V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only) -0.3V to +7.0V
DC Input Voltage ..... -0.3V to +7.0V
DC Input and Output Current 20mA
Power Dissipation 2W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Sym	Characteristics	Test Conditions	Min	Typ	Max	Units
Vcc	Supply Votage		4.75	5.0	5.25	V
V_{IH}	Input HIGH Voltage		2.4		Vcc	V
V_{IL}	Input LOW Voltage		0		0.4	V
T_A	Operating Temperature		-40	25	85	^{O}C

Note:
Typical figures are at 25°C and are for design aid only; not production tested.

DC Electrical, Power Supply and Capacitance Characteristics

Sym	Description	Test Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current	Output unloaded, 2Mb/s			50	mA
		Output unloaded, 4Mb/s			90	mA
		Output unloaded, 8Mb/s			170	mA
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IL}	Input Leakage Current (Input Pins)	V_O between GND and V_{CC}			15	µA
	Input Leakage Current(with an internal pull-up or -down)				100	
V_{OL}	Output LOW Voltage	I_{OL} = 10mA		1.0		V
V_{OH}	Output HIGH Voltage	I_{OH} = 10mA	2.4	3.5		V
I_{OZ}	Output High Impedance Leakage	V_O between GND and V_{CC}			5	µA
C_{IN}	Input Pin Capacitance				10	pF
C_{OUT}	Output Pin Capacitance				10	pF

AC Electrical Characteristics

Sym	Description	Test Conditions	Min	Typ	Max	Units
V_{TT}	TTL Threshold			1.5		V
V_{HM}	TTL Rise/Fall Threshold Voltage High			2.0		V
V_{LM}	TTL Rise/Fall Threshold Voltage Low			0.8		V

Notes

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