



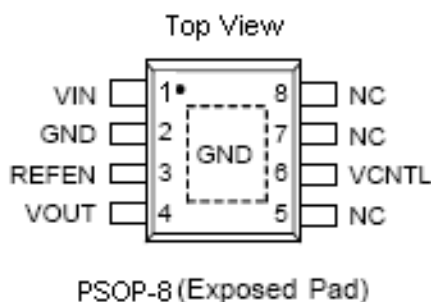
**Description**

The SE9174C is a simple, cost-effective and high-speed linear regulator designed to generate termination voltage in double data rate (DDR) memory system to comply with the JEDEC SSTL\_2 and SSTL\_18 or other specific interfaces such as HSTL, SCSI-2 and SCSI-3 etc. devices requirements. The regulator is capable of actively sinking or sourcing up to 2A while regulating an output voltage to within 40mV. The output termination voltage can be tightly regulated to track  $1/2V_{DDQ}$  by two external voltage divider resistors or the desired output voltage can be pro-grammed by externally forcing the REFEN pin voltage.

The SE9174C also incorporates a high-speed differential amplifier to provide ultra-fast response in line/load transient. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in bi-directions and on-chip thermal shut-down protection.

The SE9174C are available in the PSOP-8 (Exposed Pad) surface mount packages.

**Pin Configuration**



**Pin Description**

Pin Name	Pin function
$V_{IN}$	Power Input
GND	Ground
$V_{CNTL}$	Gate Drive Voltage
REFEN	Reference Voltage input and Chip Enable
$V_{OUT}$	Output Voltage

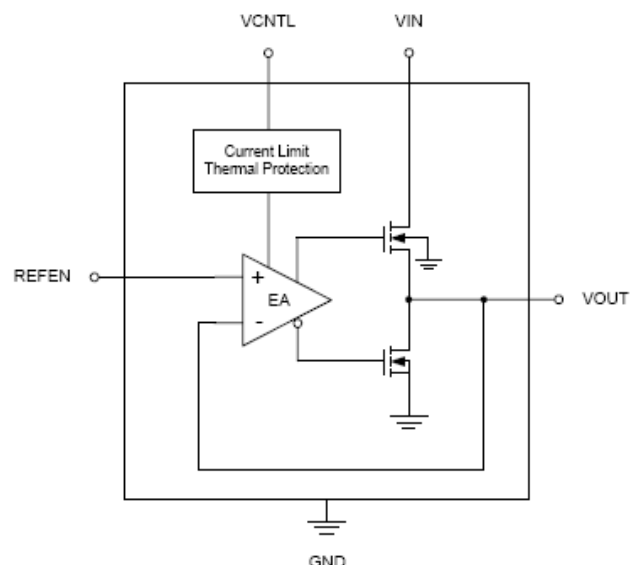
**Features**

- Ideal for DDR-I, DDR-II and DDR-III  $V_{TT}$  Applications
- Sink and Source 2A Continuous Current
- Integrated Power MOSFETs
- Generates Termination Voltage for SSTL\_2, SSTL\_18, HSTL, SCSI-2 and SCSI-3 Interfaces.
- High Accuracy Output Voltage at Full-Load
- Output Adjustment by Two External Resistors
- Low External Component Count
- Shutdown for Suspend to RAM (STR) Functionality with High-Impedance Output
- Current Limiting Protection
- On-Chip Thermal Protection
- Available in PSOP-8 (Exposed Pad) Packages
- $V_{IN}$  and  $V_{CNTL}$  No Power Sequence Issue
- 100% Lead (Pb)-Free

**Application**

- Desktop PCs, Notebooks, and Workstations
- Graphics Card Memory Termination
- Set Top Boxes, Digital TVs, Printers
- Embedded Systems
- Active Termination Buses
- DDR-I, DDR-II and DDR-III Memory Systems

**Block Diagram**





**Absolute Maximum Rating <sup>(1)</sup>**

Parameter	Symbol	Value	Unit
Input Voltage	$V_{IN}$	6	V
Control Voltage	$V_{CNTL}$	6	V
Power Dissipation	$P_D$	Internally Limited	--
ESD Rating	--	3	KV
Storage Temperature Range	$T_S$	-65 to 150	°C
Lead Temperature (Soldering, 5 sec.)	$T_{LEAD}$	260	°C
Package Thermal Resistance	$\Theta_{JC}$	28	°C/W

**Operating Rating <sup>(2)</sup>**

Parameter	Symbol	Value	Units
Input Voltage	$V_{IN}$	2.5 to 1.5 $\pm$ 3%	V
Control Voltage	$V_{CNTL}$	5.0 or 3.3 $\pm$ 5%	V
Ambient Temperature	$T_A$	-40 to +85	°C
Junction Temperature	$T_J$	-40 to +125	°C

**Electrical Characteristics**

$V_{IN}=2.5V/1.8V/1.5V$ ,  $V_{CNTL}=3.3V$ ,  $V_{REFEN}=1.25V/0.9V/0.75V$ ,  $C_{OUT}=10\mu F$  (Ceramic),  $T_A=25^\circ C$ , unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>Input</b>						
$V_{CNTL}$ Operation Current	$I_{CNTL}$	$I_{OUT}=0A$	--	1	2.5	mA
Standby Current	$I_{STBY}$	$V_{REFEN} < 0.2V$ (Shutdown), $R_{LOAD} = 180\Omega$	--	50	90	$\mu A$
<b>Output (DDR / DDR II / DDR III)</b>						
Output Offset Voltage <sup>(3)</sup>	$V_{OS}$	$I_{OUT}= 0A$	-20	--	+20	mV
Load Regulation <sup>(4)</sup>	$\Delta V_{LOAD}$	$I_{OUT}= +2A$	-20	--	+20	
		$I_{OUT}= -2A$				
<b>Protection</b>						
Current limit	$I_{LIM}$		2.2	--	--	A
Thermal Shutdown Temperature	$T_{SD}$	$3.3V \leq V_{CNTL} \leq 5V$	--	170	--	°C
Thermal Shutdown Hysteresis	$\Delta T_{SD}$	$3.3V \leq V_{CNTL} \leq 5V$	--	35	--	
<b>REFEN Shutdown</b>						
Shutdown Threshold	$V_{IH}$	Enable	0.6	--	--	V
	$V_{IL}$	Shutdown	--	--	0.2	

**Note 1:** Exceeding the absolute maximum rating may damage the device.

**Note 2:**  $V_{OS}$  offset is the voltage measurement defined as  $V_{OUT}$  subtracted from  $V_{REFEN}$

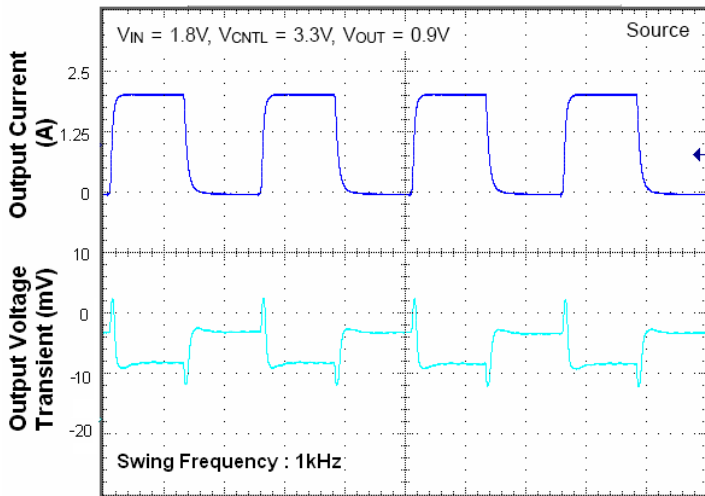
**Note 3:**  $V_{OS}$  offset is the voltage measurement defined as  $V_{OUT}$  subtracted from  $V_{REFEN}$ .

**Note 4:** Regulation is measured at constant junction temperature by using a 5ms current pulse. Devices are tested for load regulation in the load range from 0A to 2A.

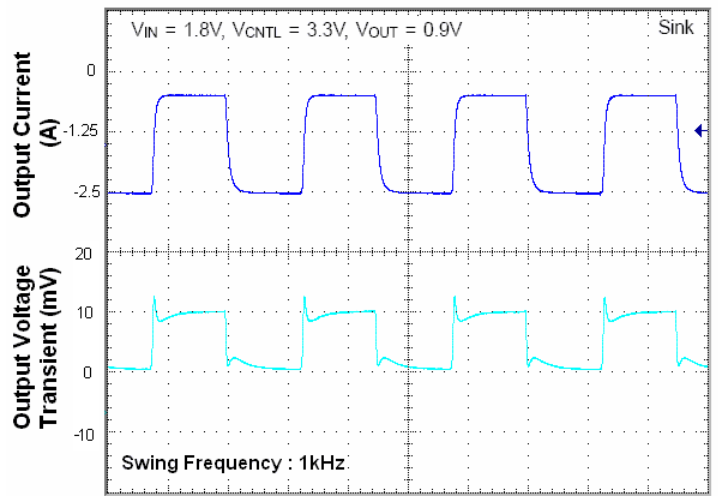


Typical Operating Characteristics

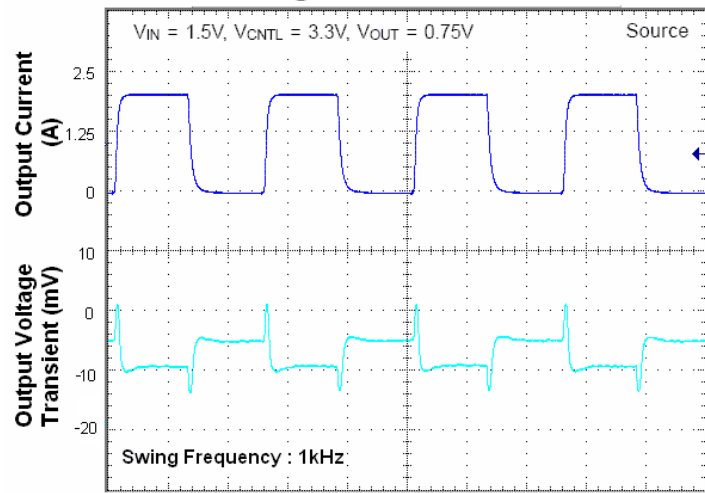
0.9V<sub>TT</sub> @ 2A Transient Response



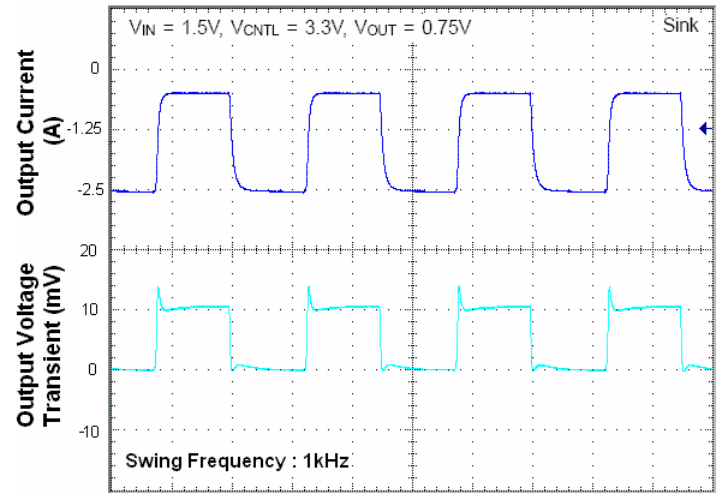
0.9V<sub>TT</sub> @ 2A Transient Response



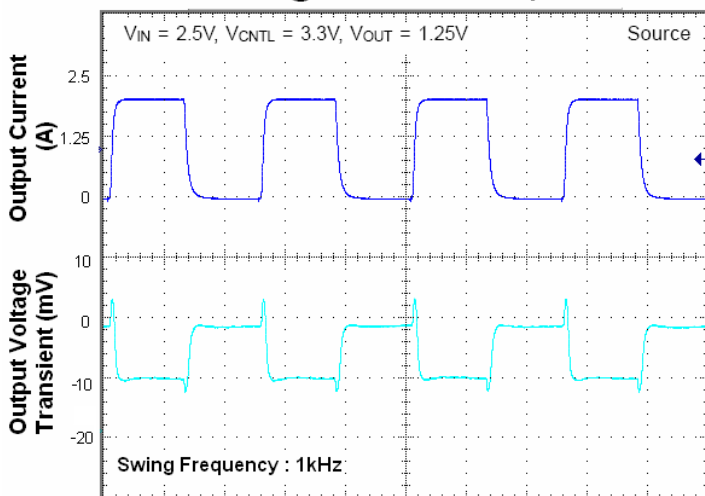
0.75V<sub>TT</sub> @ 2A Transient Response



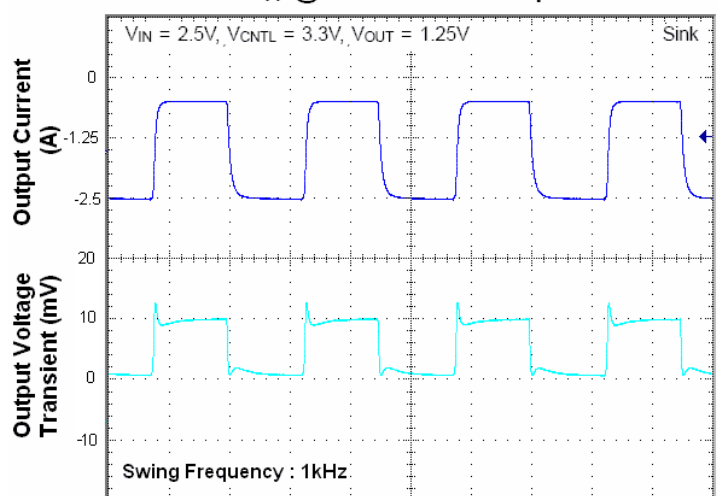
0.75V<sub>TT</sub> @ 2A Transient Response



1.25V<sub>TT</sub> @ 2A Transient Response



1.25V<sub>TT</sub> @ 2A Transient Response





## Application Information

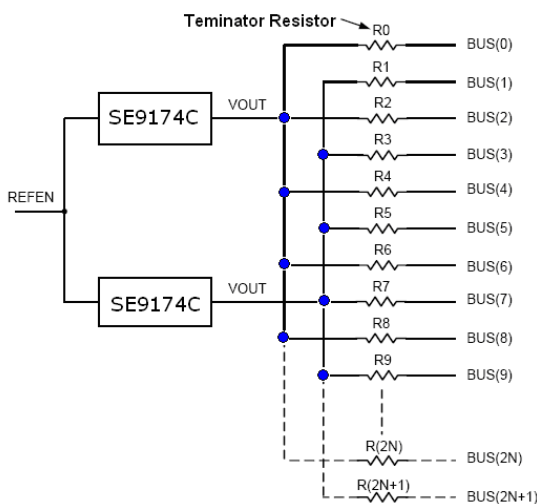
### Input Capacitor and Layout Consideration

Place the input bypass capacitor as close as possible to the SE9174C. A low ESR capacitor larger than 470uF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance.

Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between SE9174C and the preceding power converter.

### Consideration while designs the resistance of voltage divider

Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on V<sub>REFEN</sub> is below 0.2V. In addition, the capacitor and voltage divider form the lowpass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.



### Thermal Consideration

SE9174C regulators have internal thermal limiting circuitry designed to protect the device during overload conditions. For continued operation, do not exceed maximum operation junction temperature 125°C. The power dissipation definition in device is:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \Theta_{JA}$$

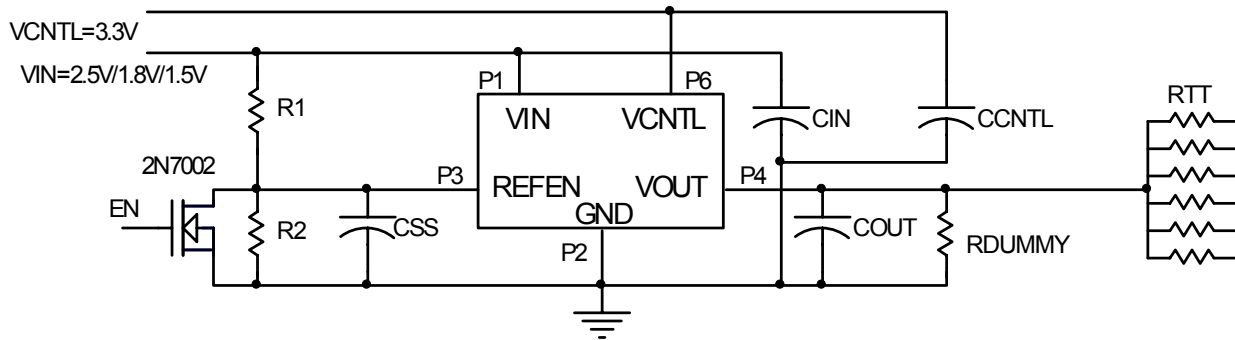
Where  $T_{J(MAX)}$  is the maximum operation junction temperature 125°C,  $T_A$  is the ambient temperature and the  $\Theta_{JA}$  is the junction to ambient thermal resistance. The junction to ambient thermal resistance ( $\Theta_{JA}$  is layout dependent) for PSOP-8 package (Exposed Pad) is 75°C/W on standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by following formula:

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / 75^\circ\text{C/W} = 1.33\text{W}$$

The thermal resistance  $\Theta_{JA}$  of PSOP-8 (Exposed Pad) is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding copper under the expose pad of PSOP-8 package. We have to consider the copper couldn't stretch infinitely and avoid the tin overflow.



### Application Diagram



$R_1 = R_2 = 100\text{k}\Omega$ ,  $R_{TT} = 50\Omega/33\Omega/25\Omega$

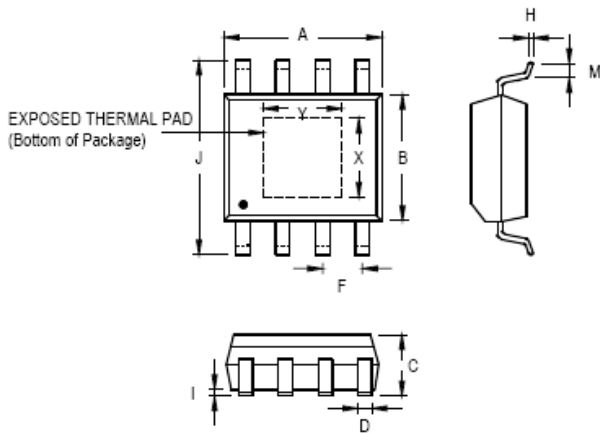
$C_{OUT, \min} = 10\mu\text{F}$  (Ceramic) +  $1000\mu\text{F}$  under the worst case testing condition

$R_{DUMMY} = 1\text{k}\Omega$  as for VOUT discharge when VIN is not present but VCNTL is present

$C_{SS} = 1\mu\text{F}$ ,  $C_{IN} = 470\mu\text{F}$  (Low ESR),  $C_{CNTL} = 47\mu\text{F}$



**Outline Drawing PSOP-8**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.191	0.254	0.008	0.010
I	0.000	0.152	0.000	0.006
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
X	2.057	2.515	0.081	0.099
Y	2.057	3.404	0.081	0.134

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