DATA SHEET

TZA3019
2.5 Gbits/s dual postamplifier with level detectors and 2 × 2 switch

Preliminary specification
File under Integrated Circuits, IC19

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Philips Semiconductors

PHILIPS

2.5 Gbits/s dual postamplifier with level detectors and 2 × 2 switch

TZA3019

FEATURES

- Dual postamplifier
- Single 3.3 V power supply
- Wideband operation from 50 kHz to 2.5 GHz (typical value)
- Fully differential
- Channels are delay matched
- On-chip DC-offset compensations without external capacitor
- Interfacing with positive or negative supplied logic
- Switching possibility between channels
- Positive Emitter Coupled Logic (PECL) or Current-Mode Logic (CML) compatible data outputs adjustable from 200 to 800 mV (p-p) single-ended
- Power-down capability for unused outputs and detectors
- Rise and fall times 80 ps (typical value)
- Possibility to invert the output of each channel separately
- Input level-detection circuits for Received Signal Strength Indicator (RSSI) or Loss Of Signal (LOS) detection, programmable from 0.4 to 400 mV (p-p) single-ended, with open-drain comparator output for direct interfacing with positive or negative logic
- Reference voltage for output level and LOS adjustment
- Automatic strongest input signal switch possibility (TZA3019 version B)
- HTQFP32 or HBCC32 plastic package with exposed pad.

APPLICATIONS

- Postamplifier for Synchronous Digital Hierarchy and Synchronous Optical Network (SDH/SONET) transponder
- SDH/SONET wavelength converter
- Crosspoint or channel switch
- PECL driver
- Fibre channel arbitrated loop
- Protection ring
- Monitoring
- Signal level detectors
- Swing converter CML 200 mV (p-p) to PECL 800 mV (p-p)
- Port bypass circuit
- 2.5 GHz clock amplification.

GENERAL DESCRIPTION

The TZA3019 is a low gain postamplifier multiplexer with a dual RSSI and/or LOS detector that is designed for use in critical signal path control applications, such as loop-through, redundant channel switching or Wavelength Division Multiplexing (WDM). The signal path is unregistered, so no clock is required for the data inputs. The signal path is fully differential and delay matched. It is capable of operating from 50 kHz to 2.5 GHz.

The TZA3019 HTQFP32 and HBCC32 packages can be delivered in three versions:

- TZA3019AHT and TZA3019AV with two RSSI signals
- TZA3019BHT and TZA3019BV with one RSSI and one LOS signal
- TZA3019CHT and TZA3019CV with two LOS signals.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3019AHT	HTQFP32	plastic, heatsink thin quad flat package; 32 leads; body 5 × 5 × 1 mm	SOT547-2
TZA3019BHT	HTQFP32	plastic, heatsink thin quad flat package; 32 leads; body 5 × 5 × 1 mm	SOT547-2
TZA3019CHT	HTQFP32	plastic, heatsink thin quad flat package; 32 leads; body 5 × 5 × 1 mm	SOT547-2
TZA3019AV	HBCC32	plastic, heatsink bottom chip carrier; 32 terminals; body 5 × 5 × 0.65 mm	SOT560-1
TZA3019BV	HBCC32	plastic, heatsink bottom chip carrier; 32 terminals; body 5 × 5 × 0.65 mm	SOT560-1
TZA3019CV	HBCC32	plastic, heatsink bottom chip carrier; 32 terminals; body 5 × 5 × 0.65 mm	SOT560-1
TZA3019U	–	bare die; 2.22 × 2.22 × 0.28 mm	–

BLOCK DIAGRAM

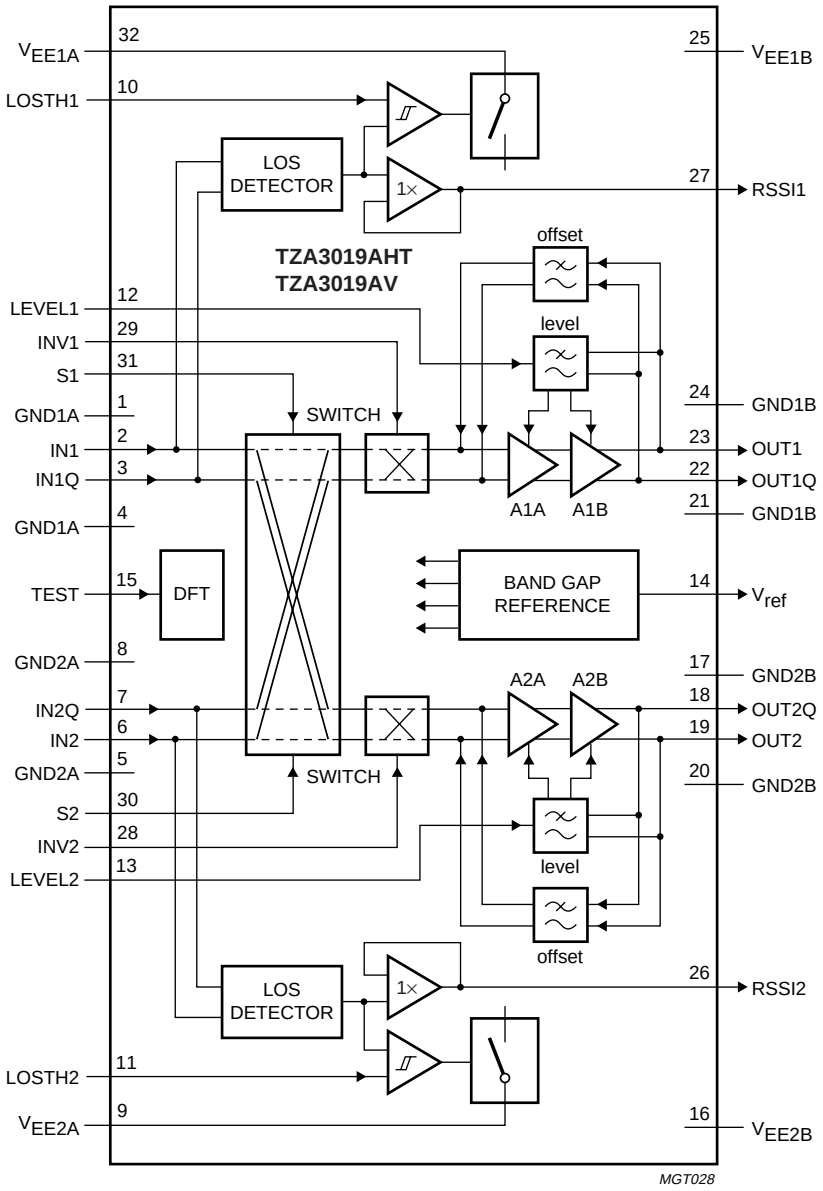


Fig.1 Block diagram (TZA3019AHT and TZA3019AV).

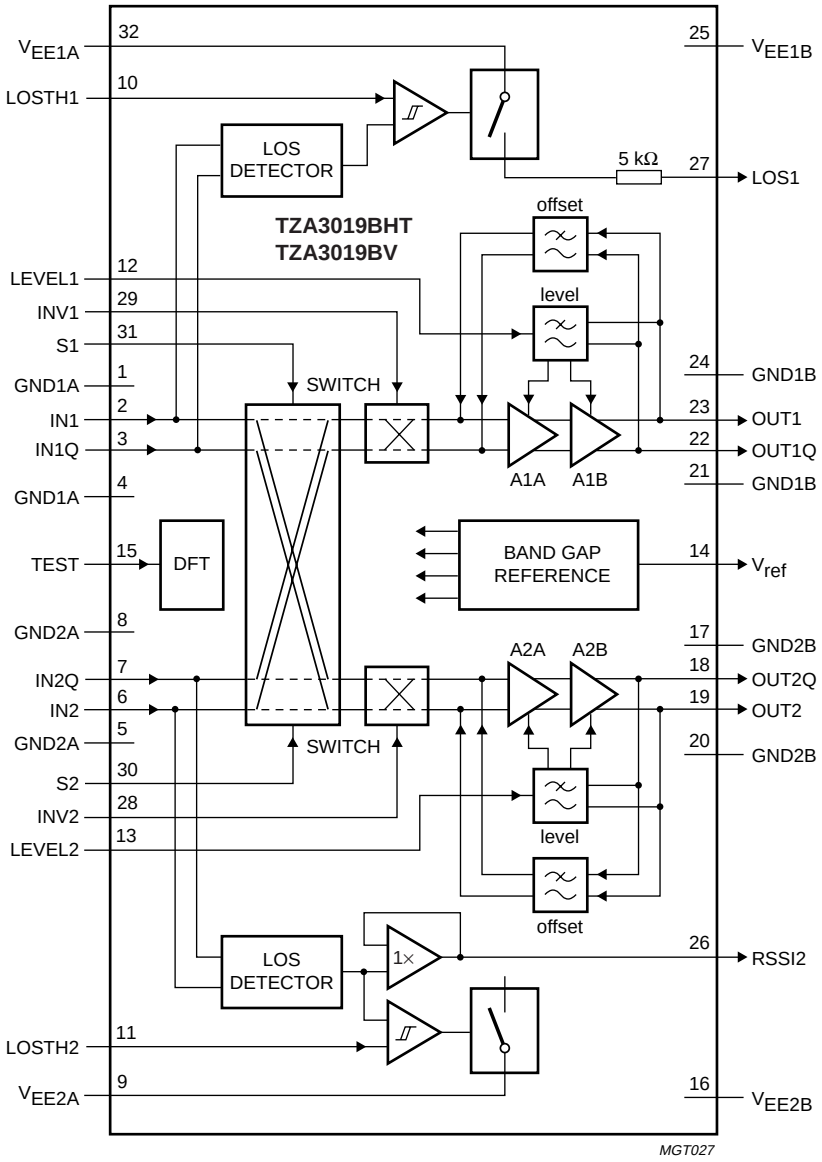


Fig.2 Block diagram (TZA3019BHT and TZA3019AV).

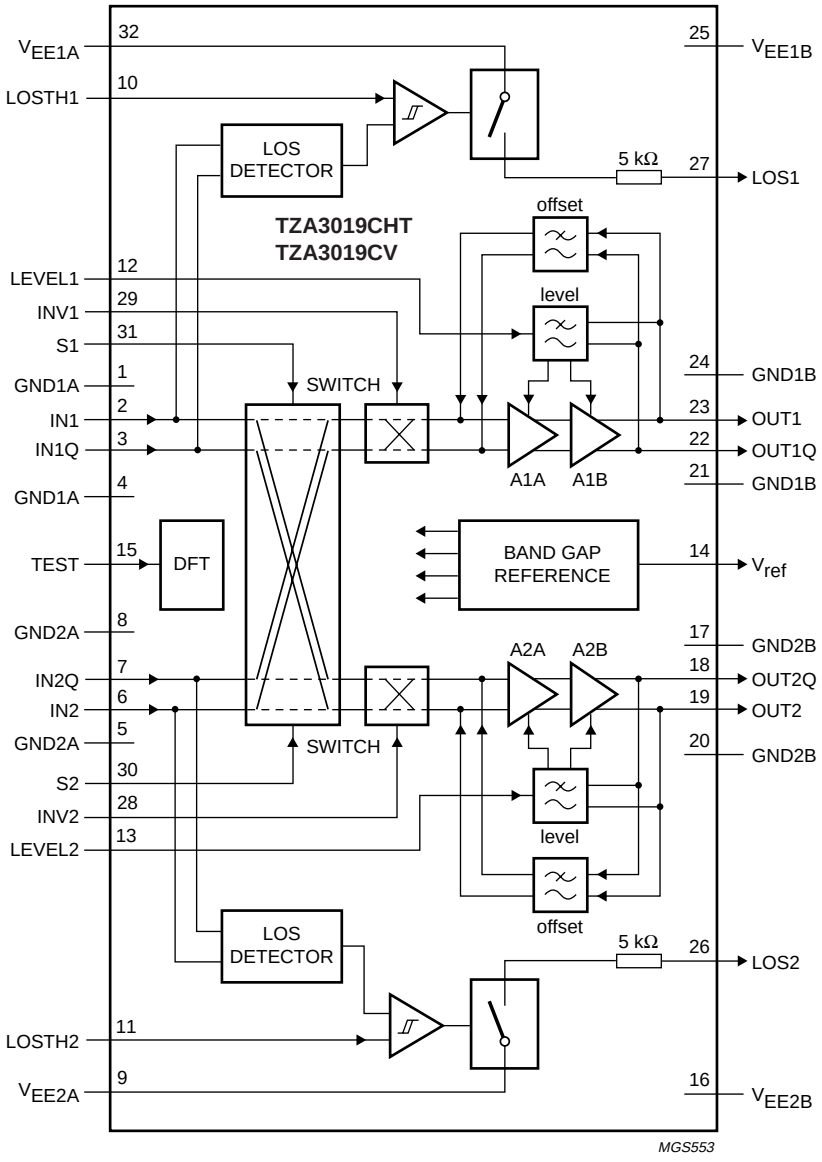


Fig.3 Block diagram (TZA3019CHT and TZA3019CV).

PINNING

SYMBOL	PIN			PAD	TYPE(2)	DESCRIPTION
	TZA3019xHT/xV(1)					
	A	B	C			
GND1A	1	1	1	1	S	ground for input 1 and LOS1 circuits
IN1	2	2	2	2	I	differential circuit 1 input; complimentary to pin IN1Q; DC bias level is set internally at approximately –0.33 V
IN1Q	3	3	3	3	I	differential circuit 1 input; complimentary to pin IN1; DC bias level is set internally at approximately –0.33 V
GND1A	4	4	4	4	S	ground for input 1 and LOS1 circuits
n.c	–	–	–	5	–	not connected
n.c	–	–	–	6	–	not connected
GND2A	5	5	5	7	S	ground for input 2 and LOS2 circuits
IN2	6	6	6	8	I	differential circuit 2 input; complimentary to pin IN2Q; DC bias level is set internally at approximately –0.33 V
IN2Q	7	7	7	9	I	differential circuit 2 input; complimentary to pin IN2; DC bias level is set internally at approximately –0.33 V
GND2A	8	8	8	10	S	ground for input 2 and LOS2 circuits
V_{EE2A}	9	9	9	11	S	negative supply voltage for input 2 and LOS2 circuits
LOSTH1	10	10	10	12	I	Input for level detector programming of input 1 circuit; threshold level is set by connecting external resistors between pins GND1A and V_{ref}. When forced to V_{EE2A} or not connected, the LOS1 circuit will be switched off.
LOSTH2	11	11	11	13	I	Input for level detector programming of input 2 circuit; threshold level is set by connecting external resistors between pins GND2A and V_{ref}. When forced to V_{EE2A} or not connected, the LOS2 circuit will be switched off.
n.c	–	–	–	14	–	not connected
LEVEL1	12	12	12	15	I	Input for programming output level of output 1 circuit; output level is set by connecting external resistors between pins GND1A and V_{ref}. When forced to GND1A or not connected, pins OUT1 and OUT1Q will be switched off.
LEVEL2	13	13	13	16	I	Input for programming output level of output 2 circuit; output level is set by connecting external resistors between pins GND2A and V_{ref}. When forced to GND2A or not connected, pins OUT2 and OUT2Q will be switched off.
V_{ref}	14	14	14	17	O	reference voltage for level circuit and LOS threshold programming; typical value is –1.6 V; no external capacitor allowed
n.c	–	–	–	18	–	
TEST	15	15	15	19	I	for test purposes only; to be left open-circuit in the application
V_{EE2B}	16	16	16	20	S	negative supply voltage for output 2 circuit
GND2B	17	17	17	21	S	ground for output 2 circuit
OUT2Q	18	18	18	22	O	PECL or CML compatible differential circuit 2 output; complimentary to pin OUT2

SYMBOL	PIN			PAD	TYPE(2)	DESCRIPTION
	TZA3019xHT/xV(1)					
	A	B	C			
OUT2	19	19	19	23	O	PECL or CML compatible differential circuit 2 output; complimentary to pin OUT2Q
GND2B	20	20	20	24	S	ground for output 2 circuit
n.c	–	–	–	25	–	not connected
n.c	–	–	–	26	–	not connected
GND1B	21	21	21	27	S	ground for output 1 circuit
OUT1Q	22	22	22	28	O	PECL or CML compatible differential circuit 1 output; complimentary to pin OUT1
OUT1	23	23	23	29	O	PECL or CML compatible differential circuit 1 output; complimentary to pin OUT1Q
GND1B	24	24	24	30	S	ground for output 1 circuit
V_{EE1B}	25	25	25	31	S	negative supply voltage for output 1 circuit
RSSI2	26	26	–	32	O	output of received signal strength indicator of detector
LOS2	–	–	26	33	O-DRN	output loss of signal detector 2; detection of input 2 signal; direct drive of positive or negative supplied logic via internal 5 kΩ resistor
RSSI1	27	–	–	34	O	output of received signal strength indicator of detector
LOS1	–	27	27	35	O-DRN	output loss of signal detector 2; detection of input 2 signal; direct drive of positive or negative supplied logic via internal 5 kΩ resistor
INV2	28	28	28	36	TTL	input to invert the signal of pins OUT2 and OUT2Q; directly positive (inverted) or negative supplied logic driven
INV1	29	29	29	37	TTL	input to invert the signal of pins OUT1 and OUT1Q; directly of positive (inverted) or negative supplied logic driven
S2	30	30	30	38	TTL	input selector output 2 circuit; directly positive (inverted) or negative supplied logic driven
S1	31	31	31	39	TTL	input selector output 1 circuit; directly positive (inverted) or negative supplied logic driven
V_{EE1A}	32	32	32	40	S	negative supply voltage for input 1 and LOS1 circuits
V_{EEP}	pad	pad	pad	–	S	negative supply voltage pad (exposed die pad)

Notes

1. The ‘x’ in TZA3019xHT/xV represents versions A, B and C.
2. Pin type abbreviations: O = output, I = input, S = power supply, TTL = logic input and O-DRN = open-drain output.

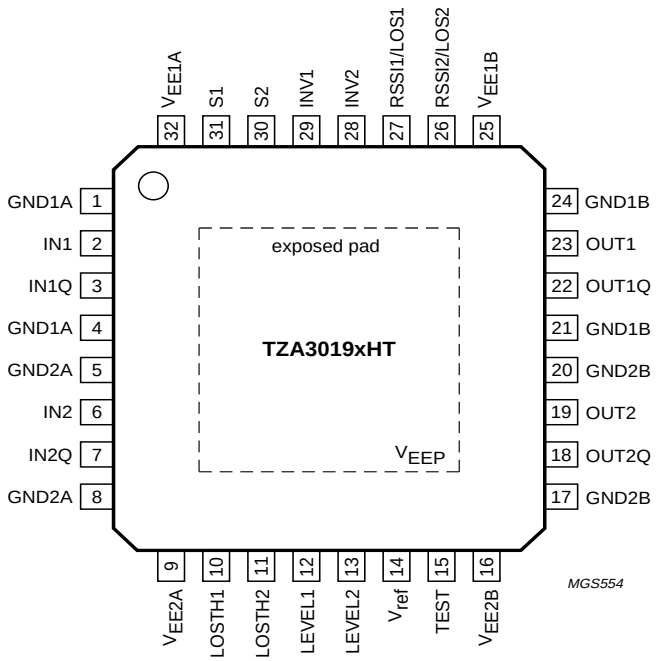


Fig.4 Pin configuration HTQFP32.

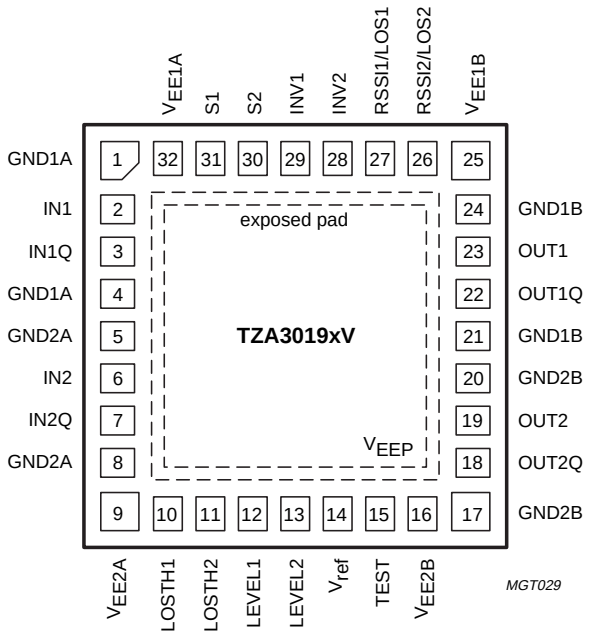


Fig.5 Pin configuration HBCC32.

FUNCTIONAL DESCRIPTION

The TZA3019 is a dual postamplifier with multiplexer and loss of signal detection see Figs 1, 2 and 3. The RF path starts with the multiplexer, which connects an amplifier to one of the two inputs. It is possible to invert the output for easy layout of the Printed-Circuit Board (PCB). The signal is amplified to a certain level. To guarantee this level with minimum distortion over the temperature range and level range, an active control part is added. The offset compensation circuit following the inverter minimizes the offset.

The Received Signal Strength Indicator (RSSI) or the Loss Of Signal (LOS) detection uses a 7-stage 'successive detection' circuit. It provides a logarithmic output. The LOS is followed by a comparator with a programmable threshold. The input signal level-detection is implemented to check if the input signal voltage is above the user programmed level. This can insure that data will only be transmitted when the input signal-to-noise ratio is sufficient for low bit error rate system operation. A second offset compensation circuit minimizes the offset of the logarithmic amplifier.

RF input circuit

The input circuit contains internal 50 Ω resistors decoupled to ground via an internal common mode 12 pF capacitor (see Fig.6).

The input pins are DC-biased at approximately −0.33 V by an internal reference generator. The TZA3019 can be DC-coupled, but AC-coupling is preferred. In case of DC-coupling, the driving source must operate within the allowable input range (−1.0 to +0.3 V). A DC-offset voltage of more than a few millivolts should be avoided, since the internal DC-offset compensation circuit has a limited correction range. When AC-coupling is used, if no DC-compatibility is required, the values of the coupling capacitors must be large enough to pass the lowest input frequency of interest. Capacitor tolerance and resistor variation must be included for an accurate calculation. Do not use signal frequencies around the low cut-off circuit frequencies ($f_{-3dB(l)}$ = 50 kHz for the postamplifiers and $f_{-3dB(l)}$ = 1 MHz for the LOS circuits).

RF output circuit

Matching the main amplifier outputs (see Fig.7) is not mandatory. In most applications, the transmission line receiving end will be properly matched, while very little reflections occur.

Matching the transmitting end to absorb reflections is only recommended for very sensitive applications.

In such cases, pull-up resistors of 100 Ω should be connected as close as possible to the IC from pins OUT1 and OUT1Q, and pins OUT2 and OUT2Q to V_{EE1B} and V_{EE2B} respectively. These matching resistors are not needed in most applications.

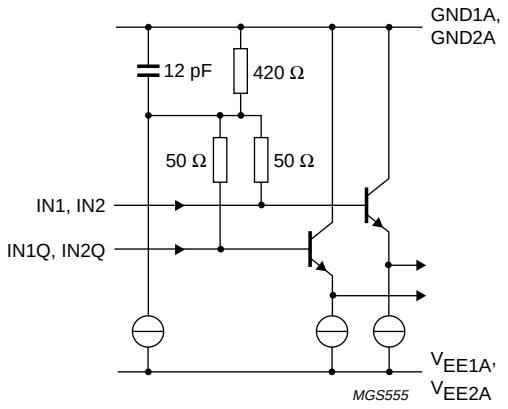


Fig.6 RF input circuit.

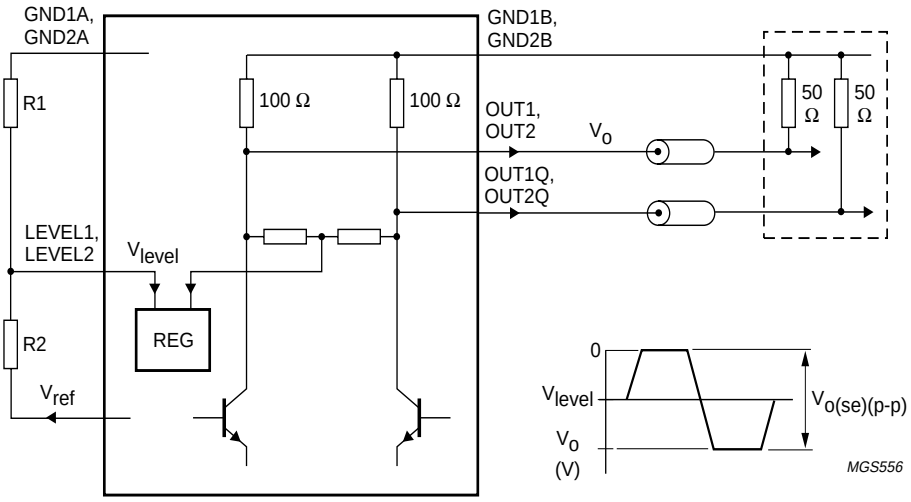
Postamplifier level adjustment

The postamplifier boosts the signal up to PECL levels. The output can be either CML- or PECL-level compatible, adjusted by means of the voltage on pins LEVEL1 and LEVEL2. The DC voltages of pins OUT1 and OUT1Q, and pins OUT2 and OUT2Q match with the DC-levels on pins LEVEL1 and LEVEL2, respectively. Due to the receiving end 50 Ω load resistance, it means that at the same level of $V_{o(p-p)}$, V_{LEVEL1} and V_{LEVEL2} with AC-coupling are not equal to V_{LEVEL1} and V_{LEVEL2} with DC-coupling (see Figs 7 and 8).

The postamplifier is in power-down state when pin LEVEL1 or LEVEL2 is connected to ground or not connected (see Fig.8).

Postamplifier DC offset cancellation loop

Offset control loops connected between the inputs of the buffers A1A and A2A and the outputs of the amplifiers A1B and A2B (see Figs 1, 2 and 3) will keep the input of both buffers at their toggle point during the absence of an input signal. The active offset compensation circuit is integrated, so no external capacitor is required. The loop time constant determines the lower cut-off frequency of the amplifier chain. The cut-off frequency of the offset compensations is fixed internally at approximately 5 kHz.

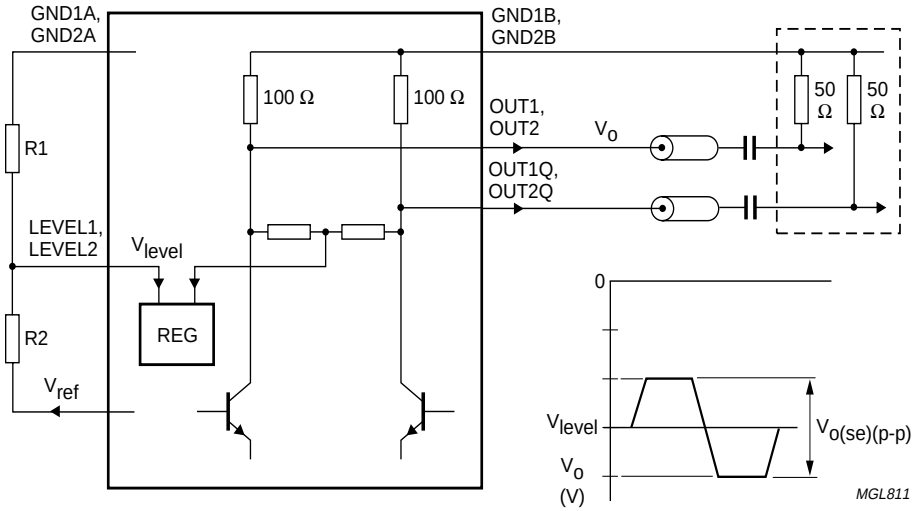


$V_{level} = 0.5 \times V_{o(se)(p-p)}$.

$V_{level} = V_{ref} \times \frac{R1}{R1 + R2}$.

Level detector in power-down mode: V_{LEVEL1} or $V_{LEVEL2} = V_{GND}$.

a. DC-coupling.



$V_{level} = 1.5 \times V_{o(se)(p-p)}$.

$V_{level} = V_{ref} \times \frac{R1}{R1 + R2}$.

Level detector in power-down mode: V_{LEVEL1} or $V_{LEVEL2} = V_{GND}$.

b. AC-coupling.

Fig.7 RF output configurations.

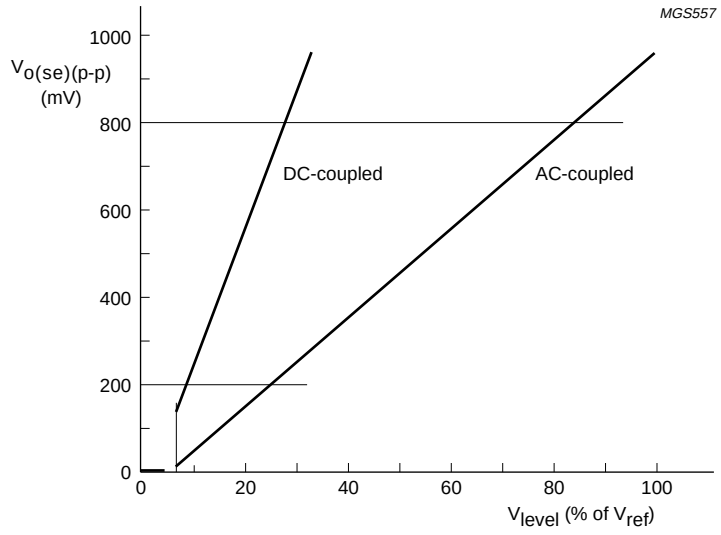


Fig.8 Output signal as a function of V_{level}.

TTL logic input of selector and inverter

The logic levels are differently defined for positive or negative logic (see Fig.9). It should be noted that positive logic levels are inverted if a negative supply voltage is used.

Outputs as a function of switch input pins S1, S2, INV1 and INV2

See Tables 1, 2, 3 and 4.

The default values for the switch input pins S1, S2, INV1 and INV2 if not connected, is zero.

Table 1 OUT1 and OUT1Q as function of input S1

S1	OUT1	OUT1Q
0	IN1	IN1Q
1	IN2	IN2Q

Table 2 OUT2 and OUT2Q as function of input S2

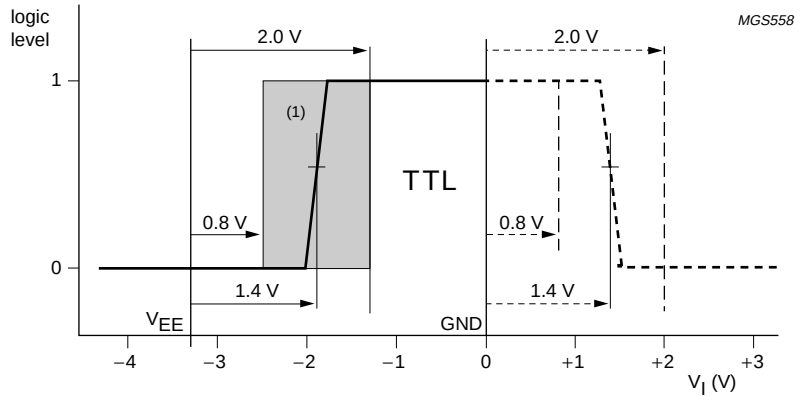
S2	OUT2	OUT2Q
0	IN2	IN2Q
1	IN1	IN1Q

Table 3 OUT1 and OUT1Q as function of INV1

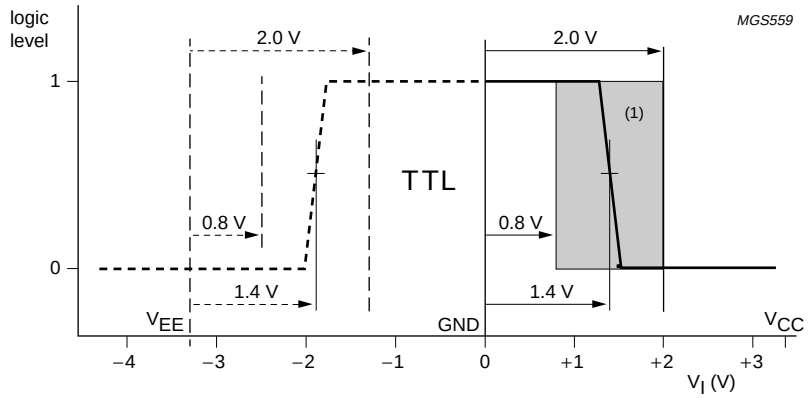
INV1	OUT1	OUT1Q
0	IN1 or IN2	IN1Q or IN2Q
1	IN1Q or IN2Q	IN1 or IN2

Table 4 OUT2 and OUT2Q as function of INV2

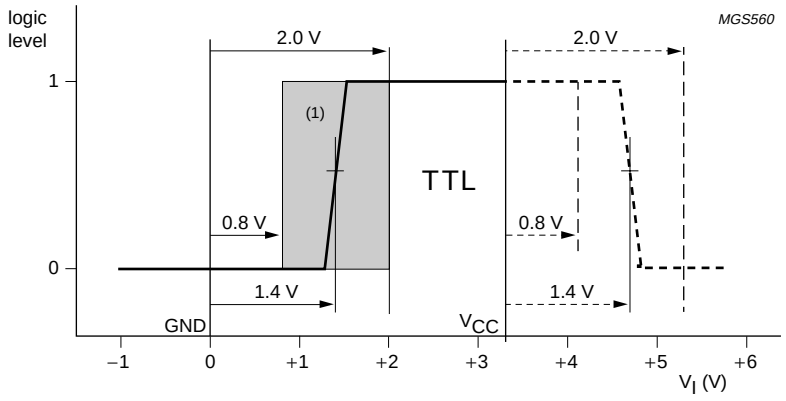
INV2	OUT2	OUT2Q
0	IN1 or IN2	IN1Q or IN2Q
1	IN1Q or IN2Q	IN1 or IN2



a. Negative circuit supply voltage V_{EE} and negative logic supply voltage V_{EE}.



b. Negative circuit supply voltage V_{EE} and positive logic supply voltage V_{CC}.



c. Positive circuit supply voltage V_{CC} and positive logic supply voltage V_{CC}.

(1) Level not defined.

Fig.9 Logic levels on pins S1, S2, INV1 and INV2 as a function of the input voltages.

RSSI and LOS detection

The TZA3019 allows AC-signal level detection. This can prevent the outputs from reacting to noise during the absence of a valid input signal, and can insure that data only will be transmitted when the signal-to-noise ratio of the input signal is sufficient to insure low bit error rate system operation.

The RSSI detection circuit uses seven limiting amplifiers in a 'successive detection' topology to closely approximate logarithmic response over a total range of 70 dB. The detectors provide full-wave rectification of the AC signals presented at each previous amplifier stage. Their outputs are current drivers. Each cell incorporates a low-pass filter, being the first step in recovering the average value of the demodulated signal of the input frequency. The summed detector output currents are converted to a voltage by an internal load resistor. This voltage is buffered and available in the A and B versions of the TZA3019. When V_{RSSI} is used V_{LOSTH} must be connected to GND to prevent the LOS comparator from switching to the standby mode. The LOS comparator detects an input signal above a fixed threshold, resulting in a LOW-level at the LOS circuit output.The threshold level is determined by the voltage on pins LOSTH1 or LOSTH2 (see Fig.10). A filter with a time constant of 1 μs nominal is included to prevent noise spikes from triggering the level detector.

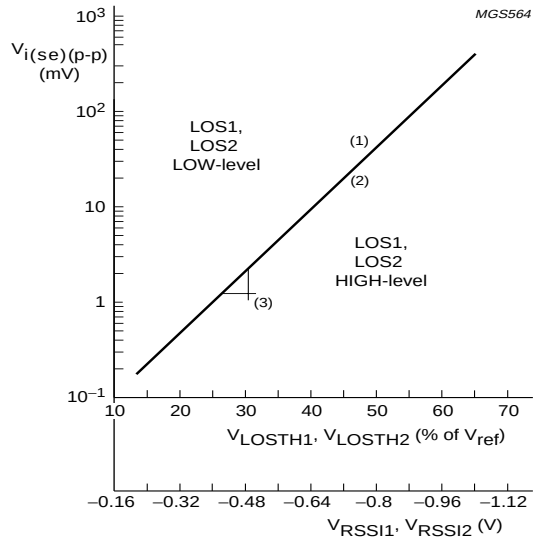
The comparator (with internal 3 dB hysteresis) drives an open-drain circuit with an internal resistor (5 kΩ) for direct interfacing to positive or negative logic (see Fig.11). Only available in the B and C versions of the TZA3019.

The response is independent of the sign of the input signal because of the particular way the circuit has been built. This is part of the demodulating nature of the detector, which results in an alternating input voltage being transformed to a rectified and filtered quasi DC-output signal. For the TZA3019 the logarithmic voltage slope is φ = 1/13 dB/mV and is essentially temperature and supply independent through four feedback loops in the reference circuit. The internal LOS detector output voltage is based on V_{ref}. The demodulator characteristic depends on the waveform and the response depends roughly on the input signal RMS value. This influences high frequencies, a square wave input of 2.4 GHz (LOS circuit bandwidth of 2.4 GHz) offsets the intercept voltage by 20%. V_{LOSTH} can be calculated using the following formulae:

$$V_{LOSTH} = V_{RSSI} = S \times 20\log^{(Vi/18\mu V)} \quad (1)$$

where S = sensitivity.

Example: a 200 mV (p-p) single-ended 1.2 GB/s PRBS signal has an RSSI from 1003 mV.

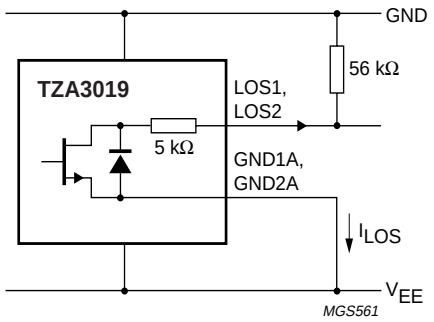


(1) PRBS pattern input signal with a frequency <1 GHz.
(2) Linearity error typically 0.5 dB.
(3) φ = 1/12.5 dB/mV.

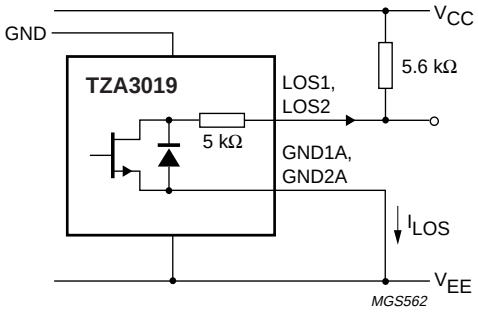
Fig.10 Loss of signal assert level.

A full understanding of the offset control loop is useful. The primary purpose of the loop is to extend the lower end of the dynamic range in any case where the offset voltage of the first stage might be high enough to cause later stages to prematurely enter limiting, caused by the high DC-gain of the amplifier system. The offset is automatically and continuously compensated via a feedback path from the last stage. An offset at the output of the logarithmic converter is equivalent to a change of amplitude at the input. Consequently, with DC-coupling, signal absence, either LOW-level or HIGH-level is detected as a full signal, only signals with an average value equal to zero give zero output.

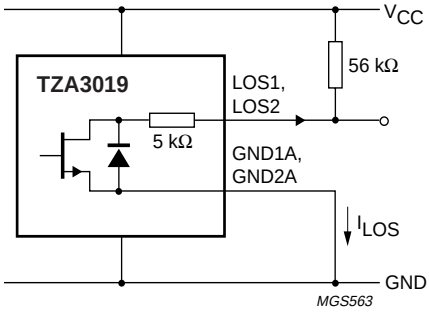
Version B can be used for an auto function, which switches the strongest input signal to output 1 and the weakest to output 2. To achieve this output V_{RSSI2} must be used as the reference voltage for input V_{LOSTH}. Then the output LOS1 can switch S1 and S2.



a. Negative supply and negative logic.



b. Negative supply and positive logic.



$V_{CC} - V_{EE} < 7$ V.

c. Positive supply and positive logic.

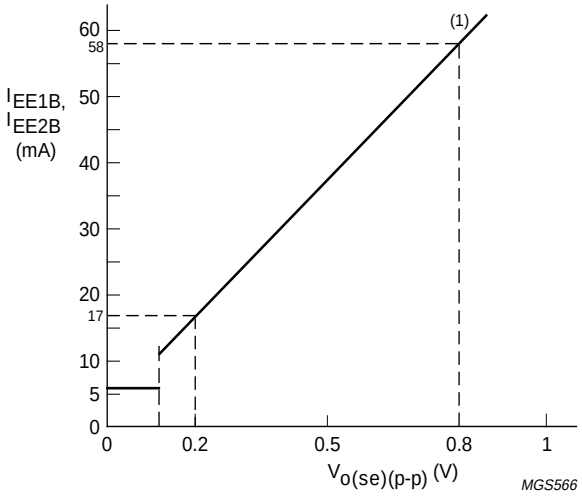
Fig.11 Loss of signal outputs, pins LOS1 and LOS2.

Supply current

For the supply currents I_{EE1B} and I_{EE2B}, see Fig.12.

Using a positive supply voltage

Although the TZA3019 has been designed to use a single −3.3 V supply voltage (see Fig.13), a +3.3 V supply (see Fig.14) can also be used. However, care should be taken with respect to RF transmission lines. The on-chip signals refer to the various ground pins as being positive supply pins in a +3.3 V application. The external transmission lines will most likely be referred to the pins V_{EE1A}, V_{EE2A}, V_{EE1B} and V_{EE2B}, being the system ground. The RF signals will change from one reference plane to another when interfacing the RF inputs and outputs. A positive supply application is very vulnerable to interference with respect to this point. For a successful +3.3 V application, special care should be taken when designing the PCB layout in order to reduce the influence of interference and to keep the positive supply voltage as clean as possible.



(1) I_{EE1B} and I_{EE2B} at 25 °C.

Fig.12 Supply current as a function of output voltage

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{EE}	negative supply voltage	–5.5	+0.5	V
V_n	DC voltage			
	pins IN1, IN1Q, IN2, IN2Q, LOSTH1, LOSTH2, LEVEL1, LEVEL2, V_{ref}, TEST, OUT2Q, OUT2, OUT1Q, OUT1, V_{EEP}, GND1A, GND2A, GND1B and GND2B	V_{EE} – 0.5	0.5	V
	pins LOS1, LOS2, INV1, INV2, S1 and S2	V_{EE} – 0.5	V_{EE} + 7	V
I_n	DC current			
	pins IN1, IN1Q, IN2 and IN2Q	–20	+20	mA
	pins LOSTH1, LOSTH2, LEVEL1 and LEVEL2	0	14	µA
	pins $V_{ref,}$ TEST, LOS1 and LOS2	–1	+1	mA
	pins OUT1, OUT1Q, OUT2 and OUT2Q	–30	+30	mA
	pins INV1, INV2, S1 and S2	0	20	µA
P_{tot}	total power dissipation	–	1.2	W
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	150	°C
T_{amb}	ambient temperature	–40	+85	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-s)}$	thermal resistance from junction to solder point (exposed die pad); note 1		15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient; note 1	1s2p multi-layer test board	33	K/W
$R_{th(s-a)}$	thermal resistance from solder point to ambient (exposed die pad); note 1	1s2p multi-layer test board	18	K/W
$R_{th(s-a)(req)}$	required thermal resistance from solder point to ambient	LOS circuits switched on		
		V_o = 200 mV (p-p) single-ended; both output circuits	60	K/W
		V_o = 800 mV (p-p) single-ended; both output circuits	30	K/W

Note

1. JEDEC standard.

CHARACTERISTICS

Typical values at T_{amb} = 25 °C and V_{EE} = –3.3 V; minimum and maximum values are valid over the entire ambient temperature range and supply voltage range; all voltages referenced to ground; unless otherwise specified; note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
SUPPLY PINS V_{EE1A}, V_{EE1B}, V_{EE2A} AND V_{EE2B}						
V_{EE}	negative supply voltage		–3.13	–3.3	–3.47	V
I_{EE1A}, I_{EE2A}	negative supply current	LOS circuit power-down	14	24	34	mA
		LOS circuit switched on	24	40	56	mA
I_{EE1B}, I_{EE2B}	negative supply current	amplifier power-down	2	6	10	mA
		V_o = 200 mV (p-p) single-ended; one output circuit	11	17	24	mA
		V_o = 800 mV (p-p) single-ended; one output circuit	47	60	77	mA
P_{tot}	total power dissipation	power-down	100	200	300	mW
		both LOS circuits switched on				
		V_o = 200 mV (p-p) single-ended; both output circuits	220	380	555	mW
		V_o = 800 mV (p-p) single-ended; both output circuits	450	660	925	mW
TC	temperature coefficient	LOS circuit switched on; I_{EE1A}; I_{EE2A}	30	50	80	µA/°C
		V_o = 800 mV (p-p) single-ended; I_{EE1A}; I_{EE2A}	15	30	50	µA/°C
T_j	junction temperature		–40	–	+125	°C
T_{amb}	ambient temperature		–40	+25	+85	°C
Inputs multiplexer and loss of signal detector						
PECL OR CML INPUT PINS IN1, IN1Q, IN2 AND IN2Q						
$V_{i(p-p)}$	input voltage swing (peak-to-peak value)	single-ended; note 2	50	–	500	mV
$V_{i(bias)}$	DC input bias voltage		–0.28	–0.33	–0.4	V
V_I	DC and AC input window voltage	note 3	–1.0	–	+0.3	V
R_i	input resistance	single-ended	35	50	70	Ω
C_i	input capacitance	single-ended; note 3	0.6	0.8	1.2	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Postamplifier						
AMPLIFIERS A1A, A1B, A2A AND A2B						
G_v	small signal voltage gain	V_o = 200 mV (p-p) single-ended; note 4	10	15	19	dB
		V_o = 800 mV (p-p) single-ended; note 4	22	29	34	dB
f_D	signal path data rate	notes 5 and 9	–	2500	–	Mbits/s
$f_{-3dB(l)}$	low –3 dB cut-off frequency DC compensation	note 3	2	5	10	kHz
$f_{-3dB(h)}$	high –3 dB cut-off frequency		–	2.0	–	GHz
t_{PD}	propagation delay	note 3	150	200	250	ps
Δt_{PD}	propagation delay difference	at the same signal levels; note 3	–	0	5	ps
J	total jitter	20 bits of the 28.5kbits pattern; notes 3 and 6	–	8	–	ps
α_{ct}	crosstalk	crosstalk of IC only	90	110	–	dB
PECL OR CML OUTPUT PINS OUT1, OUT1Q, OUT2 AND OUT2Q						
$V_{o(se)(p-p)}$	single-ended output voltage (peak-to-peak value)	50 Ω load	200	–	800	mV
TC	temperature coefficient output level		–1	0	–1	mV/K
t_r	rise time	20% to 80%; note 5	–	80	–	ps
t_f	fall time	80% to 20%; note 5	–	80	–	ps
R_o	output resistance	single-ended	70	100	130	Ω
C_o	output capacitance	single-ended; note 3	0.6	0.8	1.2	pF
LEVEL CONTROL INPUT PINS LEVEL1 AND LEVEL2						
V_i	input voltage		V_{ref}	–	0	V
R_i	input resistance	measured to GND1A or GND2A	150	350	600	kΩ
Multiplexer and inverter switch						
PECL OR CML INPUT PINS IN1, IN1Q, IN2 AND IN2Q						
$\alpha_{OS(red)}$	input offset reduction	V_o = 200 mV (p-p) single-ended; note 7	4	9	13	dB
		V_o = 800 mV (p-p) single-ended; note 7	10	14	20	dB
$V_{io(cor)}$	input offset voltage correction range	peak-to-peak value single-ended	–10	–	+10	mV
$V_{n(i)(eq)(rms)}$	equivalent input noise voltage (RMS value)	V_o = 800 mV (p-p) single-ended; note 3	–	75	170	µV
Fn	noise factor	note 3	–	5	12	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SWITCH CIRCUIT						
t_a	assert time	multiplexer and inverter	70	100	200	ns
t_d	de-assert time	multiplexer and inverter	55	80	160	ns
TTL INPUT PINS S1, S2, INV1 AND INV2						
V_{IL}	LOW-level input voltage	positive logic	2.0	–	V_{EE} + 7.3	V
		negative logic	V_{EE} – 0.3	–	–2.5	V
V_{IH}	HIGH-level input voltage	negative logic	–1.3	–	+0.3	V
		positive logic	–0.3	–	+0.8	V
R_i	input resistance	measured to V_{EE1A} or V_{EE2A}	100	180	400	kΩ
I_i	input current		–10	–	+10	μA
Received Signal Strength Indicator and Loss Of Signal detector						
RSSI AND LOS CIRCUIT						
$V_{i(se)(p-p)}$	single-ended input voltage swing (peak-to-peak value)		0.4	–	400	mV
DR	dynamic range		57	60	63	dB
S_{LOS}	LOS sensitivity	50 MHz, square; note 8	11	12.5	14	mV/dB
		620 MHz, square; note 8	10.7	11.9	13	mV/dB
		1.2 GHz, square; note 8	10	11.1	12.2	mV/dB
		100 MB/s PRBS ($2^{31} – 1$); note 8	11.2	12.7	14.2	mV/dB
		1.2 GB/s PRBS ($2^{31} – 1$); note 8	10.9	12.4	13.9	mV/dB
		100 GB/s PRBS ($2^{31} – 1$); note 8	10.7	11.9	13	mV/dB
TC_{sens}	temperature coefficient sensitivity		–2	0	–2	μV/dbK
LE	linearity error	see Fig.10	–	0.5	1	dB
$\alpha_{OS(red)}$	input offset reduction	notes 3 and 7	25	35	45	dB
$V_{io(cor)}$	input offset voltage correction range	peak-to-peak value single-ended	–5	–	+5	mV
$f_{-3dB(l)}$	low –3 dB cut-off frequency		0.5	1	2	MHz
$f_{-3dB(h)}$	high –3 dB cut-off frequency	note 8	1.5	2	2.5	GHz
LOS CIRCUIT						
hys_{LOS}	LOS hysteresis	input signal waveform dependency	2.0	3.0	4.0	dB
t_a	assert time	note 3	–	–	5	μS
t_d	de-assert time	note 3	–	–	5	μS
INPUT PINS LOSTH1 AND LOSTH2						
V_i	input voltage		V_{EE}	–	0	V
R_i	input resistance	measured to V_{EE1A} or V_{EE2A}	150	350	600	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OUTPUT PINS LOS1 AND LOS2						
V_o	output voltage		V_{EE}	–	3.5	V
$I_{o(sink)}$	output sink current		–	–	1	mA
R_o	output resistance	internal output series resistance	3.5	5	6.5	kΩ
OUTPUT PINS RSSI1 AND RSSI2						
V_o	output voltage		–1	–	0	V
I_o	output current		–1	–	+1	mA
Band gap reference circuit						
OUTPUT PIN V_{REF}						
V_{ref}	reference voltage		–1.45	–1.6	–1.8	V
C_{ext}	allowed external capacitance		–	–	10	pF
$I_{o(sink)}$	output sink current		–	–	500	µA

Notes

1. It is assumed that both CML inputs carry a complementary signal with the specified peak-to-peak value (true differential excitation).
2. Minimum signal with limiting output.
3. Guaranteed by design.
4. $G_V = \frac{V_o}{V_i}$
5. Based on –3dB cut-off frequency.
6. V_i = 100 mV (p-p) single-ended and V_o = 200 mV (p-p) single-ended.
7. Input offset reduction = $\frac{G_{AC}}{G_{DC}}$
8. Sensitivity depends on the waveform and is therefore a function of –3 dB cut-off frequency see equation (1).
9. Low limit can go as low as DC if input signal overrides input offset voltage correction range.

APPLICATION INFORMATION

RF input and output connections

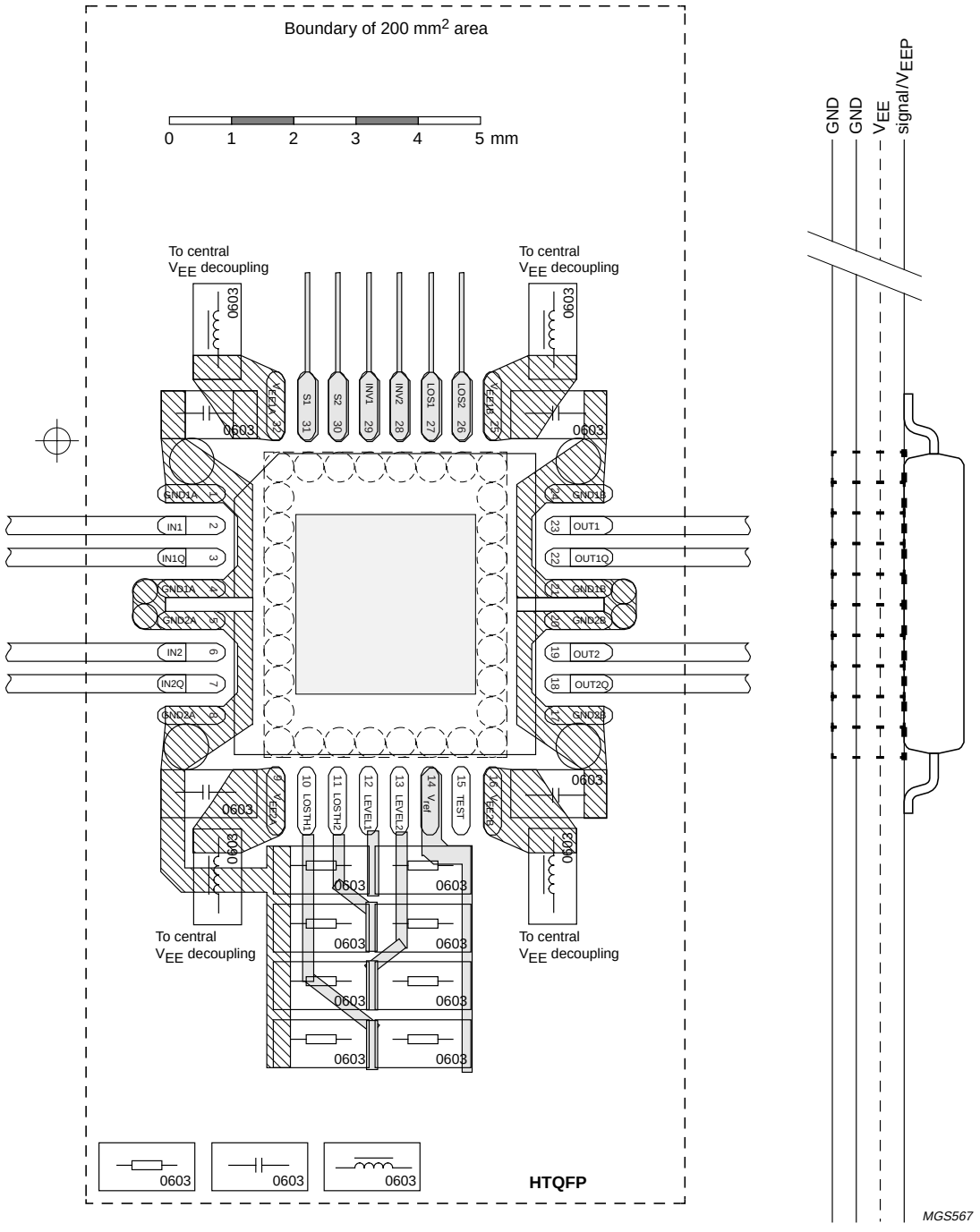
Striplines, or microstrips, with an odd mode characteristic impedance of Z_o = 50 Ω must be used for the differential RF connections on the PCB. This applies to both the signal inputs and the signal outputs. The two lines in each pair should have the same length.

Grounding and power supply decoupling

The ground connection on the PCB needs to be a large copper filled area connected to a common ground plane with an inductance as low as possible.

All V_{EE} pins (one at each corner and the exposed die pad) need to be connected to a common supply plane with an inductance as low as possible. This plane should be decoupled to ground. To avoid high frequency resonance, multiple bypass capacitors should not be mounted at the same location. To minimize low frequency switching noise in the vicinity of the TZA3019, the power supply line should be filtered once using a beaded capacitor circuit with a low cut-off frequency (see Figs 13 and 14).

The V_{EE} connection on the PCB also needs to be a large copper area to improve heat transfer to the PCB and thus support IC cooling.



In order to enable heat flow out of the package, the following measures have to be taken:

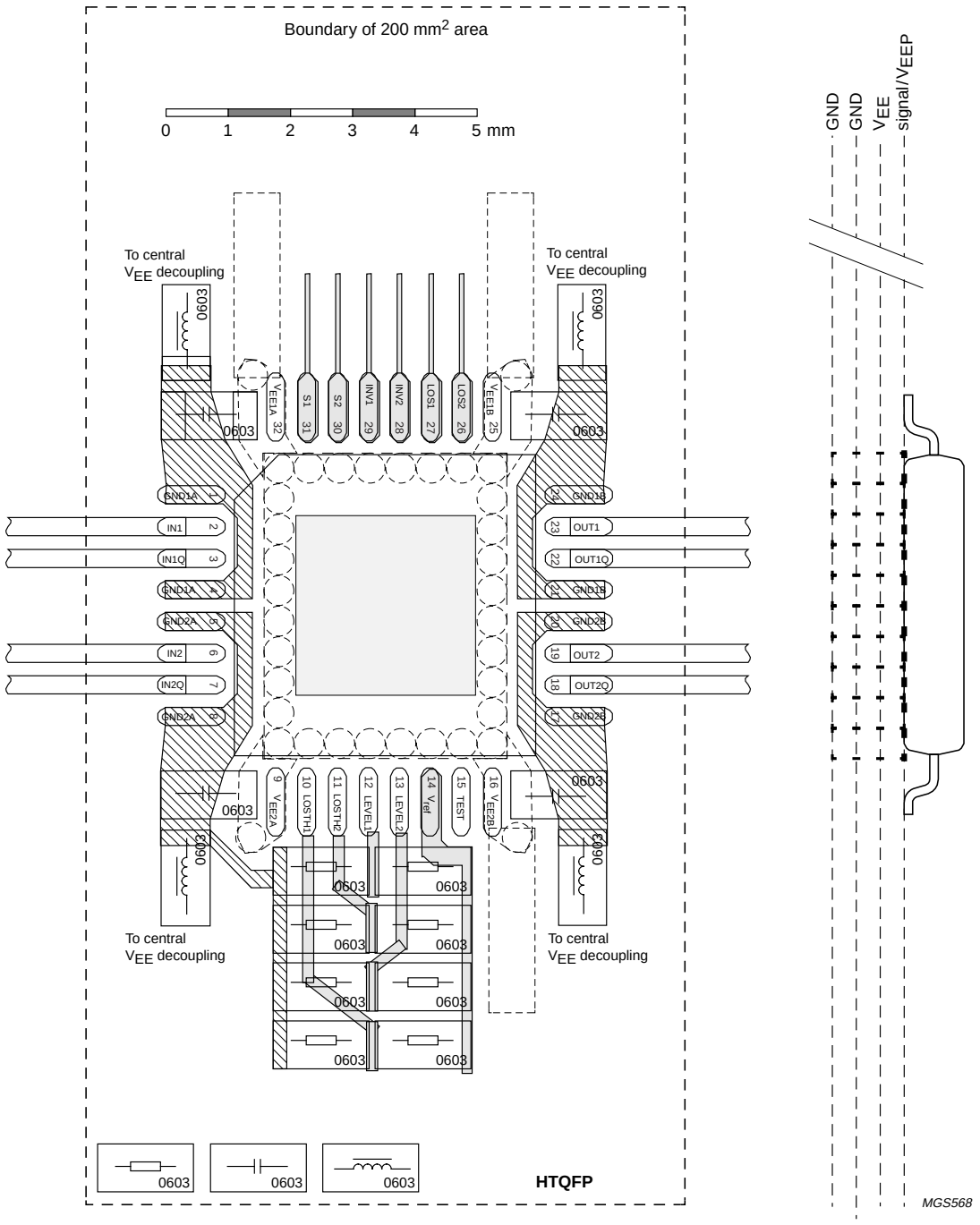
(1) Solder the 3 × 3 mm^2 die pad to a plane with maximum size.

(2) Add a plane with minimum 200 mm^2 in an inner layer, surrounded by ground layers.

(3) Use maximum amount of vias to connect two planes.

(4) Use minimum of openings in heat transport area between hot plane and ground planes.

Fig.13 PCB layout for negative supply voltage.



In order to enable heat flow out of the package, the following measures have to be taken:

(1) Solder the 3 × 3 mm^2 die pad to a plane with maximum size.

(2) Add a plane with minimum 200 mm^2 in an inner layer, surrounded by ground layers.

(3) Use maximum amount of vias to connect two planes.

(4) Use minimum of openings in heat transport area between hot plane and ground planes.

Fig.14 PCB layout for positive supply voltage.

BONDING PAD LOCATIONS

SYMBOL	PAD	COORDINATES(1)	
		x	y
GND1A	1	–928	+710
IN1	2	–928	+553
IN1Q	3	–928	+396
GND1A	4	–928	+239
n.c.	5	–928	+81
n.c.	6	–928	–81
GND2A	7	–928	–239
IN2	8	–928	–396
IN2Q	9	–928	–553
GND2A	10	–928	–710
V_{EE2A}	11	–707	–928
LOSTH1	12	–550	–928
LOSTH2	13	–393	–928
n.c.	14	–236	–928
LEVEL1	15	–79	–928
LEVEL2	16	+79	–928
VREF	17	+236	–928
n.c.	18	+393	–928
TEST	19	+550	–928
V_{EE2B}	20	+707	–928
GND2B	21	+928	–710
OUT2Q	22	+928	–553
OUT2	23	+928	–396
GND2B	24	+928	–239
n.c.	25	+928	–81
n.c.	26	+928	+81
GND1B	27	+928	+239
OUT1Q	28	+928	+396
OUT1	29	+928	+553
GND1B	30	+928	+710
V_{EE1B}	31	+707	+928
RSSI2	32	+550	+928
LOS2	33	+393	+928
RSSI1	34	+236	+928
LOS1	35	+79	+928
INV2	36	–79	+928
INV1	37	–236	+928
S2	38	–393	+928
S1	39	–550	+928
V_{EE1A}	40	–707	+928

Note

1. All x and y coordinates represent the position of the centre of the pad in μm with respect to the centre of the die (see Fig.15)

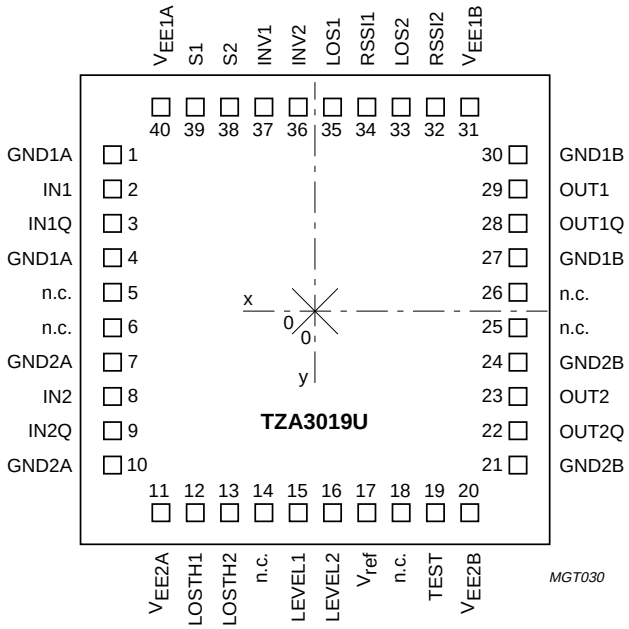
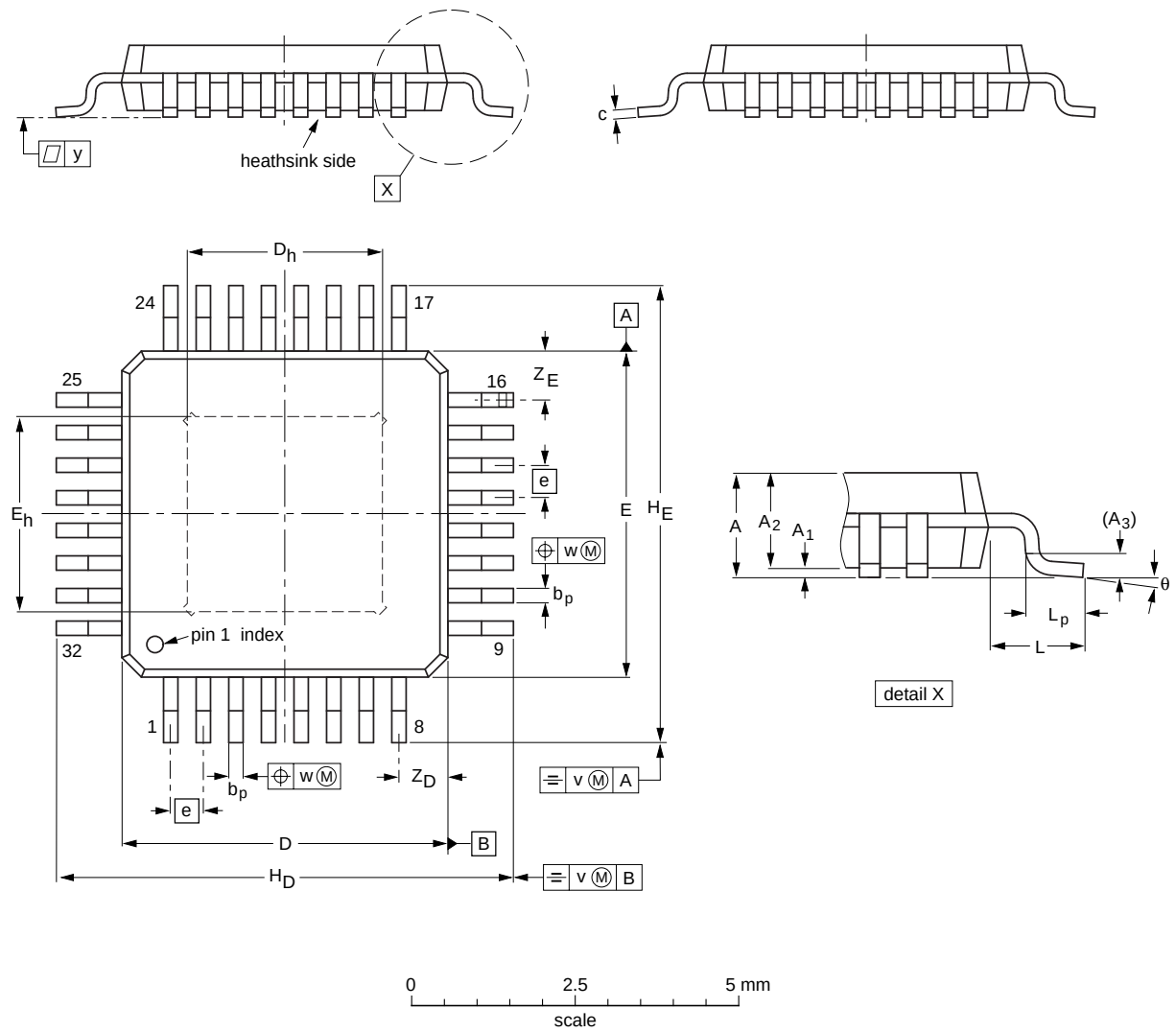


Fig.15 Bonding pad locations TZA3019U.

PACKAGE OUTLINE

HTQFP32: plastic, heatsink thin quad flat package; 32 leads; body 5 x 5 x 1.0 mm **SOT547-2**



DIMENSIONS (mm are the original dimensions)

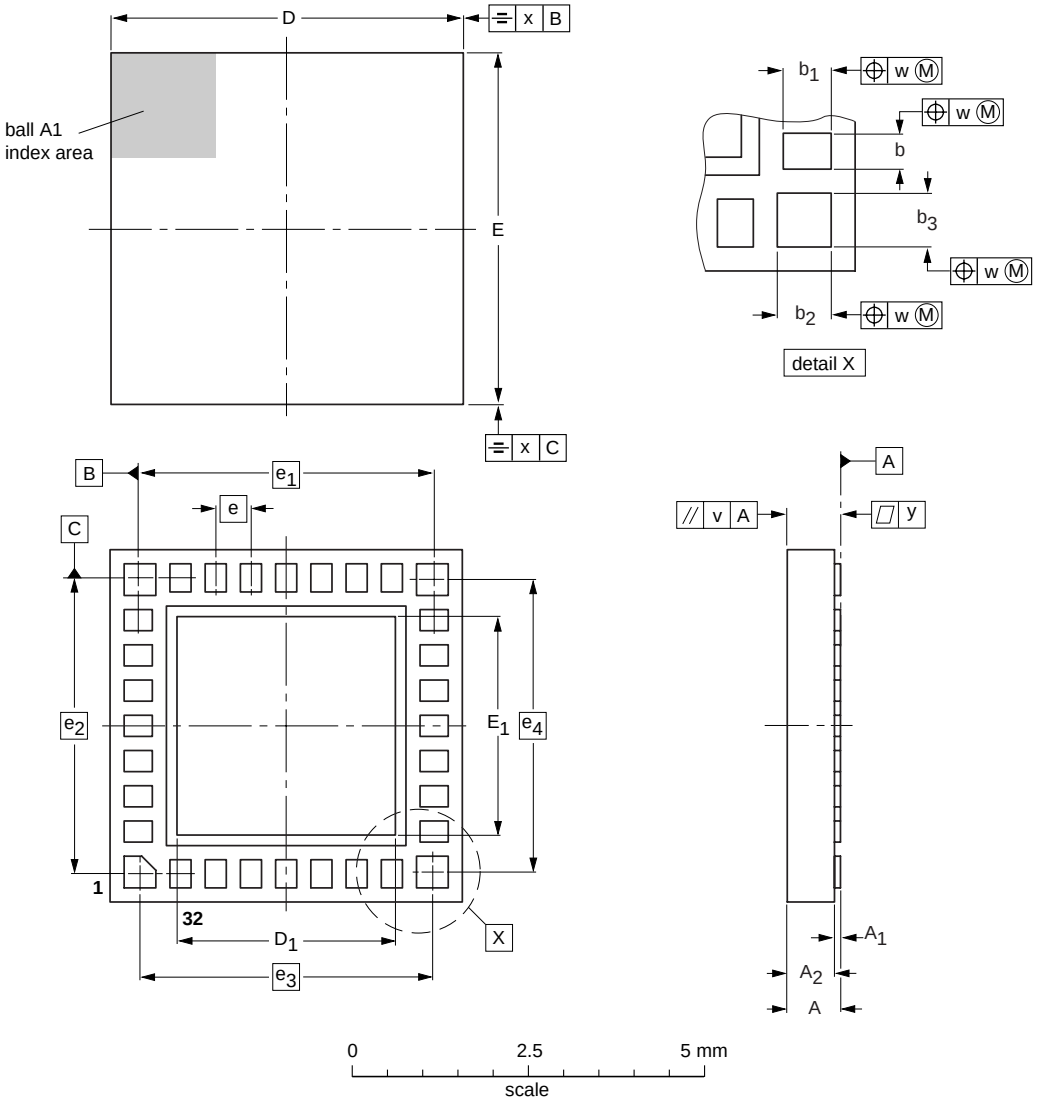
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	5.1 4.9	3.1 2.7	5.1 4.9	3.1 2.7	0.5	7.1 6.9	7.1 6.9	1.0	0.75 0.45	0.2	0.08	0.08	0.89 0.61	0.89 0.61	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT547-2						99-06-15

HBCC32: plastic, heatsink bottom chip carrier; 32 terminals; body 5 x 5 x 0.65 mm **SOT560-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	b_1	b_2	b_3	D	D_1	E	E_1	e	e_1	e_2	e_3	e_4	v	w	x	y
mm	0.80	0.10 0.05	0.70 0.60	0.35 0.20	0.50 0.30	0.50 0.35	0.50 0.35	5.1 4.9	3.2 3.0	5.1 4.9	3.2 3.0	0.5	4.2	4.2	4.15	4.15	0.2	0.15	0.15	0.05

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT560-1		MO-217				~~99-09-10~~ 00-02-01

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 3341 299, Fax.+381 11 3342 553

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International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
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