PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD29F016L

16M-BIT CMOS LOW-VOLTAGE FLASH MEMORY
2M-WORD BY 8-BIT

Description

The μPD29F016L is a low-voltage (2.2 to 2.7 V, 2.7 to 3.6 V) flash memory organized as 16,777,216 bits (2,097,152 words × 8 bits) in 35 sectors.

It is available as a T type in which the boot sector is allocated to the highest address (sector), and a B type in which the boot sector is allocated to the lowest address (sector).

The package is a 40-pin plastic TSOP (I).

Features

- Word organization : 2,097,152 words × 8 bits
- Sector organization : 35 sectors (16 Kbytes × 1 sector, 8 Kbytes × 2 sectors, 32 Kbytes × 1 sector, 64 Kbytes × 31 sectors)
- 2 types of sector organization
  - T type : Boot sector allocated to the highest address (sector)
  - B type : Boot sector allocated to the lowest address (sector)
- Automatic program
  - Unlock bypass program
- Automatic erase
  - Chip erase
  - Sector erase (sectors can be combined freely)
  - Erase suspend / resume
- Program / Erase completion detection
  - Detection through data polling and toggle bits
  - Detection through RY (/BY) pin
- Sector protection
  - Any sector can be protected
  - Any protected sector can be temporary unprotected
- Hardware reset and standby using /RESET pin
- Automatic Sleep Mode

Part number	Operating supply voltage V	Access time ns (MAX.)	Power supply current (Active mode) mA (MAX.)	Standby current (CMOS level input) μA (MAX.)
μPD29F016L-Bxxx	3.0 +0.6 / –0.3	90, 100, 120	30	5
μPD29F016L-Cxxx	2.4 +0.3 / –0.2	120, 150		

- Program / erase time
  - Program : 9.0 μs / byte (TYP.)
  - Sector erase : 1.0 s (TYP.)
- Number of program / erase : 100,000 times (MIN.)

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Ordering Information

Part number	Access time ns (MAX.)	Operating supply voltage V	Boot sector	Package
μPD29F016LGZ-B90T-LJH	90	2.7 to 3.6	Top address (sector) (T type)	40-pin plastic TSOP (I) (10 × 20 mm) (Normal bent)
μPD29F016LGZ-B10T-LJH	100			
μPD29F016LGZ-B12T-LJH	120			
μPD29F016LGZ-B90B-LJH	90		Bottom address (sector) (B type)	
μPD29F016LGZ-B10B-LJH	100			
μPD29F016LGZ-B12B-LJH	120			
μPD29F016LGZ-C12T-LJH	120	2.2 to 2.7	Top address (sector) (T type)	
μPD29F016LGZ-C15T-LJH	150			
μPD29F016LGZ-C12B-LJH	120		Bottom address (sector) (B type)	
μPD29F016LGZ-C15B-LJH	150			

Remark For address organization of sectors, see section **2. Sector Organization / Sector Address Table**.

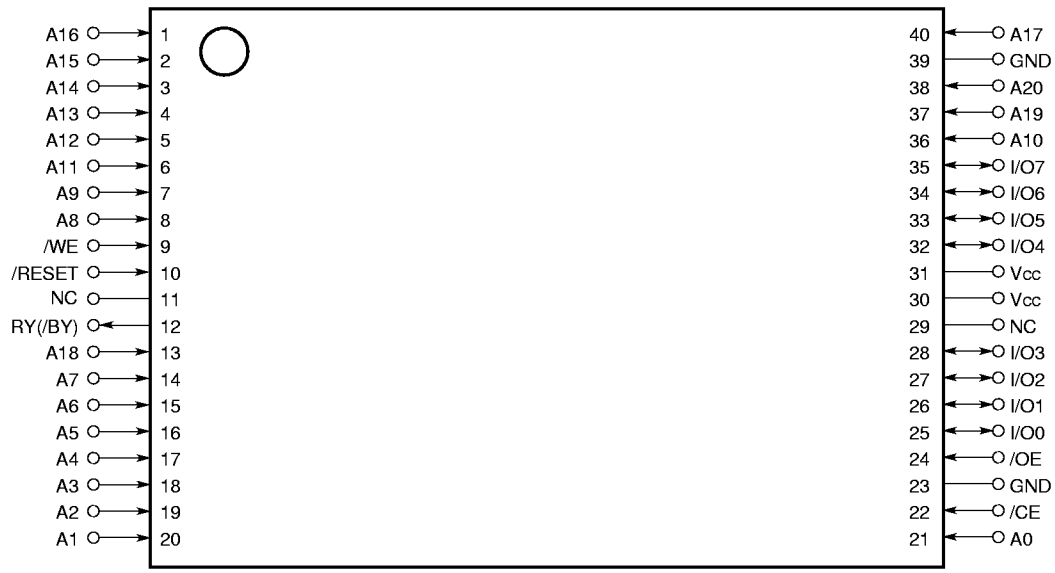
Pin Configuration (Marking Side)

/xxx indicates active low signal.

40-pin Plastic TSOP (I) (10 × 20 mm) (Normal Bent)

[μPD29F016LGZ-Bxxx-LJH]

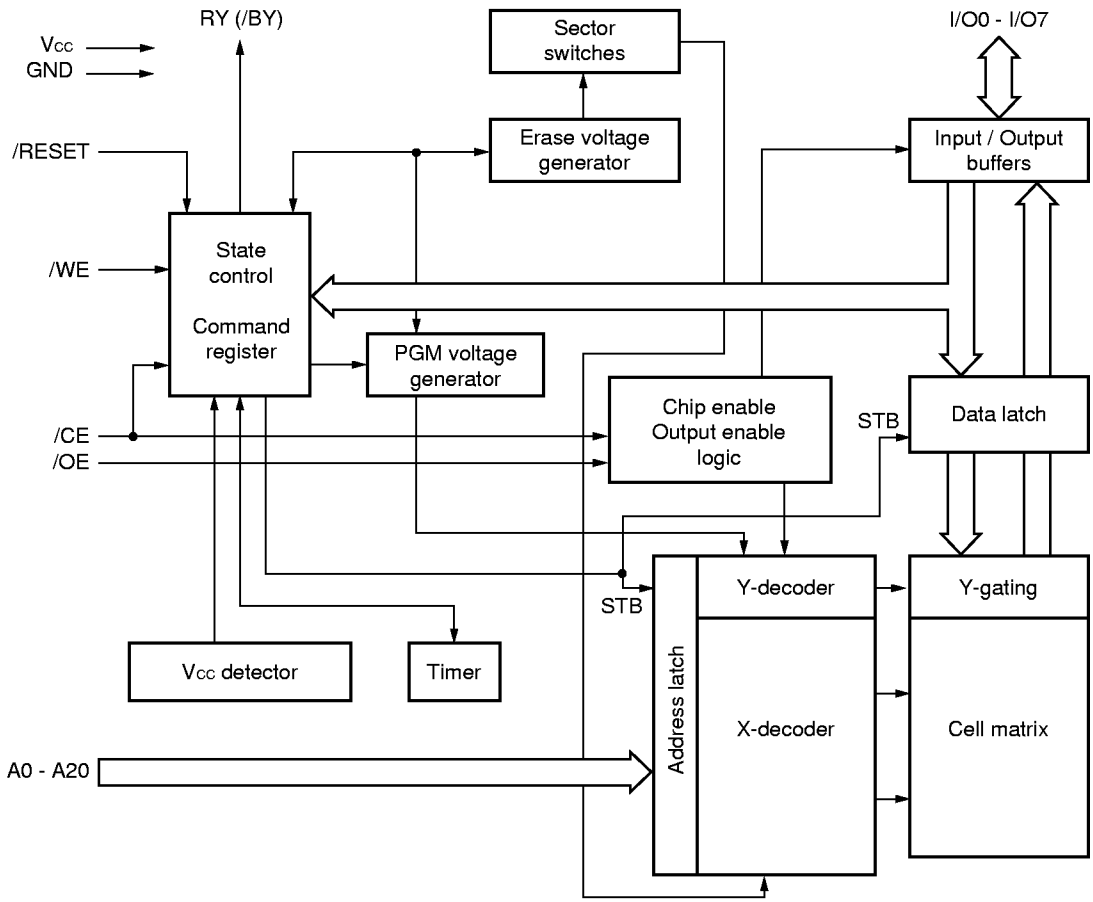
[μPD29F016LGZ-Cxxx-LJH]



A0 - A20	:	Address inputs
I/O0 - I/O7	:	Data Inputs / Outputs
/CE	:	Chip Enable
/WE	:	Write Enable
/OE	:	Output Enable
/RESET	:	Hardware reset input
RY (/BY)	:	Ready (Busy) output
Vcc	:	Supply Voltage
GND	:	Ground
NC [Note]	:	No Connection

Note Some signals can be applied because this pin is not internally connected.

Block Diagram



Contents

1. Input / Output Pin Function

Pin name	Input / Output	Function
A0 - A20	Input	Address input pin
A9	Input	Address input pin. If 11.5 to 12.5 V is applied to A9, the chip enters the product ID mode. In this mode, and input to A0 causes the following codes to be output. A0 = Low level : Manufacturer code is output. A0 = High level : Device code is output.
I/O0 - I/O7	Input / Output	Data input / output pin.
/CE	Input	This pin inputs the signal that activates the chip. When high level, the chip enters the standby mode.
/OE	Input	This pin inputs the read operation control signal. When high level, output is disabled.
/WE	Input	This pin inputs the write operation control signal. When low level, command input is accepted.
/RESET	Input	This pin inputs hardware reset. When low level, hardware reset is performed. If 11.5 to 12.5 V is applied to /RESET, the chip enters the temporary sector unprotect mode.
RY (/BY)	Output	This pin indicates whether automatic program / erase is currently being executed. It uses open drain connection. Low level indicates the busy state during which the device is performing automatic program / erase. High level indicates the device is in the ready state and will accept the next operation. In this case, the device is either in the erase suspend mode or the standby mode.
V_{CC}	–	Supply Voltage
GND	–	Ground
NC	–	No Connection

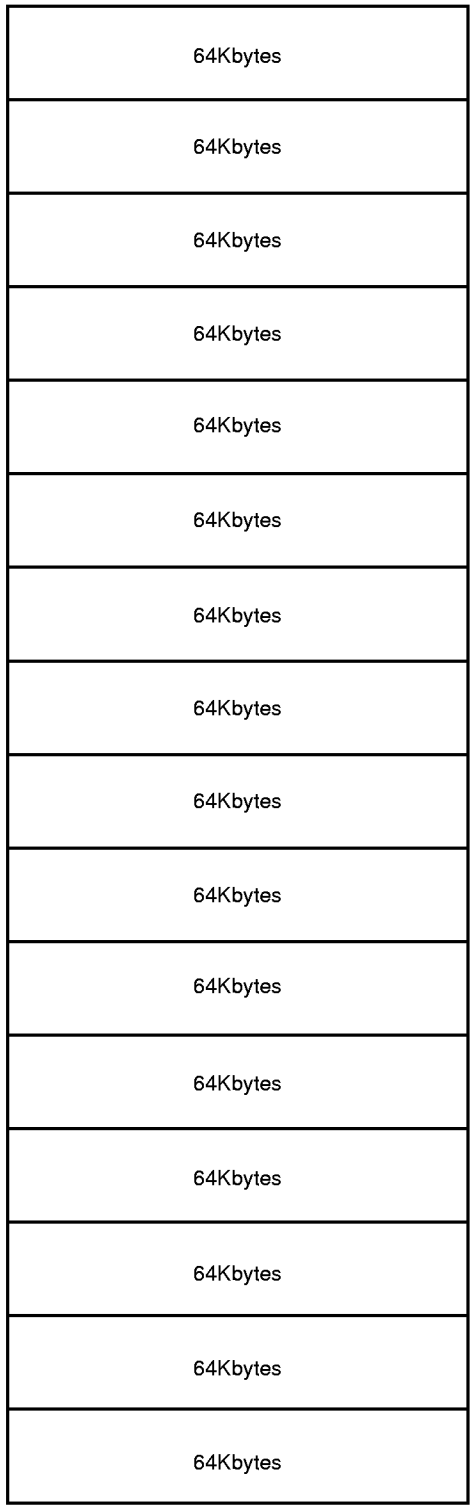
2. Sector Organization / Sector Address Table

[μPD29F016LGZ-×××T] (1/2)

Sector Layout	Address	Sector Address	A20	A19	A18	A17	A16	A15	A14	A13
16Kbytes	1FFFFFH 1FC000H	SA34	1	1	1	1	1	1	1	×
8Kbytes	1FBFFFH 1FA000H	SA33	1	1	1	1	1	1	0	1
8Kbytes	1F9FFFH 1F8000H	SA32	1	1	1	1	1	1	0	0
32Kbytes	1F7FFFH 1F0000H	SA31	1	1	1	1	1	0	×	×
64Kbytes	1EFFFFH 1E0000H	SA30	1	1	1	1	0	×	×	×
64Kbytes	1DFFFFH 1D0000H	SA29	1	1	1	0	1	×	×	×
64Kbytes	1CFFFFH 1C0000H	SA28	1	1	1	0	0	×	×	×
64Kbytes	1BFFFFH 1B0000H	SA27	1	1	0	1	1	×	×	×
64Kbytes	1AFFFFH 1A0000H	SA26	1	1	0	1	0	×	×	×
64Kbytes	19FFFFH 190000H	SA25	1	1	0	0	1	×	×	×
64Kbytes	18FFFFH 180000H	SA24	1	1	0	0	0	×	×	×
64Kbytes	17FFFFH 170000H	SA23	1	0	1	1	1	×	×	×
64Kbytes	16FFFFH 160000H	SA22	1	0	1	1	0	×	×	×
64Kbytes	15FFFFH 150000H	SA21	1	0	1	0	1	×	×	×
64Kbytes	14FFFFH 140000H	SA20	1	0	1	0	0	×	×	×
64Kbytes	13FFFFH 130000H	SA19	1	0	0	1	1	×	×	×
64Kbytes	12FFFFH 120000H	SA18	1	0	0	1	0	×	×	×
64Kbytes	11FFFFH 110000H	SA17	1	0	0	0	1	×	×	×
64Kbytes	10FFFFH 100000H	SA16	1	0	0	0	0	×	×	×

[μPD29F016LGZ-×××T] (2/2)

Sector Layout

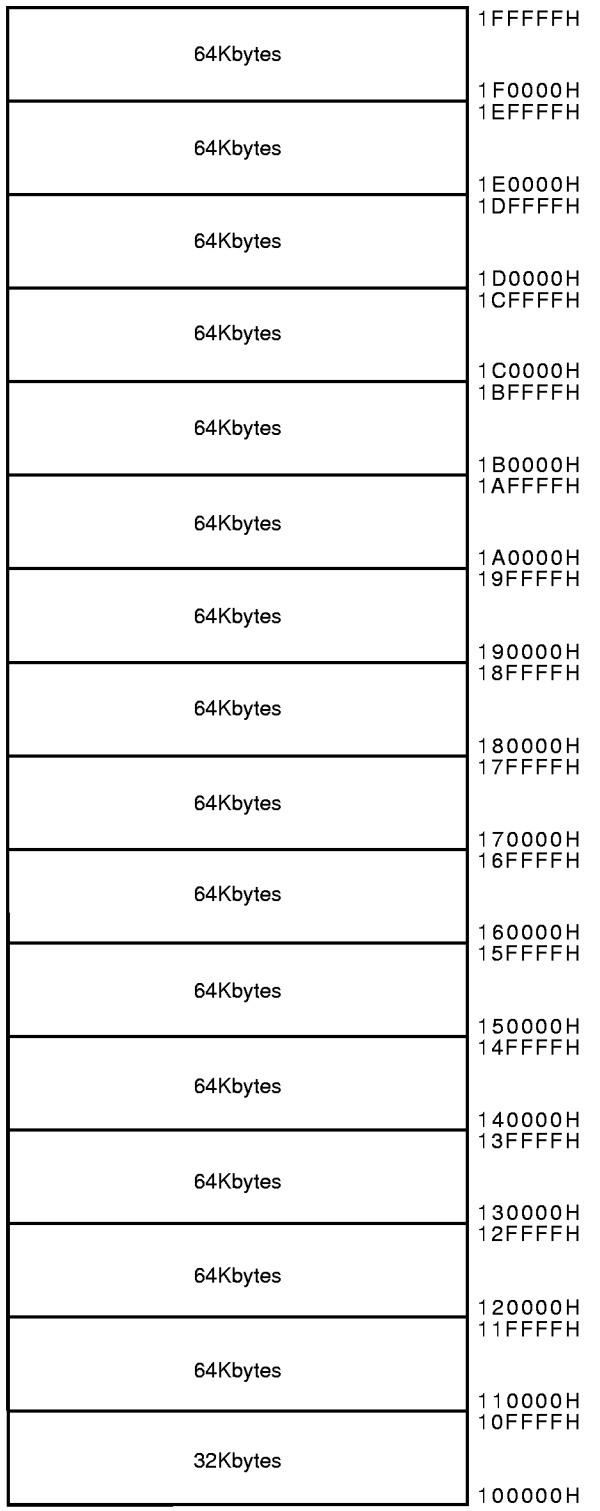


Sector Address Table

Address	Sector Address	A20	A19	A18	A17	A16	A15	A14	A13
0FFFFFH – 0F0000H	SA15	0	1	1	1	1	×	×	×
0EFFFFH – 0E0000H	SA14	0	1	1	1	0	×	×	×
0DFFFFH – 0D0000H	SA13	0	1	1	0	1	×	×	×
0CFFFFH – 0C0000H	SA12	0	1	1	0	0	×	×	×
0BFFFFH – 0B0000H	SA11	0	1	0	1	1	×	×	×
0AFFFFH – 0A0000H	SA10	0	1	0	1	0	×	×	×
09FFFFH – 090000H	SA9	0	1	0	0	1	×	×	×
08FFFFH – 080000H	SA8	0	1	0	0	0	×	×	×
07FFFFH – 070000H	SA7	0	0	1	1	1	×	×	×
06FFFFH – 060000H	SA6	0	0	1	1	0	×	×	×
05FFFFH – 050000H	SA5	0	0	1	0	1	×	×	×
04FFFFH – 040000H	SA4	0	0	1	0	0	×	×	×
03FFFFH – 030000H	SA3	0	0	0	1	1	×	×	×
02FFFFH – 020000H	SA2	0	0	0	1	0	×	×	×
01FFFFH – 010000H	SA1	0	0	0	0	1	×	×	×
00FFFFH – 000000H	SA0	0	0	0	0	0	×	×	×

[μPD29F016LGZ-×××B] (1/2)

Sector Layout



Sector Address Table

Sector Address	A20	A19	A18	A17	A16	A15	A14	A13
SA34	1	1	1	1	1	×	×	×
SA33	1	1	1	1	0	×	×	×
SA32	1	1	1	0	1	×	×	×
SA31	1	1	1	0	0	×	×	×
SA30	1	1	0	1	1	×	×	×
SA29	1	1	0	1	0	×	×	×
SA28	1	1	0	0	1	×	×	×
SA27	1	1	0	0	0	×	×	×
SA26	1	0	1	1	1	×	×	×
SA25	1	0	1	1	0	×	×	×
SA24	1	0	1	0	1	×	×	×
SA23	1	0	1	0	0	×	×	×
SA22	1	0	0	1	1	×	×	×
SA21	1	0	0	1	0	×	×	×
SA20	1	0	0	0	1	×	×	×
SA19	1	0	0	0	0	0	×	×

[μPD29F016LGZ-×××B] (2/2)

Sector Layout

	Address	Sector Address	A20	A19	A18	A17	A16	A15	A14	A13
64Kbytes	0FFFFFH 0F0000H	SA18	0	1	1	1	1	×	×	×
64Kbytes	0EFFFFH 0E0000H	SA17	0	1	1	1	0	×	×	×
64Kbytes	0DFFFFH 0D0000H	SA16	0	1	1	0	1	×	×	×
64Kbytes	0CFFFFH 0C0000H	SA15	0	1	1	0	0	×	×	×
64Kbytes	0BFFFFH 0B0000H	SA14	0	1	0	1	1	×	×	×
64Kbytes	0AFFFFH 0A0000H	SA13	0	1	0	1	0	×	×	×
64Kbytes	09FFFFH 090000H	SA12	0	1	0	0	1	×	×	×
64Kbytes	08FFFFH 080000H	SA11	0	1	0	0	0	×	×	×
64Kbytes	07FFFFH 070000H	SA10	0	0	1	1	1	×	×	×
64Kbytes	06FFFFH 060000H	SA9	0	0	1	1	0	×	×	×
64Kbytes	05FFFFH 050000H	SA8	0	0	1	0	1	×	×	×
64Kbytes	04FFFFH 040000H	SA7	0	0	1	0	0	×	×	×
64Kbytes	03FFFFH 030000H	SA6	0	0	0	1	1	×	×	×
64Kbytes	02FFFFH 020000H	SA5	0	0	0	1	0	×	×	×
64Kbytes	01FFFFH 010000H	SA4	0	0	0	0	1	×	×	×
32Kbytes	00FFFFH 008000H	SA3	0	0	0	0	0	1	×	×
8Kbytes	007FFFH 006000H	SA2	0	0	0	0	0	0	1	1
8Kbytes	005FFFH 004000H	SA1	0	0	0	0	0	0	1	0
16Kbytes	003FFFH 000000H	SA0	0	0	0	0	0	0	0	×

Sector Address Table

3. Bus Operations

The Operation modes of this device are described below.

Table 3-1. Bus Operation

Operation		/CE	/OE	/WE	A9	A6	A1	A0	I/O0 - I/O7	/RESET
Read		L	L	H	Address input				Data output	H
Write		L	H	L	Address input				Data input	H
Standby		H	×	×	×	×	×	×	Hi-Z	H
Output disable		L	H	H	×	×	×	×	Hi-Z	H
Hardware reset		×	×	×	×	×	×	×	Hi-Z	L
Sector protect		L	V_{ID}	Pulse	V_{ID}	L	H	L	×	H
Verify sector protect		L	L	H	V_{ID}	L	H	L	Code	H
Temporary sector unprotect		×	×	×	×	×	×	×	×	V_{ID}
Product ID Note	Manufacturer ID	L	L	H	V_{ID}	L	L	L	Code	H
	Device ID	L	L	H	V_{ID}	L	L	H	Code	H

Note The manufacturer code and device code can also be read by using commands. See section **4.3 Product ID**.

Remark H : V_{IH}, L : V_{IL}, × : Don't care, V_{ID} : 12.0 V ± 0.5 V

3.1 Read

At power on or reset (hardware reset or reset command), the device is set to read mode. This device will automatically power-up in the read / reset state. In this case, a command sequence is not required to read data. When reading out a data without changing address after power-up, it is necessary to input hardware reset or change /CE pin from "H" to "L".

Once the device is in read mode, no command is necessary for reading data. Data can be read using the standard microprocessor read cycle.

The read mode is maintained until the contents of the command register are changed.

3.2 Write

Command write can be done using the standard microprocessor write timing.

The command is written to the command register. The command register has the function to latch the address and data necessary for executing an instruction, and does not take up memory.

When an incorrect address or data is written, or addresses and data are written in an incorrect sequence, the device is reset to the read mode.

3.3 Standby

When no write or read is performed, the device can be placed in standby mode. In this mode, the power consumption is considerably reduced.

The device goes into standby mode when the /CE and /RESET pins are maintained at V_{IH}. At this time, the supply current can be kept at 5 μA or below by maintaining the /CE and /RESET at V_{CC} ± 0.3 V.

3.4 Output Disable

The output of the device can be disabled by maintaining /OE at V_{IH}, at which time the output goes into high impedance.

3.5 Hardware Reset

The device can be reset to read mode by maintaining the /RESET pin at V_{IL} at least during the t_{RP} period.

While the /RESET pin is held at V_{IL}, all write and read commands are ignored. Moreover, all output pins go into high impedance. At this time, the supply current can be kept at 5 μA or below by maintaining /RESET at GND ± 0.2 V.

When performing reset, the operations in progress are all interrupted. Therefore, when reset is performed during program or erase (including erase suspend), the address or sector data become undefined. In this case, after reset is completed, perform the program or erase operation again.

3.6 Sector Protect

The sector protect function enables protection of any sector. Protected sectors cannot be programmed or erased, and any combination of up to 35 sectors can be protected.

To select the sector protect mode, apply V_{ID} to A9 and /OE. Moreover, input V_{IL}, V_{IH}, and V_{IL} to A0, A1, and A6, respectively, input the sector address of the sector to be protected to A13 to A20, and input V_{IL} to /CE.

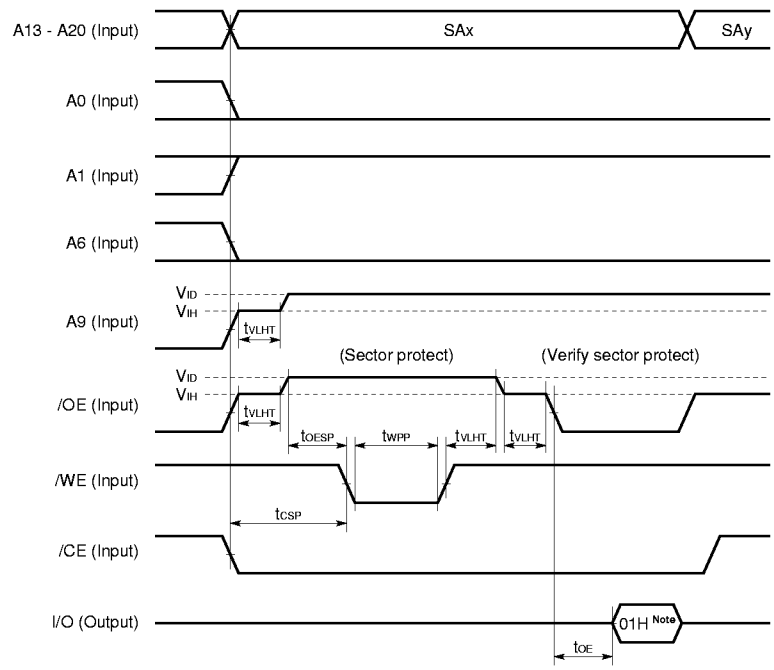
Sector protection setting starts at the falling edge of the /WE pulse and ends at the rising edge of the same pulse. Maintain the sector address at a constant level during the /WE pulse interval.

To perform sector protect verification, apply V_{ID} to A9. Also input V_{IL}, V_{IH}, and V_{IL} to A0, A1, and A6, respectively, and the sector address of the sector to be verified to A13 to A20. The other address pins are Don't Care (V_{IL} is recommended.)

When read from the input sector address is performed, the sector protect verification result is output to I/O0. If the verified sector is protected, "1" is output to I/O0. If it is not protected, "0" is output.

Sector protect enables writing commands by applying V_{ID} to /RESET. Moreover, it is also possible to unprotect the sector with the same method. For details, see section **4.9 Sector Protect (by Command Input)**, and section **4.10 Sector Unprotect**.

Figure 3-1. Sector Protect Timing Chart

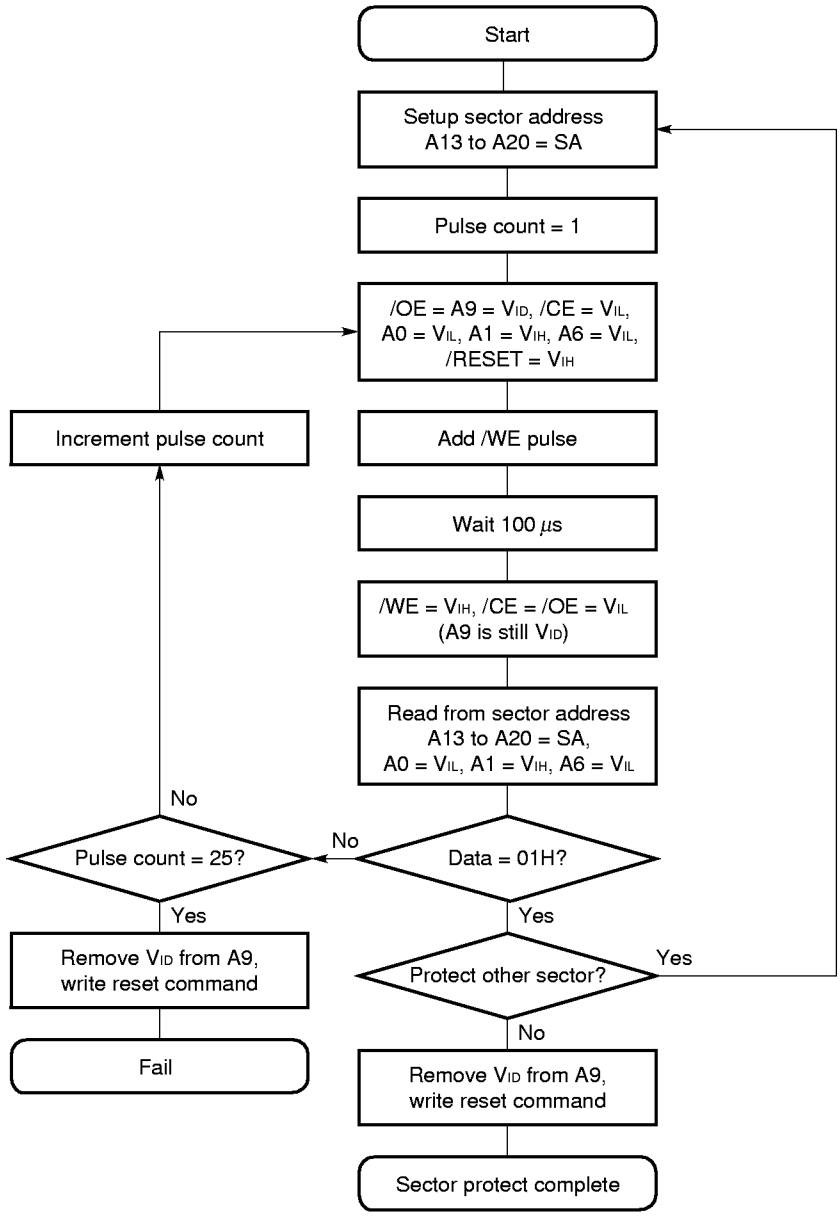


Note The sector protect verification result is output.

01H : The sector is protected.

00H : The sector is not protected.

Figure 3-2. Sector Protect Timing Chart



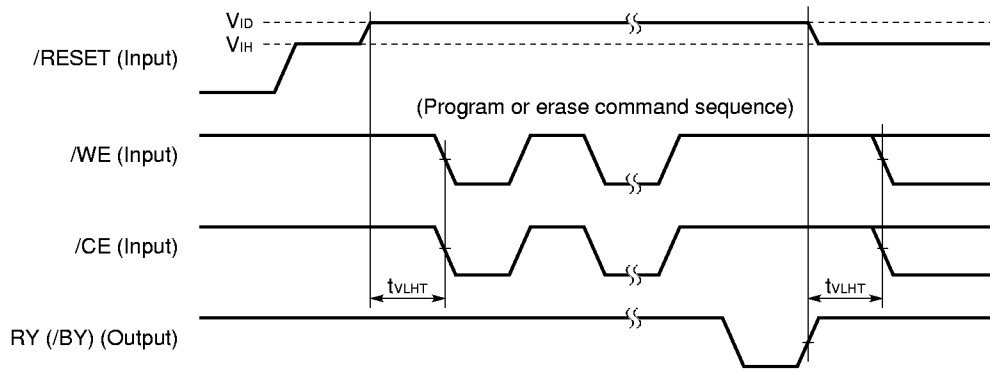
3.7 Temporary Sector Unprotect

Protected sector can be temporary unprotected in order to perform data program and erase.

To select the temporary sector unprotect mode, apply V_{ID} to /RESET. While this mode is selected, program and erase can be performed even for protected sectors.

When V_{ID} stops being applied to /RESET, the sector is again protected.

Figure 3-3. Temporary Sector Unprotect Timing Chart



3.8 Product ID

The product ID mode enables reading the manufacturer code and device code from the device.

This mode is used for example to switch the algorithm of the program device according to the device.

To select the product ID mode, apply V_{ID} to A9. Moreover, input V_{IL} to A1 and A6, and input V_{IL} to A0 to read the manufacturer code, and V_{IH} to read the device code. Other addresses are Don't Care (V_{IL} is recommended.)

When read is performed, the code described in Table 3-2 is output.

The manufacturer code and device code can be read by using a command. In this case, V_{ID} need not be applied to A9. See section **4.3 Product ID**.

Table 3-2. Product ID Code

Product ID code		Inputs			Code outputs								
		A6	A1	A0	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Hex
Manufacturer code		V_{IL}	V_{IL}	V_{IL}	0	0	0	1	0	0	0	0	10H
Device code	-B××T	V_{IL}	V_{IL}	V_{IH}	1	1	0	0	0	1	1	1	C7H
	-B××B	V_{IL}	V_{IL}	V_{IH}	0	1	0	0	1	1	0	0	4CH
	-C××T	V_{IL}	V_{IL}	V_{IH}	1	1	1	0	0	0	0	1	E1H
	-C××B	V_{IL}	V_{IL}	V_{IH}	1	1	1	0	0	0	1	0	E2H

3.9 Automatic Sleep Mode

To activate this mode, this device automatically switch themselves to low power mode when their address remains stabile during minimum access time. Since the data latched during this mode, the data are read-out continuously. It is not necessary to control /CE, /WE and /OE on the mode. Under the mode, the current consumed is less than 5μA.

If the addresses are changed, this mode is canceled automatically and the device read-out the data for change address.

4. Commands

The commands of this device and the command write method are described below.

4.1 Writing Commands

The write cycle of a standard microprocessor is used for command write.

Commands are written to the command register. The command register functions to latch addresses and data required for instruction execution, and does not take up memory.

When an incorrect address or data is written, or addresses and data are written in an incorrect sequence, the device is reset to the read mode.

Table 4-1 lists the commands and command sequence.

Table 4-1. Command Sequence

Command sequence	Bus	1st bus cycle		2nd bus cycle		3rd bus cycle		4th bus cycle		5th bus cycle		6th bus cycle	
	cycles	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Read / Reset Note 1	1	×××H	F0H	RA	RD	–	–	–	–	–	–	–	–
Read / Reset Note 1	3	555H	AAH	2AAH	55H	555H	F0H	RA	RD	–	–	–	–
Product ID	3	555H	AAH	2AAH	55H	555H	90H	IA	ID	–	–	–	–
Program	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD	–	–	–	–
Chip erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Sector erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
Sector erase suspend Note 2	1	×××H	B0H	–	–	–	–	–	–	–	–	–	–
Sector erase resume Note 3	1	×××H	30H	–	–	–	–	–	–	–	–	–	–
Unlock bypass set	3	555H	AAH	2AAH	55H	555H	20H	–	–	–	–	–	–
Unlock bypass program	2	×××H	A0H	PA	PD	–	–	–	–	–	–	–	–
Unlock bypass reset	2	×××H	90H	×××H	00H	–	–	–	–	–	–	–	–

Notes 1. The device is reset to read mode by either the read or reset command.

2. If B0H is input to any address during sector erase, erase is suspended.

3. If 30H is input to any address during sector erase suspend, erase is resumed.

Remarks 1. RA : Read address.

RD : Read data.

PA : Program address.

PD : Program data.

SA : Erase address. Select the sector to be erased with a combination of A13 to A20. See section **2. Sector Organization / Sector Address Table**.

IA : 00000H (If reading the manufacturer code).

: 00001H (If reading the device code).

ID : 10H (manufacturer code).

: C7H (B××T type device code), E1H (C××T type device code)

: 4CH (B××B type device code), E2H (C××B type device code)

2. A11 to A20 are Don't Care except when selecting a program / erase address.

3. For the bus operation, see section **3. Bus Operation**.

4.2 Read / Reset

This command resets the device to the read mode.

Once the device is in the read mode, no command is necessary for reading data. Data can be read using the standard microprocessor read cycle.

The read mode is maintained until the contents of the command register are changed.

4.3 Product ID

This command is used to read the manufacturer code or the device code of the device.

The manufacturer code (10H) is output by inputting 00000H in the address using the fourth write cycle. The device code is output when 00001H is input.

The manufacturer code and device code can be read by selecting the product ID mode by applying V_{ID} to the A9 pin (See section **3.8 Product ID**). However, applying a high voltage to the address pin is not desirable due to system design considerations. Using this command allows reading the manufacturer code and device code without applying a high voltage to the pin.

4.4 Program

This command is used to program data.

Program is performed in 1-byte units. Program can be performed regardless of the address sequence, even if the sector limit is exceeded. However, "0" cannot be changed back into "1" through the program operation. If overwriting "1" to "0" is attempted, the program operation is interrupted and "1" is output to I/O5, or successful program is indicated in data polling, but actually the data is "0" as before.

Following write by command sequence, the pulse required for program is automatically generated inside the device and program verification is automatically performed, so that control from external is not required.

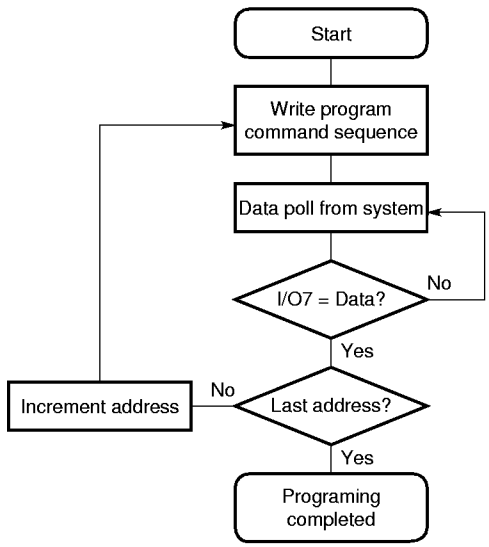
During automatic program, all commands that have been written are ignored. However, automatic program is interrupted when hardware reset is performed. Since the programmed data is not guaranteed in this case, reexecute the program command following completion of reset.

Upon completion of automatic program, the device returns to the read mode.

The operation status of automatic program can be determined by using the hardware sequence flags (I/O7, I/O6, RY (/BY) pins).

See sections **5.1 I/O7 (Data Polling)**, **5.2 I/O6 (Toggle Bit)**, and **5.6 RY (/BY) (Ready / Busy)**.

Figure 4-1. Program Flow Chart



4.5 Chip Erase

This command is used to erase the entire chip.

Following command sequence write, erase is performed after "0" is written to all memory cells and verification is performed, using the automatic erase function. Program before erase and control from external are not required.

During automatic erase, all commands that have been written are ignored. However, automatic erase is interrupted by hardware reset. Since erase is not guaranteed in this case, execute the chip erase command again after reset is completed.

Upon completion of automatic erase, the device returns to read mode.

The automatic erase operation status can be determined with the hardware sequence flags (I/O7, I/O6, RY (/BY) pins). See sections **5.1 I/O7 (Data Polling), 5.2 I/O6 (Toggle Bit)**, and **5.6 RY (/BY) (Ready / Busy)**.

4.6 Sector Erase

This command is used to erase sectors one at a time.

Following command sequence write, erase is performed after "0" is written to all sectors to be erased and verification is performed, using the automatic erase function. Data program before erase and control from external are not required.

Sector erase timeout starts after command sequence write. During this timeout, sectors to be erased can be added and selected. At this time, write the sector address and data (30H) of the sectors to be erased that have been added.

If the selected sectors include both protected sectors and unprotected sectors, only the unprotected sectors will be erased and the protected sectors will be ignored.

If a command other than sector erase or erase suspend is input during timeout, the device is reset to the read mode.

Automatic erase starts upon timeout completion. At this time, erase is started even if the last write cycle is not completed.

During automatic erase, all commands other than erase suspend are ignored. However, when hardware reset is performed, erase is interrupted. Since sector erase is not guaranteed in this case, reexecute the sector erase command following completion of reset.

Upon completion of automatic erase, the device returns to the read mode.

The operation status of automatic erase can be determined by using the hardware sequence flags (I/O7, I/O6, I/O2, RY (/BY) pins). See sections **5.1 I/O7 (Data Polling)**, **5.2 I/O6 (Toggle Bit)**, **5.3 I/O2 (Toggle Bit II)**, and **5.6 RY (/BY) (Ready / Busy)**.

Figure 4-2. Sector / Chip Erase Flow Chart

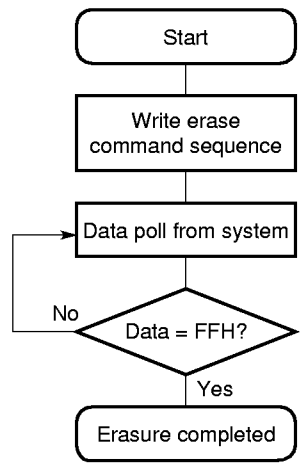
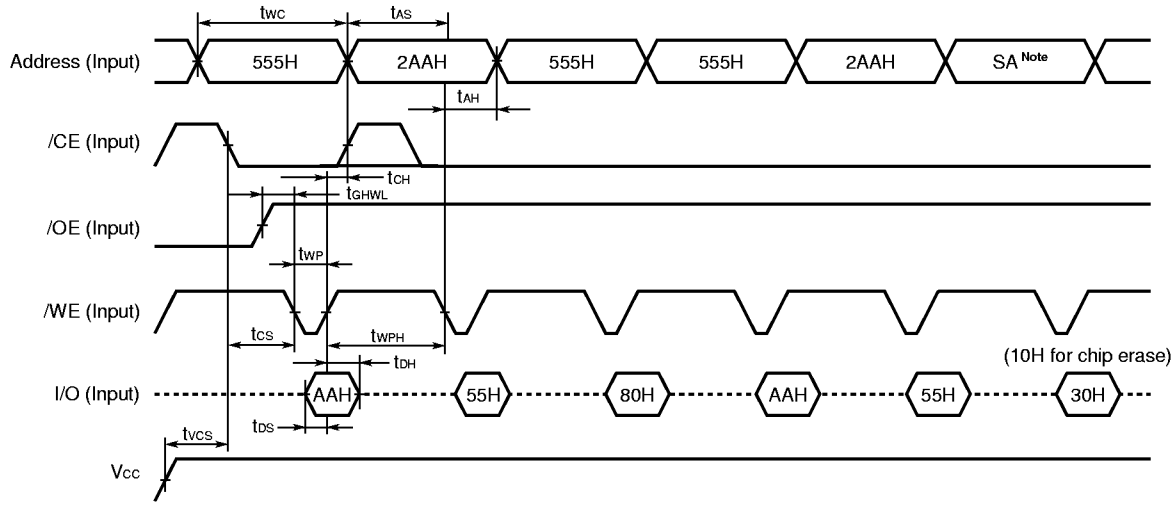


Figure 4-3. Sector / Chip Erase Timing Chart



Note SA is the sector address of the sector to be erased. For chip erase, input 555H.

4.7 Erase Suspend / Resume

This command suspends automatic erase. During erase suspend, sectors for which erase is not performed can be written to.

Suspend can be performed for sector erase (including the timeout period), but it cannot be performed for chip erase and automatic program. Suspend can be performed for all sectors for which erase is being performed.

Following command sequence write, 20 μs are required until automatic erase is suspended.

While automatic erase is suspended, any sector for which erase is not being performed can be read and programmed.

Whether automatic erase is suspended can be determined with the hardware sequence flags (I/O7, I/O6, I/O2 pins). See sections **5.1 I/O7 (Data Polling)**, **5.2 I/O6 (Toggle Bit)**, and **5.3 I/O2 (Toggle Bit II)**.

To resume erase after it has been suspended, write the command (30H) again during erase suspend.

4.8 Unlock Bypass

This device provides an unlock bypass mode to shorten the write time.

Normally, 2 unlock cycles are required during program. In contrast, with the unlock bypass mode, it is possible to perform program without unlock cycles.

In the unlock bypass mode, all commands except unlock bypass program and unlock bypass reset are ignored.

4.8.1 Unlock Bypass Set

This command sets the device to the unlock bypass mode.

4.8.2 Unlock Bypass Program

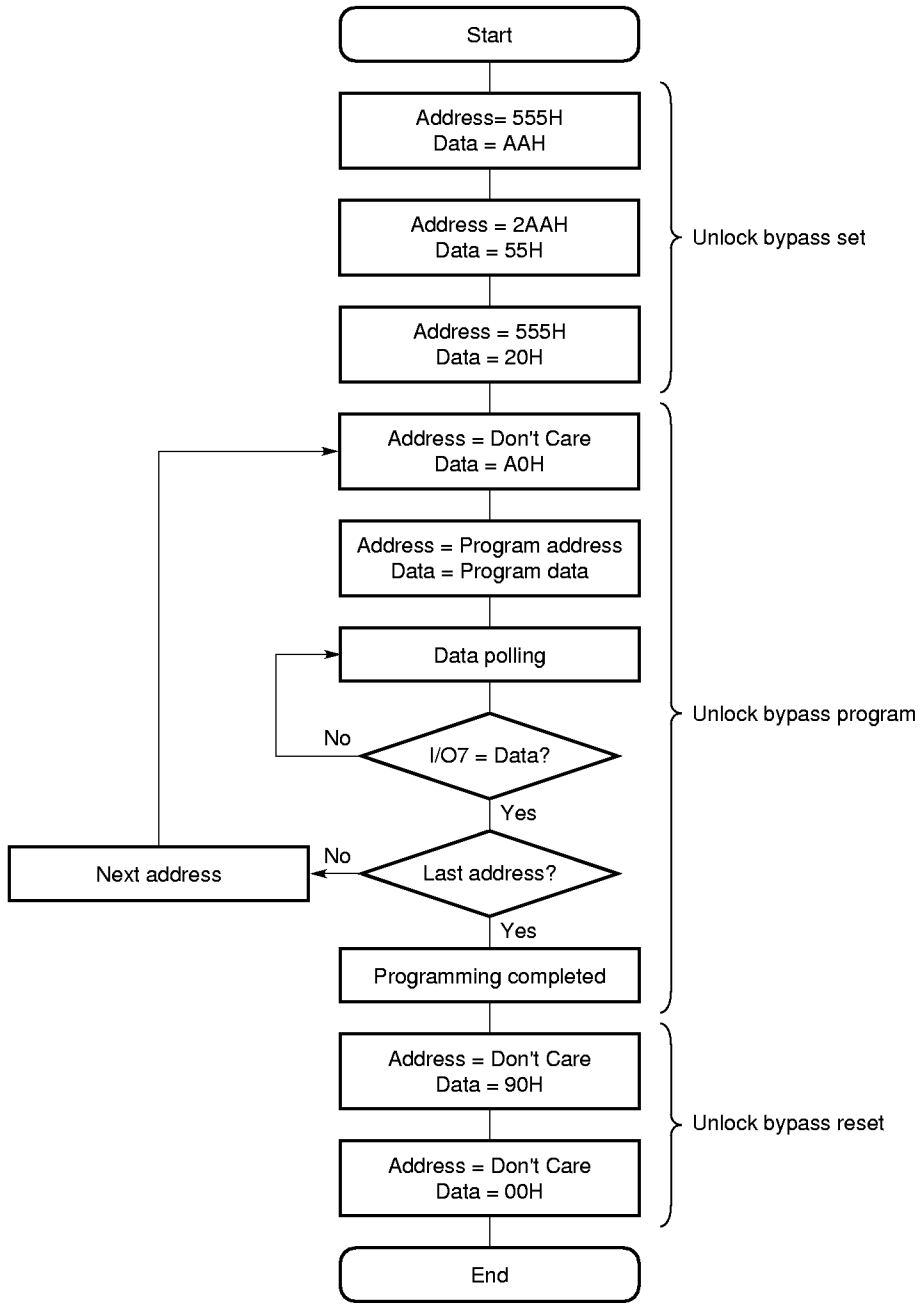
This command is used to perform program in the unlock bypass mode.

4.8.3 Unlock Bypass Reset

This command is used to quit the unlock bypass mode.

When this command is executed, the device returns to the read mode.

Figure 4-4. Unlock Bypass Flow Chart



4.9 Sector Protect (By Command Input)

This command performs sector protect.

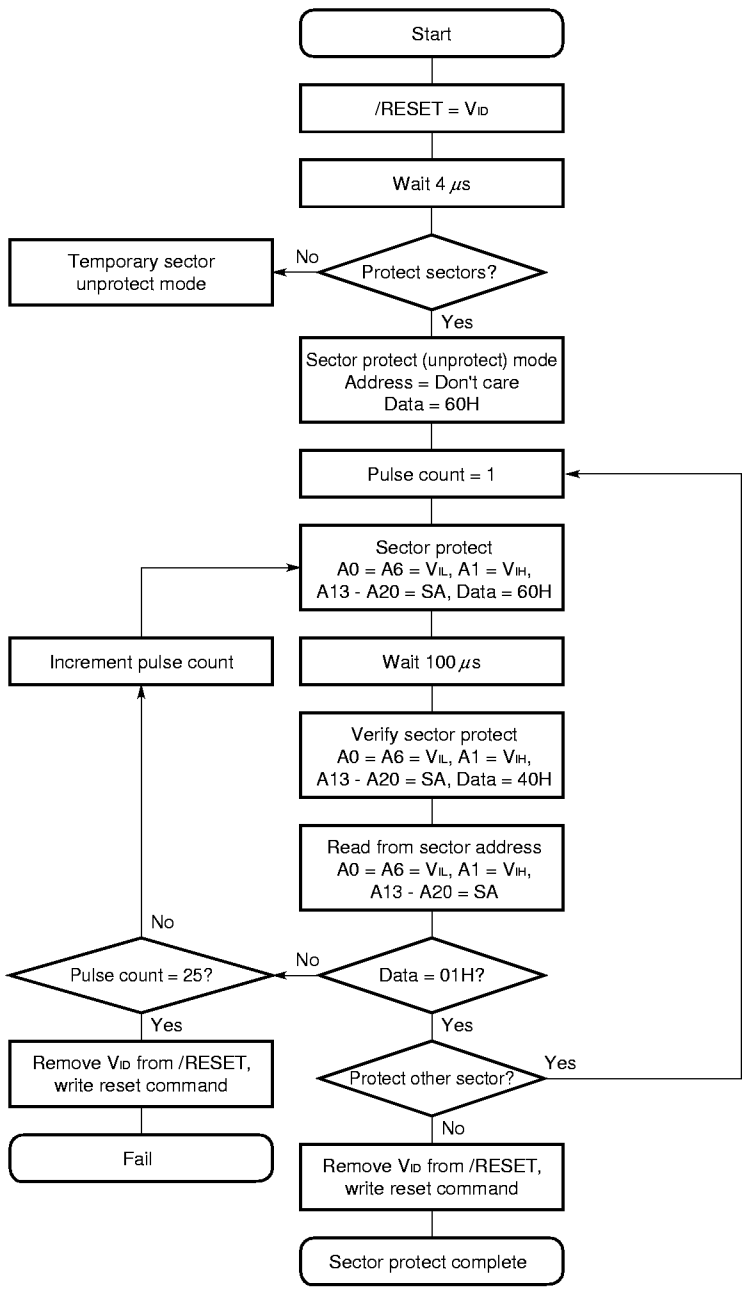
By applying V_{ID} to /RESET and writing 60H to any address, the device enters the sector protect or unprotect mode.

Sector protect is started by inputting the sector address of the sector to be protected to A13 to A20, inputting V_{IL} to A0 and A6, inputting V_{IH} to A1, and writing 60H. After a timeout of 100 μs, sector protect is completed.

Next, with the sector address input to A13 to A20, the device enters the sector protect verify mode by inputting V_{IL} to A0 and A6, V_{IH} to A1, and writing 40H. When read is performed in this state, the sector protect verify result is output to I/O0. If "1" is output to I/O0, the verified sector is protected. If "1" was not output to I/O0, sector protect failed, so perform sector protect again.

Sector protect can also be performed by inputting V_{ID} to A9 and /OE. For details, see section **3.6 Sector Protect**.

Figure 4-5. Sector Protect (By Command Input)



4.10 Sector Unprotect

This command performs sector unprotect.

Sector unprotect is performed for all sectors. Unprotect cannot be performed for specific sectors. Moreover, all sectors must be protected prior to unprotect.

The device enters the sector protect or unprotect mode by applying V_{ID} to /RESET and writing 60H to any address.

If unprotected sectors exist, first perform sector protect for these sectors. To perform sector protect, input the sector address of the sector to be protected to A13 to A20, V_{IL} to A0 and A6, and V_{IH} to A1, and write 60H. See section **4.9 Sector Protect (By Command Input)**.

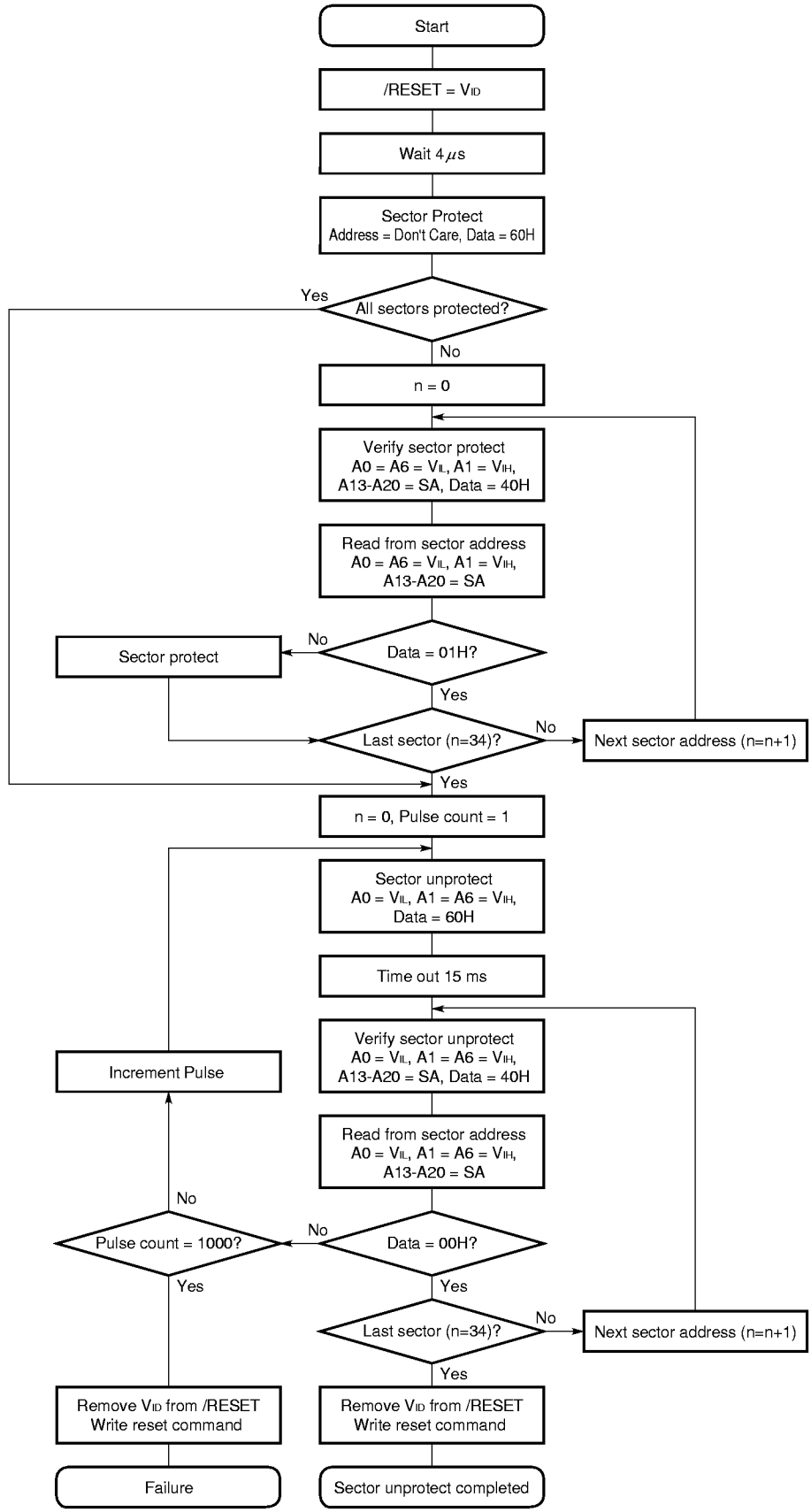
Sector unprotect is started by inputting V_{IL} to A0, V_{IH} to A1 and A6, and writing 60H to be unprotected input to A13 to A20. Following a timeout of 15 ms, sector unprotect is completed.

Unprotect verification must be performed for each sector.

The device enters the sector unprotect mode by inputting the sector address to A13 to A20 and writing 40H, with V_{IL} input to A0 and V_{IH} input to A1 and A6.

If reading is performed in this state, the sector unprotect verification result is output to I/O0. If the verified sector is unprotected, "0" is output to I/O0. If "0" is not output to I/O0, this means that unprotect failed, so perform sector unprotect again.

Figure 4-6. Sector Unprotect Flow Chart



5. Hardware Sequence Flags

The status of automatic program / erase operations can be determined from the status of the I/O2, I/O3, I/O5, I/O6, I/O7, and RY (/BY) pins.

Table 5-1. Hardware Sequence Flag

Status			I/O7[Note1]	I/O6[Note2]	I/O5[Note3]	I/O3	I/O2[Note1]	RY (/BY)
Progress	Program		/I/O7	Toggle	0	0	1	0
	Erase		0	Toggle	0	1	Toggle	0
	Erase suspend	Erase suspended sector	1	1	0	0	Toggle	1
		Non-erase suspended sector	Data	Data	Data	Data	Data	1
		Erase suspend program	/I/O7	Toggle	0	0	1	0
Exceeding time limits	Program		/I/O7	Toggle	1	0	1	0
	Erase		0	Toggle	1	1	N/A	0
	Erase suspend	Erase suspend program	/I/O7	Toggle	1	0	N/A	0

Notes 1. To read I/O7 or I/O2, a valid address must be input.

2. To read I/O6, any address can be used.

3. For I/O5, "1" is output if the automatic program / erase time exceeds the prescribed number of internal pulses.

5.1 I/O7 (Data Polling)

Data polling is a function to determine whether automatic program / erase is currently being performed by using I/O7.

Data polling is valid from the rise of the last /WE in the program / erase command sequence.

Whether automatic program is currently being executed can be determined by reading from the program destination addresses. When automatic program is in progress, the complement of the data programmed last is output. Upon completion of automatic program, the true value of the programmed data, not the complement, is output.

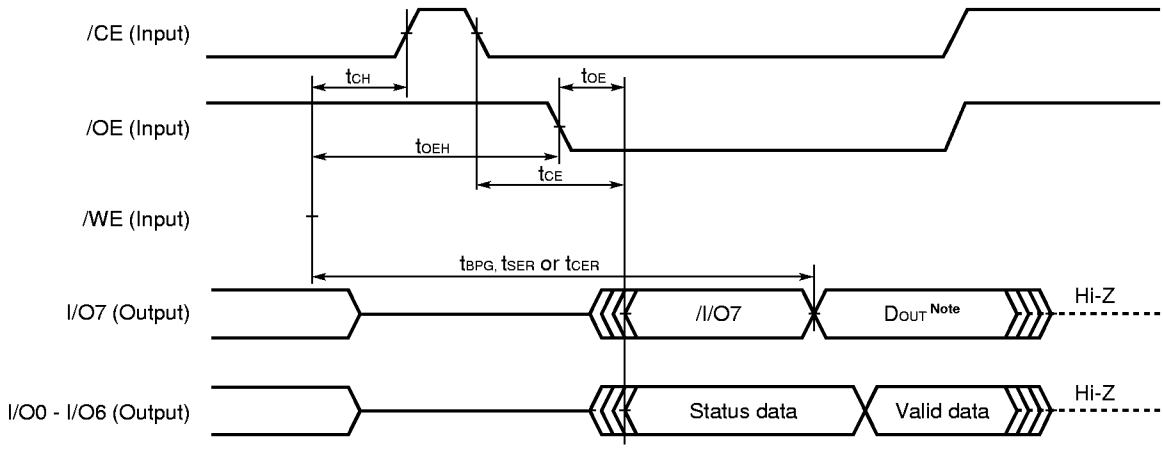
If write is performed to an address inside a protected sector, data polling is valid for approximately 1 μs, and then the device is reset to the read mode.

Whether automatic erase is in progress can be determined by reading from the addresses of the sector being erased. If erase is in progress, "0" is output to I/O7. When automatic erase is completed or suspended, "1" is output to I/O7.

During automatic erase, if all the selected sectors are protected, data polling is valid for approximately 100 μs. The device is then reset to the read mode. If the selected sectors include both protected and unprotected sectors, only unprotected sectors are erased, and protected sectors are ignored.

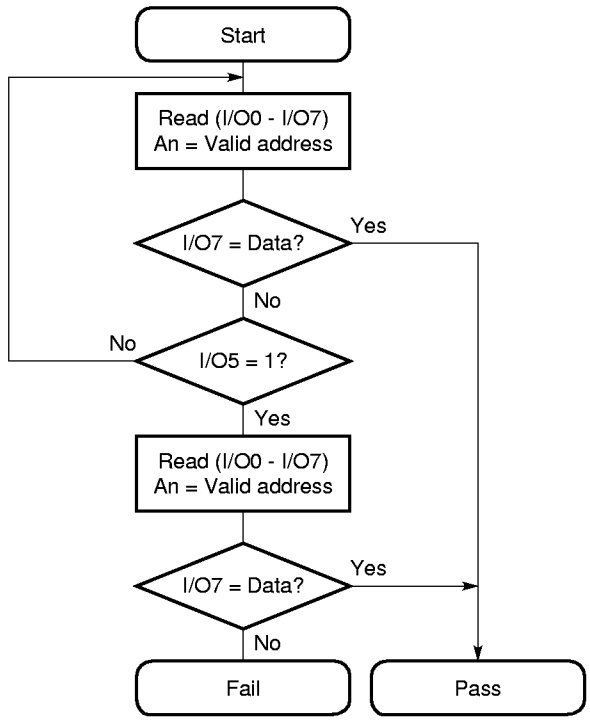
Upon completion of automatic program / erase, after the data output to I/O7 changes from the complement to the true value, I/O7 changes asynchronously like I/O0 to I/O6 while /OE is maintained at low level.

Figure 5-1. Data Polling Timing Chart



Note I/O7 = DOUT : True value of write data (indicates completion of automatic program / erase)

Figure 5-2. Data Polling Flow Chart



5.2 I/O6 (Toggle Bit)

The toggle bit is a function that uses I/O6 to determine whether automatic program / erase is in progress.

The toggle bit becomes valid from the rise of the last /WE in the program / erase command sequence.

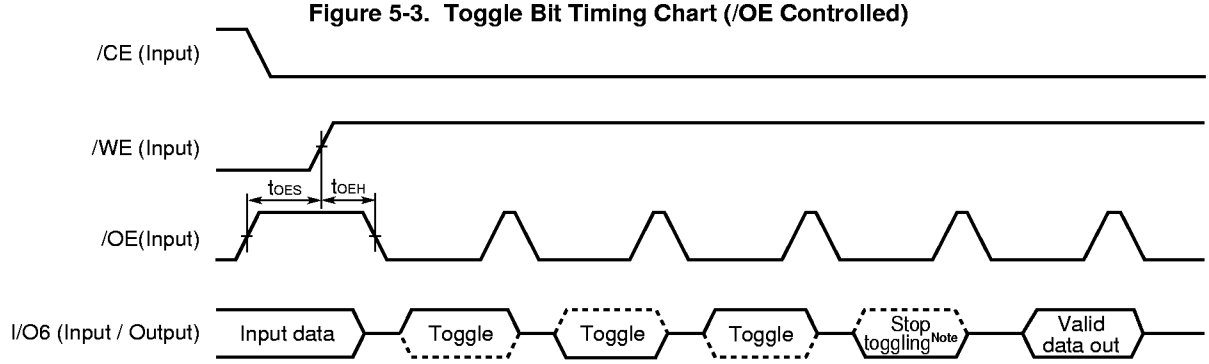
During automatic program / erase, I/O6 is toggled when continuous read is performed from any address. Upon automatic program / erase completion or suspend, I/O6 stops being toggled and outputs valid data for read. Continuous read control is performed with the /OE or /CE pins.

If program is performed for addresses inside a protected sector, I/O6 is toggled approximately 2 μs, and then the device is reset to the read mode.

Moreover, if all the sectors selected at the time of automatic erase are protected, I/O6 is toggled approximately 100 μs, and then the device is reset to the read mode. If the selected sectors include both protected and unprotected sectors, only unprotected sectors are erased, and protected sectors are ignored.

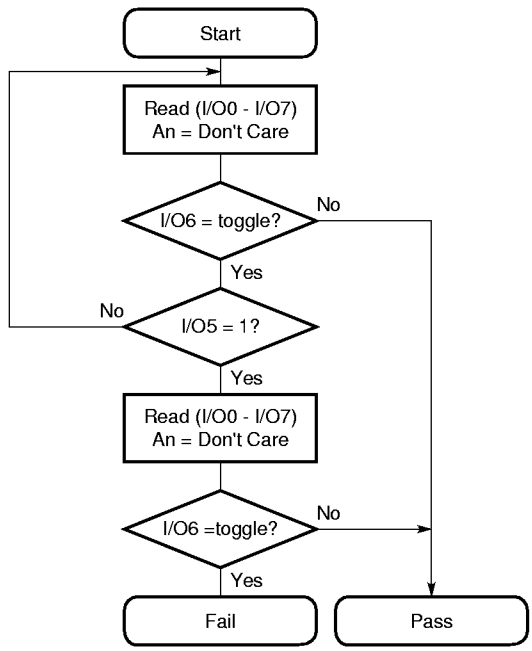
In this way, by using I/O6, it is possible to determine whether automatic erase is in progress (or suspended), but to determine which sector is being erased, I/O2 (toggle bit II) is used. See section **5.3 I/O2 (Toggle Bit II)**.

Figure 5-3. Toggle Bit Timing Chart (/OE Controlled)



Note I/O6 stops the toggle (indicates automatic program / erase completion).

Figure 5-4. Toggle Bit Flow Chart



5.3 I/O2 (Toggle Bit II)

Toggle bit II is a function that determines whether automatic erase (or erase suspend) is in progress for a particular sector by using I/O2.

I/O2 is toggled when continuous read is performed from addresses in a sector during automatic erase (or erase suspend). Either /OE or /CE is used to control continuous read.

When write to a sector that is not subject to erase suspend is attempted during erase suspend, read from sectors that are not subject to erase suspend cannot be performed until program is completed. In this case, if continuous read is performed from addresses in sectors that are not subject to erase suspend, "1" is not output to I/O2.

In this way, it is possible to determine whether automatic erase (including erase suspend) is in progress for sectors specified using I/O2, but whether the state is erase in progress or erase suspend cannot be determined with I/O2. To determine this, I/O6 (toggle bit) must be used. See section **5.2 I/O6 (Toggle Bit)**.

5.4 I/O5 (Exceeding Timing Limits)

If the program / erase time exceeds the prescribed number of pulses during automatic program / erase (exceeding timing limit), "1" is output to I/O5 and automatic program / erase failure is indicated.

Moreover, if overwriting "0" to "1" is attempted, the device judges data overwrite to be impossible, and "1" is output to I/O5 when the timing limit is exceeded.

When this happens, execute command reset.

5.5 I/O3 (Sector Erase Timer)

A 50 μs timeout period occurs following write with the sector erase command sequence before automatic erase starts.

During this timeout period, "0" is output to I/O3. When automatic erase starts upon completion of the timeout period, "1" is output to I/O3.

If sector erase is performed, first confirm whether the device has received a command by using I/O7 (data polling) or I/O6 (toggle bit). Then, using I/O3, check whether automatic erase has started. If I/O3 is "0", the timeout period is not over, and so it is possible to add sectors to erase. If I/O3 is "1", automatic erase starts and other commands (except erase suspend) are ignored until erase is completed.

If a sector to erase is added during the sector erase timeout period, it is recommended to check I/O3 prior to and following the addition. If I/O3 is "1" following the addition, that addition may not be accepted.

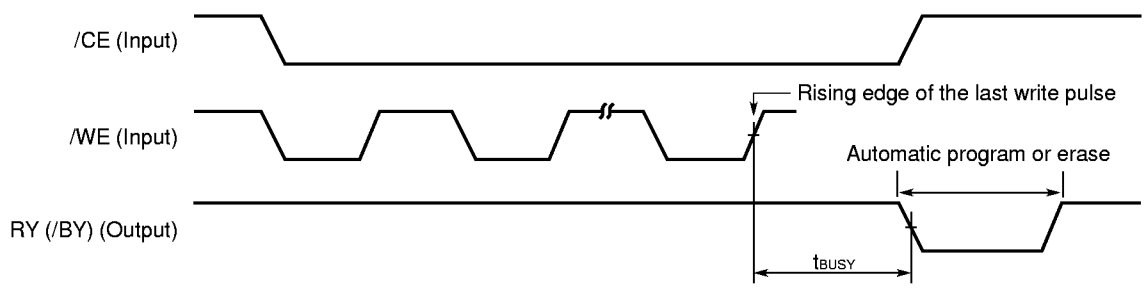
5.6 RY (/BY) (Ready / Busy)

The RY (/BY) pin is a dedicated output pin used to check whether automatic program / erase is in progress.

During automatic program / erase, "0" is output to the RY (/BY) pin. If "1" is output, this signifies that the device is either in the read mode (including erase suspend) or standby mode.

Since the RY (/BY) pin is an open-drain output pin, it is possible to connect several RY (/BY) pins in series by connecting a pull-up resistor to V_{CC}.

Figure 5-5. RY (/BY) (Ready / Busy) Timing Chart



6. Hardware Data Protection

This device requires two unlock cycles for program / erase command sequence to prevent illegal program / erase. Moreover, a hardware data protect function is provided as follows.

6.1 Low V_{CC} Write Inhibit

To prevent an illegal write cycle during V_{CC} transition, the command register and program / erase circuit is disabled and all write cycles are ignored while V_{CC} is V_{LKO} or lower. Write commands are ignored until V_{CC} becomes equal to or greater than V_{LKO}.

6.2 Logical Inhibit

The write cycle is inhibited under any of the following conditions : /OE = V_{IL}, /CE = V_{IH}, or /WE = V_{IH}. To start a write cycle, /CE = V_{IL} and /WE = V_{IL} must be set while /OE = V_{IH}.

6.3 Power-Up Write Inhibit

Even if /WE = /CE = V_{IL} and /OE = /V_{IH} are satisfied at power-up, no commands are accepted at the rising edge of /WE. The device is automatically reset to the read mode at power ON.

7. Electrical Characteristics

Absolute Maximum Ratings

Condition	Symbol	Test condition		Rating	Unit
Supply voltage	V_{CC}	with respect to GND		–0.5 to + 5.5	V
Input voltage	V_I	with respect to GND	except GND, A9, /RESET, /OE	–0.5[Note 1] to +5.5[Note 2]	V
			GND, A9, /RESET, /OE	–0.5[Note 1] to +13.5[Note 2]	
Output voltage	V_O	with respect to GND		–0.5[Note 1] to V_{CC} +0.5[Note 2]	V
Ambient operating temperature	T_A			0 to 70	°C
Storage temperature	T_{stg}			–65 to +125	°C
	T_{bias}	under bias		0 to 70	

Notes 1. –2.0 V (MIN.) (pulse width ≤ 20 ns)

2. V_{CC} + 2.0 V (MAX.) (pulse width ≤ 20 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	V_{IN} = 0 V		6.0	7.5	pF
Output capacitance	C_O	V_{OUT} = 0 V		8.5	12.0	pF

Recommended Operating Conditions

Parameter	Symbol	Test condition	μPD29F016L-Bxxx			μPD29F016L-Cxxx			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply voltage	V_{CC}		2.7		3.6	2.2		2.7	V
High level input voltage	V_{IH}		2.0		V_{CC}+0.3[Note 1]	0.7×V_{CC}		V_{CC}+0.3[Note 1]	V
	V_{ID}	High voltage is applied (A9, /RESET, /OE)	11.5		12.5	11.5		12.5	
Low level input voltage	V_{IL}		–0.5[Note 2]		+0.8	–0.5[Note 2]		+0.8	V
Ambient operating temperature	T_A		0		70	0		70	°C

Notes 1. V_{CC} + 0.6 V (MAX.) (pulse width ≤ 20 ns)

2. –0.6 V (MIN.) (pulse width ≤ 20 ns)

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter		Symbol	Test condition	μPD29F016L-Bxxx			μPD29F016L-Cxxx			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
High level output voltage		V_{OH1}	I_{OH} = –2.0 mA, V_{CC} = V_{CC} (MIN.)	2.4			0.85×V_{CC}			V
		V_{OH2}	I_{OH} = –100 μA, V_{CC} = V_{CC} (MIN.)	V_{CC}–0.4			V_{CC}–0.4			
Low level output voltage		V_{OL}	I_{OL} = 4.0 mA, V_{CC} = V_{CC} (MIN.)			0.45			0.45	V
Input leakage current		I_{LI1}	V_I = GND to V_{CC}, V_{CC} = V_{CC} (MAX.)	–1.0		+1.0	–1.0		+1.0	μA
	under high voltage	I_{LI2}	A9, /OE, /RESET = 12.5 V			35			35	
Output leakage current		I_{LO}	V_O = GND to V_{CC}, V_{CC} = V_{CC} (MAX.)	–1.0		+1.0	–1.0		+1.0	μA
Power supply current	Read	I_{CC1}	/CE = V_{IL}, /OE = V_{IH}, Cycle = 5 MHz, I_{OUT} = 0 mA		7	12		7	12	mA
	Program, Erase	I_{CC2}	/CE = V_{IL}, /OE = V_{IH}		20	30			30	mA
	Standby	I_{CC3}	V_{CC} = V_{CC} (MAX.), /CE = V_{CC} ± 0.3 V, /RESET = V_{CC} ± 0.3 V, /OE = V_{IL}		0.2	5		0.075	5	μA
	Standby, Reset	I_{CC4}	V_{CC} = V_{CC} (MAX.), /RESET = GND ± 0.2 V		0.2	5		0.075	5	μA
	Automatic sleep mode	I_{CC5}	V_{IH} = V_{CC} ± 0.2 V, V_{IL} = GND ± 0.2 V		0.2	5		0.075	5	μA
Low V_{CC} lock-out voltage[Note]		V_{LKO}		2.3		2.5	1		1.5	V

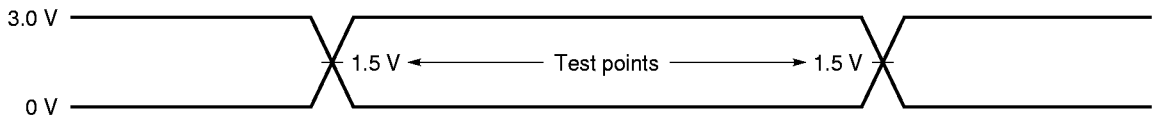
Note When V_{CC} is equal to or lower than V_{LKO}, the device ignores all write cycles. See section **6.1 Low V_{CC} Write Inhibit**.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

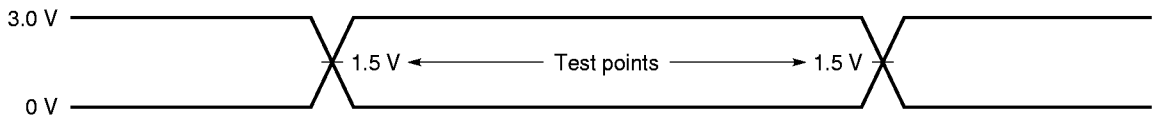
AC Test Conditions

[μPD29F016L-Bxxx]

Input Waveform (Rise and Fall Time ≤ 5 ns)

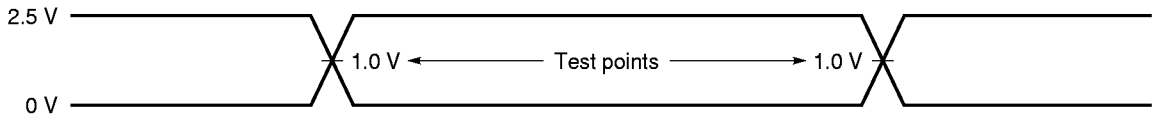


Output Waveform

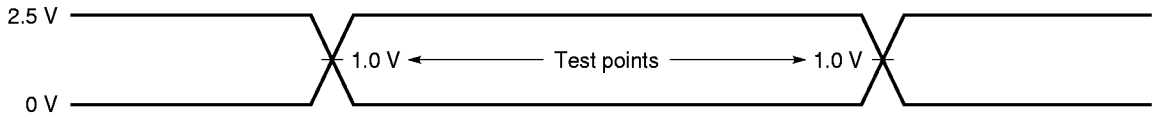


[μPD29F016L-Cxxx]

Input Waveform (Rise and Fall Time ≤ 5 ns)

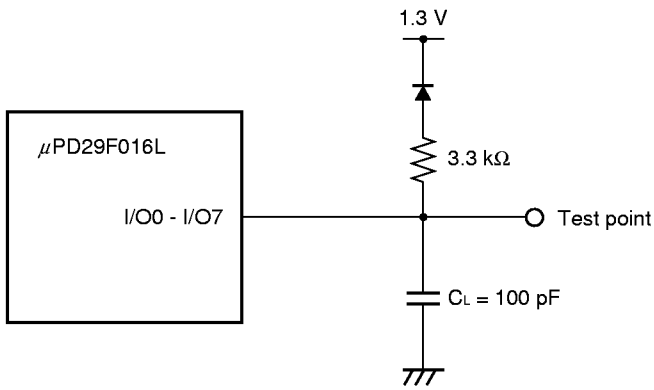


Output Waveform



[μPD29F016L-Bxxx, Cxxx]

Output Load



Remark C_L includes capacitance of the probe and jig, and stray capacitances.

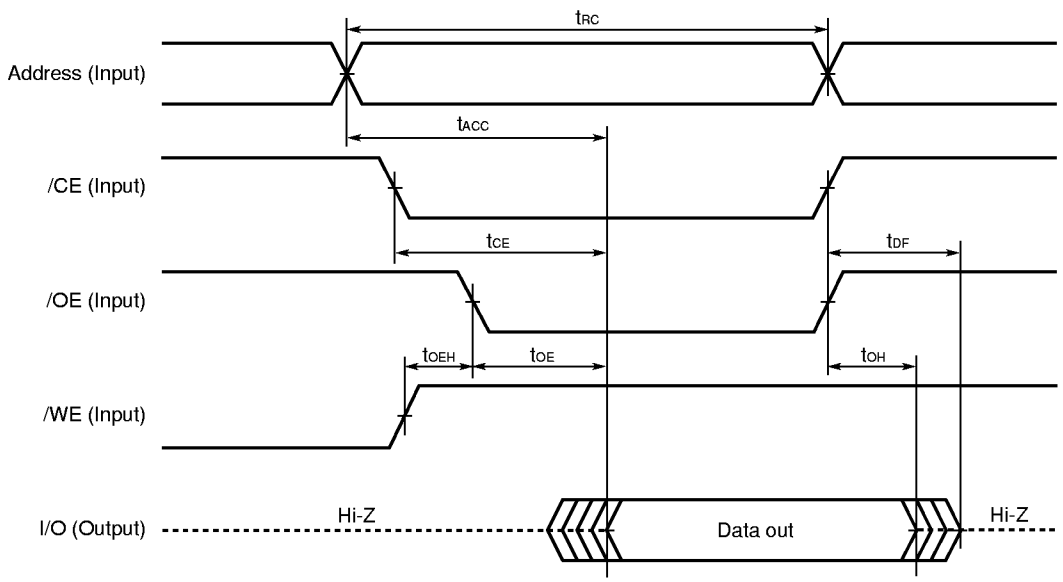
Read Cycle

Parameter	Symbol	μPD29F016L -B90x		μPD29F016L -B10x		μPD29F016L -B12x		μPD29F016L -C12x		μPD29F016L -C15x		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	90		100		120		120		150		ns	
Address access time	t_{ACC}		90		100		120		120		150	ns	1
/CE access time	t_{CE}		90		100		120		120		150	ns	2
/OE access time	t_{OE}		35		40		50		50		55	ns	
Output disable time	t_{DF}		30		30		30		30		40	ns	
Output hold time	t_{OH}	0		0		0		0		0		ns	
/RESER pulse width	t_{RP}	500		500		500		500		500		ns	
/RESET hold time before read	t_{RH}	500		500		500		500		500		ns	
/RESET pin low to read mode	t_{READY}		20		20		20		20		20	μs	

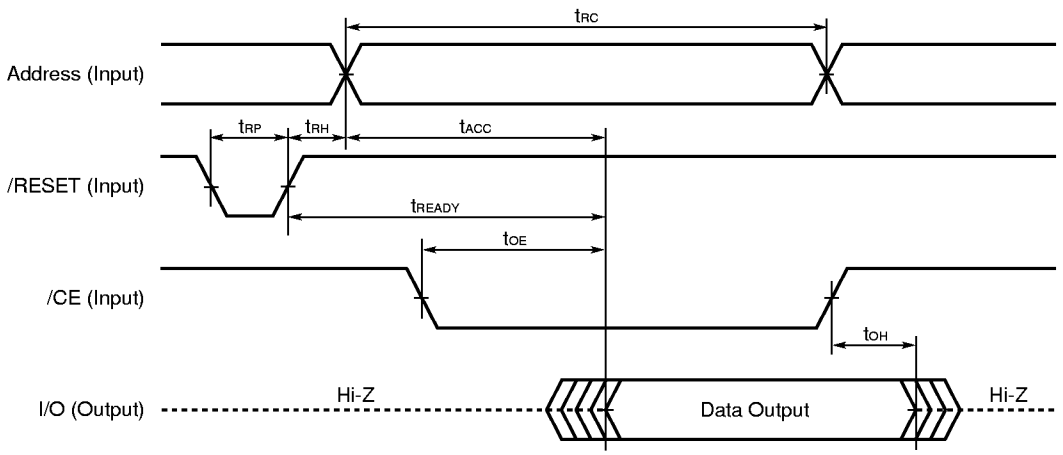
Note 1. /CE = /OE = V_{IL}

2. /OE = V_{IL}

Read Cycle Timing Chart 1



Read Timing Chart 2



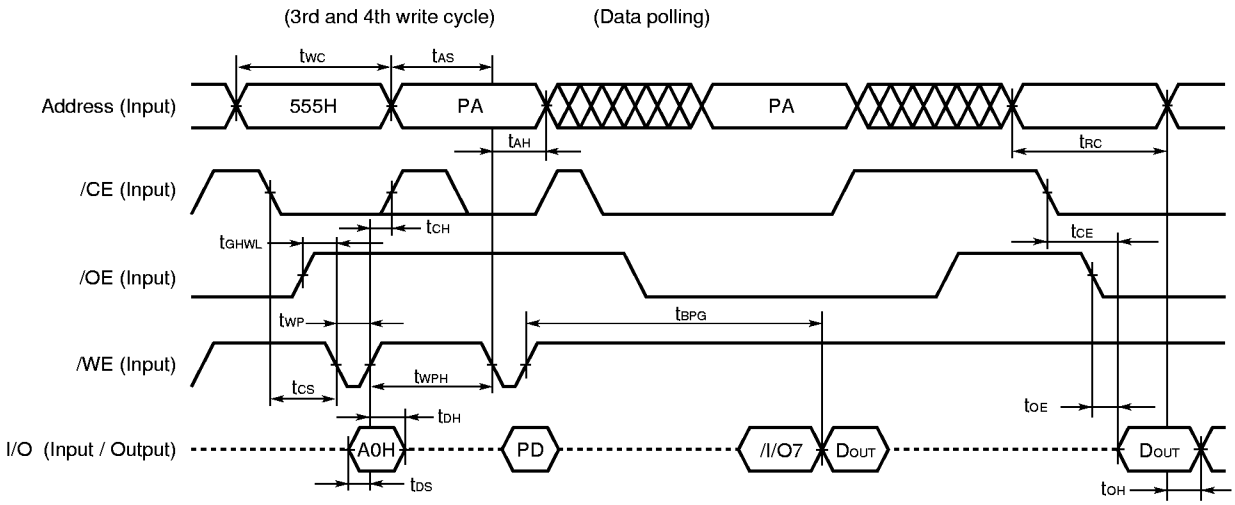
Write Cycle (Program / Erase) (/WE Controlled)

Parameter		Symbol	μPD29F016L -B90x			μPD29F016L -B10x			μPD29F016L -B12x			μPD29F016L -C12x			μPD29F016L -C15x			Unit	Note
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Write cycle time		t_{WC}	90			100			120			120			150			ns	
Address setup time		t_{AS}	0			0			0			0			0			ns	
Address hold time		t_{AH}	45			50			50			65			65			ns	
Data setup time		t_{DS}	45			50			50			65			65			ns	
Data hold time		t_{DH}	0			0			0			0			0			ns	
/OE setup time		t_{OES}	0			0			0			0			0			ns	
/OE hold time	Read	t_{OEH}	0			0			0			0			0			ns	
	Toggle bit, Data poling		10			10			10			10			10			ns	
Read recovery time before write (/OE high to /WE low)		t_{GHWL}	0			0			0			0			0			ns	
/CE setup time		t_{CS}	0			0			0			0			0			ns	
/CE hold time		t_{CH}	0			0			0			0			0			ns	
Write pulse width		t_{WP}	35			50			50			65			65			ns	
Write pulse width high		t_{WPH}	30			30			30			35			35			ns	
Vcc setup time		t_{VCS}	50			50			50			50			50			μs	
Voltage transition time		t_{VLHT}	4			4			4			4			4			μs	1
Write pulse width during sector protect		t_{WPP}	100			100			100			100			100			μs	1
/OE setup time for valid /WE		t_{OESP}	4			4			4			4			4			μs	1
/CE setup time for valid /WE		t_{CSP}	4			4			4			4			4			μs	1
RY (/BY) recovery time		t_{RB}	0			0			0			0			0			ns	
/RESET pulse width		t_{RP}	500			500			500			500			500			ns	
/RESET hold time before read		t_{RH}	500			500			500			500			500			ns	
RY (/BY) delay time from /RESET low		t_{RRB}	20			20			20			20			20			μs	
RY (/BY) delay time from valid program or erase operation		t_{BUSY}	90			90			90			90			90			ns	
Byte programming operation time		t_{BPG}		9	500		9	500		9	500		9	500		9	500	μs	
Chip programming operation time		t_{CPG}		19	200		19	200		19	200		19	200		19	200	s	
Sector erase operation time		t_{SER}		1	10		1	10		1	10		1	10		1	10	s	2
Chip erase operation time		t_{CER}		35			35			35			35			35		s	2

Notes 1. Sector protect only.

2. The preprogramming time prior to the erase operation is not included.

Write Cycle Timing Chart (/WE Controlled)



Remarks 1. This timing chart shows the last two write cycles among the write command sequence's four write cycles, and data polling.

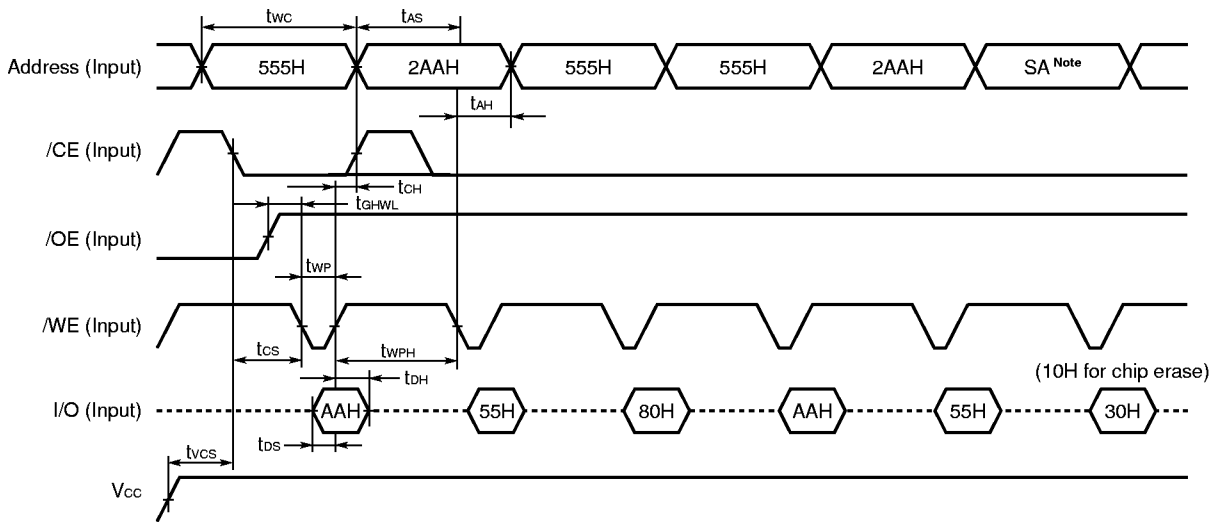
2. PA : Program address

PD : Program data

/I/O7 : The output of the complement of the data written to the device.

DOUT : The output of the data written to the device.

Sector / Chip Erase Timing Chart



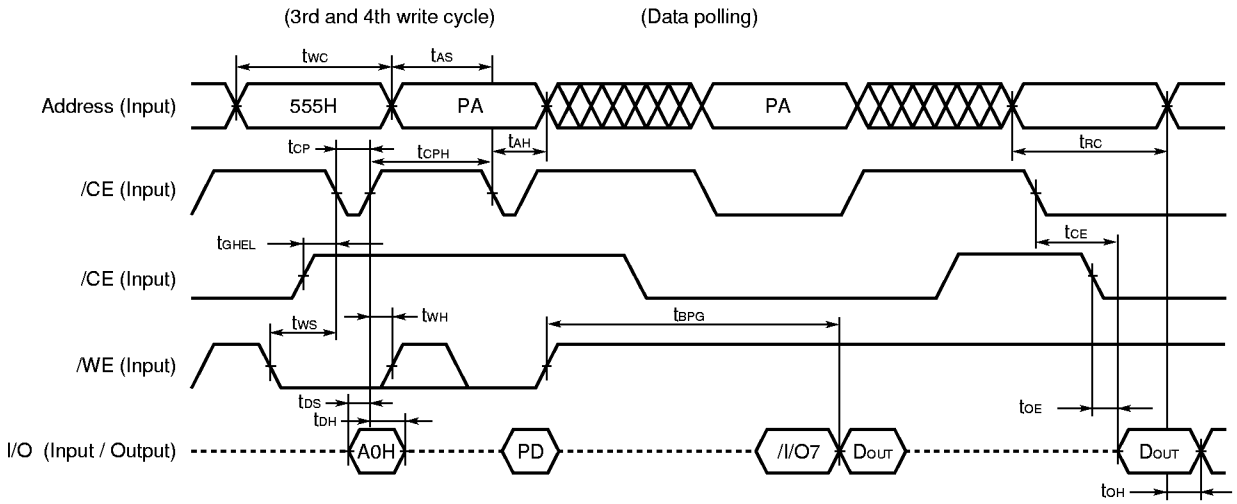
Note SA is the sector address to be erased. In the case of chip erase, input 555H.

Write Cycle (Program / Erase) (/CE Controlled)

Parameter		Symbol	μPD29F016L -B90x			μPD29F016L -B10x			μPD29F016L -B12x			μPD29F016L -C12x			μPD29F016L -C15x			Unit	Note
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Write cycle time		t_{WC}	90			100			120			120			150			ns	
Address setup time		t_{AS}	0			0			0			0			0			ns	
Address hold time		t_{AH}	45			50			50			65			65			ns	
Data setup time		t_{DS}	45			50			50			65			65			ns	
Data hold time		t_{DH}	0			0			0			0			0			ns	
/OE setup time		t_{OES}	0			0			0			0			0			ns	
/OE hold time	Read	t_{OEH}	0			0			0			0			0			ns	
	Toggle bit, Data poling		10			10			10			10			10			ns	
Read recovery time before write (/OE high to /CE low)		t_{GHEL}	0			0			0			0			0			ns	
/WE setup time		t_{WS}	0			0			0			0			0			ns	
/WE hold time		t_{WH}	0			0			0			0			0			ns	
Write pulse width		t_{CP}	35			50			50			65			65			ns	
Write pulse width high		t_{CPH}	30			30			30			35			35			ns	
Byte programming operation time		t_{BPG}		9	500		9	500		9	500		9	500		9	500	μs	
Chip programming operation time		t_{CPG}		19	200		19	200		19	200		19	200		19	200	s	
Sector erase operation time		t_{SER}		1	10		1	10		1	10		1	10		1	10	s	1
Chip erase operation time		t_{CER}		35			35			35			35			35		s	1

Notes 1. The preprogramming time prior to the erase operation is not included.

Write Cycle Timing Chart (/CE Controlled)



Remarks 1. This timing chart shows the last two write cycles among the write command sequence's four write cycles, and data polling.

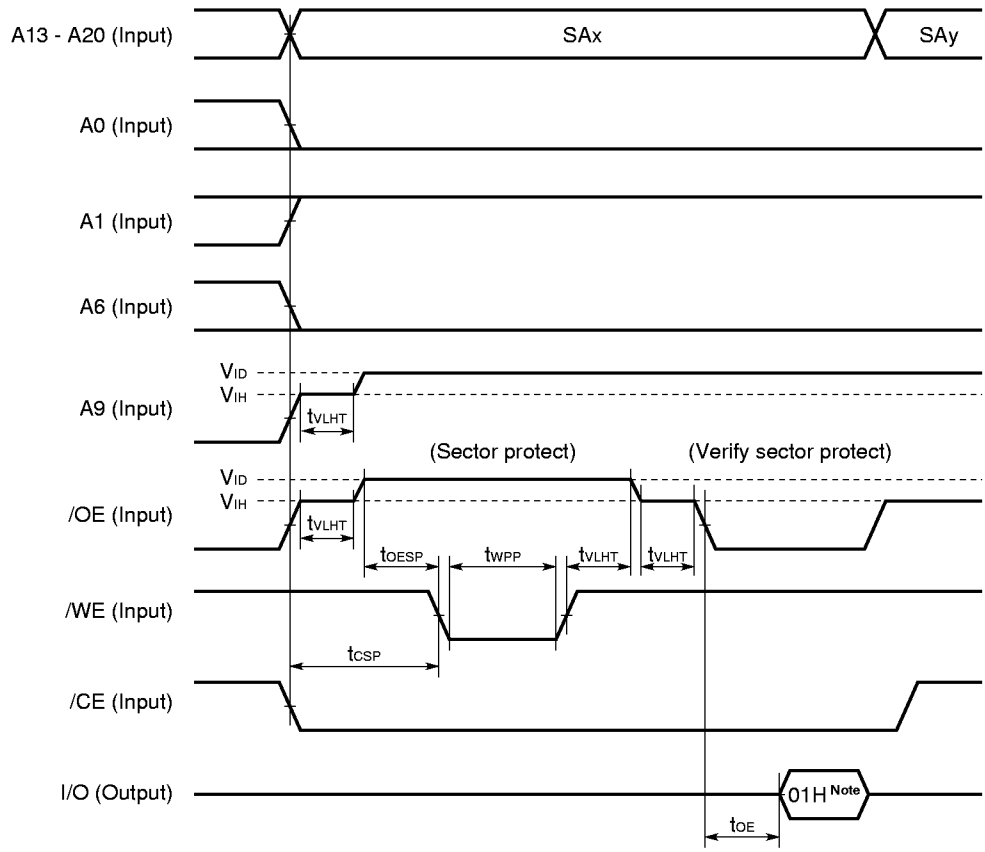
2. PA : Program address

PD : Program data

/I/O7 : The output of the complement of the data written to the device.

DOUT : The output of the data written to the device.

Sector Protect Timing Chart



Remark SAx : First sector address

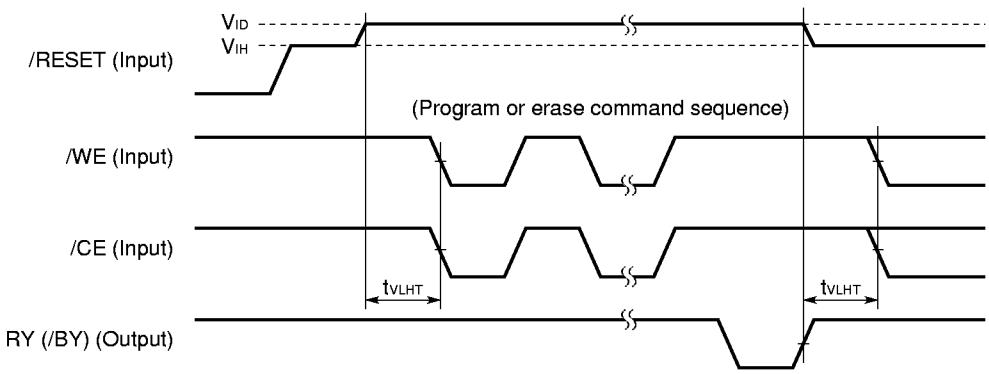
SAy : Next sector address

Note The sector protect verification result is output.

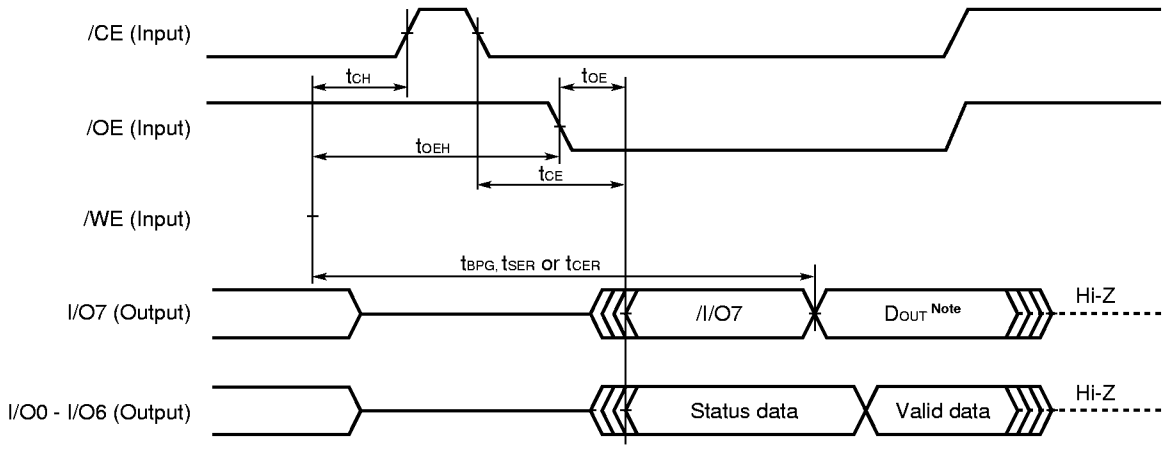
01H : The sector is protected.

00H : The sector is not protected.

Temporary Sector Unprotect Timing Chart

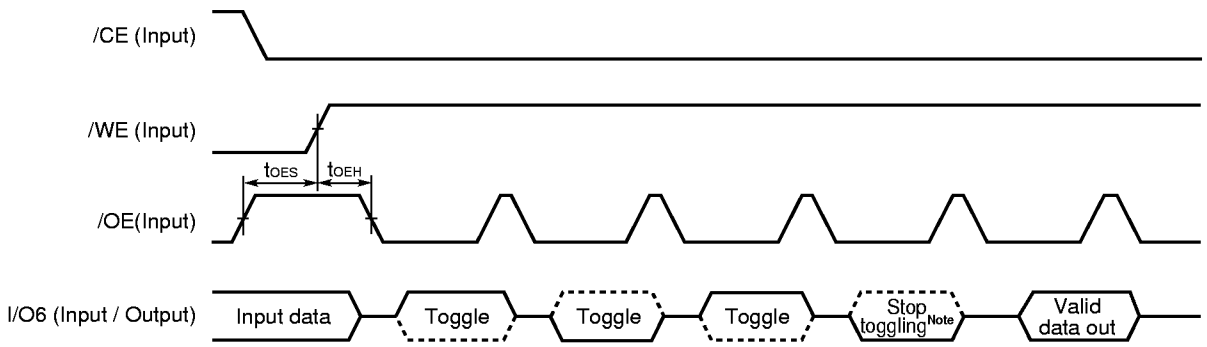


Data Polling during Automatic Program / Erase Operations Timing Chart



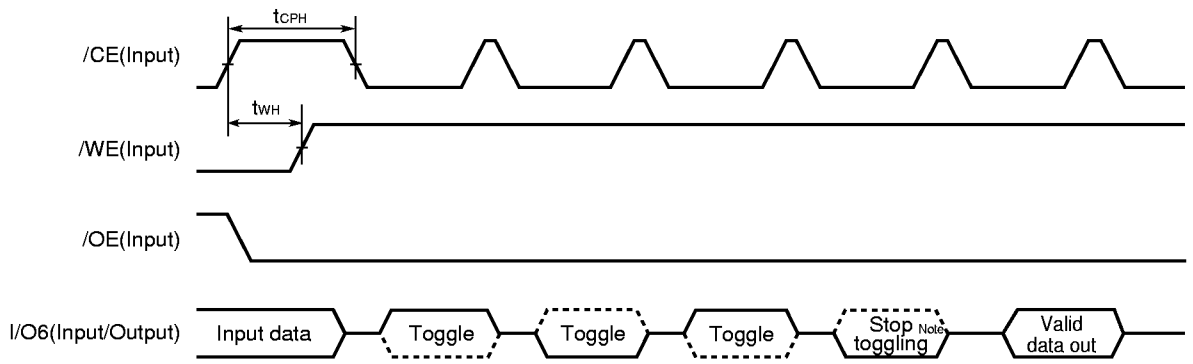
Note I/O7 = DOUT : True value of write data (indicates automatic program / erase completion)

Toggle Bit during Automatic Program / Erase Operations Timing Chart (/OE Controlled)



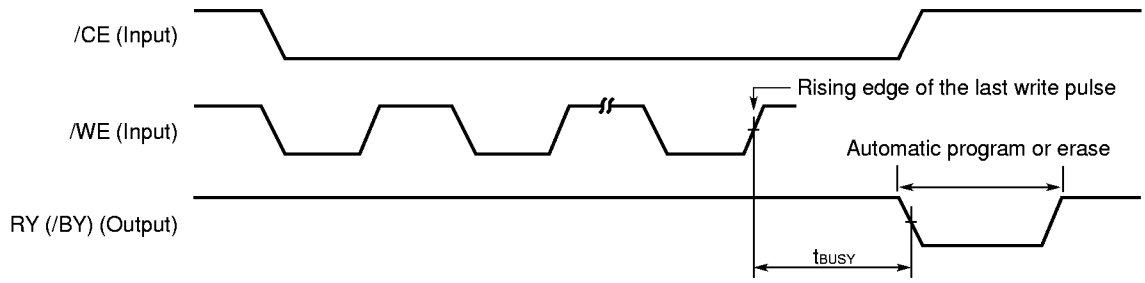
Note I/O6 stops toggle (indicates automatic program / erase completion)

Toggle Bit during Automatic Program / Erase Operations Timing Chart (/CE Controlled)

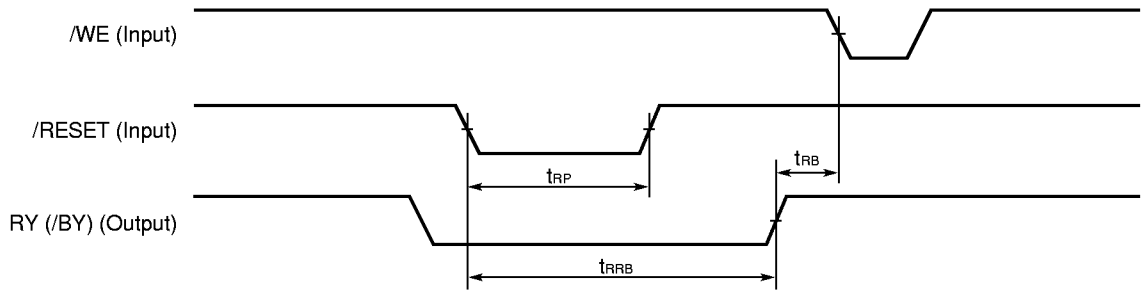


Note I/O6 stops toggle (indicates automatic program / erase completion)

RY (/BY) during Write / Erase Operations Timing Chart

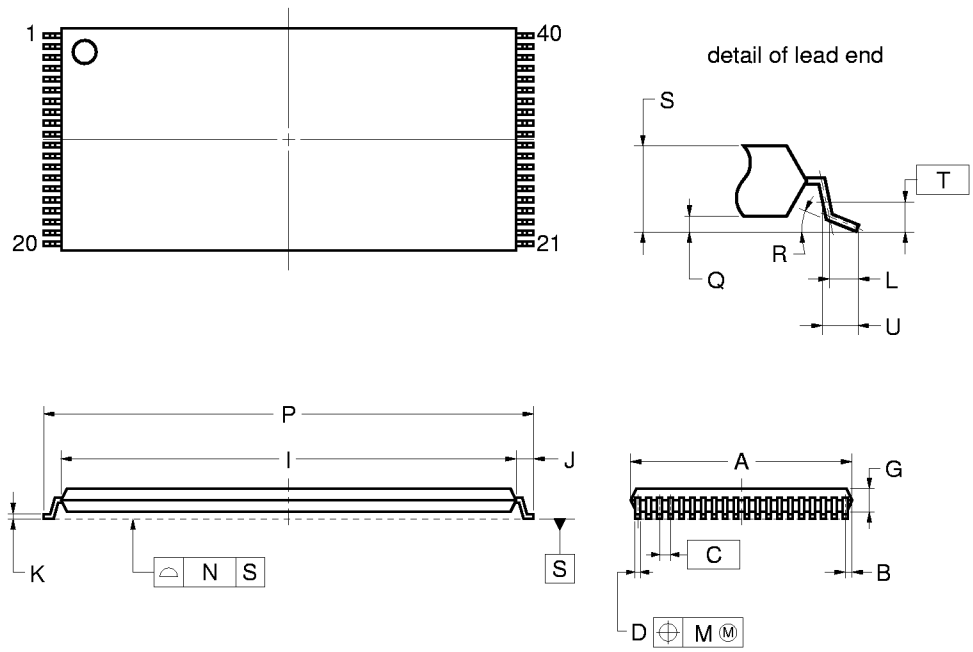


Reset / RY (BY) Timing Chart



8. Package Drawing

40 PIN PLASTIC TSOP(I) (10x20)



NOTES

1. Controlling dimention —— millimeter.
2. Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.
3. "A" excludes mold flash. (Includes mold flash : 10.4 mm MAX. <0.410 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	10.0±0.1	$0.394^{+0.004}_{-0.005}$
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.22±0.05	$0.009^{+0.002}_{-0.003}$
G	0.97±0.05	$0.038^{+0.003}_{-0.002}$
I	18.4±0.1	$0.724^{+0.005}_{-0.004}$
J	0.8±0.1	$0.031^{+0.005}_{-0.004}$
K	0.145±0.05	$0.006^{+0.004}_{-0.002}$
L	0.5	0.020
M	0.10	0.004
N	0.10	0.004
P	20.0±0.2	$0.787^{+0.009}_{-0.008}$
Q	0.1±0.05	$0.004^{+0.002}_{-0.003}$
R	$3°^{+5°}_{-3°}$	$3°^{+5°}_{-3°}$
S	1.2 MAX.	0.047 MAX.
T	0.25	0.010
U	0.6±0.15	$0.024^{+0.006}_{-0.007}$

S40GZ-50-LJH1

9. Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD29F016L.

Type of Surface Mount Device

μPD29F016LGZ-LJH : 40-pin plastic TSOP (I) (10 × 20 mm) (Normal bent)

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.