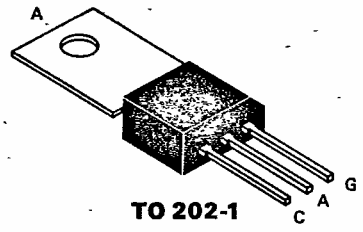
TAG SEMICONDUCTORS LTD



TO 202-1

X0402BE – X0402NE SCR'S

4.0 A 200–800 V <200 µA

The X0402 series silicon controlled rectifiers are high performance PNPN devices diffused with TAG's proprietary Top Glass™ Process. These parts are intended for general purpose applications where gate sensitivity is required.

Absolute Maximum Ratings $T_A = 25\,°C$ unless otherwise noted

Parameter	Part Nr.	Symbol	Min.	Max.	Unit	Test Conditions
Repetitive Peak Off State Voltage	X0402BE		200		V	
	X0402DE	V_{DRM}	400		V	$T_j = -40\,°C$ to $125\,°C$
	X0402ME	V_{RRM}	600		V	$R_{GK} = 1\,K\Omega$
	X0402NE		800		V	
On-State Current		$I_{T(RMS)}$	4.0		A	All Conduction Angles $T_C = 85\,°C$
Average On-State Current		$I_{T(AV)}$	2.5		A	Half Cycle, $\Theta = 180°$, $T_C = 85\,°C$
Nonrept. On-State Current		I_{TSM}	33		A	Half Cycle, 60 Hz
Nonrept. On-State Current		I_{TSM}	30		A	Half Cycle, 50 Hz
Fusing Current		I^2t	4.5		A^2s	t = 10 ms, Half Cycle
Peak Reverse Gate Voltage		V_{GRM}	8		V	$I_{GR} = 10\,\mu A$
Peak Gate Current		I_{GM}	1.2		A	10µs max.
Peak Gate Dissipation		P_{GM}	3		W	10µs max.
Gate Dissipation		$P_{G(AV)}$	0.2		W	20 ms max.
Operating Temperature		T_j	−40	125	°C	
Storage Temperature		T_{stg}	−40	150	°C	
Soldering Temperature		T_{sld}		250	°C	1.6 mm from case, 10 s max.

Electrical Characteristics $T_A = 25\,°C$ unless otherwise noted

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Off-State Leakage Current	I_{DRM}/I_{RRM}		0.2	mA	@$V_{DRM} + V_{RRM}$, $R_{GK} = 1\,K\Omega$, $T_j = 125\,°C$
Off-State Leakage Current	I_{DRM}/I_{RRM}		5	µA	@$V_{DRM} + V_{RRM}$, $R_{GK} = 1\,K\Omega$, $T_j = 25\,°C$
On-State Voltage	V_T		2.11	V	at $I_T = 8\,A$, $T_j = 25\,°C$
On-State Threshold Voltage	$V_{T(TO)}$		1.05	V	$T_j = 125\,°C$
On-State Slope Resistance	r_T		150	mΩ	$T_j = 125\,°C$
Gate Trigger Current	I_{GT}		200	µA	$V_D = 7\,V$
Gate Trigger Voltage	V_{GT}		0.8	V	$V_D = 7\,V$
Holding Current	I_H		5	mA	$R_{GK} = 1\,K\Omega$
Latching Current	I_L		6	mA	$R_{GK} = 1\,K\Omega$
Critical Rate of Voltage Rise	dv/dt	30		V/µs	$V_D = .67 \times V_{DRM}$ $R_{GK} = 1\,K\Omega$ $T_j = 125\,°C$
Critical Rate of Current Rise	di/dt	50		A/µs	$I_G = 10\,mA$ $di_G/dt = 0.1\,A/\mu s$ $T_j = 125\,°C$
Gate Controlled Delay Time	t_{gd}		2	µs	$I_G = 10\,mA$ $di_G/dt = 0.1\,A/\mu s$
Commutated Turn-Off Time	t_q		50	µs	$T_C = 85\,°C$ $V_D = .67 \times V_{DRM}$ $V_R = 35\,V$ $I_T = I_{T(AV)}$
Thermal Resistance junc. to case	$R_{\Theta jc}$		7.5	K/W	
Thermal Resistance junc. to amb.	$R_{\Theta ja}$		75	K/W	