AAT1142

800mA Voltage-Scaling Step-Down Converter

SwitchReg™

General Description

The AAT1142 SwitchReg is a dynamically programmable 2.2MHz step-down converter with an input voltage range of 2.7V to 5.5V and output from 0.6V to 2.0V. Its low supply current, high level of integration, and small footprint make the AAT1142 the ideal choice for microprocessor core power in systems such as smartphones.

The 2.2MHz switching frequency allows the use of a small external inductor and capacitors. Peak current mode control and internal compensation provide stable operation and fast voltage response without over/undershoot or ringing.

The AAT1142 delivers up to 800mA of output current while consuming 35µA of typical no load quiescent current. Dynamic Voltage Management is provided through I²C or AnalogicTech's S²Cwire™ (Simple Serial Control™) single wire interface. The user can program the output from 0.6V to 2.0V in 50mV steps.

The AAT1142 optimizes power efficiency throughout the load range via PWM/PFM mode. Pulling the MODE/SYNC pin high enables PWM Only mode, maintaining constant frequency and low noise across the operating range. Alternatively, the converter may be synchronized to an external clock input via the MODE/SYNC pin. Over-temperature and short-circuit protection safeguard the AAT1142 and system components from damage.

The AAT1142 is available in a Pb-free, space-saving 2.85x3.0x1.0mm TSOPJW-12 package or a Pb-free, low-profile 3x3x0.8mm TDFN33-12 package. The device is rated over the -40°C to +85°C temperature range.

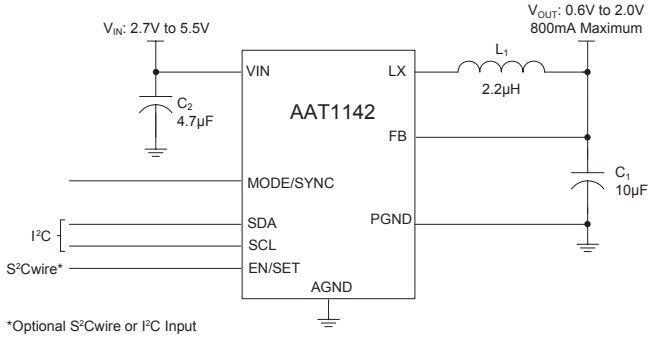
Features

- V_{IN} Range: 2.7V to 5.5V
- V_{OUT} Programmable Range: 0.6V to 2.0V
- Dynamic Voltage Management:
  - 50mV Output Resolution
  - Fast, Stable Response
- Serial Control Options:
  - I²C Two-Wire Interface
  - S²Cwire Single-Wire Interface
- 800mA Output Current
- Up to 93% Efficiency
- Line, Load Regulation Less Than ±0.5%
- 2.2MHz Switching Frequency
- Ultra-Small External Filter
- Low 35µA No Load Quiescent Current
- 100% Duty Cycle Low Dropout Operation
- Internal Soft Start
- Over-Temperature Protection
- Current Limit Protection
- Multi-Function MODE/SYNC Pin:
  - PFM/PWM for High Efficiency
  - PWM Only for Low Noise
  - Clock Input to Synchronize to System Clock
- TSOPJW-12 or TDFN33-12 Package
- Temperature Range: -40°C to +85°C

Applications

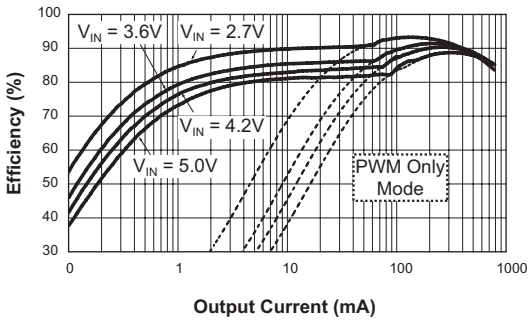
- Camcorders
- Cellular Phones and Smartphones
- Digital Still Cameras
- Handheld Instruments
- Microprocessor / DSP Core
- MP3, Portable Music, and Portable Media Players
- PDAs and Handheld Computers

Typical Application



*Optional S²Cwire or I²C Input

Efficiency vs. Load
(V_{OUT} = 1.8V)

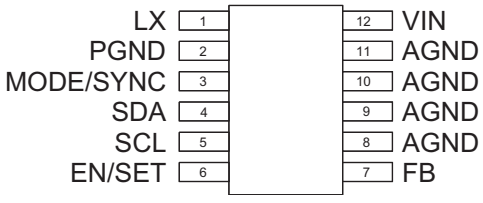


Pin Descriptions

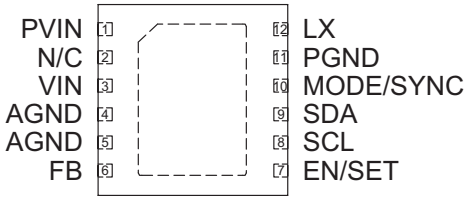
Pin # TSOPJW-12	Pin # TDFN33-12	Symbol	Function
1	12	LX	Connect the output inductor to this pin. The switching node is internally connected to the drain of both high- and low-side MOSFETs.
2	11	PGND	Main power ground return pin. Connect to the output and input capacitor return.
3	10	MODE/SYNC	Connect to ground for PFM/PWM mode and optimized efficiency throughout the load range. Connect to high for low noise PWM Only operation under all operating conditions. Connect to an external clock for synchronization (PWM Only).
4	9	SDA	I²C control pin: Data input.
5	8	SCL	I²C control pin: Clock input.
6	7	EN/SET	IC enable pin. Pull high to enable the AAT1142; pull low to disable the AAT1142. Also serves as S²Cwire input for programmable output voltages.
7	6	FB	Feedback input pin. This pin is connected directly to the converter output for programmable output.
8, 9, 10, 11	4, 5	AGND	Ground connection pin.
12[1]	3	VIN	Input voltage for the converter.
12[1]	1	PVIN	Input voltage for the power switches.
n/a	2	N/C	Not connected.
n/a	EP		Exposed paddle (bottom); connect to ground as closely as possible to the device.

Pin Configuration

TSOPJW-12
(Top View)



TDFN33-12
(Top View)



1. VIN and PVIN are tied together in the TSOPJW-12 package.

Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{IN}, PV_{IN}	Input Voltage and Input Power to GND	6.0	V
V_{LX}	LX to GND	-0.3 to V_{IN} + 0.3	V
V_{FB}	FB to GND	-0.3 to V_{IN} + 0.3	V
$V_{SDA/SCL}$	SDA/SCL to GND	-0.3 to 6.0	V
$V_{MODE/SYNC}$, $V_{EN/SET}$	MODE/SYNC and EN/SET to GND	-0.3 to 6.0	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Thermal Information[2]

Symbol	Description		Value	Units
P_D	Maximum Power Dissipation	TSOPJW-12[3]	625	mW
		TDFN33-12[4]	2.0	W
θ_{JA}	Thermal Resistance	TSOPJW-12	160	°C/W
		TDFN33-12	50	

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board.
3. Derate 6.25mW/°C above 25°C.
4. Derate 20mW/°C above 25°C.

Electrical Characteristics[1]

L = 2.2µH, C_{IN} = C_{OUT} = 10µF, V_{IN} = 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Step-Down Converter						
V_{IN}	Input Voltage		2.7		5.5	V
V_{UVLO}	UVLO Threshold	V_{IN} Rising			2.7	V
		Hysteresis		250		mV
		V_{IN} Falling	2.0			V
V_{OUT}	Output Voltage Tolerance	I_{OUT} = 0mA to 800mA, V_{IN} = 2.7V to 5.5V	-3.0		3.0	%
V_{OUT}	V_{OUT} Programmable Range		0.6		2.0	V
V_{SLEW}	Output Voltage Programming Slew Rate	C_{OUT} = 10µF		10		mV/µs
I_Q	Quiescent Current	No Load		35	70	µA
I_{SHDN}	Shutdown Current	EN/SET = AGND = PGND			1.0	µA
I_{LIM}	P-Channel Current Limit			1.0		A
$R_{DS(ON)H}$	High Side Switch On Resistance			0.29		Ω
$R_{DS(ON)L}$	Low Side Switch On Resistance			0.24		Ω
I_{LXLEAK}	LX Leakage Current	V_{IN} = 5.5V, V_{LX} = 0V to V_{IN}			1	µA
$\Delta V_{OUT}/V_{OUT}*\Delta V_{IN}$	Line Regulation	V_{IN} = 2.7V to 5.5V		0.2		%/V
R_{OUT}	Output Impedance		250			kΩ
T_S	Start-Up Time	From Enable to Output Regulation		100		µs
F_{OSC}	Oscillator Frequency			2.2		MHz
F_{SYNC}	SYNC Frequency Range		1.0		3.0	MHz
T_{SD}	Over-Temperature Shutdown Threshold			140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C

1. The AAT1142 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.

Electrical Characteristics[1]

L = 2.2µH, C_{IN} = C_{OUT} = 10µF, V_{IN} = 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
EN/SET and MODE/SYNC						
$V_{EN/SET(L)}$	Enable Threshold Low				0.6	V
$V_{EN/SET(H)}$	Enable Threshold High		1.4			V
$T_{EN/SET(L)}$	EN/SET Low Time	$V_{EN/SET}$ < 0.6V	0.3		75	µs
$T_{EN/SET(H)}$	EN/SET High Time	$V_{EN/SET}$ > 1.4V		50	75	µs
T_{OFF}	EN/SET Timeout	$V_{EN/SET}$ < 0.6V			500	µs
T_{LATCH}	EN/SET Latch Timeout	$V_{EN/SET}$ > 1.4V			500	µs
$I_{EN/SET}$	Input Low Current	V_{IN} = V_{FB} = 5.5V	-1.0		1.0	µA
$V_{MODE/SYNC(L)}$	Enable Threshold Low				V_{IN} × 0.4	V
$V_{MODE/SYNC(H)}$	Enable Threshold High		V_{IN} × 0.7			V
$I_{MODE/SYNC}$	Input Low Current		-1.0		1.0	µA

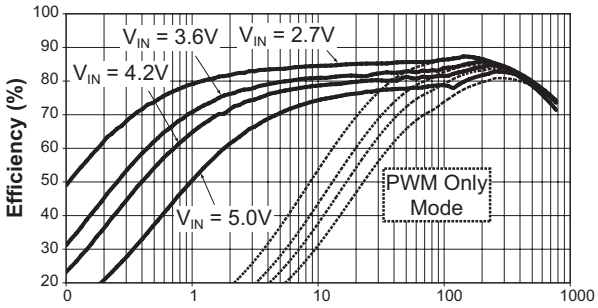
Characteristics of SDA and SCL Bus Lines

Parameter	Symbol	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
SCL Clock Frequency	f_{SCL}		100		400	kHz
Hold Time for START Condition; After this Period, the First Clock Pulse is Generated	$t_{HD;STA}$	4.0		0.6		µs
LOW Period of the SCL Clock	t_{LOW}	4.7		1.3		µs
HIGH Period of the SCL Clock	t_{HIGH}	4.0		0.6		µs
Set-up Time for a Repeated START Condition	$t_{SU;STA}$	4.7		0.6		µs
Data in Hold Time	$t_{HD;DAT}$	0	3.45	0	0.9	µs
Data in Set-Up Time	$t_{SU;DAT}$	350		350		ns
Set-Up Time for STOP Condition	$t_{SU;STO}$	4.0		0.6		µs
Bus Free Time Between a STOP and START Condition	t_{BUF}	4.7		1.3		µs
Input Low Level	V_{IL}		V_{IN} · 0.3		V_{IN} · 0.3	V
Input High Level	V_{IH}	V_{IN} · 0.7		V_{IN} · 0.7		V

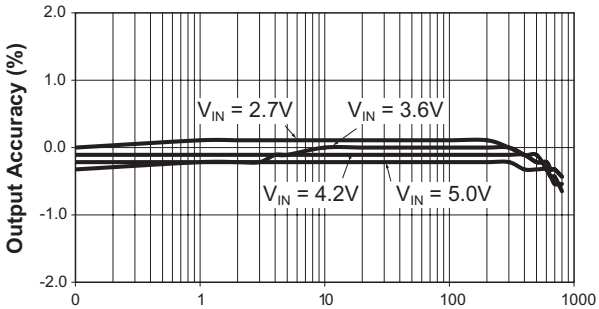
1. The AAT1142 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.

Typical Characteristics

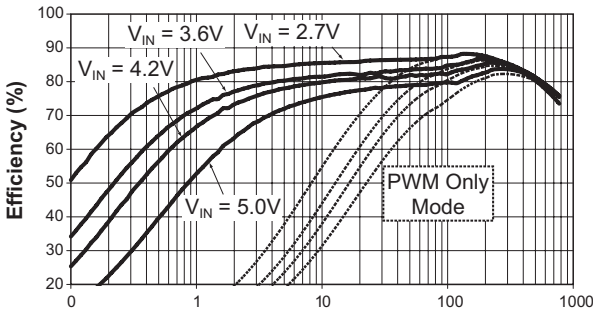
Efficiency vs. Load
(V_{OUT} = 0.9V)



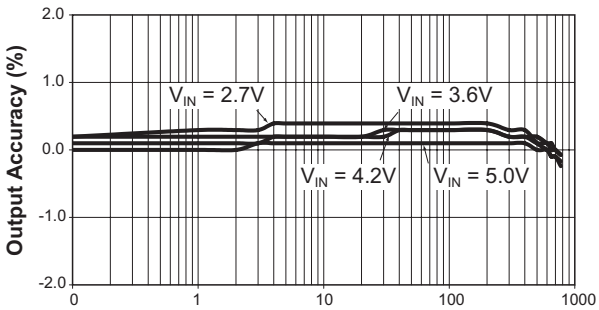
DC Regulation
(V_{OUT} = 0.9V)



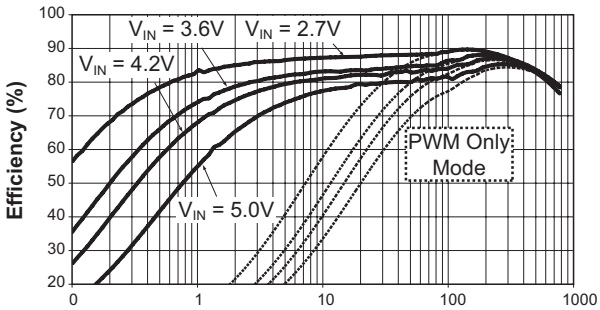
Efficiency vs. Load
(V_{OUT} = 1.0V)



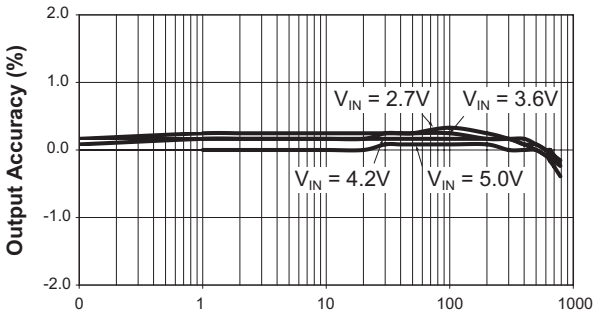
DC Regulation
(V_{OUT} = 1.0V)



Efficiency vs. Load
(V_{OUT} = 1.2V)

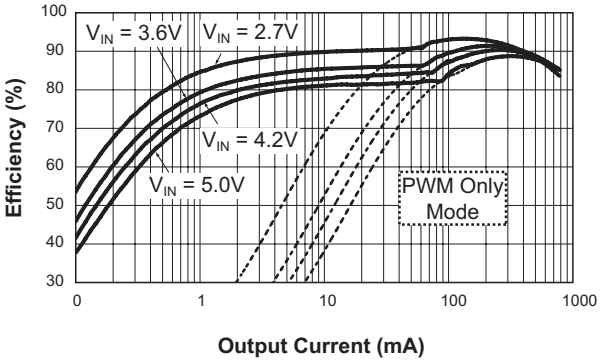


DC Regulation
(V_{OUT} = 1.2V)

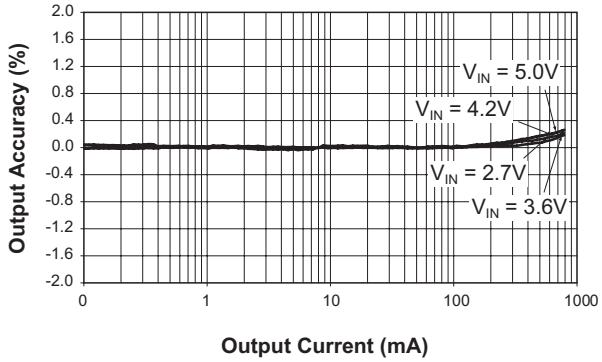


Typical Characteristics

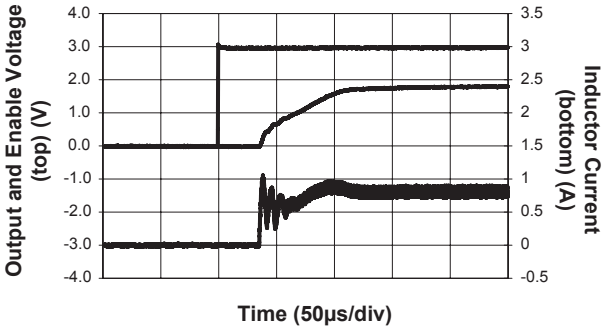
Efficiency vs. Load
(V_{OUT} = 1.8V)



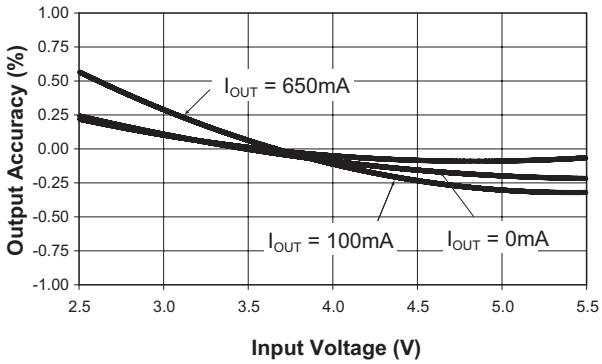
DC Regulation
(V_{OUT} = 1.8V)



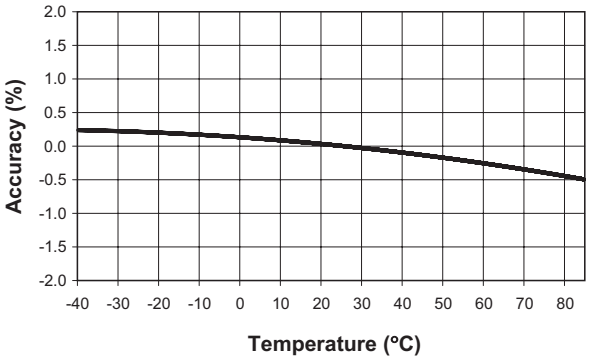
Soft Start
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 800mA)



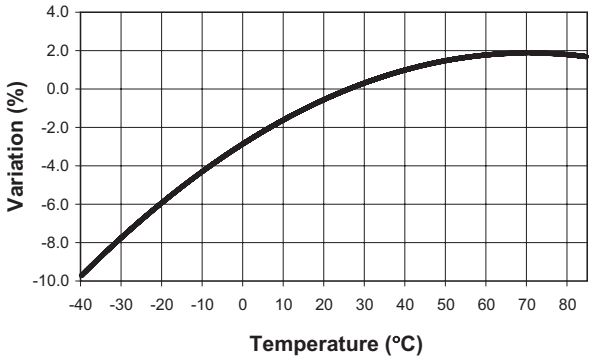
Line Regulation
(V_{OUT} = 1.0V)



Output Voltage Accuracy vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 1.0V; I_{OUT} = 400mA)

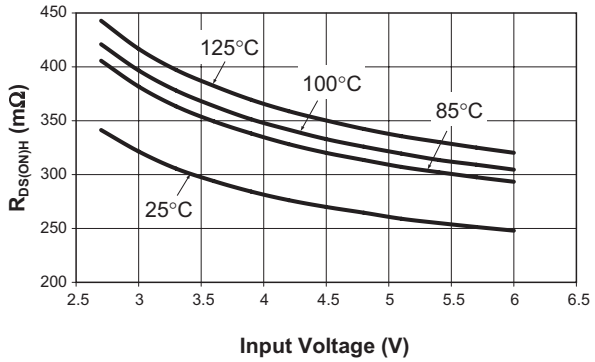


Switching Frequency vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 1.0V; I_{OUT} = 400mA)

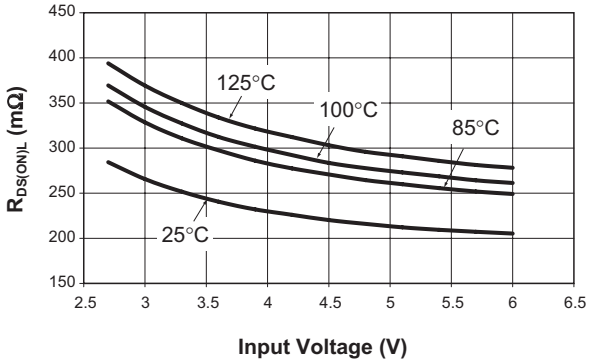


Typical Characteristics

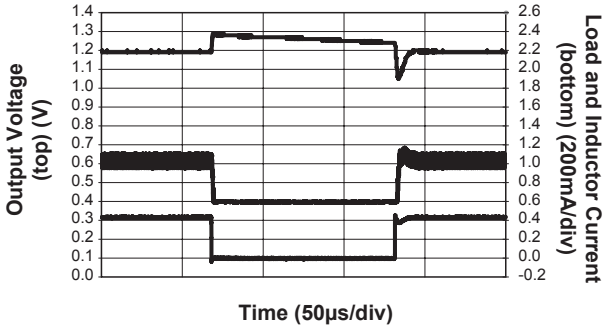
P-Channel $R_{DS(ON)}$ vs. Input Voltage



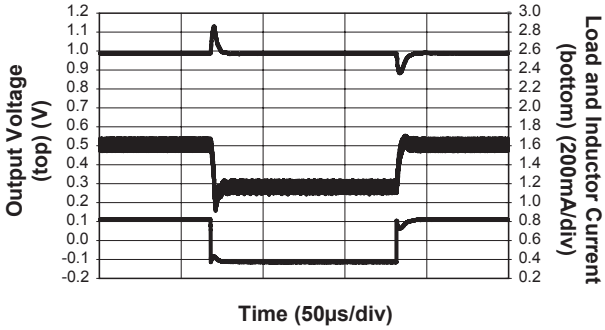
N-Channel $R_{DS(ON)}$ vs. Input Voltage



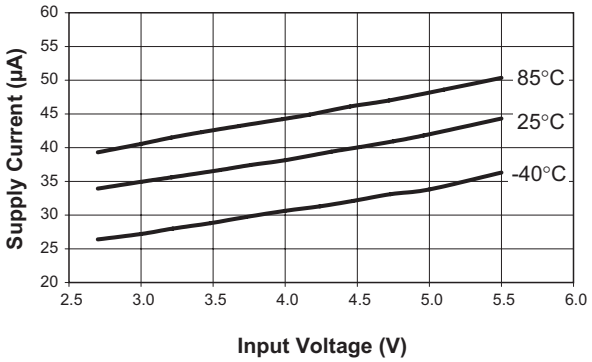
Load Transient Response
(10mA to 400mA; V_{IN} = 3.6V; V_{OUT} = 1.2V)



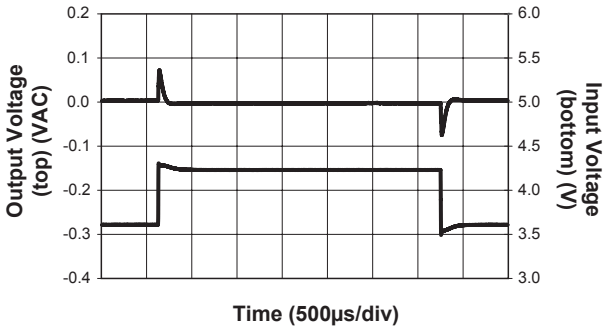
Load Transient Response
(400mA to 800mA; V_{IN} = 3.6V; V_{OUT} = 1.0V)



No Load Quiescent Current vs. Input Voltage
(V_{OUT} = 1.8V)

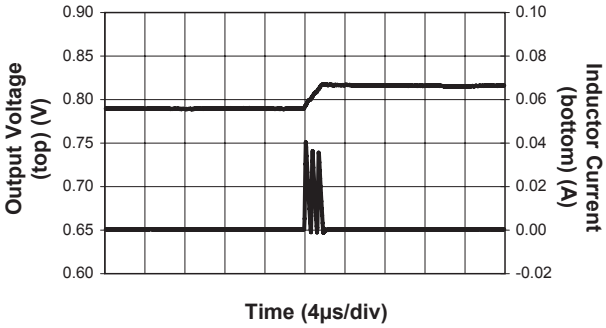


Line Response
(V_{OUT} = 1.2V; I_{OUT} = 650mA)

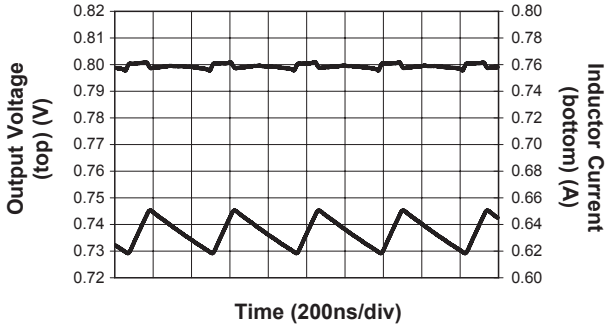


Typical Characteristics

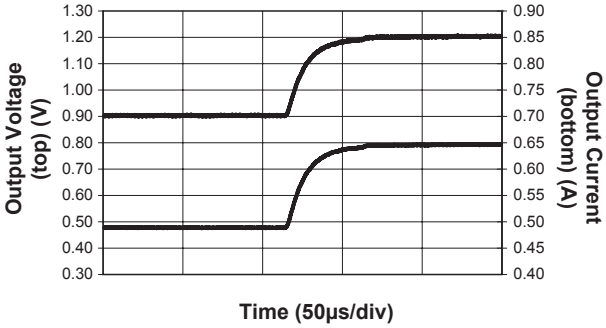
Output Ripple
(V_{IN} = 4.2V; V_{OUT} = 0.8V; No Load)



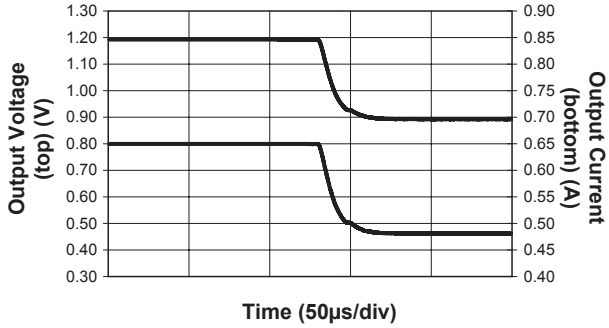
Output Ripple
(V_{IN} = 4.2V; V_{OUT} = 0.8V; I_{OUT} = 650mA)



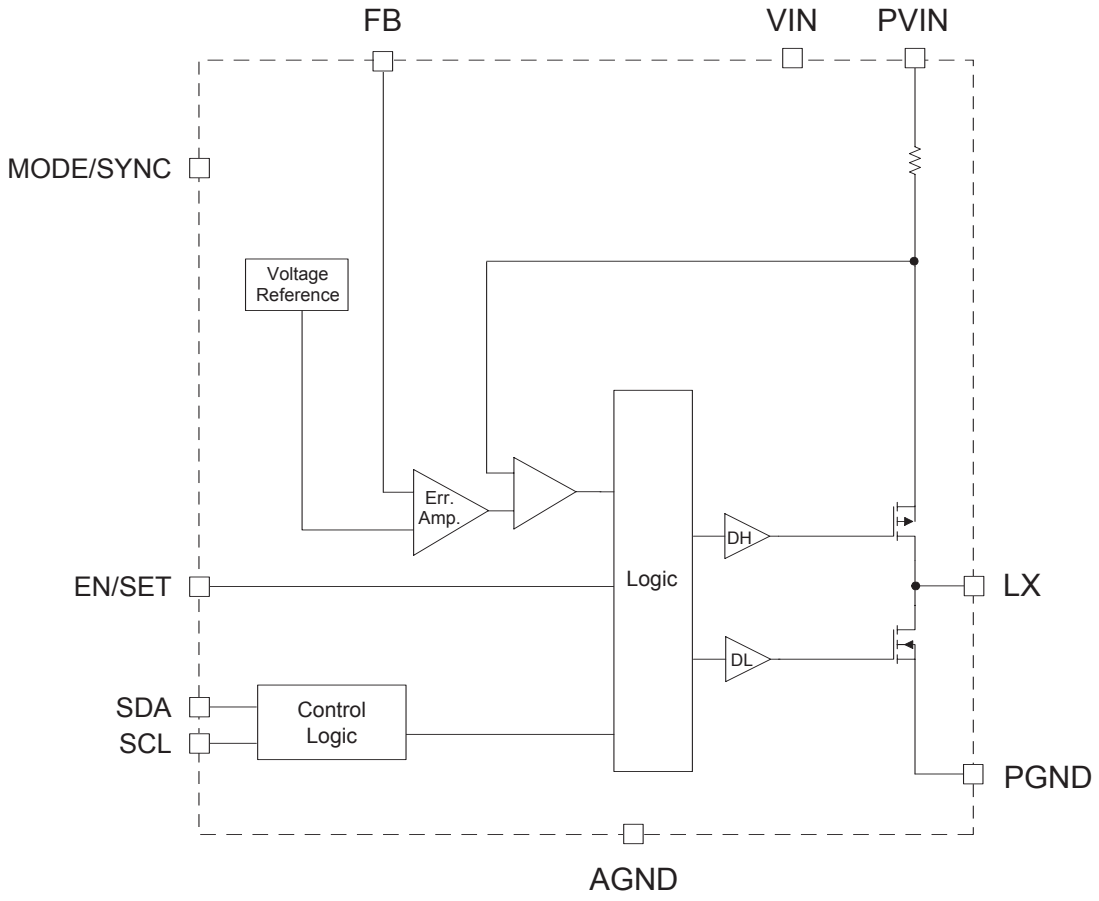
Output Programming Step from 0.9V to 1.2V
(V_{IN} = 3.6V; R_{OUT} = 1.85Ω)



Output Programming Step from 1.2V to 0.9V
(V_{IN} = 3.6V; R_{OUT} = 1.85Ω)



Functional Block Diagram



Functional Description

The AAT1142 is a high performance, 800mA step-down converter with an input voltage range from 2.7V to 5.5V. The AAT1142 uses Dynamic Voltage Management, which allows the system host to quickly set the output voltage through the integrated I²C or S²Cwire interface. Through this interface, the host can change the output voltage to track processor idle and active states, greatly extending battery life without degrading system performance. I²C provides an industry-standard, dual-line interface, while S²Cwire provides a single-line, high-speed serial interface.

The 2.2MHz switching frequency allows the use of small external components. Only three external components are needed to program the output from 0.6V to 2.0V. Typically, one 4.7µF capacitor, one 10µF capacitor, and one 2.2µH inductor are required.

The integrated low-loss MOSFET switches provide up to 93% efficiency. PFM operation maintains high efficiency under light load conditions (typically <50mA). Pulling the MODE/SYNC pin high allows optional PWM Only low noise mode. This maintains constant frequency and low output ripple across all load conditions. Alternatively, the IC can be synchronized to an external clock via the MODE/SYNC input. External synchronization can be maintained between 1MHz and 3MHz.

At low input voltages, the converter dynamically adjusts the operating frequency prior to dropout to maintain the required duty cycle and provide accu-

rate output regulation. Output regulation is maintained until the dropout voltage, or minimum input voltage, is reached.

The AAT1142 achieves better than ±0.5% output regulation across the input voltage and output load range. Maximum continuous load is 800mA. A current limit of 1A (typical) protects the IC and system components from short-circuit damage. Typical no load quiescent current is 35µA.

Thermal protection completely disables switching when the maximum junction temperature is detected. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once an over-temperature or over-current fault condition is removed, the output voltage automatically recovers.

Peak current mode control and optimized internal compensation provide high loop bandwidth and excellent response to input voltage and fast load transient events. The output voltage is stable across all operating conditions, ensuring fast transitions with no overshoot or ringing. Soft start eliminates output voltage overshoot when the enable or the input voltage is applied. Under-voltage lockout prevents spurious start-up events.

Control Loop

The AAT1142 is a peak current mode step-down converter. The current through the P-channel MOSFET (high side) is sensed for current loop control, as well as short-circuit and overload protection. A fixed slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The peak current mode loop appears as a voltage-programmed current source in parallel with the output capacitor.

The output of the voltage error amplifier programs the current mode loop for the necessary peak switch current to force a constant output voltage for all load and line conditions. Internal loop compensation terminates the transconductance voltage error amplifier output. Loop stability and fast transient response are maintained across the entire input and output voltage range with a small 2.2µH output inductor and 10µF output capacitor.

Soft Start/Enable

Soft start limits the current surge seen at the input and eliminates output voltage overshoot. When pulled low, the enable input forces the AAT1142 into a low-power, non-switching state. The total input current during shutdown is less than 1µA. The turn-on time from EN to output regulation is 100µs (typical).

Alternatively, the EN/SET pin serves as the input for S^2Cwire single line control. Details of S^2Cwire operation and timing diagrams are provided in the Applications Information section of this datasheet.

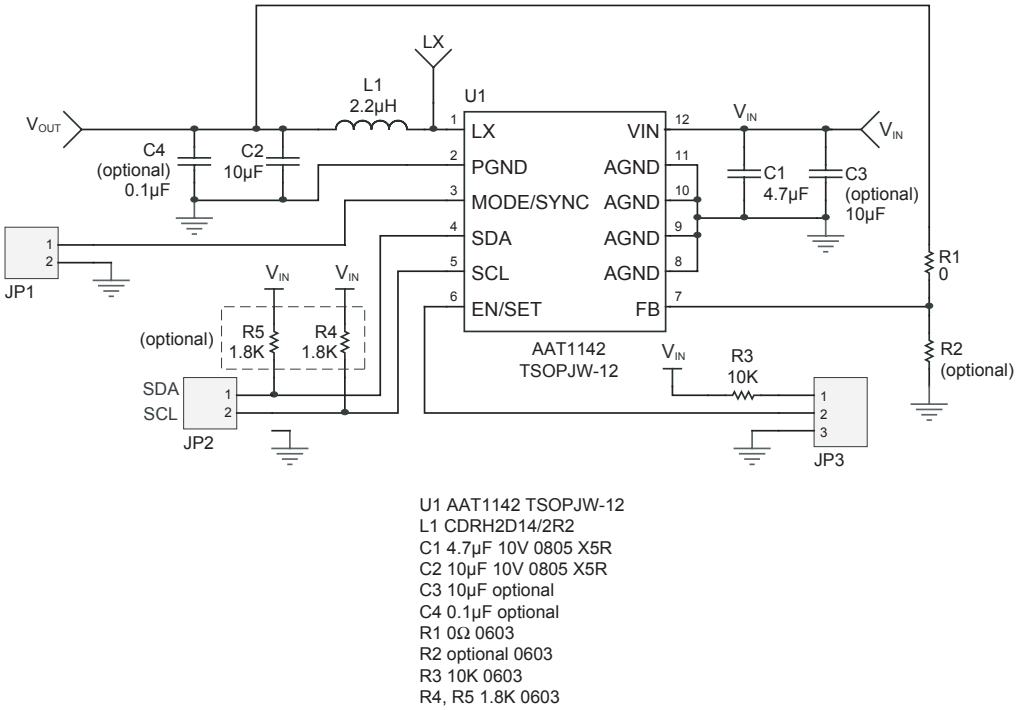
Current Limit and Over-Temperature Protection

Switching is terminated after entering current limit for a series of pulses to minimize power dissipation and stresses under overload and short-circuit conditions. Switching is terminated for seven consecutive clock cycles after a current limit has been sensed for a series of four consecutive clock cycles.

Thermal protection completely disables switching when internal dissipation becomes excessive. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once an over-temperature or over-current fault condition is removed, the output voltage automatically recovers.

Under-Voltage Lockout

Internal bias of all circuits is controlled via the VIN input. Under-voltage lockout (UVLO) guarantees sufficient V_{IN} bias and proper operation of all internal circuitry prior to activation.



U1 AAT1142 TSOPJW-12
L1 CDRH2D14/2R2
C1 4.7µF 10V 0805 X5R
C2 10µF 10V 0805 X5R
C3 10µF optional
C4 0.1µF optional
R1 0Ω 0603
R2 optional 0603
R3 10K 0603
R4, R5 1.8K 0603

Figure 1: AAT1142 Evaluation Board Schematic.

Applications Information

The AAT1142 output voltage may be programmed from 0.6V to 2.0V through I²C or S²Cwire serial interface. When using I²C or S²Cwire, the output voltage can be programmed across the entire output voltage range or in increments as small as ±50mV (see Figure 2).

I²C Serial Interface

The AAT1142 is compatible with the I²C interface, which is a widely used two-line serial interface. The I²C two-wire communications bus consists of SDA and SCL lines. SDA provides data, while SCL provides clock input. SDA data consists of an address bit sequence followed by a data bit sequence. SDA data transfer is synchronized to SCL rising clock edges.

When using the I²C interface, EN/SET is pulled high to enable the output or low to disable the output. To ensure a disable event, the EN/SET pulse width must be greater than the latch time (500µs maximum).

The I²C serial interface requires a master to initiate all the communications with slave devices. The I²C protocol is a bidirectional bus allowing both read and write actions to take place; while the AAT1142 is a slave device and only supports the write protocol.

The AAT1142 is a receiver-only (or write-only) slave device and the Read / Write (R/W) bit is set low. The AAT1142 address is preset to 0x14 (Hex).

I²C START and STOP Conditions

START and STOP conditions are initialized by the I²C bus master. The master determines the START (beginning) and STOP (end) of a transfer with the slave device. Prior to initiating a START or after STOP, both the SDA and SCL lines are in bus-free mode. Bus-free mode is when SDA and SCL are both in the high state (see Figure 3).

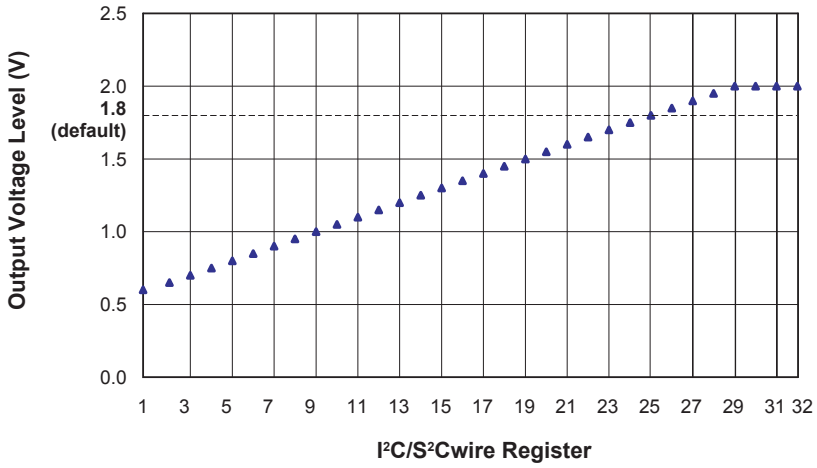


Figure 2: AAT1142 Graphical Output Voltage Programming Map.

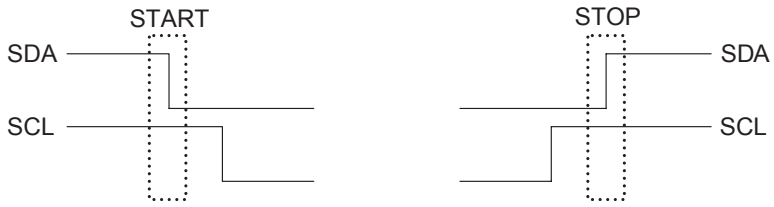


Figure 3: I²C Start and Stop Conditions.
START: A High "1" to Low "0" Transition on the SDA Line While SCL is High "1"
STOP: A Low "0" to High "1" Transition on the SDA Line While SCL is High "1"

I²C Address Bit Map

Figure 4 illustrates the address bit map format. The 7-bit address is sent with the Most Significant Bit (MSB) first and is valid when SCL is high. This is followed by the R/W bit in the Least Significant Bit (LSB) location. The R/W bit determines the direction of the transfer ('1' for read, '0' for write). The AAT1142 is a write-only device and this bit must be set low when communicating with the AAT1142. The Acknowledge bit (ACK) is set to low by the AAT1142 slave to acknowledge receipt of the address.

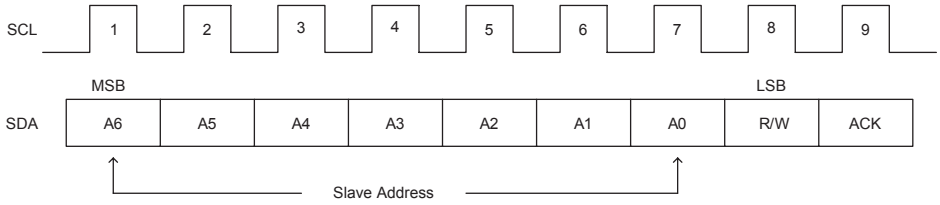


Figure 4: I²C Address Bit Map;
7-bit Slave Address (A6-A0), 1-bit Read/Write (R/W), 1-bit Acknowledge (ACK).

I²C Data Bit Map

Figure 5 illustrates the data bit format. The 8-bit data is always sent with the most significant bit first and is valid when SCL is high. The ACK bit is set low by the AAT1142 slave device to acknowledge receipt of the data.

I²C Acknowledge Bit

The ACK bit is the ninth bit in the address and data byte. The master must first release the SDA line, and then the slave will pull the SDA line low. The AAT1142 sends a low bit to acknowledge receipt of each byte. This occurs during the ninth clock cycle of Address and Data transfers (see Figures 5 and 6).

I²C Software Protocol

An I²C master / slave data transfer, detailing the address and data bits, is shown in Figure 6. The programming sequence is as follows:

1. Send a start condition
2. Send the I²C slave address with the R/W bit set low
3. Wait for acknowledge within the clock cycle
4. Send the data bits
5. Wait for acknowledge within the clock cycle
6. Send the stop condition

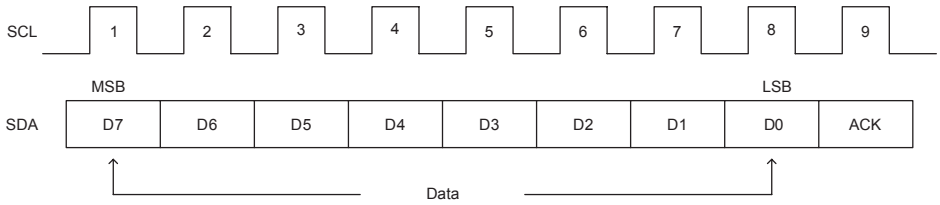


Figure 5: I²C Data Bit Map;
8-bit Data (D7-D0), 1-bit Acknowledge (ACK).

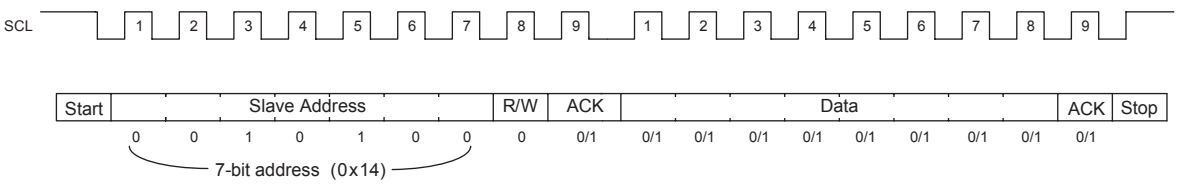


Figure 6: I²C SCL, SDA Transfer Protocol Example;
7-bit Slave Address (A6-A0 = 0x14), 1-bit Read/Write (R/W = 0), 1-bit Acknowledge (ACK),
8-bit Data (D7-D0), 1-bit Acknowledge (ACK).

I²C Output Voltage Programming

The AAT1142 output voltage is programmed through the I²C interface according to Table 1. The data register encoded on the SCL and SDA lines determines the output voltage set-point after initial start-up. Upon power-up and prior to I²C programming, the default output voltage is set to 1.8V.

Data Register	Data Bits								Output Voltage (V)
	D7	D6	D5	D4	D3	D2	D1	D0	
1	X	X	0	0	0	0	0	0	0.60
2	X	X	0	0	0	0	0	1	0.65
3	X	X	0	0	0	0	1	0	0.70
4	X	X	0	0	0	0	1	1	0.75
5	X	X	0	0	0	1	0	0	0.80
6	X	X	0	0	0	1	0	1	0.85
7	X	X	0	0	0	1	1	0	0.90
8	X	X	0	0	0	1	1	1	0.95
9	X	X	0	0	1	0	0	0	1.00
10	X	0	0	0	1	0	0	1	1.05
11	X	X	0	0	1	0	1	0	1.10
12	X	X	0	0	1	0	1	1	1.15
13	X	X	0	0	1	1	0	0	1.20
14	X	X	0	0	1	1	0	1	1.25
15	X	X	0	0	1	1	1	0	1.30
16	X	X	0	0	1	1	1	1	1.35
17	X	X	0	1	0	0	0	0	1.40
18	X	X	0	1	0	0	0	1	1.45
19	X	X	0	1	0	0	1	0	1.50
20	X	X	0	1	0	0	1	1	1.55
21	X	X	0	1	0	1	0	0	1.60
22	X	X	0	1	0	1	0	1	1.65
23	X	X	0	1	0	1	1	0	1.70
24	X	X	0	1	0	1	1	1	1.75
25	X	X	0	1	1	0	0	0	1.80 (default)
26	X	X	0	1	1	0	0	1	1.85
27	X	X	0	1	1	0	1	0	1.90
28	X	X	0	1	1	0	1	1	1.95
29	X	X	0	1	1	1	0	0	2.00
30	X	X	0	1	1	1	0	1	2.00
31	X	X	0	1	1	1	1	0	2.00
32	X	X	0	1	1	1	1	1	2.00

Table 1: AAT1142 I²C Output Voltage Programming Map (X = don't care).

S²Cwire Serial Interface

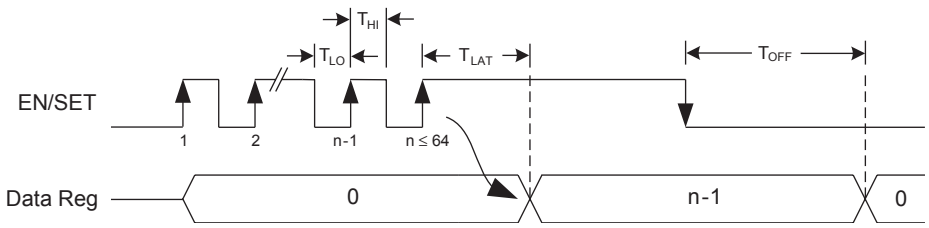
AnalogicTech's S²Cwire serial interface is a proprietary high-speed single-wire interface. The S²Cwire interface records rising edges of the EN/SET input and decodes them into one of 32 registers which determines the output voltage, as shown in Table 2. Each state corresponds to an output voltage setting.

When using the S²Cwire interface, both I²C inputs should be tied to the ground return. This disables the I²C functionality.

S²Cwire Serial Interface Timing

The S²Cwire serial interface has flexible timing. Data can be clocked-in at speeds up to 1MHz. After data has been submitted, EN/SET is held high to latch the data for a period T_{LAT}. The output is subsequently changed to the predetermined voltage. When EN/SET is set low for a time greater than T_{OFF}, the AAT1142 is disabled. When disabled, the data register is reset to the default value.

S²Cwire Timing Diagram



S²Cwire Output Voltage Programming

The AAT1142 is programmed through the S²Cwire interface according to Table 2. The rising clock edges received through the EN/SET pin corresponding to a given data register determine the output voltage set-point. Upon power-up and prior to S²Cwire programming, the default output voltage is set to 1.8V.

Rising Clock Edges/ Data Register	Output Voltage (V)	Rising Clock Edges/ Data Register	Output Voltage (V)
1	No change	17	1.40
2	0.65	18	1.45
3	0.70	19	1.50
4	0.75	20	1.55
5	0.80	21	1.60
6	0.85	22	1.65
7	0.90	23	1.70
8	0.95	24	1.75
9	1.00	25	1.80 (default)
10	1.05	26	1.85
11	1.10	27	1.90
12	1.15	28	1.95
13	1.20	29	2.00
14	1.25	30	2.00
15	1.30	31	2.00
16	1.35	32	2.00

Table 2: AAT1142 S²Cwire Output Voltage Programming Map.

Component Selection

Inductor Selection

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. The internal slope compensation for the programmable AAT1142 is 0.61A/µsec. This equates to a slope compensation that is 75% of the inductor current down slope for a 1.8V output and 2.2µH inductor.

$$m = \frac{0.75 \cdot V_O}{L} = \frac{0.75 \cdot 1.8V}{2.2\mu H} = 0.61 \frac{A}{\mu sec}$$

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

The 2.2µH CDRH2D14 series Sumida inductor has a 94mΩ DCR and a 1.5A DC current rating. At full 800mA load, the inductor DC loss is 60mW which gives a 4.8% loss in efficiency for an 800mA, 1.0V output.

Input Capacitor

Select a 4.7µF to 10µF X7R or X5R ceramic capacitor for the input. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PP}) and solve for C. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_S}$$

$$\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1}{4} \text{ for } V_{IN} = 2 \cdot V_O$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_S}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10µF, 6.3V, X5R ceramic capacitor with 5.0V DC applied is actually about 6µF.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$\sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = \sqrt{D \cdot (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

for $V_{IN} = 2 \cdot V_O$

$$I_{RMS(MAX)} = \frac{I_O}{2}$$

The term $\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations and is a maximum when V_O is twice V_{IN}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT1142. Low ESR/ESL X7R and X5R ceramic

capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

Proper placement of the input capacitor (C1) is shown in the evaluation board layout in Figure 7.

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result.

Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic capacitor should be placed in parallel with the low ESR, ESL bypass ceramic capacitor. This dampens the high Q network and stabilizes the system.

Output Capacitor

The output capacitor limits the output ripple and provides holdup during large load transitions. A 4.7µF to 10µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple. A smaller capacitor may result in slightly increased no load output regulation and output ripple with input voltages above 5V. This should be verified under actual operating conditions.

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

The internal voltage loop compensation also limits the minimum output capacitor value to 4.7µF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

Thermal Calculations

There are three types of losses associated with the AAT1142 step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the losses is given by:

$$P_{TOTAL} = \frac{I_O^2 \cdot (R_{DS(ON)H} \cdot V_O + R_{DS(ON)L} \cdot [V_{IN} - V_O])}{V_{IN}}$$

$$+ (t_{sw} \cdot F_S \cdot I_O + I_Q) \cdot V_{IN}$$

I_Q is the step-down converter quiescent current. The term t_{sw} is used to estimate the full load step-down converter switching losses.

For the condition where the step-down converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_{TOTAL} = I_O^2 \cdot R_{DS(ON)H} + I_Q \cdot V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the TSOPJW-12 package which is 160°C/W.

$$T_{J(MAX)} = P_{TOTAL} \cdot \Theta_{JA} + T_{AMB}$$

Layout

The suggested PCB layout for the AAT1142 in a TSOPJW-12 package is shown in Figures 7 and 8. The following guidelines should be used to help ensure a proper layout.

1. The input capacitor (C2) should connect as closely as possible to VIN (Pin 12) and PGND (Pin 2).
2. C1 and L1 should be connected as closely as possible. The connection of L1 to the LX pin (Pin 1) should be as short as possible.
3. The feedback pin (Pin 7) should be separate from any power trace and connected close to the VOUT terminal. Sensing along a high-current load trace will degrade VOUT load regulation.
4. The resistance of the trace from the GND terminal to PGND (Pin 2) should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. Connect unused signal pins to ground to avoid unwanted noise coupling. When using S²Cwire, connect SDA and SCL to ground to disable I²C functionality.
6. When using the TDFN33-12 package, connect the exposed paddle (EP) to the GND plane.

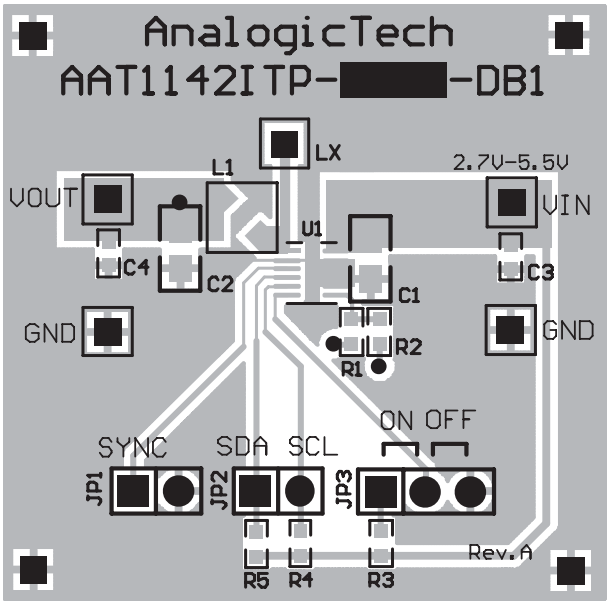


Figure 7: AAT1142 Evaluation Board Top Side Layout (TSOPJW-12 Package).

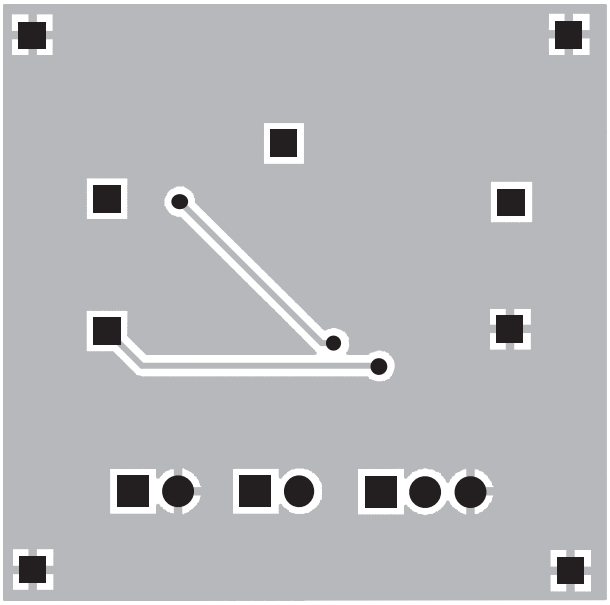


Figure 8: AAT1142 Evaluation Board Bottom Side Layout (TSOPJW-12 Package).

Manufacturer	Part Number	Inductance (µH)	Max DC Current (A)	DCR (Ω)	Size (mm) LxWxH	Type
Sumida	CDRH3D16-2R2	2.2	1.20	0.072	3.8x3.8x1.8	Shielded
Sumida	CDRH2D14-2R2	2.2	1.50	0.094	3.2x3.2x1.55	Shielded
Taiyo Yuden	NR3010T2R2M	2.2	1.10	0.095	3.0x3.0x1.0	Shielded
Taiyo Yuden	CBC3225T2R2MR	2.2	1.13	0.080	3.2x2.5x2.5	Non-Shielded

Table 3: Typical Surface Mount Inductors.

Manufacturer	Part Number	Type	Value	Voltage	Temp. Co.	Case
MuRata	GRM188R60J106ME47D	Ceramic	10	6.3	X5R	0603
MuRata	GRM21BR60J106KE19L	Ceramic	10	10	X5R	0805
MuRata	GRM188R60J475KE19D	Ceramic	4.7	6.3	X5R	0603
MuRata	GRM21BR61A475KA73L	Ceramic	4.7	10	X5R	0805

Table 4: Surface Mount Capacitors.

Ordering Information

Package	Marking[1]	Part Number (Tape and Reel)[2]
TSOPJW-12	RIXYY	**AAT1142ITP-1.8-T1**
TDFN33-12		AAT1142IWP-1.8-T1

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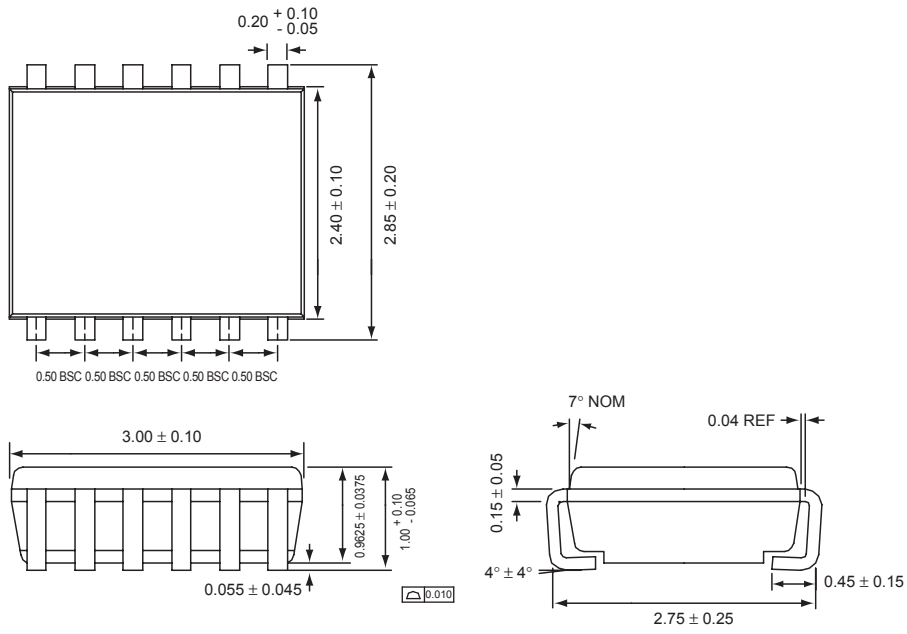
Package Information

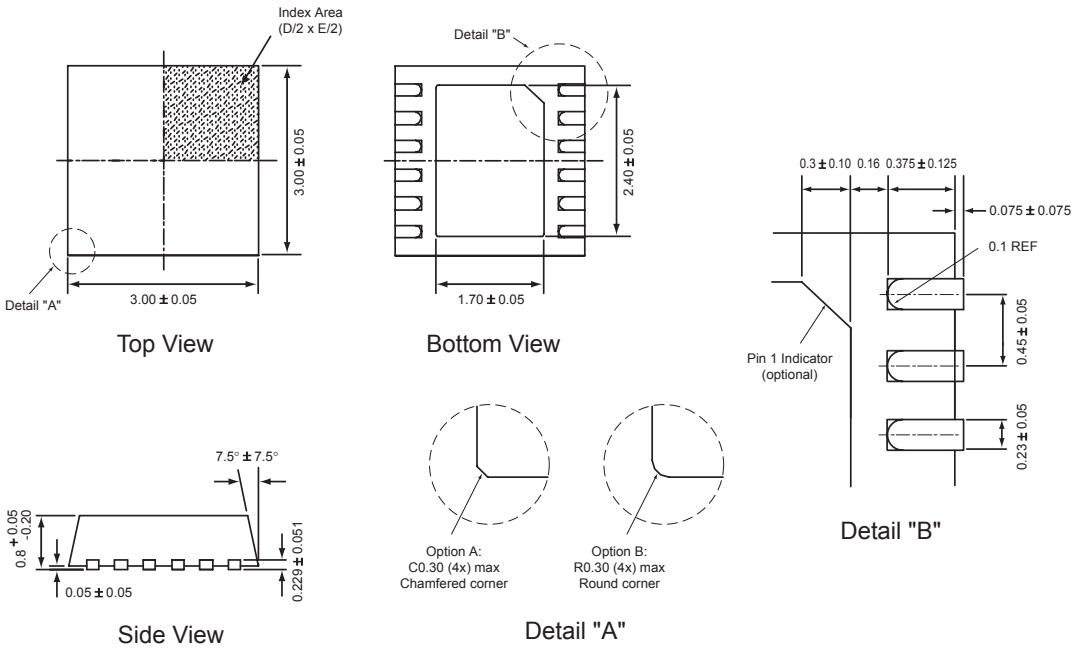
TSOPJW-12



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

TDFN33-12



All dimensions in millimeters.

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