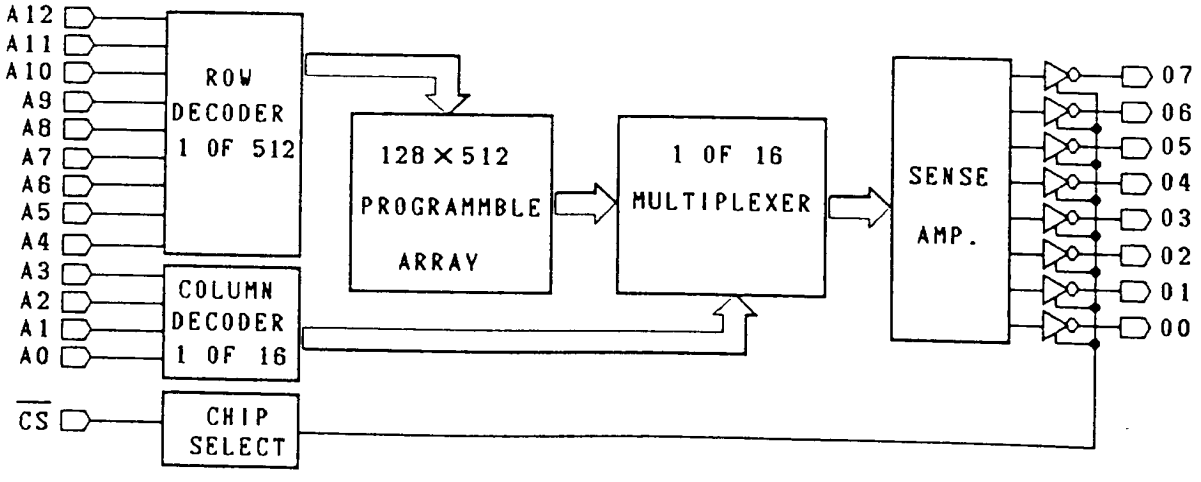
AK27CX641 / 642

64Kbit CMOS High-Speed UV-Erasable PROM

Features

- ☐ 8,192word × 8bit
- ☐ Advanced CMOS EPROM Technology
- ☐ High Performance
  - — AK27CX641/642-40 · · t_{AA} = 40nS max.
  - — AK27CX641/642-45 · · t_{AA} = 45nS max.
  - — AK27CX641/642-55 · · t_{AA} = 55nS max.
- ☐ Low Power Consumption
  - — I_{CC} = 80mA max.
- ☐ TTL-Compatible I/O
- ☐ Reprogrammability
  - — Adds convenience, reduces costs
  - — Windowed package for UV erasure
  - — Allows 100% factory testing
- ☐ Bipolar PROM replacement
  - — Pin-compatible with Bipolar PROMs
  - — Higher speed
  - — Lower power consumption
  - — 300-mil(AK27CX642) and 600-mil(AK27CX641) packages



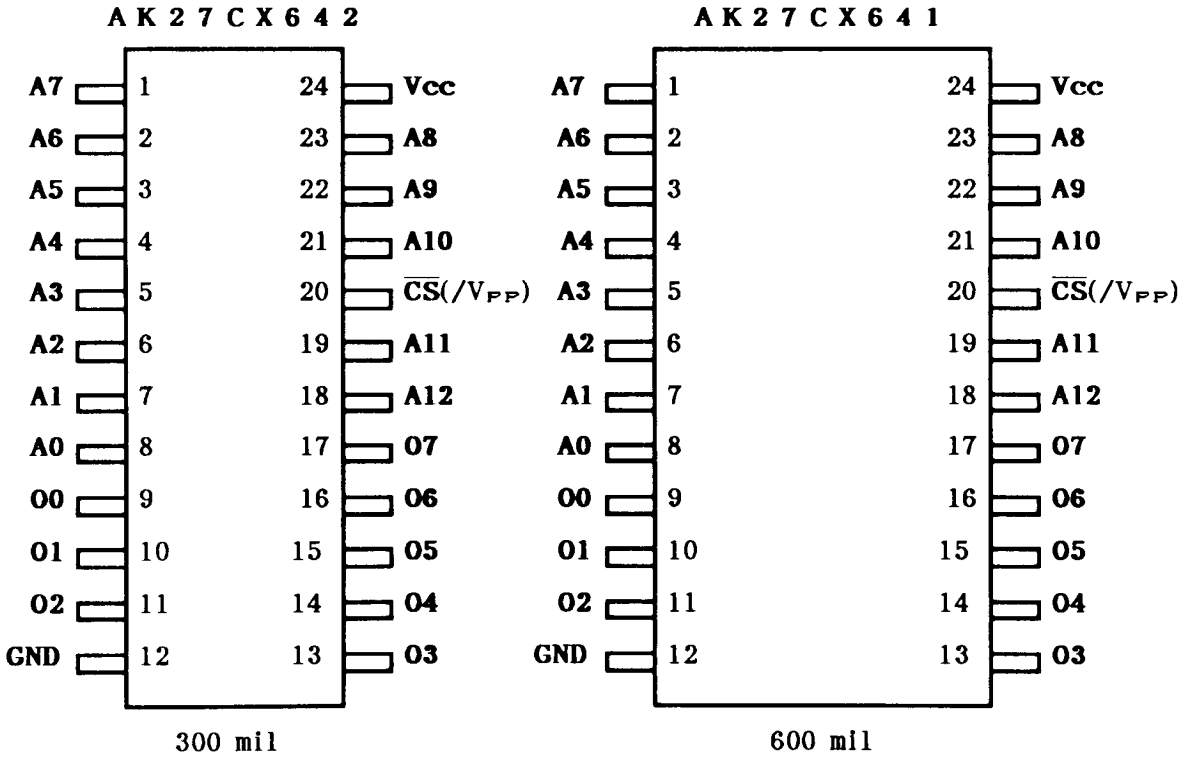
Block Diagrams

General Description

The AKM AK27CX641 and AK27CX642 are 8,192 × 8-bit, CMOS, high-speed, UV-erasable PROMs that provide a low-power, reprogrammable alternative to bipolar fuse-link PROMs. Available in both 600mil (AK27CX641) and 300mil (AK27CX642) packages, these devices are pin/socket-compatible with many popular bipolar PROMs. The AK27CX641/642 is designed in an advanced CMOS EPROM technology and utilize differential memory cell techniques to provide access times comparable to high-speed bipolar PROMs (as fast as 40nS), with a significant improvement in power consumption.

The reprogrammability of the AK27CX641/642 not only adds convenience and reduces development and field retrofit costs, but enhances factory testability, allowing for 100% field programmability and function.

■ Pin Diagrams



A0-A12 = Address Input
O0-O7 = Data Output
$\overline{CS}$ = Chip Select (/VPP Programming Voltage)
GND = Ground
Vcc = Power Supply(+5V)

Erasure Characteristics

The AK27CX641/642 is erased by exposure to ultraviolet light. For complete erasure, the recommended minimum integrated dose (UV intensity × exposure time) is 15 Watt-second/cm^2 of ultraviolet light with a wavelength of 2537 . For an ultraviolet lamp with a 12mW/cm^2 power rating, the exposure time would be approximately 20 minutes. The AK27CX641/642 should be placed within one inch of the lamp during erasure. Exposing the CMOS EPROM to high-intensity UV light for extended periods may affect device reliability.

Programming the AK27CX641/642

The AK27CX641/642 employs a dual-transistor differential memory cell design. Initially, and after erasure, all bits of the AK27CX641/642 are in an undefined state. Verifying a blank device will yield erroneous results. The desired state of each bit must be programmed into the device to ensure proper operation. Programming support is available from AKM and third-party vendors.

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	-0.6 ~ +7.0	V
V_{IO}	Voltage Applied to Any Pin	Relative to GND	-0.6 ~ V_{CC}+0.6	V
T_A	Ambient Temp., Power Applied		-10 ~ +85	℃
T_{ST}	Storage Temperature		-65 ~ +125	℃
T_{LT}	Lead Temperature	Soldering 10 seconds	+260	℃

Read Operation

Operation Ranges

Symbol	Parameter	Conditions	min.	max.	Unit
V_{CC}	Supply Voltage		4.75	5.25	V
T_A	Ambient Temperature		0	70	℃

D.C. Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	min.	max.	Unit
V_{IH}	Input HIGH Level		2.0		V
V_{IL}	Input LOW Level			0.8	V
V_{OH}	Output HIGH Voltage*1	V_{CC}=min., I_{OH}=-4.0mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC}=min., I_{OL}=12mA		0.45	V
I_L	Input Leakage Current	V_{CC}=Max, GND$\leq V_I \leq V_{CC}$		10	μA
I_{OS}	Output Short Circuit Current	V_{CC}=max., $\overline{CS}$=GND, V_O=GND	-15	-90	mA
I_{OZ}	Output Leakage Current	V_{CC}=max., $\overline{CS}$=V_{IH}, V_O=V_{CC} or GND		10	μA
I_{CC}	Power Supply Current*2	All inputs=(GND or V_{CC})$\pm$0.3V		80	mA
V_{IC}	Input Clamp Voltage	V_{CC}=min., I_{IN}=-18mA		-1.2	V

Notes :

1. The AK27CX641/642 provide true CMOS output interface levels. The specifications shown are for TTL interface.
2. Maximum value for I_{CC} when all cells are programmed.

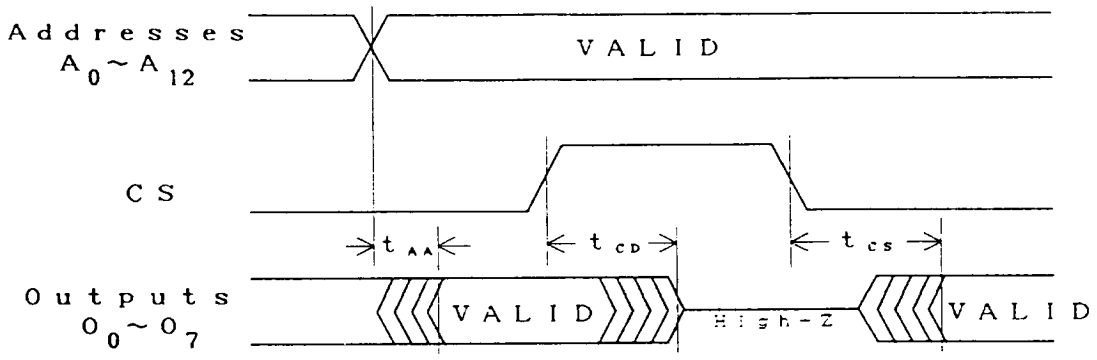
Capacitance These measurements are periodically sample tested

Symbol	Parameter	Conditions	min.	max.	Unit
C_{IN}	Input Capacitance	V_{IN}=0.0V f=1MHz		6	pF
C_{OUT}	Output Capacitance			12	pF
C_{CS}	$\overline{CS}$ Pin Capacitance			15	pF

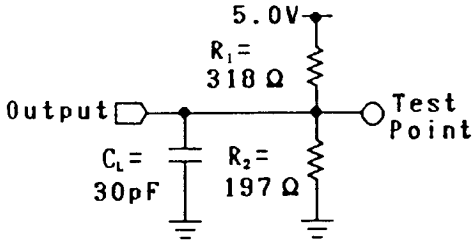
A.C. Electrical Characteristics Over the Operating Range[3]

Symbol	Parameter	27CX641-40 27CX642-40		27CX641-45 27CX642-45		27CX641-55 27CX642-55		Unit
		min.	max.	min.	max.	min.	max.	
t_{AA}	Access Time From Address To Output		40		45		55	nS
t_{CS}	Access Time From Chip Select to Output[*4]		20		25		35	nS
t_{CD}	Chip Disable to High-Z[*4,*5]		20		25		35	nS

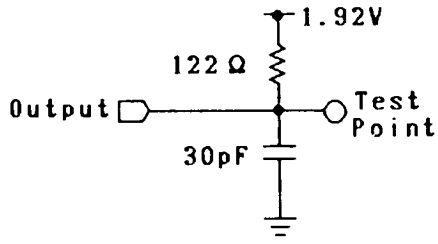
Switching Waveforms (READ)



Test Loads



Test Load



Thevenin Equivalent

Note :

3. Test conditions assume: signal transition times of 5 nS or less from the 10% and 90% points; timing reference levels of 1.5V(unless otherwise specified); and test loads shown above.
4. t_{CS}, t_{CD}, are measured at the midpoint between output (O_{D-7}) steady-state high-Z level and V_{OH} or V_{OL}.
5. C_L includes scope and jig capacitance. t_{CD} is tested with C_L=5pF.

Program operation

Operation Ranges

Symbol	Parameter	Conditions	min.	max.	Unit
T_A	Ambient Temperature		20	30	℃

D.C. Electrical Characteristics Ta = 25℃

Symbol	Parameter	min.	typ.	max.	Unit
Vccp	Vcc during programming	5.75	6	6.25	V
V_{IHP}	Input HIGH Level during programming	3.0		6.25	V
V_{ILP}	Input LOW Level during programming	0		0.45	V
Vpp	Programming Voltage	11.75	12	12.25	V
Ipp	Vpp Supply Current		25	50	mA

A.C. Electrical Characteristics Ta = 25℃

Symbol	Parameter	min.	typ.	max.	Unit
t_{AS}	Address set-up to Vpp pulse	0			ns
t_{DS}	Data set-up to Vpp pulse	0			ns
t_{PW}	Vpp program pulse width *6			50	μs
t_{RF}	Vpp rise and fall ramp time *7	1			ns/V
t_{DH}	Data hold time	10			ns
t_{PV}	Vpp pulse to verify delay *8		2	5	μs

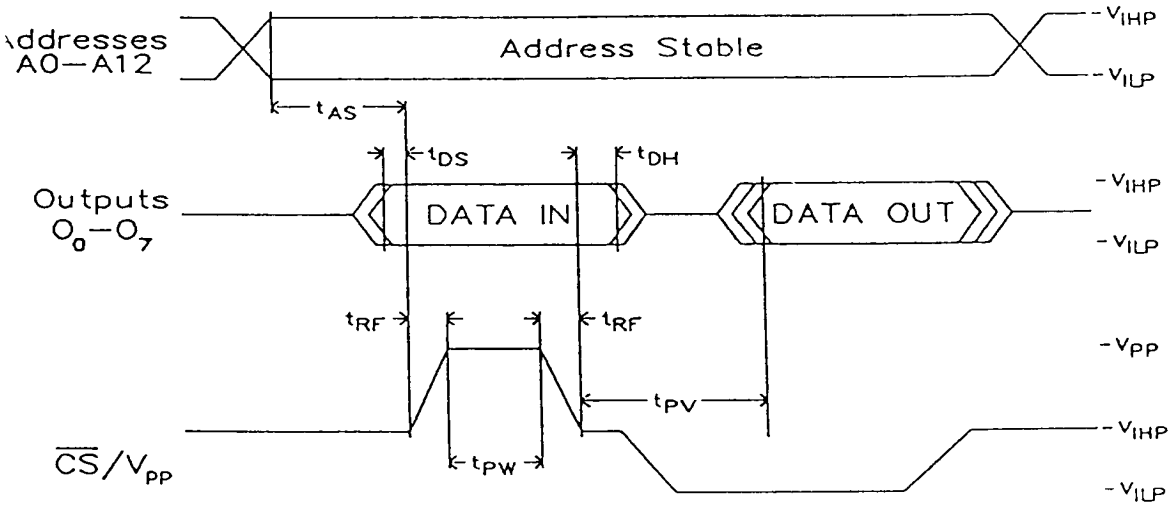
Note :

*6: It is recommended to use 50 μs for the Vpp Program pilse width in the interetive section to ensure maximum device performance.

*7: In using the recommended rise and fall ramp times,any overshoot due to system and/or tester noise must not exceed the maximum Vccp voltage.

*8: This timing parameter is the device internal delay. After the $\overline{CS}$/Vpp pin has been ramped down from the Vpp to the V_{ILP} voltage (to do a data read for data verification), the outputs will have a t_{PV} delay before they are valid .

Switching Waveforms (PROGRAMMING) <Vccp=6V>



Programming Flow