2A Sink/Source Regulator for Front Side Bus and DDR Memory Bus Termination

Features

- Ideal for both PC Front Side Bus and DDR memory V_{TT} applications
- Sinks and sources 2A
- Over current protection
- Over temperature protection
- Shutdown function
- Integrated power MOSFETs
- Excellent accuracy (0.5% of load regulation)
- Minimum external components
- 8 pin PSOP package
- Lead-free version available

Applications

- PC Front Side Bus termination regulator
- DDR Memory termination regulator
- Active termination buses
- Graphics card DDR memory termination

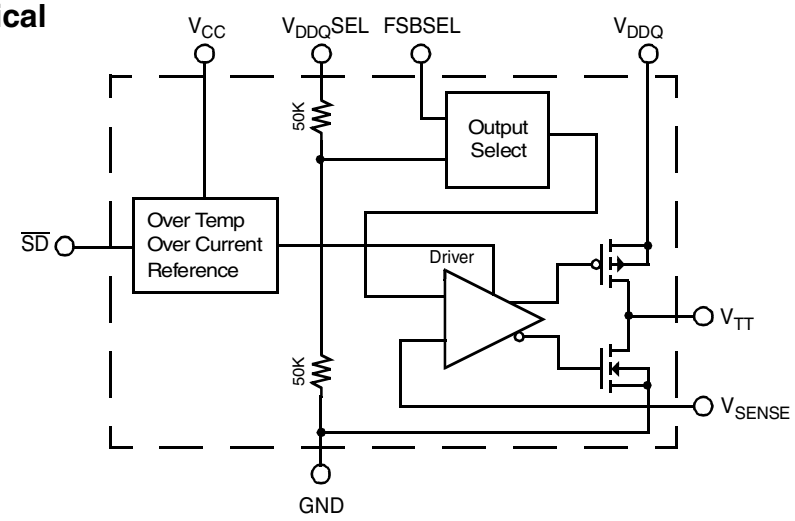
Product Description

The CM3109 is a sinking and sourcing regulator specifically designed for series-parallel bus termination for high speed chip set buses as well as DDR memory systems. It can source and sink current up to 2A with high accuracy of 0.5 %. The V_{TT} output voltage is selectable by V_{DDQ}SEL and FSBSEL pins. The V_{DDQ}SEL pin controls whether the CM3109 is in DDR memory mode with $V_{TT} = V_{DDQ}/2$, or in FSB mode. In FSB mode, FSBSEL controls whether V_{TT} is 1.225V or 1.45V. This allows the same chip to be used in two different circuits on PC motherboards that support both Northwood and Prescott processors.

The CM3109 requires no external components to use the GMCH Enable signal in Intel chipset or corresponding signals for other chip sets when powering up the PC. For the boards which support Suspend to RAM (STR) functionality, CM3109 provides a shutdown ($\overline{SD}$) pin. When $\overline{SD}$ is set low, V_{TT} will be in tri-state mode, causing the output to go high impedance. In this mode, CM3109 power is saved by significantly reducing the quiescent current.

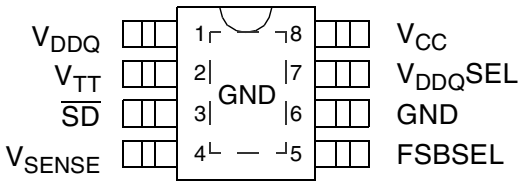
The CM3109 provides over current and over temperature protection. These features protect the chip from excessive heating due to high current and high temperature. The CM3109 is housed in an 8-pin PSOP package and is available with optional lead-free finishing.

Simplified Electrical Schematic



PACKAGE / PINOUT DIAGRAM

TOP VIEW



8-lead PSOP

Note: This drawing is not to scale.

PIN DESCRIPTIONS

LEAD(S)	NAME	DESCRIPTION
1	V_{DDQ}	Input Voltage V_{DDQ}
2	V_{TT}	Outputs either 1.225V/1.45V FSB or V_{DDQ}/2 DDR (See note 1)
3	$\overline{SD}$	Shutdown input
4	V_{SENSE}	Feedback voltage input
5	FSBSEL	Select input for FSB output. Selects either V_{TT}=1.225V or 1.45V.
6	GND	GROUND
7	V_{DDQ}SEL	Select input for DDR/FSB Output
8	V_{CC}	Power for control blocks

Note 1: Assumes V_{DDQ} and V_{DDQ}SEL are tied together in DDR application.

Ordering Information

PART NUMBERING INFORMATION

		Standard Finish		Lead-free Finish	
Leads	Package	Ordering Part Number[1]	Part Marking	Ordering Part Number[1]	Part Marking
8	PSOP-8	CM3109-00SB	CM3109-00SB	CM3109-00SH	CM3109-00SH

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
V_{CC} Operating Supply Voltage	7	V
V_{DDQ} Input Voltage	7	V
Pin Voltages V_{TT} Output Any other pins	 7 7	 V V
Storage Temperature Range	-40 to +150	°C
Operating Temperature Range Ambient Junction	 -45 to +85 -45 to +150	 °C °C
Power Dissipation (See note 1)	Internally Limited	W

Note 1: These devices must be derated based on thermal resistance at elevated temperatures. The CM3109-xxSB/ must be derated at θ_{JA} = 40°C/W . Please consult with factory for thermal evaluation assistance.

STANDARD OPERATING CONDITIONS		
PARAMETER	**VALUE**	**UNITS**
V_{DDQ}, V_{DDQ}	2.5	V
Ambient Operating Temperature	25	°C
C_{OUT}	220 ±20%	µF

Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{IN}	Input Voltage Range V_{DDQ} V_{CC}		 2.2 2.2	 2.5 2.5	 V_{CC} 5.5	 V V
I_{CC}	V_{CC} Quiescent Current	I_{VTT} = 0A		450		µA
V_{TT}	Output Voltage	I_{VTT} = 0A, V_{DDQ} = 2.5V, V_{DDQ}SEL= "1" = 2.5V V_{DDQ}SEL="0", FSBSEL="0" V_{DDQ}SEL = "0", FSBSEL = "1" I_{VTT} = 0A, V_{DDQ} = 3.3V, V_{DDQ}SEL="0", FSBSEL="0" V_{DDQ}SEL = "0", FSBSEL = "1"	 1.225 1.200 1.425 1.200 1.425	 1.250 1.225 1.450 1.225 1.450	 1.275 1.250 1.475 1.250 1.475	 V V V V V V
V_{RLOAD}	Load Regulation	0A ≤ I_{VTT} ≤ 2.0A or 0A ≤ I_{VTT} ≤ -2.0A		6.25		mV
CL_{VTT}	V_{TT} Current Limit			2.5		A
V_{FSBSEL}	Output Selection Logic (FSBSEL) Logic "1" Level Logic "0" Level		 1.5		 0.4	 V V
V_{SD}	Shutdown Logic Logic "1" Level Logic "0" Level		 1.5		 0.4	 V V
$T_{DISABLE}$ T_{HYST}	Shutdown Temperature Thermal Hysteresis			150 30		°C °C

Note 1: Operating Characteristics are over Standard Operating Conditions unless otherwise specified.

Performance Information

Typical DC Characteristics (nominal conditions unless otherwise specified)

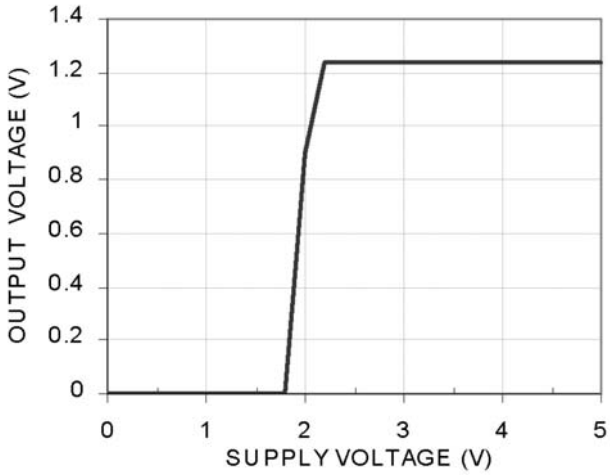


Figure 1. Output Voltage with V_{CC}Supply (V_{DDQ}=2.5V)

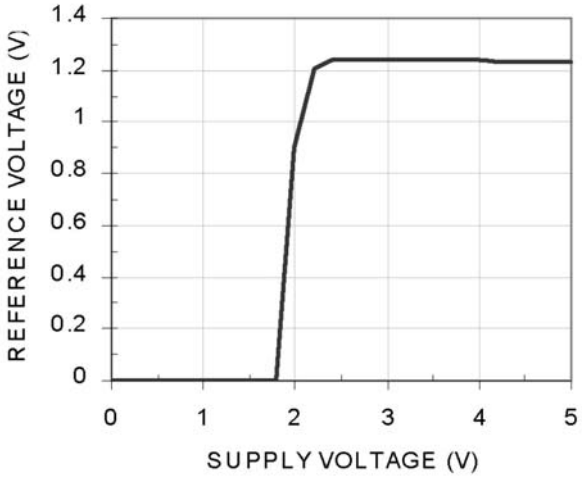


Figure 3. Reference Voltage with V_{CC} Supply (V_{DDQ}=2.5V)

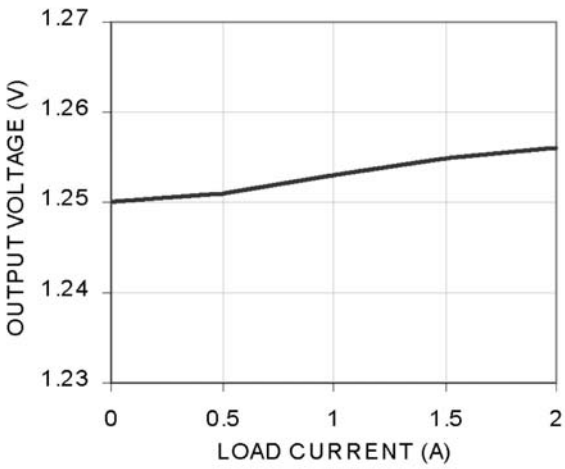


Figure 2. Load Regulation (Sink)

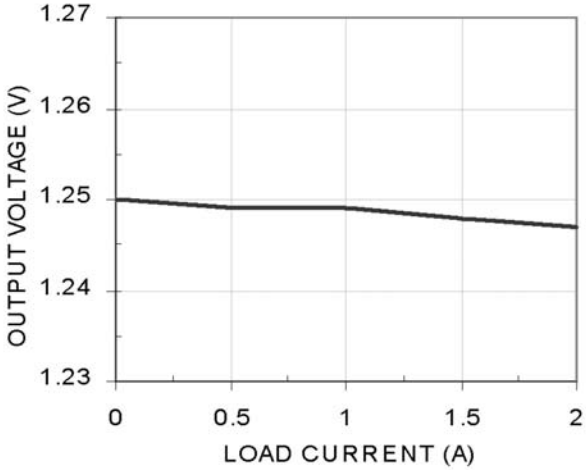


Figure 4. Load Regulation (Source)

Performance Information (cont'd)

Typical DC Characteristics (nominal conditions unless otherwise specified)

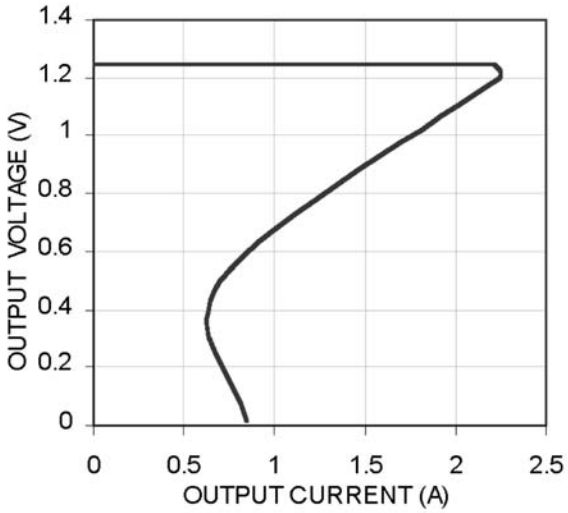


Figure 5. Over Current Limit (Sink)

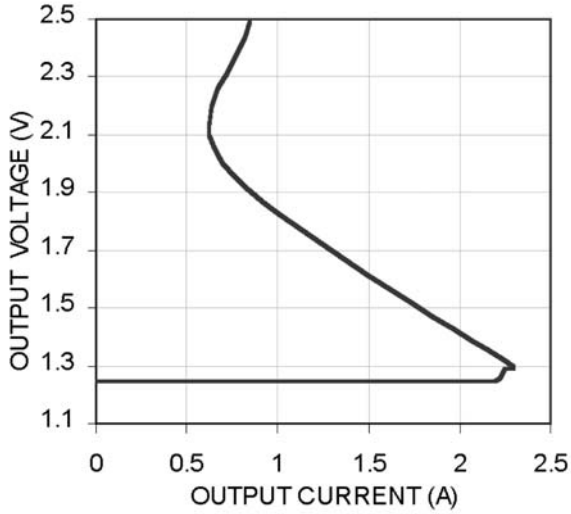


Figure 7. Over Current Limit (Source)

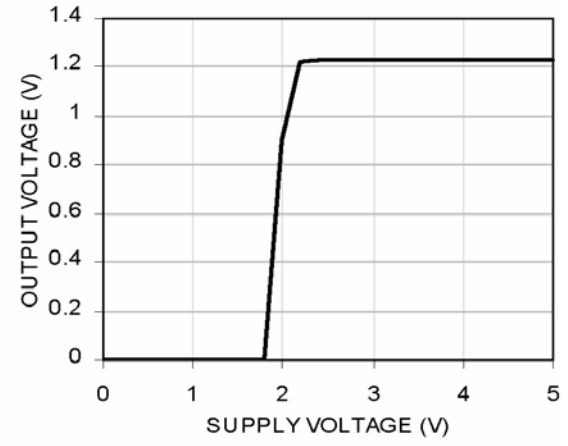


Figure 6. Output Voltage with V_{CC} Supply Voltage (V_{DDQ}SEL = 0V, FSBSEL = 0V)

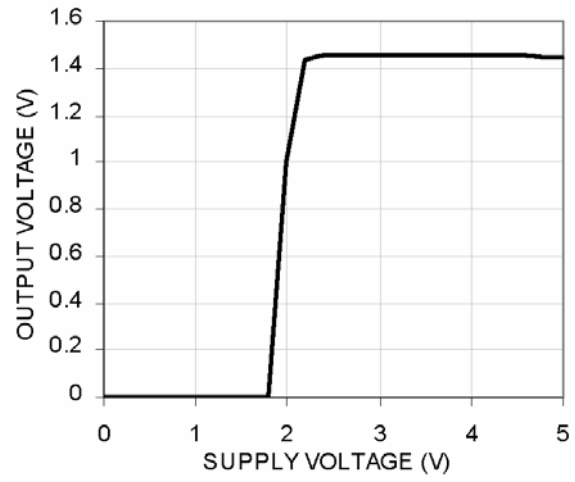


Figure 8. Output Voltage with V_{CC} Supply Voltage (V_{DDQ}SEL = 0V, FSBSEL = 2.5V)

Performance Information (cont'd)

Typical DC Characteristics (nominal conditions unless otherwise specified)

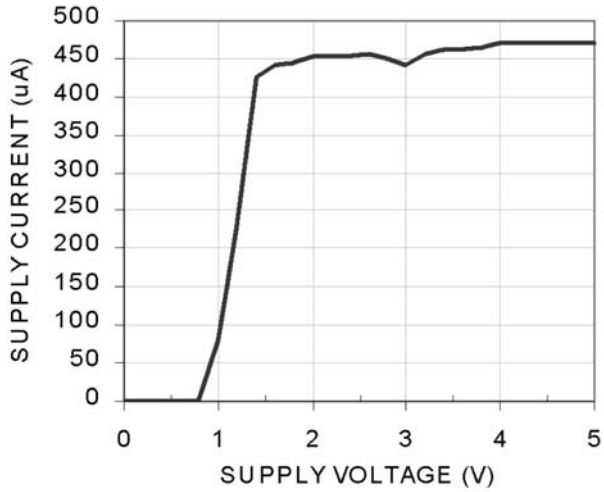


Figure 9. V_{CC} Supply Current with Supply Voltage

Typical Transient Characteristics (nominal conditions unless otherwise specified)

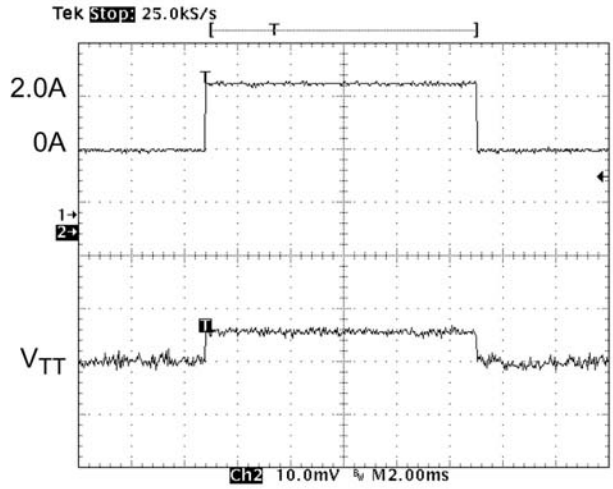


Figure 10. Load Transient (0A to 1.5A Sink)

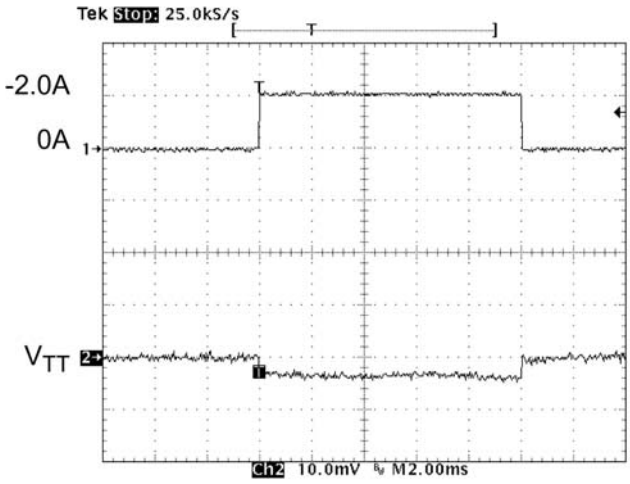


Figure 11. Line Transient (0A to 1.5A Source)

Performance Information (cont'd)

Typical Thermal Characteristics

The overall junction to ambient thermal resistance (θ_{JA}) for device power dissipation (P_D) consists primarily of two paths in series. The first path is the junction to the case (θ_{JC}) which is defined by the package style, and the second path is case to ambient (θ_{CA}) thermal resistance which is dependent on board layout. The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

$$T_{JUNC} = T_{AMB} + P_D (\theta_{JC}) + P_D (\theta_{CA})$$

$$= T_{AMB} + P_D (\theta_{JA})$$

When a CM3109-00SB/SH (PSOP) is mounted on a double sided printed circuit board with two square inches of copper allocated for "heat spreading", the resulting θ_{JA} is 40°C/W. Based on the over temperature limit of 150°C with an ambient of 85°C, the available power of this package will be:

$$P_D = (150°C - 85°C) / 40°C/W = 1.625W$$

DDR Memory Application

Since the output voltage is 1.25V, and the device can either source current from V_{DDQ} or sink current to Ground, the power dissipated in the device at any time is 1.25V times the current load. This means the maximum average RMS current (in either direction) is 1.3A for CM3109-00SB/SH. The maximum instantaneous current is specified at 2A, so this condition should not be exceeded 65% of the time. It is highly unlikely in most usage of DDR memory that this might occur, because it means the DDR memory outputs are either all high or all low for 65% of the time.

If the ambient temperature is 40°C instead of 85°C, which is typically the maximum in most DDR memory applications, the power dissipated ($P_{D)}$ can be 2.75W. So the maximum RMS current increases from 1.3A to 2.2A. Thus, the maximum continuous current can be 2A all the time.

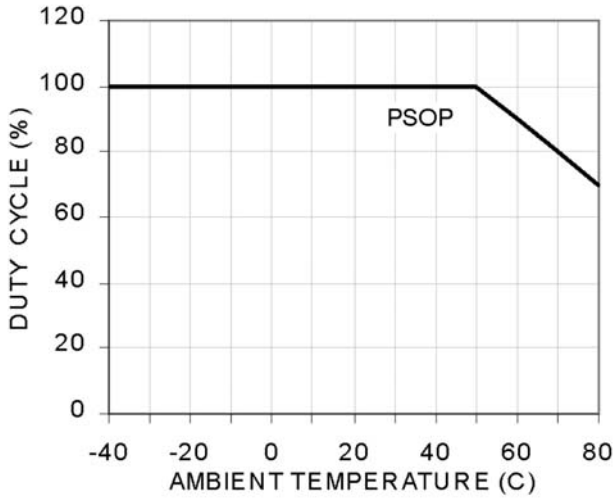


Figure 12. Duty Cycle vs. Ambient Temperature (I_{LOAD} = 2A)

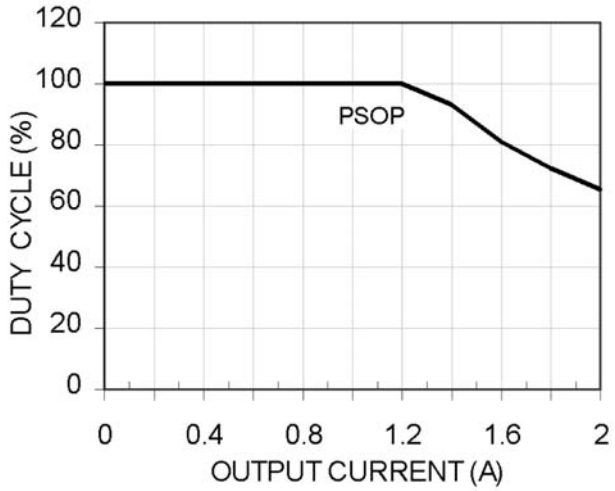


Figure 13. Duty Cycle vs. Output Current (Temp=70°C)

Performance Information (cont'd)

Typical Thermal Characteristics (cont'd)

Front Side Bus Application

If the CM3109-00SB/SH is instead used for the Front Side Bus application, where V_{DDQ} could be connected to the 3.3V V_{CC} rail for ease of connectivity, the power dissipated will increase to [3.3V-1.4V] = 1.9V times the sourcing current, or [1.4V - 0V] = 1.4V times the sinking current.

So the worst case is with all FSB outputs low for a period of time, such that the maximum average source current at an ambient of 40°C is [2.75W / 1.9V] = 1.45A. If this average current is exceeded, the device will go over-temperature and the output will drop to 0V.

The theoretical calculations of these relationships show the safe operating area of the CM3109 in the PSOP package.

Thermal characteristics were measured using a double sided board with two square inches of copper area connected to the GND pins for "heat spreading".

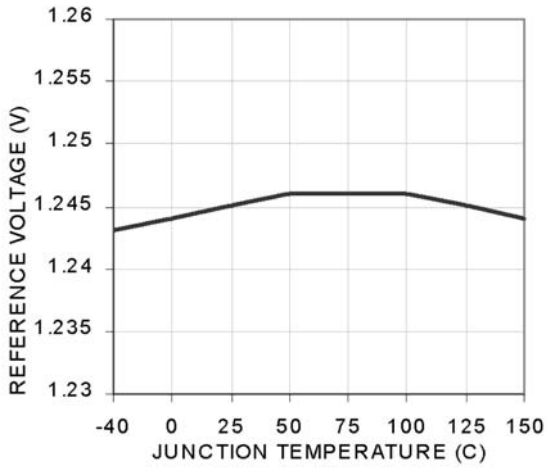


Figure 14. Reference Voltage vs. Temperature

Measurements showing performance up to a junction temperature of 150°C were performed under light load conditions (5mA). This allows the ambient temperature to be representative of the internal junction temperature.

Note: The use of multi-layer board construction with separate ground and power planes will further enhance the overall thermal performance.

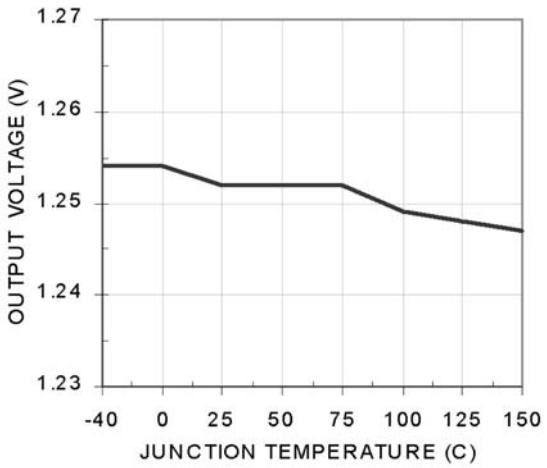


Figure 15. Output Voltage vs. Ambient Temperature (I_{LOAD}=5mA)

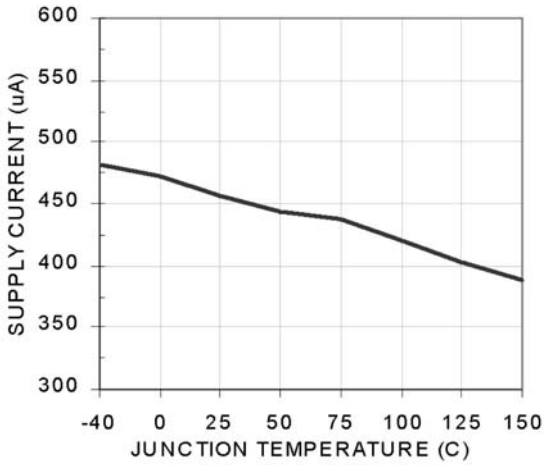


Figure 16. Quiescent Current vs. Temperature

Application Information

PCB Layout Considerations

The CM3109-00SB/SH has a heat spreader attached to the underneath of the PSOP-8 package in order for heat to be transferred much easier from the package to the PCB. The heat spreader is a copper pad of dimensions just smaller than the package itself. By positioning the matching pad on the PCB top layer to connect to the spreader during manufacturing, the heat will be transferred between the two pads. The drawing below shows the recommended PCB layout. Note that there are six vias on either side to allow the heat to dissipate into the ground and power planes on the inner layers of the PCB. Vias can be placed underneath the chip, but this can cause blockage of the solder. The ground and power planes should be at least 2 sq in. of copper by the vias. It also helps dissipation to spread if the chip is positioned away from the edge of the PCB, and not near other heat dissipating devices. A good thermal link from the PCB pad to the rest of the PCB will ensure a thermal link from the CM3109 package to ambient, θ_{JA}, of around 40°C/W.

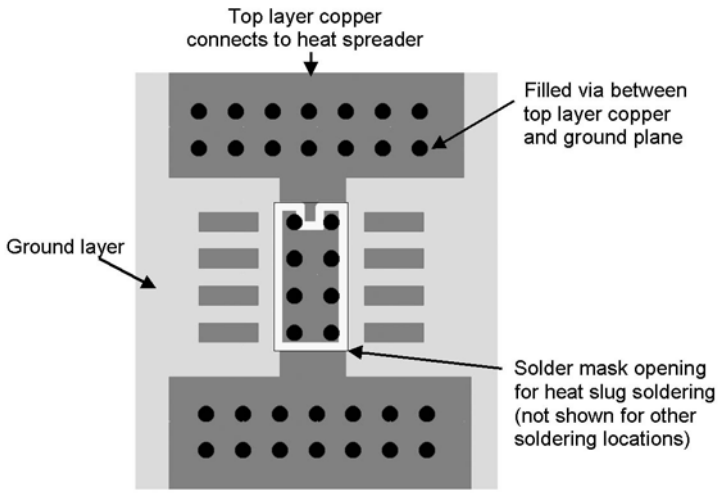


Figure 17. Recommended Heat Sink PCB Layout

Application Information (cont'd)

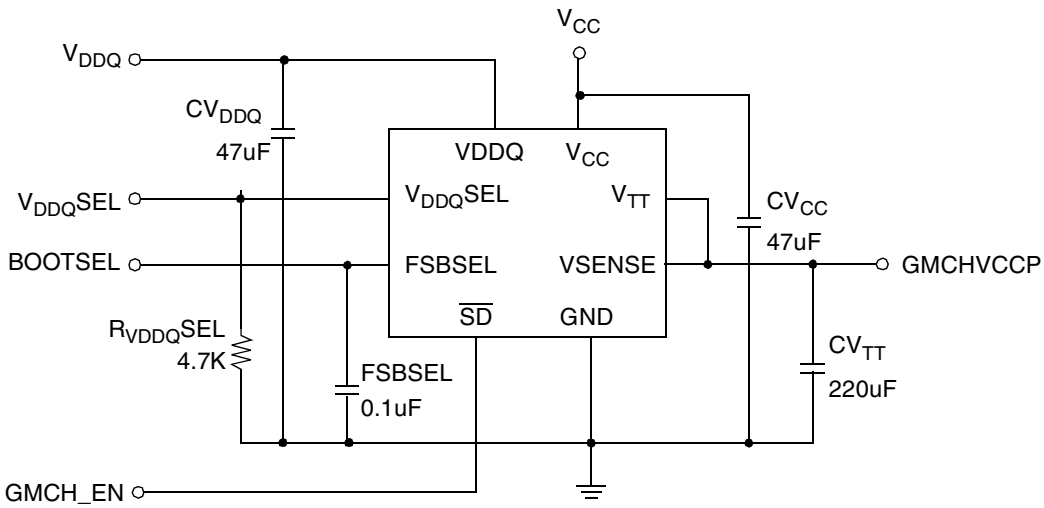


Figure 18. Typical Front Side Bus with Suspend to RAM Application Circuit

The above diagram shows the CM3109 connected to the Intel 865 GMCH Front Side Bus V_{TT} pin GMCH-VCCP. The Enable signal GMCH_EN is used to shut down the output of the CM3109 to save power during shutdown periods. The V_{DDQ}SEL input ensures that the CM3109 is in Front Side Bus mode, and the BOOT-SEL from the GMCH ensures the right Microprocessor V_{TT} voltage is applied.

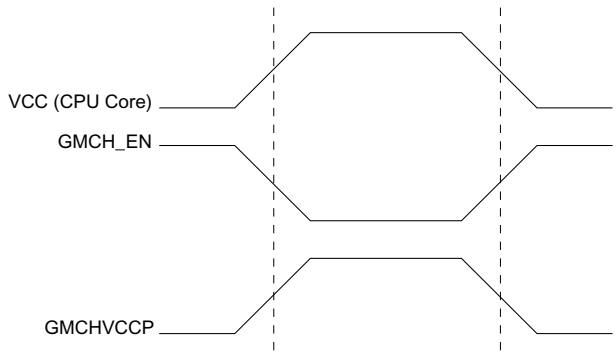


Figure 19. Front Side Bus Timing diagram

V_{DDQ}SEL	FSBSEL	V_{TT}	NOTE
"1"	Don't Care	V_{DDQ}SEL/2 (see note 1)	For DDR
Open or "0"	"0"	1.225V	For FSB
Open or "0"	"1"	1.45V	For FSB

Note 1:Assumes V_{DDQ} and V_{DDQ}SEL are tied together in DDR application.

Table 1: V_{TT} Output Selection Truth Table.

Mechanical Details

PSOP-8 Mechanical Specifications

Dimensions for CM3109 devices packaged in 8-pin PSOP packages with an integrated heatslug are presented below.

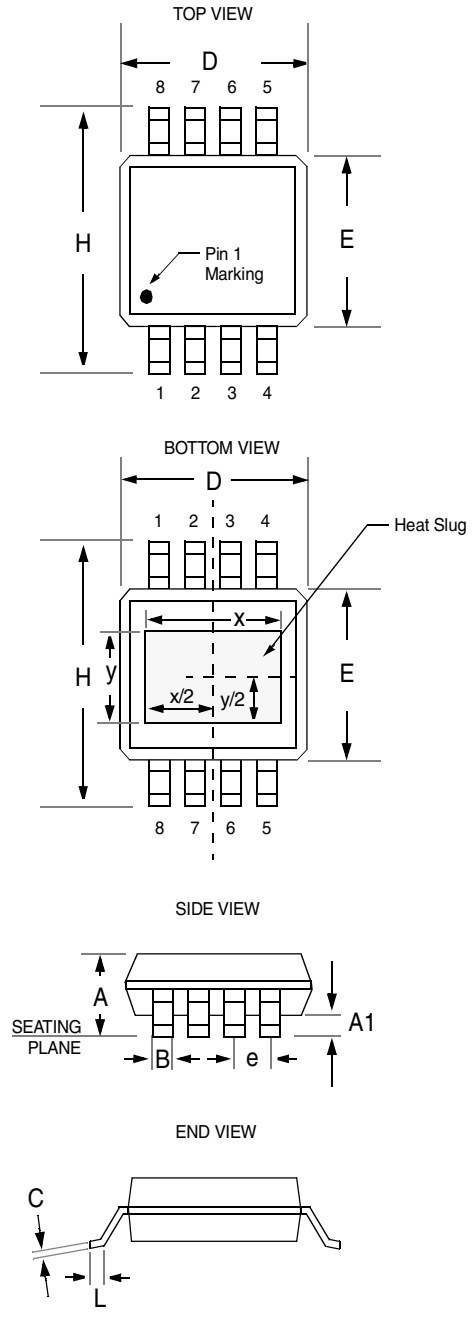
For complete information on the PSOP-8 package, see the California Micro Devices PSOP-8 Package Information document.

PACKAGE DIMENSIONS				
Package	PSOP-8			
Leads	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.30	1.62	0.051	0.064
A_1	0.03	0.10	0.001	0.004
B	0.33	0.51	0.013	0.020
C	0.18	0.25	0.007	0.010
D	4.83	5.00	0.190	0.197
E	3.81	3.99	0.150	0.157
e	1.02	1.52	0.040	0.050
H	5.79	6.20	0.228	0.244
L	0.41	1.27	0.016	0.050
x**	3.56	4.06	0.130	0.150
y**	2.29	2.79	0.090	0.110
# per tube	100 pieces*			
# per tape and reel	2500 pieces			
Controlling dimension: inches				

* This is an approximate number which may vary.

** Centered on package centerline.

Mechanical Package Diagrams



Package Dimensions for PSOP-8