Preliminary Notice: This is not a final specification.

Some parametric limits are subject to change.

M6MGB/T33BS8BWG-P

33,554,432-BIT (2,097,152-WORD BY 16-BIT) CMOS FLASH MEMORY & 8,388,608-BIT (524,288-WORD BY 16-BIT) CMOS SRAM

Stacked-CSP (Chip Scale Package)

Description

The M6MGB/T33BS8BWG-P is a Stacked Chip Scale Package (S-CSP) that contents 32M-bit Flash memory and 8M-bit SRAM in a 66-pin Stacked CSP with leaded solder ball.

32M-bit Flash memory is a 2,097,152 words, single power supply and high performance non-volatile memory fabricated by CMOS technology for the peripheral circuit and DINOR (Divided bit-line NOR) architecture for the memory cell. All memory blocks are locked and can not be programmed or erased, when F-WP# is Low. Using Software Lock Release function, program or erase operation can be executed.

8M-bit SRAM is a 524,288 words asynchronous SRAM fabricated by CMOS technology.

The M6MGB/T33BS8BWG-P is suitable for a high performance cellular phone and a mobile PC that are required to be small mounting area, weight and small power dissipation.

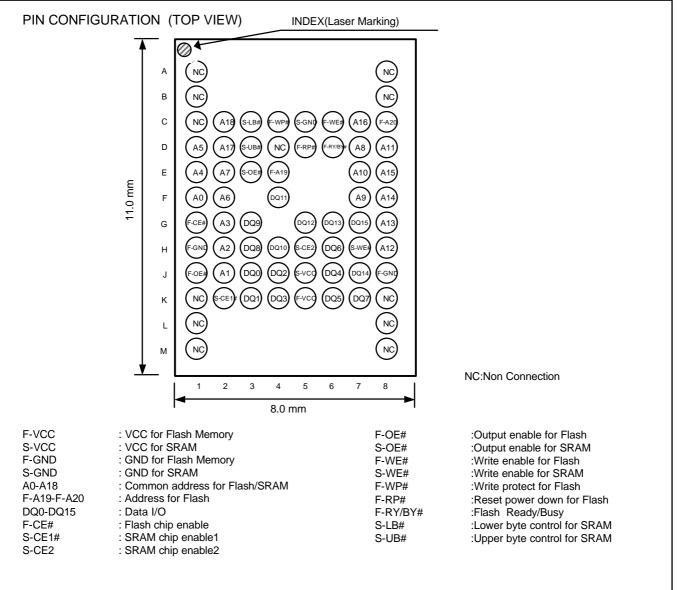
Features

Flash							
SRAM							
Ambient Temperature							

70ns (Max.) 85ns (Max.) F-VCC =VCC=2.7 ~ 3.0V Ta=-40 ~ 85 °C 66 pin S-CSP Ball pitch 0.80mm Outer-ball: Sn - Pb

Application

Mobile communication products





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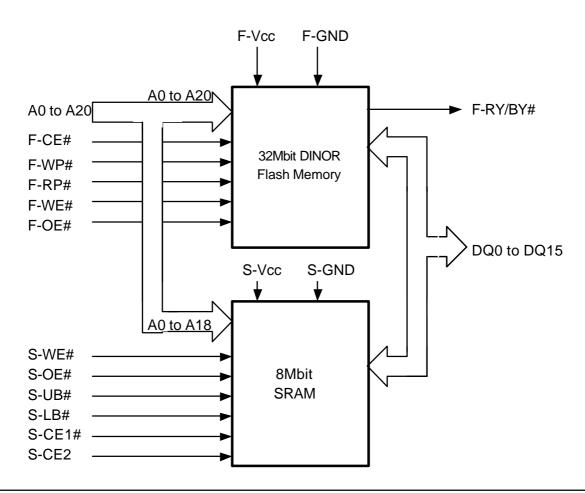
Preliminary

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M6MGB/T33BS8BWG-P

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MCP Block Diagram



Note: In the data sheet there are "VCC"s which mean "F-VCC". In the SRAM part there are "UB#" and "LB#" which mean "S-UB#" and "S-LB#", respectively.

Capacitance

Symbol	Parameter	Conditions	Limits			Unit	
Cymbol		i didileter	Conditions	Min.	Тур.	Max.	Onit
CIN	Input capacitance	A20-A0, F-OE#, S-OE#,F-WE#, S-WE#,F- CE#, F-WP#, F-RP#, S-CE1#, S-CE2, S-LB#, S-UB#	Ta=25°C, f=1MHz, Vin=Vout=0V			18	pF
СОИТ	Output Capacitance	DQ15-DQ0,F-RY/BY#				22	pF



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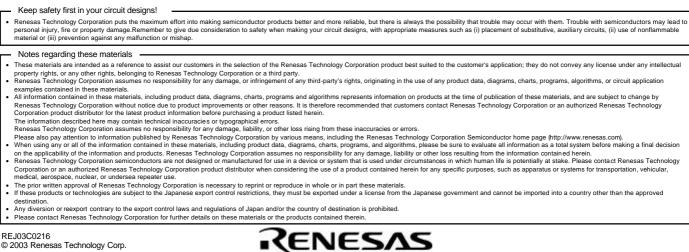
M6MGB/T33BS8BWG-P

33,554,432-BIT (2,097,152-WORD BY 16-BIT) CMOS FLASH MEMORY & 8,388,608-BIT (524,288-WORD BY 16-BIT) CMOS SRAM

Stacked-CSP (Chip Scale Package)

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