

R1EX24004ASAS0A

R1EX24004ATAS0A

Two-wire serial interface
4k EEPROM (512-word × 8-bit)

REJ03C0353-0100

Rev.1.00

Apr. 21, 2008

Description

R1EX24xxx series are two-wire serial interface EEPROM (Electrically Erasable and Programmable ROM). They realize high speed, low power consumption and a high level of reliability by employing advanced MNOS memory technology and CMOS process and low voltage circuitry technology. They also have a 16-byte page programming function to make their write operation faster.

Note: Renesas Technology's serial EEPROM are authorized for using consumer applications such as cellular phone, camcorders, audio equipment. Therefore, please contact Renesas Technology's sales office before using industrial applications such as automotive systems, embedded controllers, and meters.

Features

- Single supply: 1.8 V to 5.5 V
- Two-wire serial interface (I²C serial bus)
- Clock frequency: 400 kHz
- Power dissipation:
 - Standby: 2 μA (max)
 - Active (Read): 1 mA (max)
 - Active (Write): 2.5 mA (max)
- Automatic page write: 16-byte/page
- Write cycle time: 5 ms
- Endurance: 10⁶ Cycles
- Data retention: 10 Years

R1EX24004AxxS0A

- Small size packages: SOP-8pin, TSSOP-8pin
- Shipping tape and reel
 - TSSOP 8-pin: 3,000 IC/reel
 - SOP 8-pin: 2,500 IC/reel
- Temperature range: -40 to +85°C
- Lead free products.

Ordering Information

| Type No. | Internal organization | Operating voltage | Frequency | Package |
|-----------------|-------------------------|-------------------|-----------|---|
| R1EX24004ASAS0A | 4k bit (512 × 8-bit) | 1.8 V to 5.5 V | 400 kHz | 150 mil 8-pin plastic SOP PRSP0008DF-B (FP-8DBV) Lead free |
| R1EX24004ATAS0A | 4k bit (512 × 8-bit) | 1.8 V to 5.5 V | 400 kHz | 8-pin plastic TSSOP PTSP0008JC-B (TTP-8DAV) Lead free |

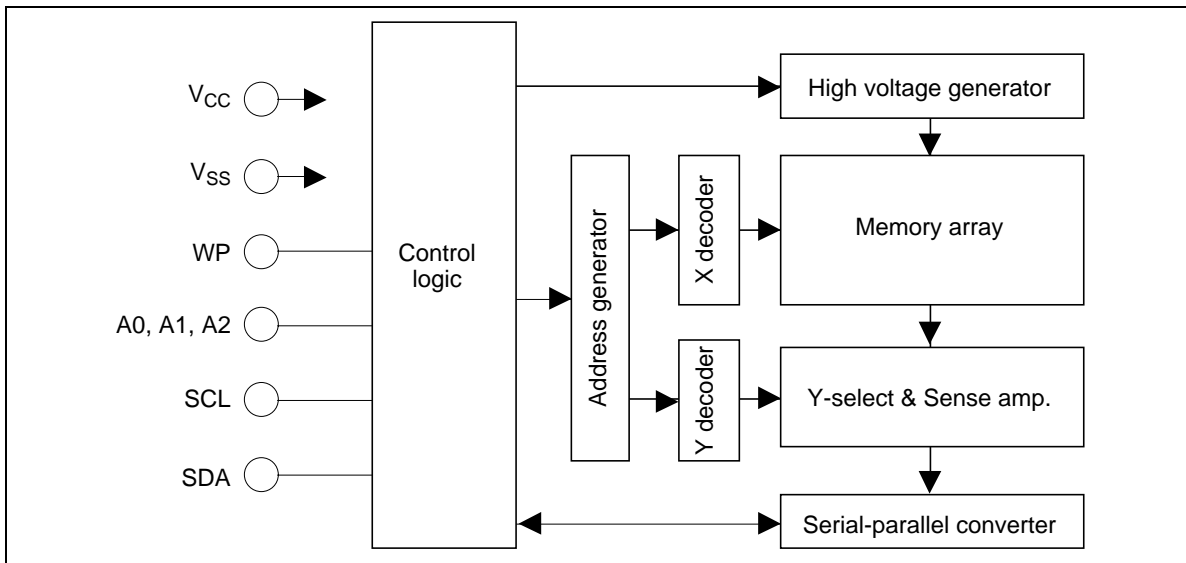
Pin Arrangement



Pin Description

| Pin name | Function |
|-----------------|--------------------------|
| A0 to A2 | Device address |
| SCL | Serial clock input |
| SDA | Serial data input/output |
| WP | Write protect |
| V _{CC} | Power supply |
| V _{SS} | Ground |
| NC | No connection |

Block Diagram



Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|--|-----------------|--|------|
| Supply voltage relative to V _{SS} | V _{CC} | -0.6 to +7.0 | V |
| Input voltage relative to V _{SS} | V _{in} | -0.5* ² to +7.0* ³ | V |
| Operating temperature range* ¹ | Topr | -40 to +85 | °C |
| Storage temperature range | Tstg | -55 to +125 | °C |

- Notes: 1. Including electrical characteristics and data retention.
 2. V_{in} (min): -3.0 V for pulse width ≤ 50 ns.
 3. Should not exceed V_{CC} + 1.0 V.

DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|-----------------------|-----------|---------------------|-----|---------------------|------|
| Supply voltage | V_{CC} | 1.8 | — | 5.5 | V |
| | V_{SS} | 0 | 0 | 0 | V |
| Input high voltage | V_{IH} | $V_{CC} \times 0.7$ | — | $V_{CC} + 0.5$ | V |
| Input low voltage | V_{IL} | -0.3^{*1} | — | $V_{CC} \times 0.3$ | V |
| Operating temperature | T_{opr} | -40 | — | +85 | °C |

Notes: 1. V_{IL} (min): -1.0 V for pulse width ≤ 50 ns.

DC Characteristics (Ta = -40 to +85°C, V_{CC} = 1.8 V to 5.5 V)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|--------------------------|-----------|-----|-----|-----|---------|--|
| Input leakage current | I_{LI} | — | — | 2.0 | μ A | $V_{CC} = 5.5$ V, $V_{in} = 0$ to 5.5 V |
| Output leakage current | I_{LO} | — | — | 2.0 | μ A | $V_{CC} = 5.5$ V, $V_{out} = 0$ to 5.5 V |
| Standby V_{CC} current | I_{SB} | — | 1.0 | 2.0 | μ A | $V_{in} = V_{SS}$ or V_{CC} |
| Read V_{CC} current | I_{CC1} | — | — | 1.0 | mA | $V_{CC} = 5.5$ V, Read at 400 kHz |
| Write V_{CC} current | I_{CC2} | — | — | 2.5 | mA | $V_{CC} = 5.5$ V, Write at 400 kHz |
| Output low voltage | V_{OL2} | — | — | 0.4 | V | $V_{CC} = 2.7$ to 5.5 V, $I_{OL} = 3.0$ mA |
| | V_{OL1} | — | — | 0.2 | V | $V_{CC} = 1.8$ to 2.7 V, $I_{OL} = 1.5$ mA |

Capacitance (Ta = +25°C, f = 1 MHz)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---------------------------------------|---------------|-----|-----|-----|------|-----------------|
| Input capacitance (A0 to A2, SCL, WP) | C_{in}^{*1} | — | — | 6.0 | pF | $V_{in} = 0$ V |
| Output capacitance (SDA) | C_{IO}^{*1} | — | — | 6.0 | pF | $V_{out} = 0$ V |

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics ($T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 1.8$ to 5.5 V)

Test Conditions

- Input pules levels:
 - $V_{IL} = 0.2 \times V_{CC}$
 - $V_{IH} = 0.8 \times V_{CC}$
- Input rise and fall time: ≤ 20 ns
- Input and output timing reference levels: $0.5 \times V_{CC}$
- Output load: TTL Gate + 100 pF

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|-----------------------------|--------------|------|--------|-----|--------|-------|
| Clock frequency | f_{SCL} | — | — | 400 | kHz | |
| Clock pulse width low | t_{LOW} | 1200 | — | — | ns | |
| Clock pulse width high | t_{HIGH} | 600 | — | — | ns | |
| Noise suppression time | t_I | — | — | 50 | ns | 1 |
| Access time | t_{AA} | 100 | — | 900 | ns | |
| Bus free time for next mode | t_{BUF} | 1200 | — | — | ns | |
| Start hold time | $t_{HD,STA}$ | 600 | — | — | ns | |
| Start setup time | $t_{SU,STA}$ | 600 | — | — | ns | |
| Data in hold time | $t_{HD,DAT}$ | 0 | — | — | ns | |
| Data in setup time | $t_{SU,DAT}$ | 100 | — | — | ns | |
| Input rise time | t_R | — | — | 300 | ns | 1 |
| Input fall time | t_F | — | — | 300 | ns | 1 |
| Stop setup time | $t_{SU,STO}$ | 600 | — | — | ns | |
| Data out hold time | t_{DH} | 50 | — | — | ns | |
| Write protect hold time | $t_{HD,WP}$ | 1200 | — | — | ns | |
| Write protect setup time | $t_{SU,WP}$ | 0 | — | — | ns | |
| Write cycle time | t_{WC} | — | — | 5 | ms | 2 |
| Erase/Write Endurance | — | — | 10^6 | — | cycles | 3 |

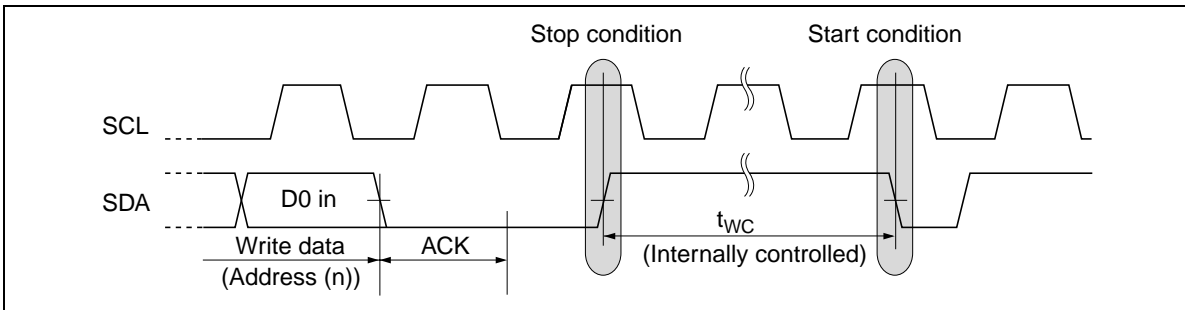
- Notes:
1. This parameter is sampled and not 100% tested.
 2. t_{WC} is the time from a stop condition to the end of internally controlled write cycle.
 3. This parameter is sampled and not 100% tested.
 - 10^6 Cycles ($T_a = 25^\circ\text{C}$)
 - 10^5 Cycles ($T_a = 85^\circ\text{C}$)

Timing Waveforms

Bus Timing



Write Cycle Timing



Pin Function

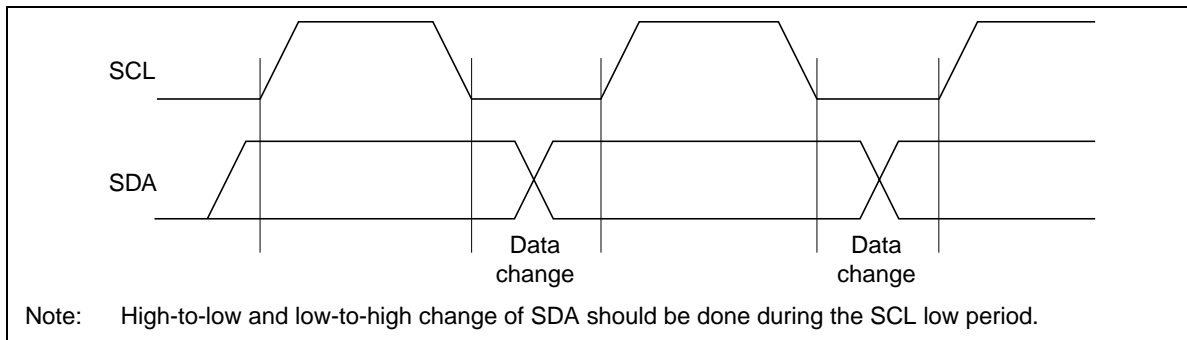
Serial Clock (SCL)

The SCL pin is used to control serial input/output data timing. The SCL input is used to positive edge clock data into EEPROM device and negative edge clock data out of each device. Maximum clock rate is 400 kHz.

Serial Input/Output Data (SDA)

The SDA pin is bidirectional for serial data transfer. The SDA pin needs to be pulled up by resistor as that pin is open-drain driven structure. Use proper resistor value for your system by considering V_{OL} , I_{OL} and the SDA pin capacitance. Except for a start condition and a stop condition which will be discussed later, the SDA transition needs to be completed during the SCL low period.

Data Validity (SDA data change timing waveform)



R1EX24004AxxS0A

Device Address (A0, A1, A2)

Four devices can be wired for one common data bus line as maximum. Device address pins are used to distinguish each device and device address pins should be connected to V_{CC} or V_{SS} . When device address code provided from SDA pin matches corresponding hard-wired device address pins A0 to A2, that one device can be activated.

Pin Connections for A0 to A2

| Memory size | Max connect number | Pin connection | | | Note |
|-------------|--------------------|----------------------|----------------------|---------------|------------------------------|
| | | A2 | A1 | A0 | |
| 4k bit | 4 | V_{CC}/V_{SS}^{*1} | V_{CC}/V_{SS}^{*1} | \times^{*2} | Use A0 for memory address a8 |

Note: 1. During floating, " V_{CC}/V_{SS} " are fixed to V_{SS} .
2. Floating state can be possible.

Write Protect (WP)

When the Write Protect pin (WP) is high, the write protection feature is enabled and operates as shown in the following table.

Also, acknowledgment "0" is outputted after inputting device address and memory address. After inputting write data, acknowledgment "1" (**NO ACK**) is outputted.

When the WP is low, write operation for all memory arrays are allowed. The read operation is always activated irrespective of the WP pin status.

Write Protect Area

| WP pin status | Write protect area |
|---------------|-----------------------------|
| | 4k bit |
| V_{IH} | Full (4k bit) |
| V_{IL} | Normal read/write operation |

Functional Description

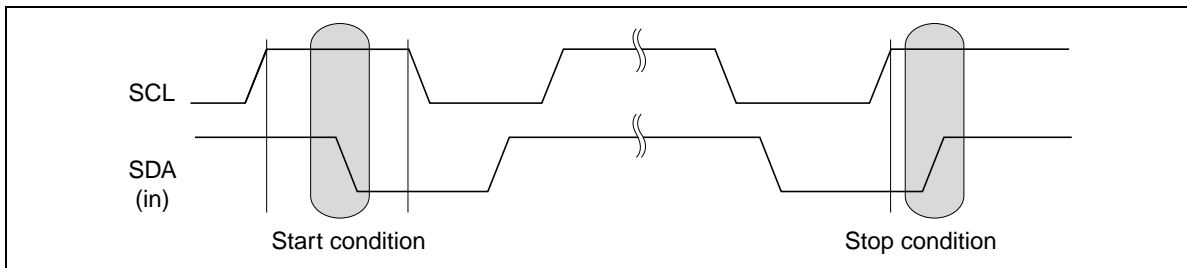
Start Condition

A high-to-low transition of the SDA with the SCL high is needed in order to start read, write operation (See start condition and stop condition).

Stop Condition

A low-to-high transition of the SDA with the SCL high is a stop condition. The stand-by operation starts after a read sequence by a stop condition. In the case of write operation, a stop condition terminates the write data inputs and place the device in a internally-timed write cycle to the memories. After the internally-timed write cycle which is specified as t_{wc} , the device enters a standby mode (See write cycle timing).

Start Condition and Stop Condition



Acknowledge

All addresses and data words are serially transmitted to and from in 8-bit words. The receiver sends a zero to acknowledge that it has received each word. This happens during ninth clock cycle. The transmitter keeps bus open to receive acknowledgment from the receiver at the ninth clock. In the write operation, EEPROM sends a zero to acknowledge after receiving every 8-bit words. In the read operation, EEPROM sends a zero to acknowledge after receiving the device address word. After sending read data, the EEPROM waits acknowledgment by keeping bus open. If the EEPROM receives zero as an acknowledge, it sends read data of next address. If the EEPROM receives acknowledgment "1" (no acknowledgment) and a following stop condition, it stops the read operation and enters a stand-by mode. If the EEPROM receives neither acknowledgment "0" nor a stop condition, the EEPROM keeps bus open without sending read data.

Acknowledge Timing Waveform



Device Addressing

The EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or a write operation. The device address word consists of 4-bit device code, 3-bit device address code and 1-bit read/write(R/W) code. The most significant 4-bit of the device address word are used to distinguish device type and this EEPROM uses “1010” fixed code. The device address word is followed by the 2-bit device address code A2, A1 memory address a8. The device address code selects one device out of four devices which are connected to the bus. This means that the device is selected if the inputted 2-bit device address code are equal to the corresponding hard-wired A2 , A1 pin status.

The eighth bit of the device address word is the read/write(R/W) bit. A write operation is initiated if this bit is “0” and a read operation is initiated if this bit is “1” . The EEPROM turns to a stand-by state if the device code is not “1010” or device address code doesn’t coincide with status of the correspond hard-wired device address pins A2 to A0.

Device Address Word

| Device address word (8-bit) | | | | | | | | |
|-----------------------------|---------------------|---|---|---|---------------------|----|----|------------------------|
| | Device code (fixed) | | | | Device address code | | | R/W code ^{*1} |
| 4k | 1 | 0 | 1 | 0 | A2 | A1 | a8 | R/W |

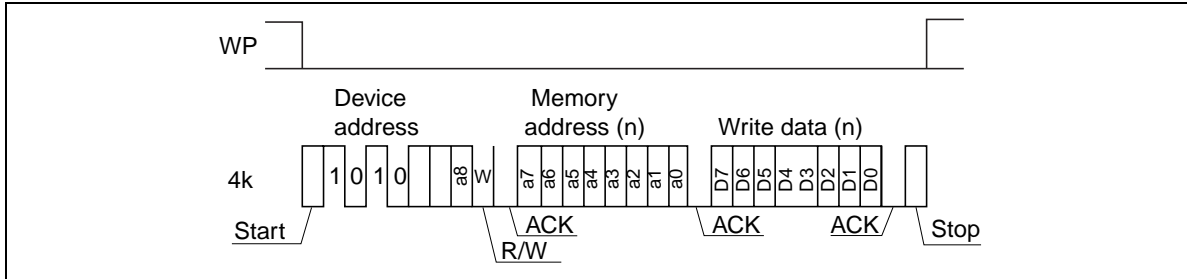
Note: 1. R/W=“1” is read and R/W = “0” is write.

Write Operations(WP=Low)

Byte Write: (Write operation during WP=Low status)

A write operation requires an 8-bit device address word with R/W = "0". Then the EEPROM sends acknowledgment "0" at the ninth clock cycle. After these, the 4k bit EEPROM receives 8-bit memory address words. Upon receipt of this memory address, the EEPROM outputs acknowledgment "0" and receives a following 8-bit write data. After receipt of write data, the EEPROM outputs acknowledgment "0". If the EEPROM receives a stop condition, the EEPROM enters an internally-timed write cycle and terminates receipt of SCL, SDA inputs until completion of the write cycle. The EEPROM returns to a standby mode after completion of the write cycle.

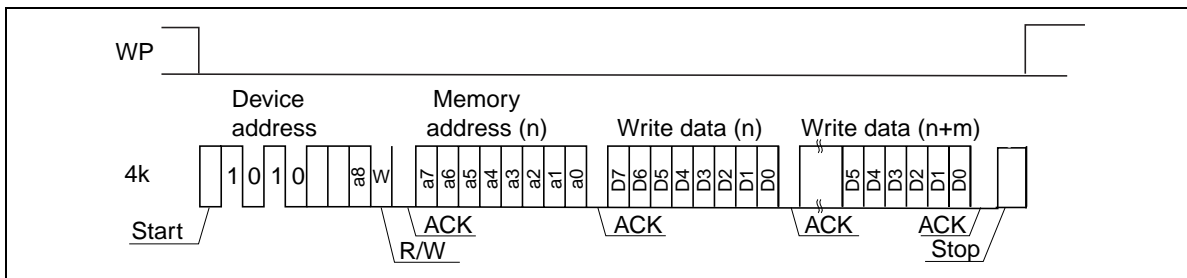
Byte Write Operation



Page Write:

The EEPROM is capable of the page write operation which allows any number of bytes up to 16 bytes to be written in a single write cycle. The page write is the same sequence as the byte write except for inputting the more write data. The page write is initiated by a start condition, device address word, memory address(n) and write data (Dn) with every ninth bit acknowledgment. The EEPROM enters the page write operation if the EEPROM receives more write data (Dn+1) instead of receiving a stop condition. The a0 to a3 address bits are automatically incremented upon receiving write data (Dn+1). The EEPROM can continue to receive write data up to 16 bytes. If the a0 to a3 address bits reaches the last address of the page, the a0 to a3 address bits will roll over to the first address of the same page and previous write data will be overwritten. Upon receiving a stop condition, the EEPROM stops receiving write data and enters internally-timed write cycle.

Page Write Operation

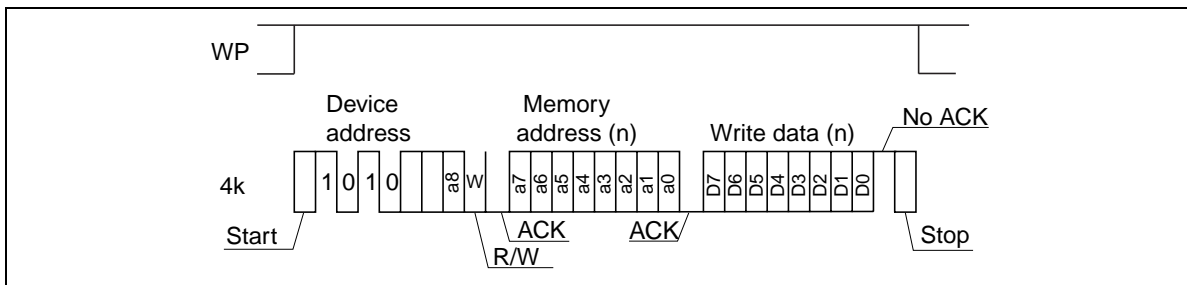


Write Operations(WP=High)

Byte Write: (Write operation during WP=High status)

A write operation requires an 8-bit device address word with R/W = "0". Then the EEPROM sends acknowledgment "0" at the ninth clock cycle. After these, the 4k bit EEPROM receives 8-bit memory address. Upon receipt of this memory address, the EEPROM outputs acknowledgment "0". After receipt of 8-bit write data, the EEPROM outputs acknowledgment "1" (**NO ACK**). Then the EEPROM write operations are not allowed.

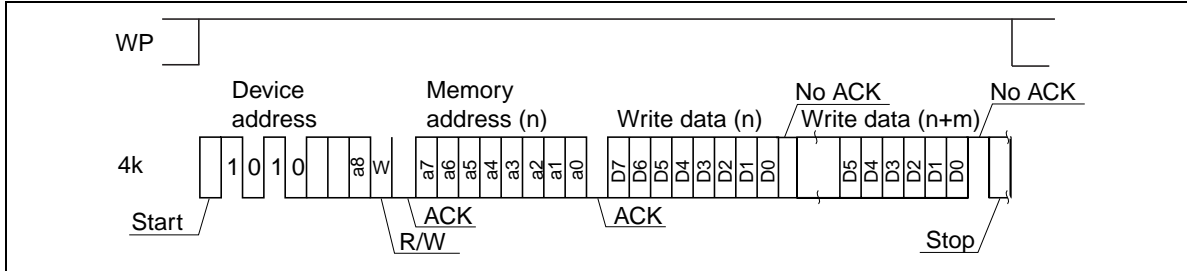
Byte Write Operation



Page Write:

The page write is the same sequence as the byte write. The page write is initiated by a start condition, device address word and memory address(n) with every ninth bit acknowledgment "0". But after inputting write data(Dn) , the EEPROM outputs acknowledgment "1"(NO ACK). Then the EEPROM write operations are not allowed.

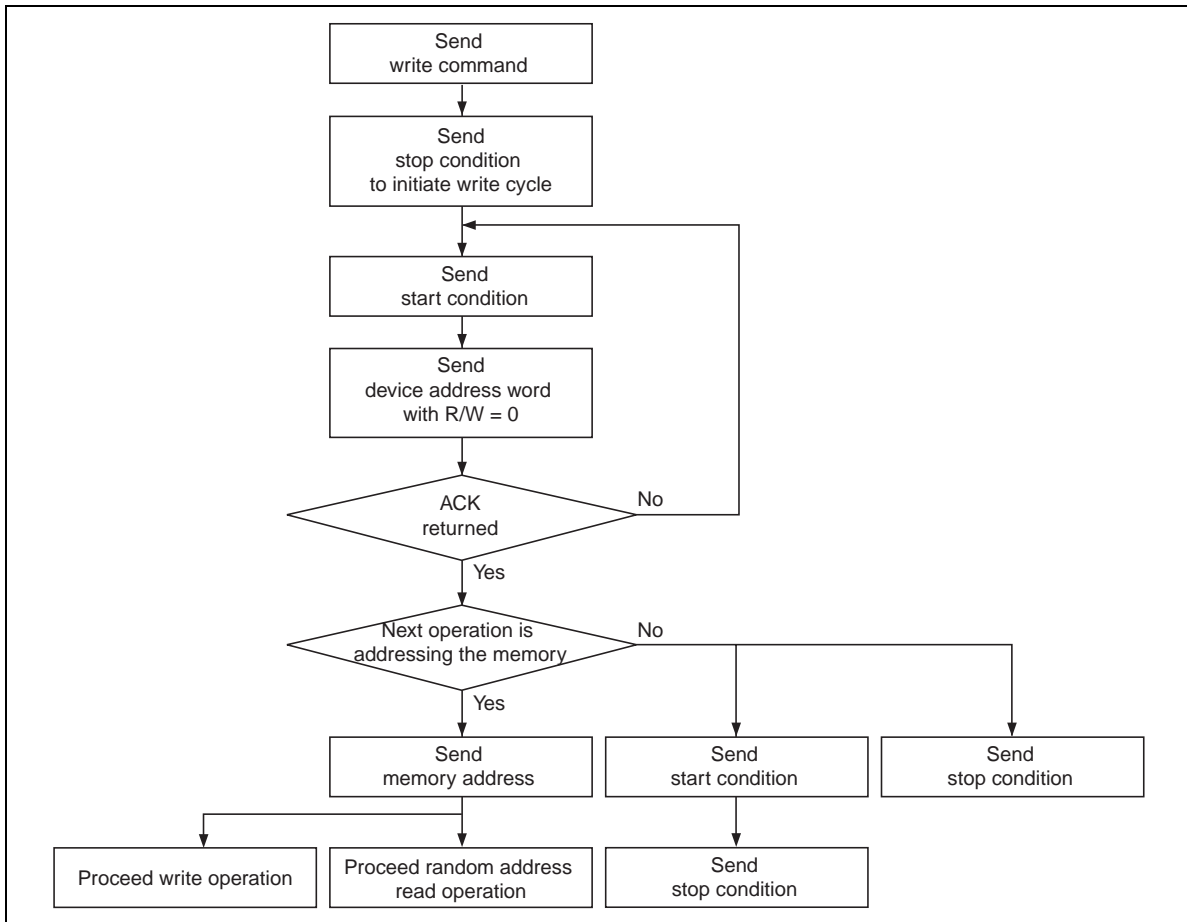
Page Write Operation



Acknowledge Polling:

Acknowledge polling feature is used to show if the EEPROM is in a internally-timed write cycle or not. This feature is initiated by the stop condition after inputting write data. This requires the 8-bit device address word following the start condition during a internally-timed write cycle. Acknowledge polling will operate when the R/W code = "0". Acknowledgment "1" (no acknowledgment) shows the EEPROM is in a internally-timed write cycle and acknowledgment "0" shows that the internally-timed write cycle has completed. See Write Cycle Polling using ACK.

Write Cycle Polling Using ACK



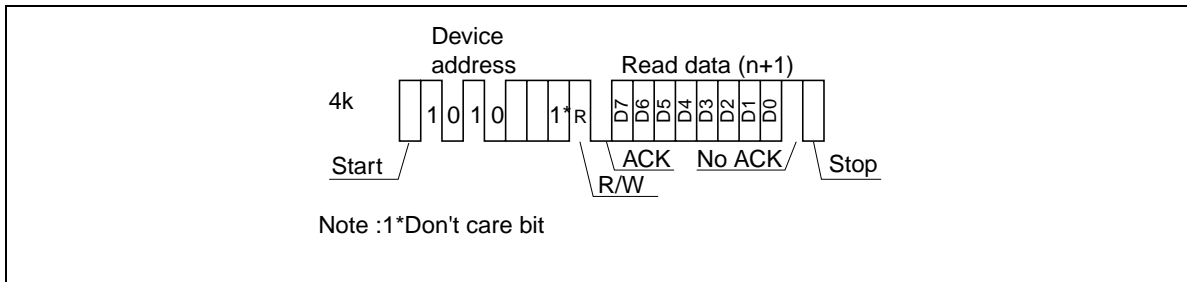
Read Operation

There are three read operations: current address read, random read, and sequential read. Read operations are initiated the same way as write operations with the exception of R/W = "1".

Current Address Read:

The internal address counter maintains the last address accessed during the last read or write operation, with incremented by one. Current address read accesses the address kept by the internal address counter. After receiving a start condition and the device address word (R/W is "1"), the EEPROM outputs the 8-bit current address data from the most significant bit following acknowledgment "0". If the EEPROM receives acknowledgment "1" (no acknowledgment) and a following stop condition, the EEPROM stops the read operation and is turned to a standby state. In case the EEPROM has accessed the last address of the last page at previous read operation, the current address will roll over and returns to zero address. In case the EEPROM has accessed the last address of the page at previous write operation, the current address will roll over within page addressing and returns to the first address in the same page. The current address is valid while power is on. The current address after power on will be indefinite. The random read operation described below is necessary to define the memory address.

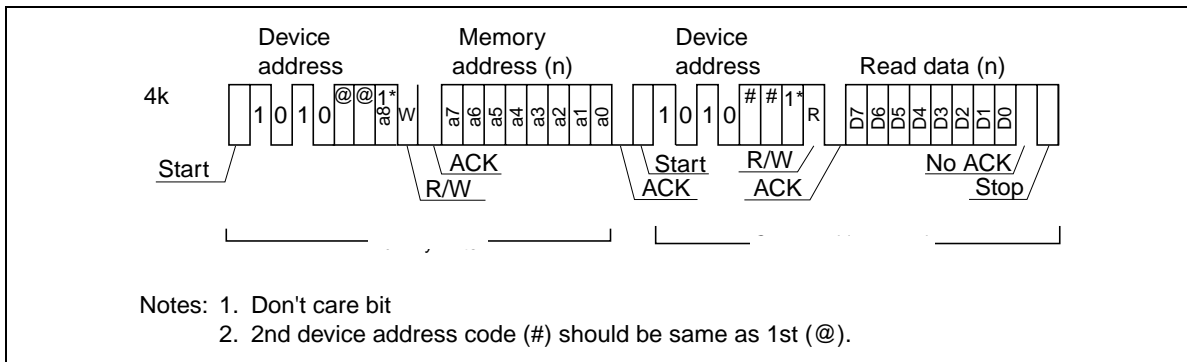
Current Address Read Operation



Random Read:

This is a read operation with defined read address. A random read requires a dummy write to set read address. The EEPROM receives a start condition, device address word (R/W=0) and memory address 8-bit sequentially. The EEPROM outputs acknowledgment “0” after receiving memory address then enters a current address read with receiving a start condition. The EEPROM outputs the read data of the address which was defined in the dummy write operation. After receiving acknowledgment “1”(no acknowledgment) and a following stop condition, the EEPROM stops the random read operation and returns to a standby state.

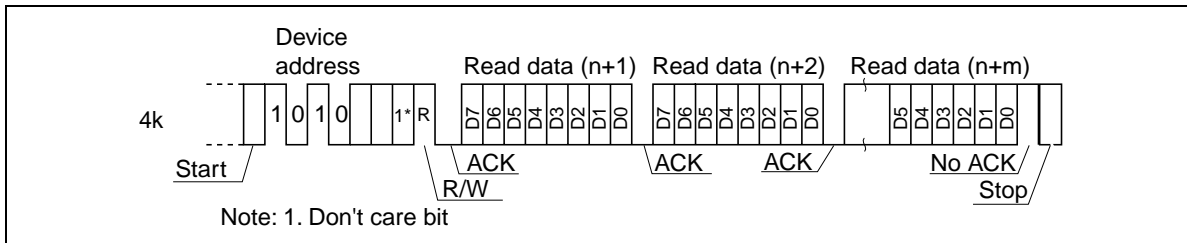
Random Read Operation



Sequential Read:

Sequential reads are initiated by either a current address read or a random read. If the EEPROM receives acknowledgment “0” after 8-bit read data, the read address is incremented and the next 8-bit read data are coming out. This operation can be continued as long as the EEPROM receives acknowledgment “0”. The address will roll over and returns address zero if it reaches the last address of the last page. The sequential read can be continued after roll over. The sequential read is terminated if the EEPROM receives acknowledgment “1” (no acknowledgment) and a following stop condition.

Sequential Read Operation



Notes

Data Protection at V_{cc} On/Off

When V_{cc} is turned on or off, noise on the SCL and SDA inputs generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to unintentional program mode. To prevent this unintentional programming, this EEPROM has a power on reset function. Be careful of the notices described below in order for the power on reset function to operate correctly.

- SCL and SDA should be fixed to V_{cc} or V_{ss} during V_{cc} on/off. Low to high or high to low transition during V_{cc} on/off may cause the trigger for the unintentional programming.
- V_{cc} should be turned off after the EEPROM is placed in a standby state.
- V_{cc} should be turned on from the ground level(V_{ss}) in order for the EEPROM not to enter the unintentional programming mode.
- V_{cc} turn on speed should be longer than 10 μ s.

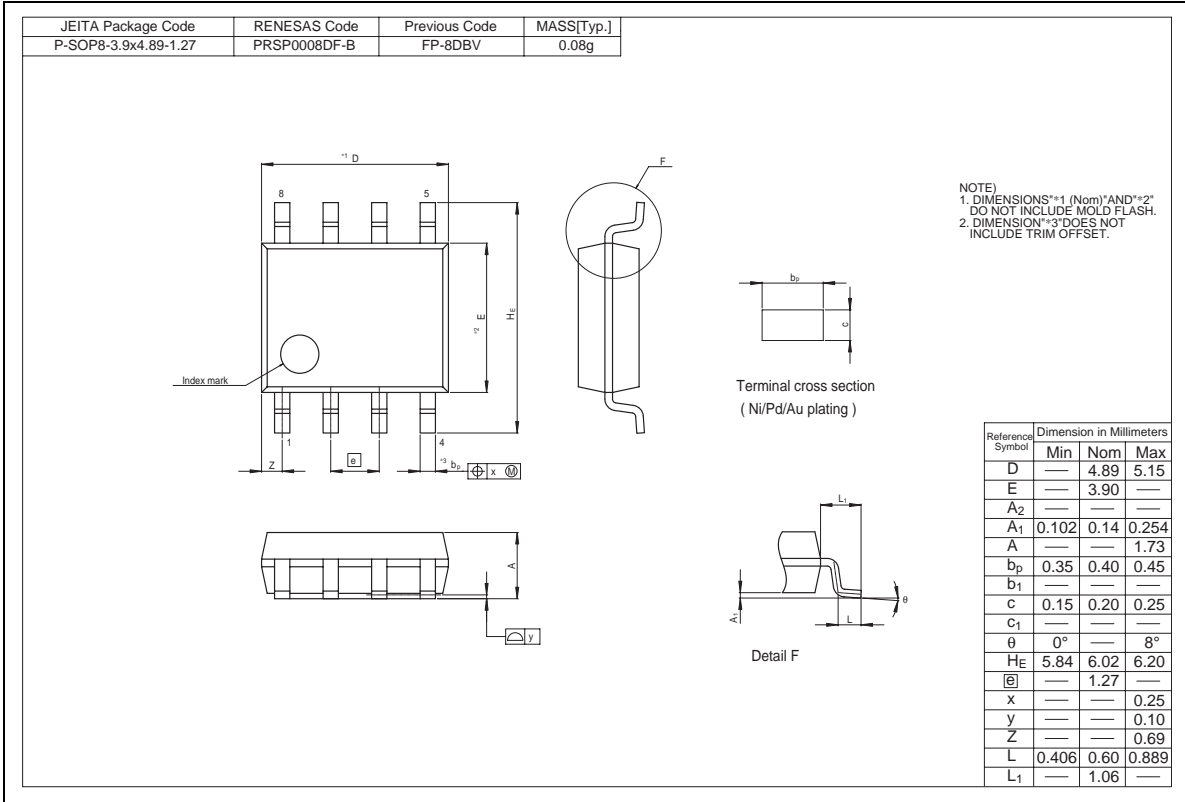
Noise Suppression Time

This EEPROM have a noise suppression function at SCL and SDA inputs, that cut noise of width less than 50 ns. Be careful not to allow noise of width more than 50 ns.

R1EX24004AxxS0A

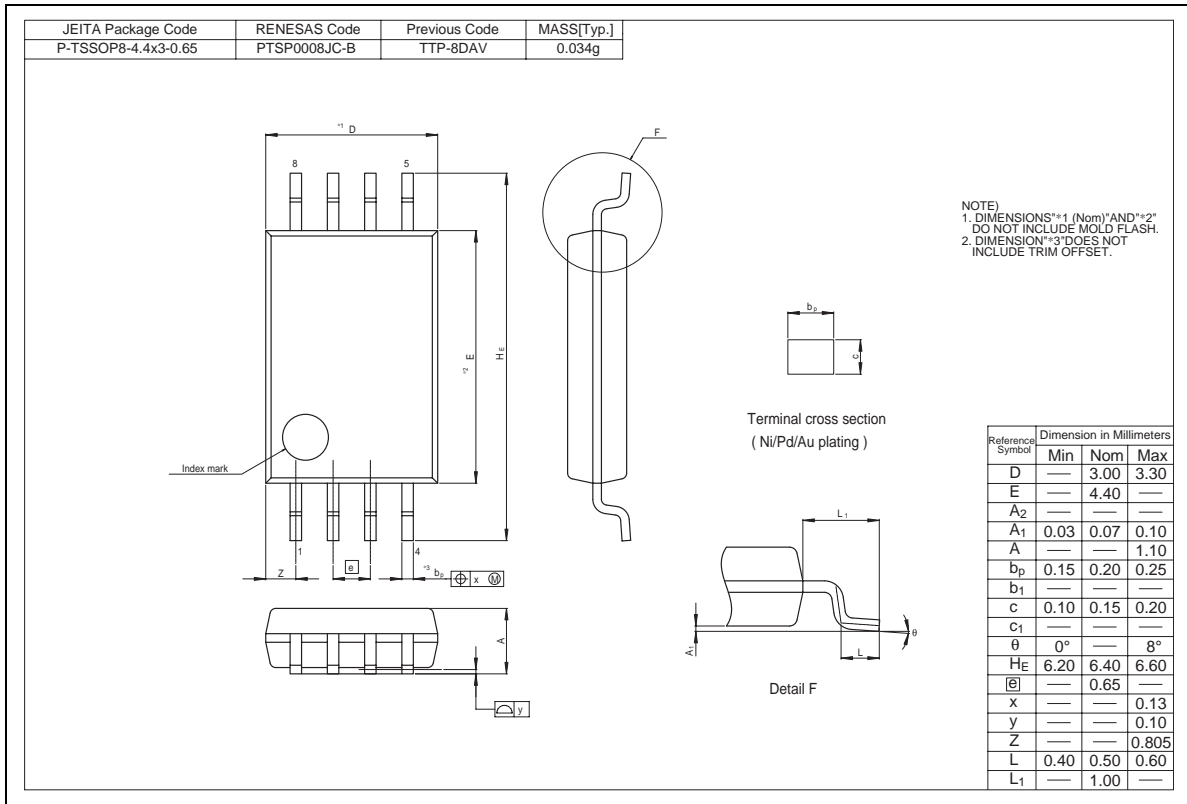
Package Dimensions

R1EX24004ASAS0A (PRSP0008DF-B / Previous Code: FP-8DBV)



R1EX24004AxxS0A

R1EX24004ATAS0A (PTSP0008JC-B / Previous Code: TTP-8DAV)



Revision History**R1EX24004AxxS0A Data Sheet**

| Rev. | Date | Contents of Modification | |
|------|-----------------|--------------------------|-------------------------|
| | | Page | Description |
| 0.01 | Dec. 26, 2007 | — | Initial issue |
| 1.00 | April. 21, 2008 | — | Deletion of preliminary |

Notes:

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (<http://www.renesas.com>)
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guarantees regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
 - (1) artificial life support devices or systems
 - (2) surgical implantations
 - (3) healthcare intervention (e.g., excision, administration of medication, etc.)
 - (4) any other purposes that pose a direct threat to human lifeRenesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510