

RFM10N12L/15L RFP10N12L/15L

N-Channel Logic Level Power Field-Effect Transistors (L²FET)

August 1991

Features

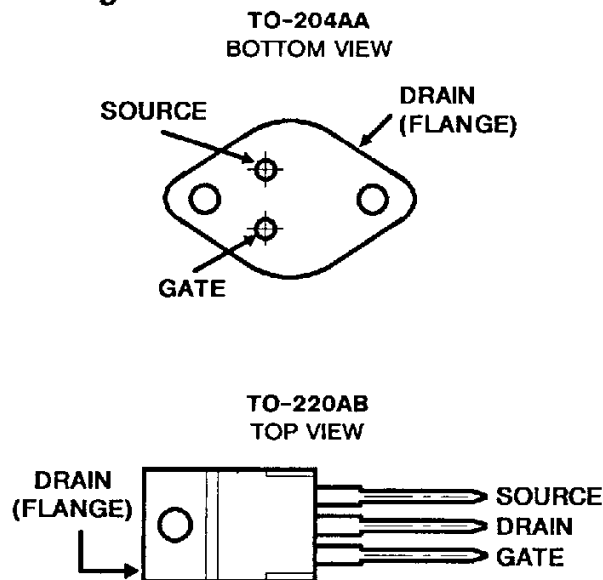
- 10A, 120V and 150V
- $r_{DS(ON)} = 0.3\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Description

The RFM10N12L and RFM10N15L and the RFP10N12L and RFP10N15L are N-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

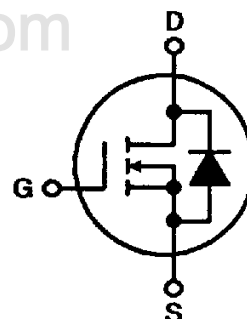
The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$) Unless Otherwise Specified

	RFM10N12L	RFM10N15L	RFP10N12L	RFP10N15L	UNITS	
Drain-Source Voltage	V_{DS}	120	150	120	150	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	120	150	120	150	V
Continuous Drain Current						
RMS Continuous	I_D	10	10	10	10	A
Pulsed Drain Current	I_{DM}	25	25	25	25	A
Gate-Source Voltage	V_{GS}	± 10	± 10	± 10	± 10	V
Maximum Power Dissipation						
$T_C = +25^\circ\text{C}$	P_D	75	75	60	60	W
Above $T_C = +25^\circ\text{C}$, Derate Linearly		0.6	0.6	0.48	0.48	W/ $^\circ\text{C}$
Operating and Storage Junction	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	$^\circ\text{C}$
Temperature Range						

Specifications RFM10N12L, RFM10N15L, RFP10N12L, RFP10N15L**ELECTRICAL CHARACTERISTICS, At Case Temperature ($T_C = 25^\circ\text{C}$) unless otherwise specified**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10N12L RFP10N12L		RFM10N15L RFP10N15L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 1\text{ mA}$ $V_{GS} = 0$	120	—	150	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$ $I_D = 2\text{ mA}$	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}$	—	1	—	—	μA
		$V_{DS} = 120\text{ V}$	—	—	—	1	
		$T_C = 125^\circ\text{C}$	—	50	—	—	
		$V_{DS} = 100\text{ V}$	—	—	—	50	
		$V_{DS} = 120\text{ V}$	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 10\text{ V}$ $V_{DS} = 0$	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}^a$	$I_D = 5\text{ A}$ $V_{GS} = 5\text{ V}$	—	1.5	—	1.5	V
		$I_D = 10\text{ A}$ $V_{GS} = 5\text{ V}$	—	4	—	4	
Static Drain-Source On Resistance	$r_{DS(on)}^a$	$I_D = 5\text{ A}$ $V_{GS} = 5\text{ V}$	—	0.3	—	0.3	Ω
Forward Transconductance	g_{fs}^a	$V_{DS} = 10\text{ V}$ $I_D = 5\text{ A}$	4.0	—	4.0	—	mho
Input Capacitance	C_{iss}	$V_{DS} = 25\text{ V}$	—	1200	—	1200	pF
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	—	250	—	250	
Reverse-Transfer Capacitance	C_{rss}	$f = 1\text{ MHz}$	—	120	—	120	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 75\text{ V}$ $I_D = 5\text{ A}$ $R_{gen} = \infty$ $R_{gs} = 6.25\ \Omega$ $V_{GS} = 5\text{ V}$	15(typ)	60	15(typ)	60	ns
Rise Time	t_r		50(typ)	135	50(typ)	135	
Turn-Off Delay Time	$t_{d(off)}$		90(typ)	135	90(typ)	135	
Fall Time	t_f		90(typ)	135	90(typ)	135	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM10N12L, RFM10N15L	—	1.67	—	1.67	$^\circ\text{C/W}$
		RFP10N12L, RFP10N15L	—	2.083	—	2.083	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10N12L RFP10N12L		RFM10N15L RFP10N15L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}^a	$I_{SD} = 5\text{ A}$	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	$I_F = 4\text{ A}$, $dI_F/dt = 100\text{ A}/\mu\text{s}$	150 (typ)		150 (typ)		ns

^a Pulse Test Width $\leq 300\ \mu\text{s}$, Duty cycle $\leq 2\%$

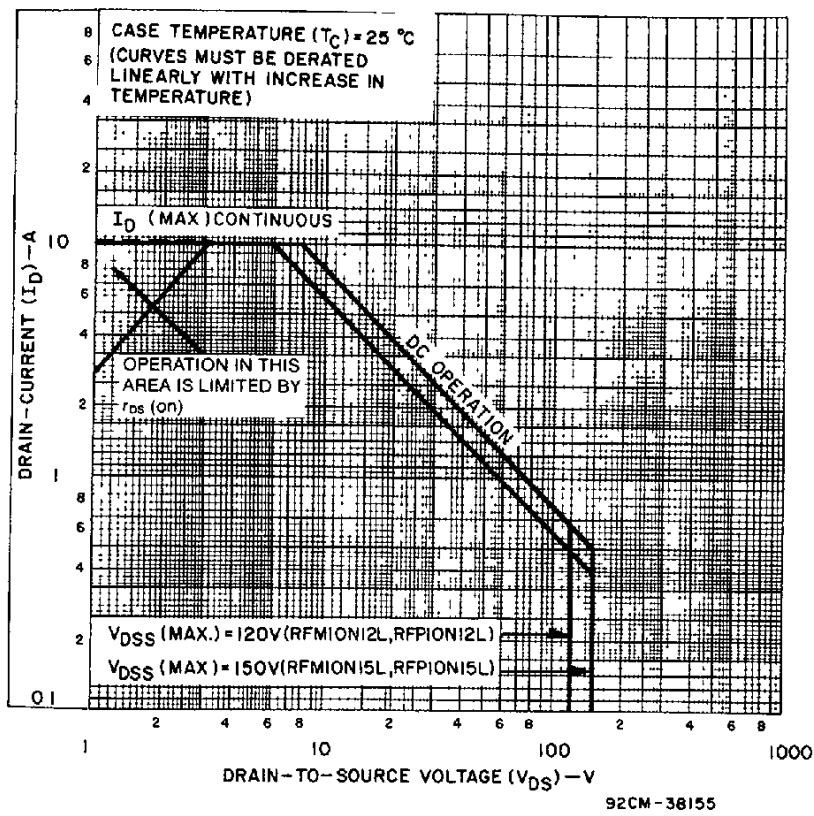


Fig. 1 - Maximum safe operating areas for all types.

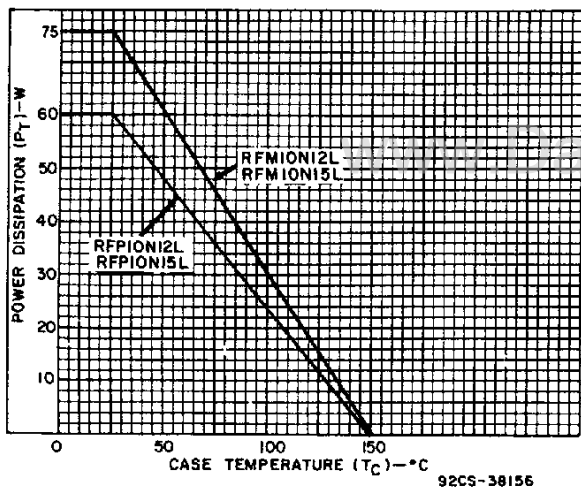


Fig 2 - Power vs temperature derating curve for all types.

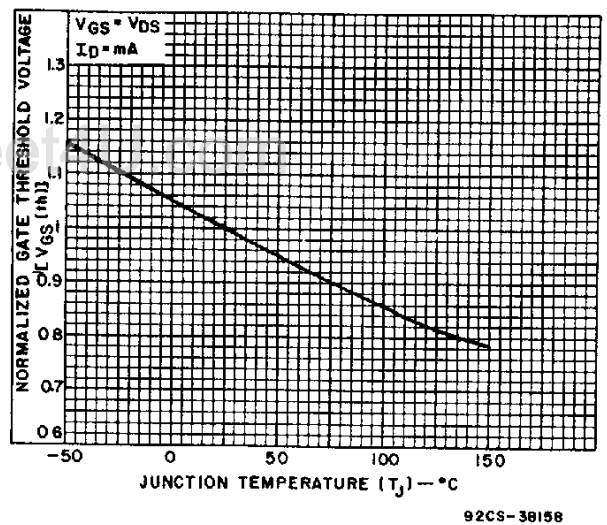


Fig 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

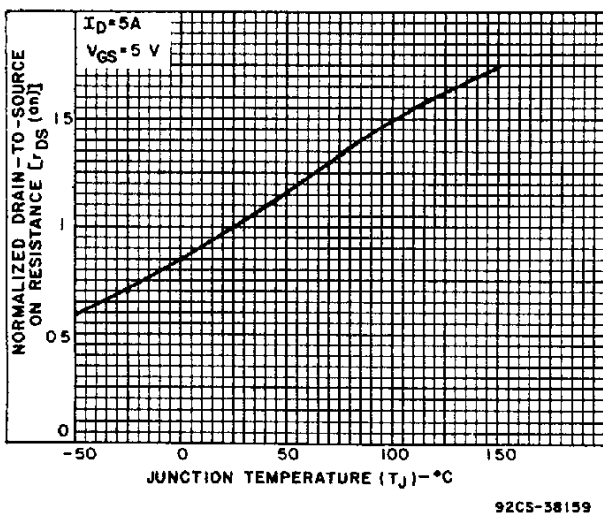


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

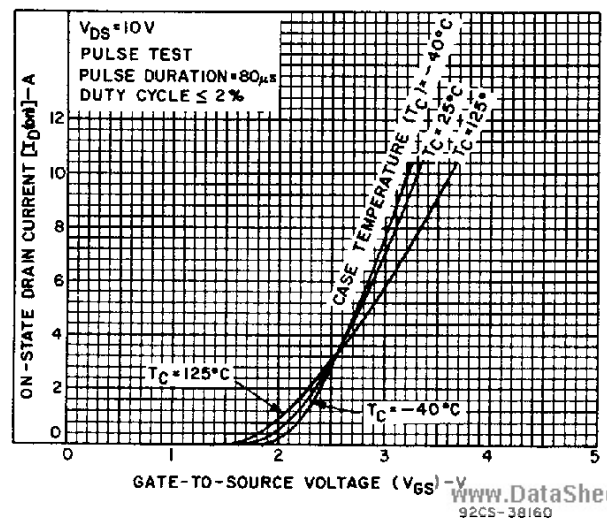


Fig. 5 - Typical transfer characteristics for all types.

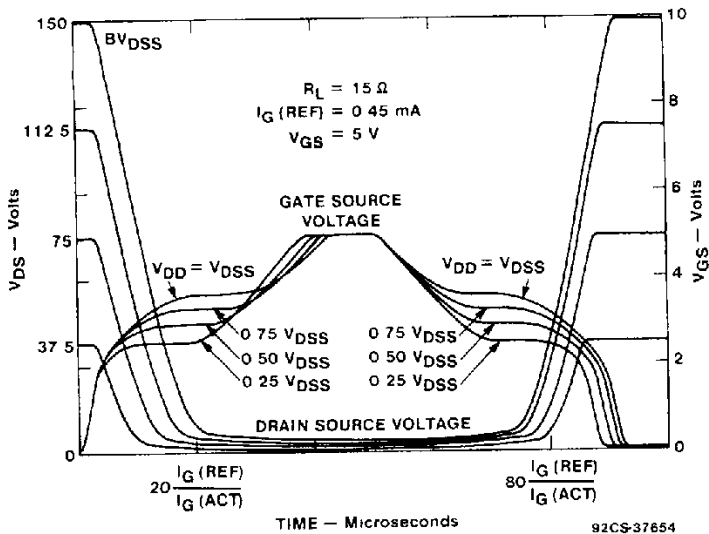


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

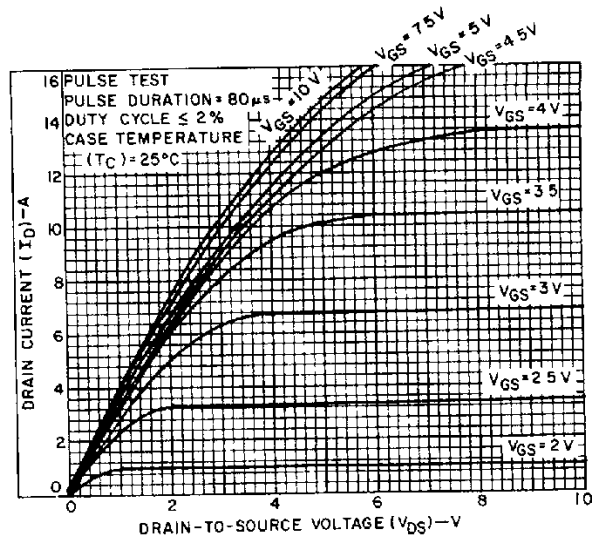


Fig 7 - Typical saturation characteristics for all types

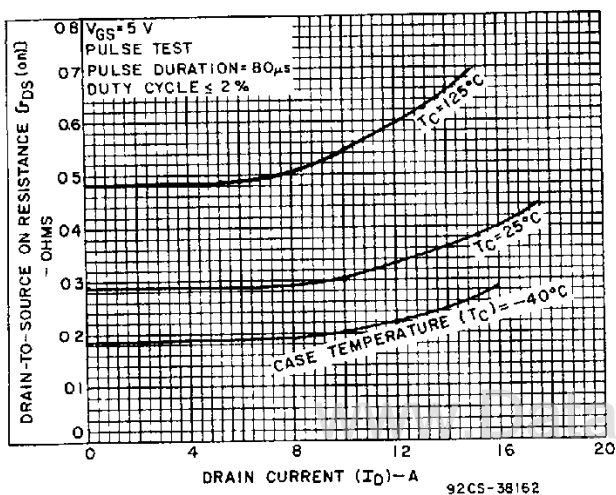


Fig 8 - Typical drain-to-source on resistance as a function of drain current for all types.

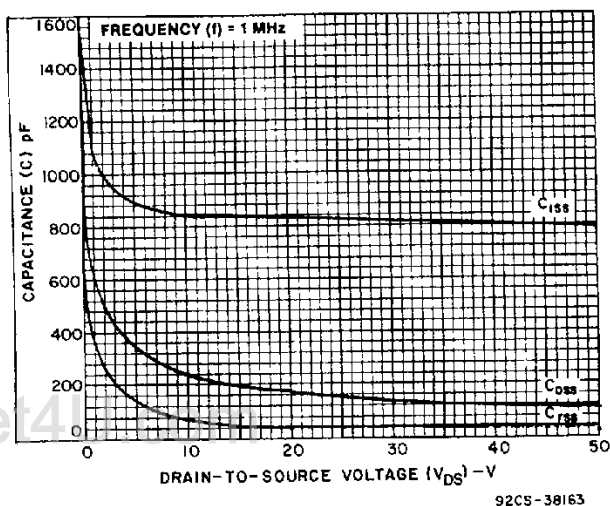


Fig 9 - Capacitance as a function of drain-to-source voltage for all types

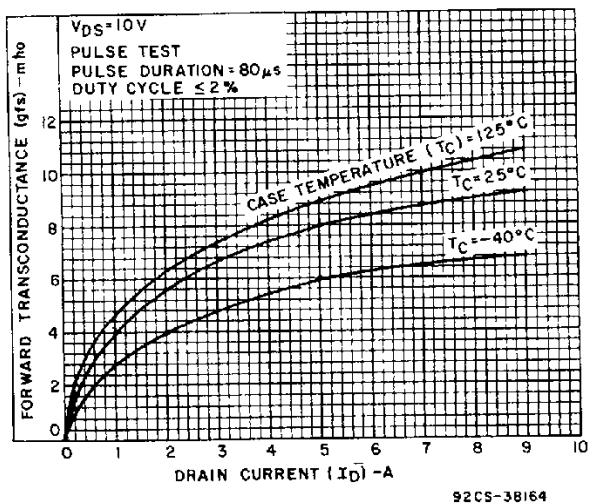


Fig 10 - Typical forward transconductance as a function of drain current for all types.

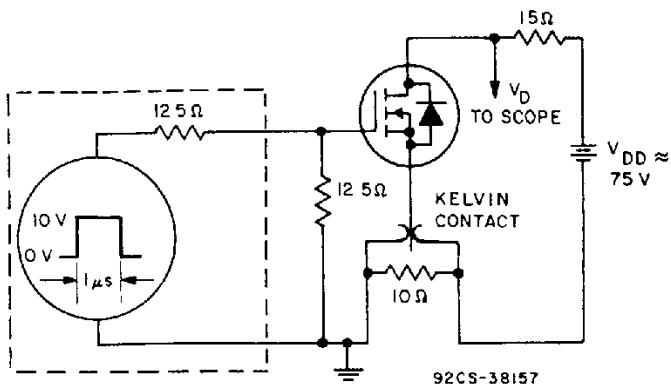


Fig 11 - Switching Time Test Circuit