Memory
ATL60 SRAMs
Compiled Gate Level

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Compiled Gate Level SRAMs

Atmel offers a variety of compiled gate level SRAMs for the ATL60 series of gate arrays. These static asynchronous SRAMs utilize the personalization layers and occupy standard gate array sites. The SRAMs come in either dual port or single port architectures.

The dual port SRAMs have two sets of address inputs, a read address (RD_ADDR) and a write address (WR_ADDR). The output of the SRAM is the word which is pointed to by the read address. When the WE (Write Enable) input goes low, the word on the DIN bus is written to the address specified by the write address.

The single port SRAMs have one set of address inputs (ADDR) which control both write and read operations. The output of the SRAM is always the word which is pointed to by the address inputs. When the WRITE input goes low, the word on the DIN bus is written to the address specified by the address input.

Both single port and dual port SRAMs have enables (OE) on their outputs. The outputs stay high while the output enable signal is high.

The SRAMs can be compiled in depths ranging from 2 words to 32 words. The following tables give size information for some common SRAM sizes. Contact Atmel for the exact size of any SRAM not listed.

Common Single Port SRAM Sizes

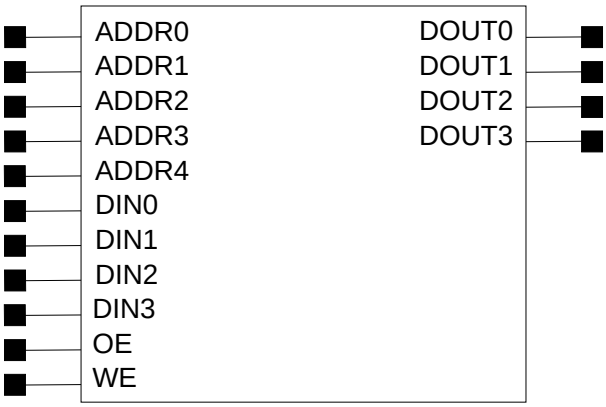
		SRAM Width (bits)				
		8	**12**	**16**	**24**	**32**
Depth (words)	**4**	294 sites PRAM4X8SUB32	378 sites PRAM4X12SUB32	462 sites PRAM4X16SUB32	630 sites PRAM4X24SUB32	798 sites PRAM4X32SUB32
	8	490 sites PRAM8X8SUB32	630 sites PRAM8X12SUB32	770 sites PRAM8X16SUB32	1050 sites PRAM8X24SUB32	1330 sites PRAM8X32SUB32
	12	686 sites PRAM12X8SUB32	882 sites PRAM12X12SUB32	1078 sites PRAM12X16SUB32	1470 sites PRAM12X24SUB32	1862 sites PRAM12X32SUB32
	16	882 sites PRAM16X8SUB32	1134 sites PRAM16X12SUB32	1386 sites PRAM16X16SUB32	1890 sites PRAM16X24SUB32	2394 sites PRAM16X32SUB32
	24	1274 sites PRAM24X8	1638 sites PRAM24X12	2002 sites PRAM24X16	2730 sites PRAM24X24	3458 sites PRAM24X32
	32	1666 sites PRAM32X8	2142 sites PRAM32X12	2618 sites PRAM32X16	3570 sites PRAM32X24	4522 sites PRAM32X32

Common Dual Port SRAM Sizes

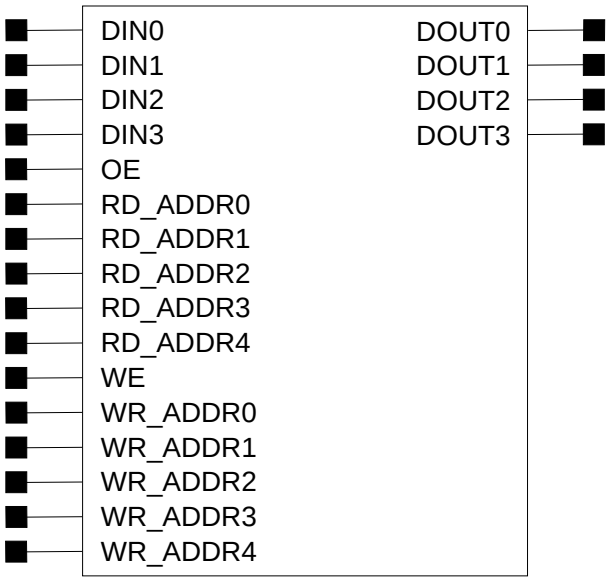
		SRAM Width (bits)				
		8	**12**	**16**	**24**	**32**
DEPTH (words)	**4**	360 sites PRAM4X8DSUB32	456 sites PRAM4X12DSUB32	552 sites PRAM4X16DSUB32	744 sites PRAM4X24DSUB32	936 sites PRAM4X32DSUB32
	8	570 sites PRAM8X8DSUB32	722 sites PRAM8X12DSUB32	874 sites PRAM8X16DSUB32	1178 sites PRAM8X24DSUB32	1482 sites PRAM8X32DSUB32
	12	780 sites PRAM12X8DSUB32	988 sites PRAM12X12DSUB32	1196 sites PRAM12X16DSUB32	1612 sites PRAM12X24DSUB32	2028 sites PRAM12X32DSUB32
	16	990 sites PRAM16X8DSUB32	1254 sites PRAM16X12DSUB32	1518 sites PRAM16X16DSUB32	2046 sites PRAM16X24DSUB32	2574 sites PRAM16X32DSUB32
	24	1410 sites PRAM24X8D	1786 sites PRAM24X12D	2162 sites PRAM24X16D	2914 sites PRAM24X24D	3666 sites PRAM24X32D
	32	1830 sites PRAM32X8D	2318 sites PRAM32X12D	2806 sites PRAM32X16D	3782 sites PRAM32X24D	4758 sites PRAM32X32D

Below are symbols for 4 x 4 single and dual port SRAMs (PRAM4X4SUB32 and PRAM4X4SUB32). Note that the unused address inputs must be tied to VSS or the SRAM will not function properly (i.e. ADDR4 is tied low for SRAMs smaller than 18 words, ADDR3 for SRAMs smaller than 10 words, ADDR2 for SRAMs smaller than 6 words, and ADDR1 for a 2 word SRAM). Unused RD_ADDR and WR_ADDR inputs need to be tied to VSS for dual port SRAMs. The SRAMs can be multiplexed to create a deeper SRAM.

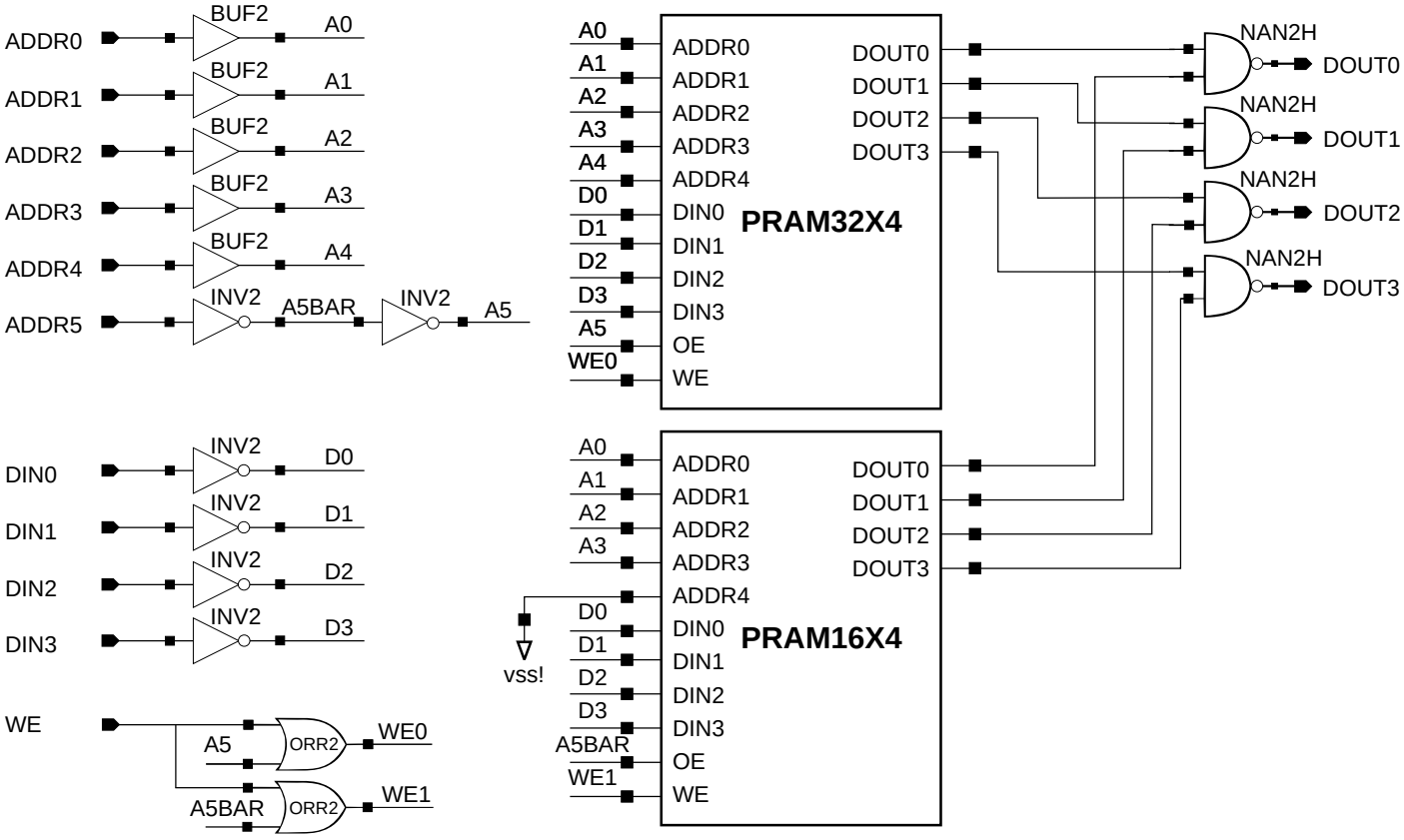
PRAM4X4SUB32



PRAM4X4DSUB32



PRAM48X4



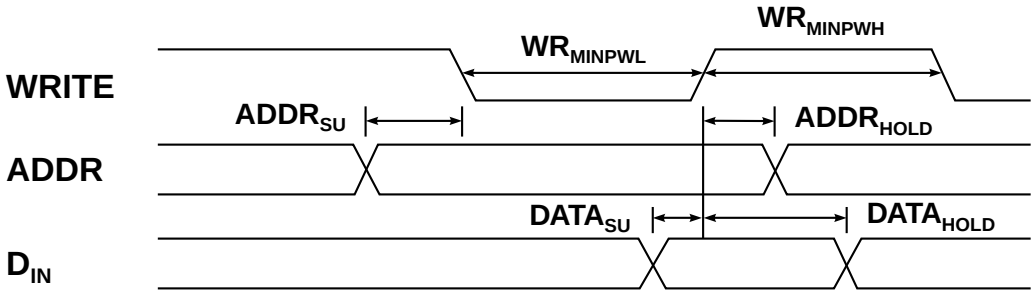
The following pages contain the SRAM write and read timing which was gathered from running Spice simulations. The write timing was determined by measuring the propagation delay from the WRITE, ADDR, and DIN pins to the memory latch bit on a large (32x36) and small (2x2) SRAM. The times given were measured from the input pins to when the actual data in memory changed. This was done by initializing the SRAM to a specific state such that if only the input pin under analysis changed, the memory bit would be changed. The delays were measured for the memory bit rising and falling. The longest path to a memory latch bit on the large SRAM represents the maximum delay and the shortest path to a memory latch bit on the small SRAM represents the minimum delay. The setup and hold timing were derived from these delays. The equations used are given with the specifications. The read timing was determined by measuring the propagation delay through the SRAMs. These Spice simulations were run with best, typical, and worst temperature and process conditions. Four unit loads were applied to the SRAM outputs for the Spice simulations.

Compiled Gate Level SRAMs — Single Port Operation 0.6µ

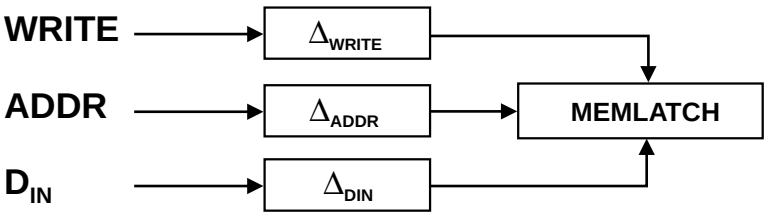
Conditions

Best Case Process, Temperature (T = -55)
Voltage (VDD = 5.5 Volts)
Output Loading = 4 Unit Loads (4 x .033pf)
Input Rise/Fall Time = 2 ns

Write Cycle Timing



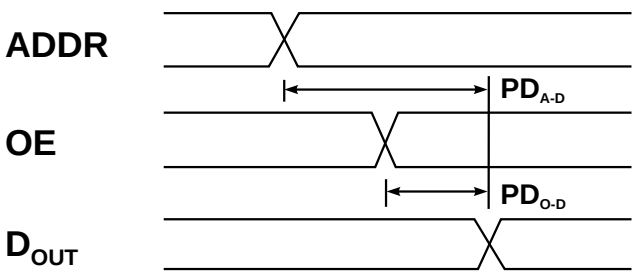
Write Cycle Propagation Delay



	MINIMUM (SP2x2)	MAXIMUM (SP32x36)
Δ_{WRITE} (r)	0.12 ns	0.96 ns
Δ_{WRITE} (f)	0.83 ns	1.54 ns
Δ_{ADDR}	0.82 ns	1.96 ns
Δ_{DIN}	0.03 ns	0.68 ns

$ADDR_{SU}$	= Δ_{ADDR} (MAX) - Δ_{WRITE} (f) (MIN)	= 1.96 ns - 0.83 ns	= 1.13 ns
$ADDR_{HOLD}$	= Δ_{WRITE} (r) (MAX) - Δ_{ADDR} (MIN)	= 0.96 ns - 0.82 ns	= 0.14 ns
$DATA_{SU}$	= Δ_{DIN} (MAX) - Δ_{WRITE} (r) (MIN)	= 0.68 ns - 0.12 ns	= 0.56 ns
$DATA_{HOLD}$	= Δ_{WRITE} (r) (MAX) - Δ_{DIN} (MIN)	= 0.96 ns - 0.03 ns	= 0.93 ns
WR_{MINPWL}	= Δ_{WRITE} (f) (MAX)	=	= 1.54 ns
WR_{MINPWH}	= $ADDR_{SU}$ + $DATA_{HOLD}$	= 1.13 ns + 0.93 ns	= 2.06 ns

Read Timing



	MINIMUM (DP2x2)	MAXIMUM (DP32x36)
PD_{A-D}	0.68 ns	2.29 ns
PD_{O-D}	0.07 ns	1.18 ns

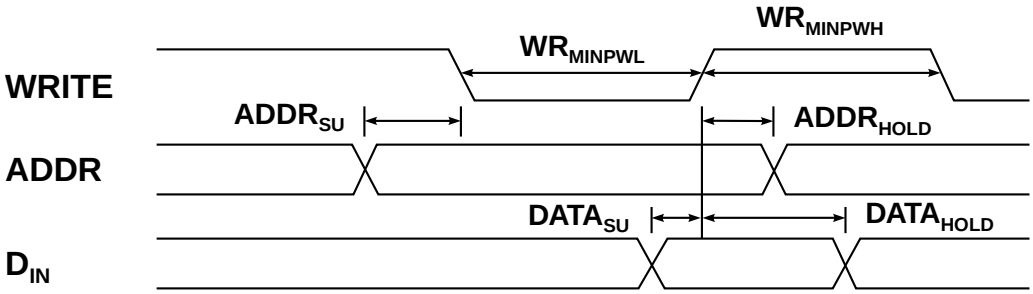
Compiled Gate Level SRAMs — Single Port Operation 0.6µ

Conditions

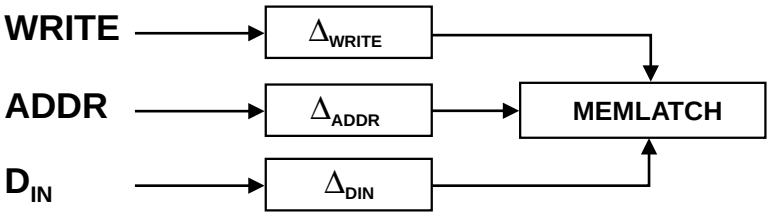
Typical Case Process, Temperature (T = 25)
Voltage (VDD = 5.0 Volts)

Output Loading = 4 Unit Loads (4 x .033pf)
Input Rise/Fall Time = 2 ns

Write Cycle Timing



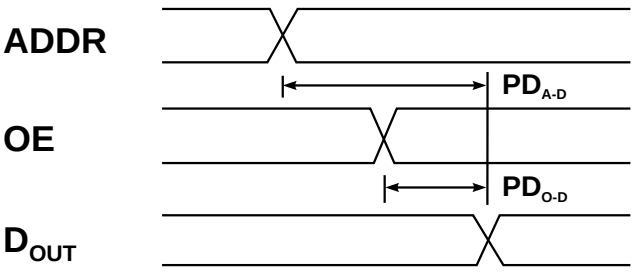
Write Cycle Propagation Delay



	MINIMUM (SP2x2)	MAXIMUM (SP32x36)
Δ_{WRITE} (r)	0.36 ns	1.51 ns
Δ_{WRITE} (f)	1.13 ns	2.29 ns
Δ_{ADDR}	1.42 ns	3.02 ns
Δ_{DIN}	0.20 ns	0.92 ns

$ADDR_{SU}$	=	Δ_{ADDR} (MAX) - Δ_{WRITE} (f) (MIN)	= 3.02 ns - 1.13 ns	= 1.89 ns
$ADDR_{HOLD}$	=	Δ_{WRITE} (r) (MAX) - Δ_{ADDR} (MIN)	= 1.51 ns - 1.42 ns	= 0.09 ns
$DATA_{SU}$	=	Δ_{DIN} (MAX) - Δ_{WRITE} (r) (MIN)	= 0.92 ns - 0.36 ns	= 0.56 ns
$DATA_{HOLD}$	=	Δ_{WRITE} (r) (MAX) - Δ_{DIN} (MIN)	= 1.51 ns - 0.20 ns	= 1.31 ns
WR_{MINPWL}	=	Δ_{WRITE} (f) (MAX)	=	= 2.29 ns
WR_{MINPWH}	=	$ADDR_{SU}$ + $DATA_{HOLD}$	= 1.89 ns + 1.31 ns	= 3.20 ns

Read Timing



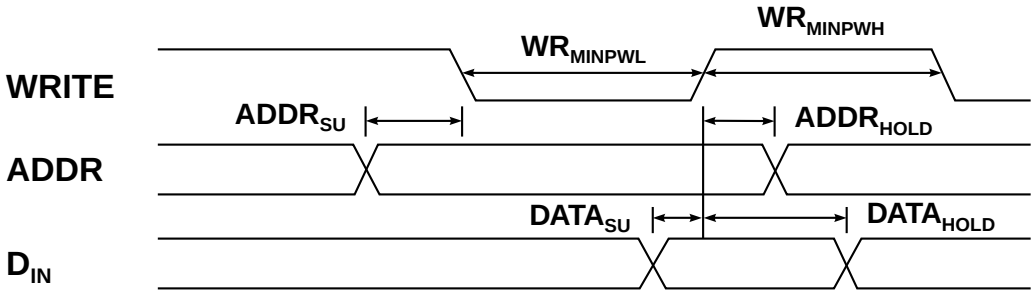
	MINIMUM (DP2x2)	MAXIMUM (DP32x36)
PD_{A-D}	1.17 ns	3.52 ns
PD_{O-D}	0.20 ns	1.64 ns

Compiled Gate Level SRAMs — Single Port Operation 0.6µ

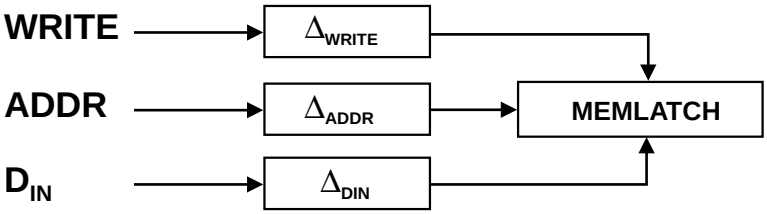
Conditions

Worst Case Process, Temperature (T = 125)
Voltage (VDD = 4.5 Volts)
Output Loading = 4 Unit Loads (4 x .033pf)
Input Rise/Fall Time = 2 ns

Write Cycle Timing



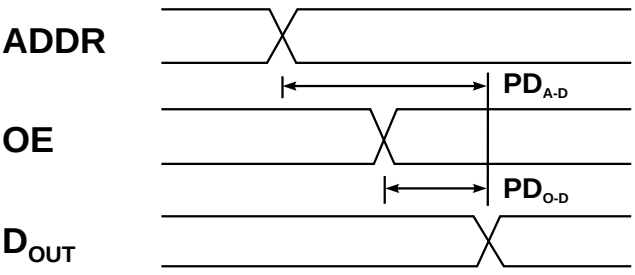
Write Cycle Propagation Delay



	MINIMUM (SP2x2)	MAXIMUM (SP32x36)
Δ_{WRITE} (r)	0.73 ns	2.53 ns
Δ_{WRITE} (f)	1.62 ns	3.70 ns
Δ_{ADDR}	2.50 ns	5.05 ns
Δ_{DIN}	0.51 ns	1.18 ns

$ADDR_{SU}$	= Δ_{ADDR} (MAX) - Δ_{WRITE} (f) (MIN)	= 5.05 ns - 1.62 ns	= 3.43 ns
$ADDR_{HOLD}$	= Δ_{WRITE} (r) (MAX) - Δ_{ADDR} (MIN)	= 2.53 ns - 2.50 ns	= 0.03 ns
$DATA_{SU}$	= Δ_{DIN} (MAX) - Δ_{WRITE} (r) (MIN)	= 1.18 ns- 0.73 ns	= 0.45 ns
$DATA_{HOLD}$	= Δ_{WRITE} (r) (MAX) - Δ_{DIN} (MIN)	= 2.53 ns - 0.51 ns	= 2.02 ns
WR_{MINPWL}	= Δ_{WRITE} (f) (MAX)	=	= 3.70 ns
WR_{MINPWH}	= $ADDR_{SU}$ + $DATA_{HOLD}$	= 3.43 ns + 2.02 ns	= 5.45 ns

Read Timing



	MINIMUM (DP2x2)	MAXIMUM (DP32x36)
PD_{A-D}	2.13 ns	5.93 ns
PD_{O-D}	0.44 ns	2.53 ns

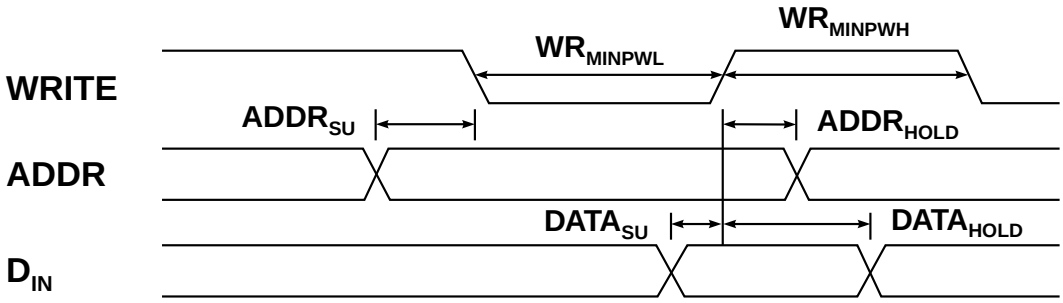
Compiled Gate Level SRAMs — Dual Port Operation 0.6μ

Conditions

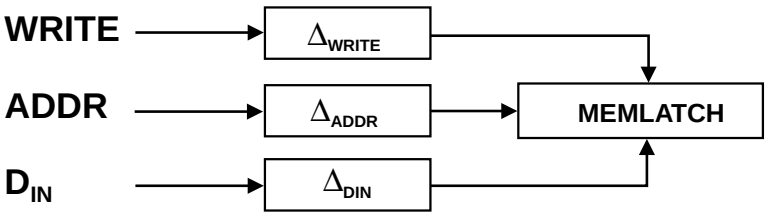
Best Case Process, Temperature (T=-55)
Voltage (VDD = 5.5 Volts)

Output Loading = 4 Unit Loads (4 X .033pf)
Input Rise/Fall Time = 2 ns

Write Cycle Timing



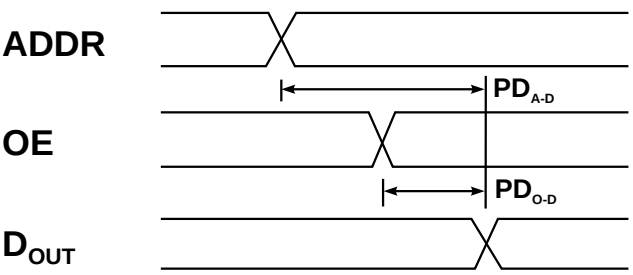
Write Cycle Propagation Delay



	MINIMUM (DP2x2)	MAXIMUM (DP32x36)
Δ_{WRITE} (r)	0.12 ns	0.94 ns
Δ_{WRITE} (f)	0.82 ns	1.57 ns
Δ_{ADDR}	0.55 ns	1.79 ns
Δ_{DIN}	0.08 ns	0.68 ns

$ADDR_{SU}$	= Δ_{ADDR} (MAX) - Δ_{WRITE} (f) (MIN)	= 1.79 ns - 0.82 ns	= 0.97 ns
$ADDR_{HOLD}$	= Δ_{WRITE} (r) (MAX) - Δ_{ADDR} (MIN)	= 0.94 ns - 0.55 ns	= 0.39 ns
$DATA_{SU}$	= Δ_{DIN} (MAX) - Δ_{WRITE} (r) (MIN)	= 0.68 ns - 0.12 ns	= 0.56 ns
$DATA_{HOLD}$	= Δ_{WRITE} (r) (MAX) - Δ_{DIN} (MIN)	= 0.94 ns - 0.08 ns	= 0.86 ns
WR_{MINPWL}	= Δ_{WRITE} (f) (MAX)	=	= 1.57 ns
WR_{MINPWH}	= $ADDR_{SU}$ + $DATA_{HOLD}$	= 0.97 ns + 0.86 ns	= 1.83 ns

Read Timing



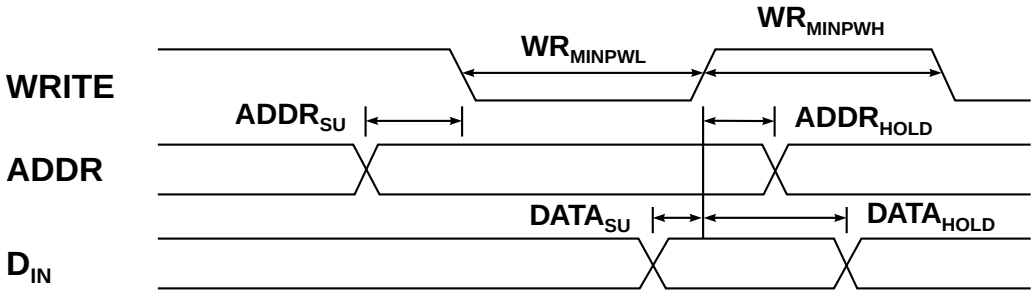
	MINIMUM (DP2x2)	MAXIMUM (DP32x36)
PD_{A-D}	0.65 ns	2.27 ns
PD_{O-D}	0.07 ns	1.18 ns

Compiled Gate Level SRAMs — Dual Port Operation 0.6µ

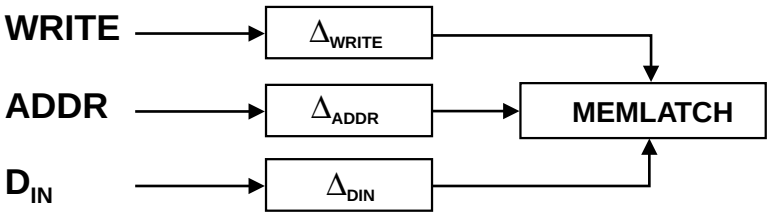
Conditions

Typical Case Process, Temperature (T=25)
Voltage (VDD = 5.0 Volts)
Output Loading = 4 Unit Loads (4 x .033pf)
Input Rise/Fall Time = 2 ns

Write Cycle Timing



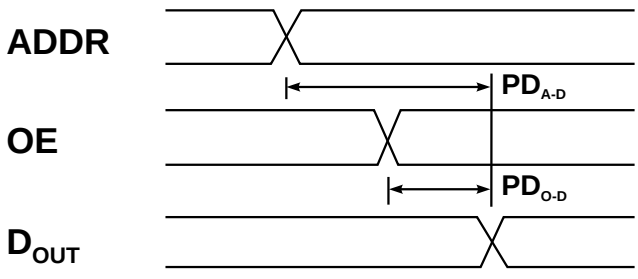
Write Cycle Propagation Delay



	MINIMUM (DP2x2)	MAXIMUM (DP32x36)
Δ_{WRITE} (r)	0.36 ns	1.48 ns
Δ_{WRITE} (f)	1.11 ns	2.24 ns
Δ_{ADDR}	0.99 ns	2.59 ns
Δ_{DIN}	0.20 ns	0.91 ns

$ADDR_{SU}$	= Δ_{ADDR} (MAX) - Δ_{WRITE} (f) (MIN)	= 2.59 ns - 1.11 ns	= 1.48 ns
$ADDR_{HOLD}$	= Δ_{WRITE} (r) (MAX) - Δ_{ADDR} (MIN)	= 1.48 ns - 0.99 ns	= 0.49 ns
$DATA_{SU}$	= Δ_{DIN} (MAX) - Δ_{WRITE} (r) (MIN)	= 0.91 ns - 0.36 ns	= 0.55 ns
$DATA_{HOLD}$	= Δ_{WRITE} (r) (MAX) - Δ_{DIN} (MIN)	= 1.48 ns- 0.20 ns	= 1.28 ns
WR_{MINPWL}	= Δ_{WRITE} (f) (MAX)	=	= 2.24 ns
WR_{MINPWH}	= $ADDR_{SU}$ + $DATA_{HOLD}$	= 1.48 ns + 1.28 ns	= 2.76 ns

Read Timing



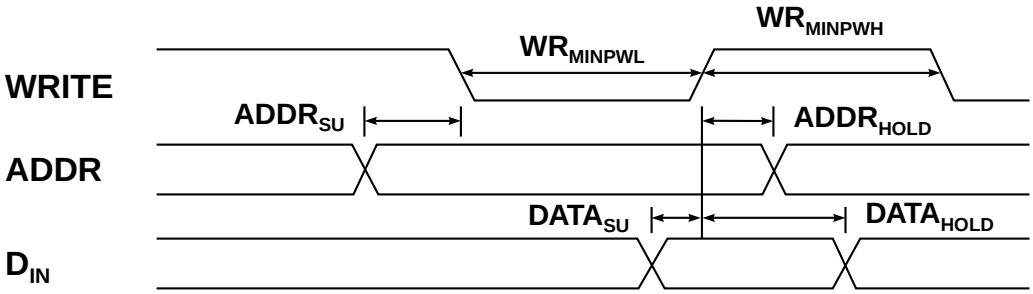
	MINIMUM (DP2x2)	MAXIMUM (DP32x36)
PD_{A-D}	1.13 ns	3.37 ns
PD_{O-D}	0.20 ns	1.64 ns

Compiled Gate Level SRAMs — Dual Port Operation 0.6µ

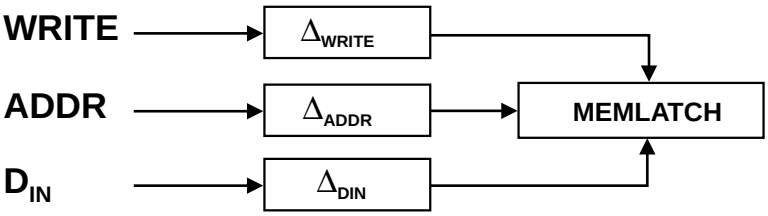
Conditions

Worst Case Process, Temperature (T = 125)
Voltage (VDD = 4.5 Volts)
Output Loading = 4 Unit Loads (4 x .033pf)
Input Rise/Fall Time = 2 ns

Write Cycle Timing



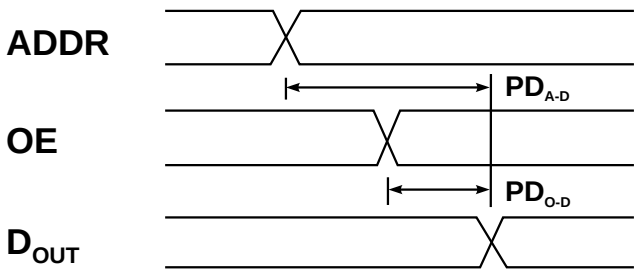
Write Cycle Propagation Delay



	MINIMUM (DP2x2)	MAXIMUM (DP32x36)
Δ_{WRITE} (r)	0.72 ns	2.48 ns
Δ_{WRITE} (f)	1.63 ns	3.63 ns
Δ_{ADDR}	1.79 ns	4.34 ns
Δ_{DIN}	0.51 ns	1.18 ns

$ADDR_{SU}$	= Δ_{ADDR} (MAX) - Δ_{WRITE} (f) (MIN)	=	4.34 ns - 1.63 ns	= 2.71ns
$ADDR_{HOLD}$	= Δ_{WRITE} (r) (MAX) - Δ_{ADDR} (MIN)	=	2.48 ns - 1.79 ns	= 0.69 ns
$DATA_{SU}$	= Δ_{DIN} (MAX) - Δ_{WRITE} (r) (MIN)	=	1.18 ns - 0.72 ns	= 0.46 ns
$DATA_{HOLD}$	= Δ_{WRITE} (r) (MAX) - Δ_{DIN} (MIN)	=	2.48 ns - 0.51 ns	= 1.97 ns
WR_{MINPWL}	= Δ_{WRITE} (f) (MAX)	=		= 3.63 ns
WR_{MINPWH}	= $ADDR_{SU}$ + $DATA_{HOLD}$	=	2.71 ns + 1.97 ns	= 4.68 ns

Read Timing



	MINIMUM (DP2x2)	MAXIMUM (DP32x36)
PD_{A-D}	2.01 ns	5.66 ns
PD_{O-D}	0.44 ns	2.53 ns