National Semiconductor

# NMC3764 65,536 x 1-Bit Dynamic RAM

## General Description

The NMC3764 is a 65,536 by 1-bit dynamic RAM. It is fabricated with National's XMOS™ N-channel process and uses double polysilicon gate technology. This provides high density and improved reliability. The chip is passivated with a silicone coating for alpha particle immunity.

The NMC3764 operates with a single 5V power supply with ±10% tolerance. All inputs and outputs are TTL compatible.

Multiplexed address inputs with separate row and column strobes allow the NMC3764 to be packaged in a standard 16-pin DIP.

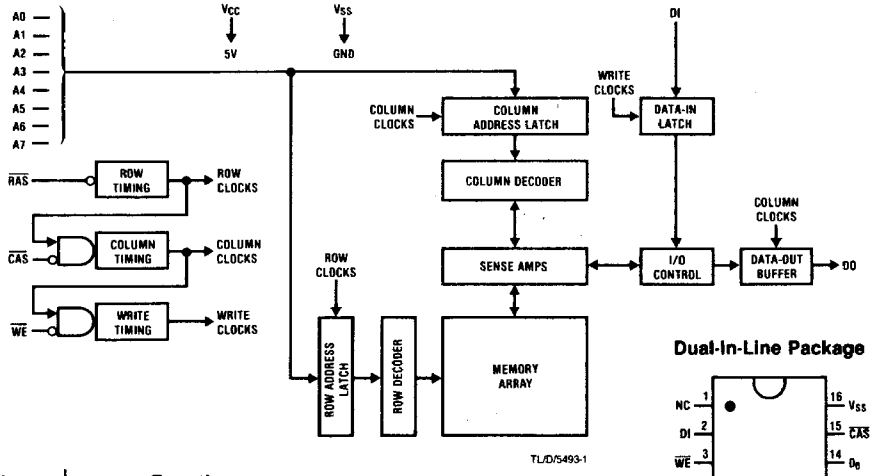
The NMC3764 must be refreshed every 2 ms. This is accomplished by performing any routine which cycles the row address strobe ($\overline{RAS}$) active during each of the 128 different row addresses defined by row address inputs A0–A6 (the additional addresses provided by row address input A7 are not necessary for refreshing.) Any read, write, $\overline{RAS}$-only refresh or hidden refresh cycle refreshes all cells at the selected row address. The $\overline{RAS}$-only refresh mode permits $\overline{RAS}$ to be cycled while the column address strobe ($\overline{CAS}$) is held high, i.e., inactive.

Conversely the buried refresh mode allows the memory to be refreshed by cycling $\overline{RAS}$ while $\overline{CAS}$ is held low, i.e., active, thus maintaining valid data on the output.

## Features

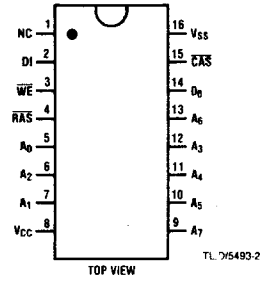
- MST™ screen available*
- High performance: 120, 150, 200 ns access times
- Single power supply: 5V ± 10%
- On chip substrate bias generator
- Low power: 248 mW (max) active
- Read, Write and Read-Modify-Write cycles
- Common I/O capability using Early Write cycle
- Page Mode operation
- Gated $\overline{CAS}$-noncritical timing
- $\overline{RAS}$-only Refresh and Buried Refresh capability
- 128 cycle, 2 ms refresh
- TTL compatible: all inputs and outputs
- TRI-STATE® output
- Industry standard 16-pin configuration

## Block And Connection Diagrams




| Pin Names | Function |
|---|---|
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| $\overline{WE}$ | Write Enable |
| $A_0$–$A_7$ | Address Inputs |
| DI | Data Input |
| DO | Data Output |
| $V_{CC}$ | Power (+5V) |
| $V_{SS}$ | Ground |

**Dual-In-Line Package**




**Order Number NMC3764N**
**NS Package Number N16F**

*See the MST™ Program.

## Absolute Maximum Ratings (Note 1)

| | | | |
|---|---|---|---|
| Operating Temperature Range | 0°C to +70°C | Voltage on Any Pin Relative to VSS | −1.0V to +7V |
| Storage Temperature | −65°C to +150°C | Lead Temperature (Soldering, 10 seconds) | 300°C |
| Power Dissipation | 1W | Short Circuit Output Current | 50 mA |

## Recommended DC Operating Conditions

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_A$ | Ambient Temperature | 0 | 70 | °C |
| $V_{CC}$<br>$V_{SS}$ | Supply Voltages (Notes 2, 3) | 4.5<br>0 | 5.5<br>0 | V<br>V |
| $V_{IH}$ | Input High Voltage, All Inputs (Note 2) | 2.4 | 6.5 | V |
| $V_{IL}$ | Input Low Voltage, All Inputs (Note 2) | −1.0 | 0.8 | V |

## DC Electrical Characteristics (at recommended operating conditions)

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $I_{CC1}$ | **Operating Current**<br>Average Power Supply Operating Current<br>($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN, DO = High Impedance) (Note 4) | | 45 | mA |
| $I_{CC2}$ | **Standby Current**<br>Power Supply Standby Current<br>($\overline{RAS} = V_{IH}$, DO = High Impedance) | | 5 | mA |
| $I_{CC3}$ | **Refresh Current**<br>Average Power Supply Current, Refresh Mode<br>($\overline{RAS}$ Cycling: $t_{RC} = t_{RC}$ MIN, DO = High Impedance) (Note 4) | | 35 | mA |
| $I_{CC4}$ | **Page Mode Current**<br>Average Power Supply Current, Page Mode<br>($\overline{RAS} = V_{IL}$, $\overline{CAS}$ Cycling: $t_{PC} = t_{PC}$ MIN, DO = High Impedance) (Note 4) | | 42 | mA |
| $I_{LI}$ | **Input Leakage**<br>Input Leakage Current, Any Input<br>($0V < V_{IN} < V_{CC}$, All Other Pins Not Under Test = 0V) | −10 | 10 | μA |
| $I_{LO}$ | **Output Leakage**<br>Output Leakage Current<br>(DO is Disabled, $0V < V_{OUT} < V_{CC}$) | −10 | 10 | μA |
| | **Output Levels** | | | |
| $V_{OH}$ | Output High Voltage ($I_{OUT} = -5$ mA) | 2.4 | $V_{CC}$ | V |
| $V_{OL}$ | Output Low Voltage ($I_{OUT}$ = 4.2 mA) | 0 | 0.4 | V |

## Capacitance

| Symbol | Parameter | Max | Units |
|---|---|---|---|
| $C_I$ | Input Capacitance, A0–A7, DI (Note 5) | 5 | pF |
| $C_C$ | Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ (Note 5) | 10 | pF |
| $C_O$ | Output Capacitance, DO (Note 5) | 7 | pF |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Recommended DC Operating Conditions" provides conditions for actual device operation.

**Note 2:** All voltages referenced to $V_{SS}$.

**Note 3:** When applying voltages to the device, $V_{CC}$ should never be 1.0V more negative than $V_{SS}$.

**Note 4:** $I_{CC1}$, $I_{CC3}$ and $I_{CC4}$ depend on cycle rate.

**Note 5:** Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = \Delta T/\Delta V$. Capacitance is guaranteed by periodic testing.

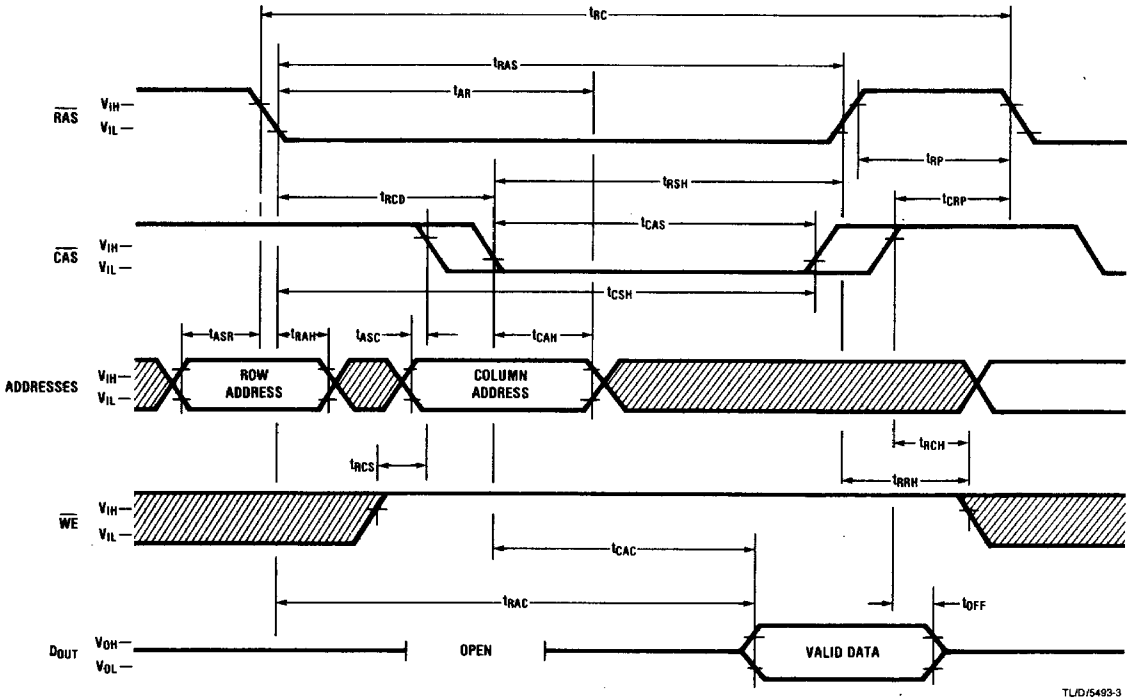
## AC Electrical Characteristics (at recommended operating conditions) (Notes 6, 7, 8)

| Symbol | Parameter | NMC3764-12 | | NMC3764-15 | | NMC3764-20 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| **READ, WRITE CYCLES** | | | | | | | | |
| $t_{RAC}$ | Access Time from $\overline{RAS}$ (Notes 12, 13) | | 120 | | 150 | | 200 | ns |
| $t_{CAC}$ | Access Time from $\overline{CAS}$ (Notes 12, 14) | | 80 | | 100 | | 135 | ns |
| $t_{RP}$ | $\overline{RAS}$ Precharge Time | 90 | | 100 | | 120 | | ns |
| $t_{RAS}$ | $\overline{RAS}$ Pulse Width | 120 | 10k | 150 | 10k | 200 | 10k | ns |
| $t_{CAS}$ | $\overline{CAS}$ Pulse Width | 80 | 10k | 100 | 10k | 135 | 10k | ns |
| $t_{RC}$ | Random Read or Write Cycle Time | 240 | | 270 | | 330 | | ns |
| $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ Delay Time (Note 9) | 30 | 40 | 30 | 50 | 35 | 65 | ns |
| $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | 0 | | 0 | | 0 | | ns |
| $t_{RSH}$ | $\overline{RAS}$ Hold Time | 80 | | 100 | | 135 | | ns |
| $t_{CSH}$ | $\overline{CAS}$ Hold Time | 120 | | 150 | | 200 | | ns |
| $t_{ASR}$ | Row Address Set-Up Time | 0 | | 0 | | 0 | | ns |
| $t_{RAH}$ | Row Address Hold Time | 20 | | 20 | | 25 | | ns |
| $t_{ASC}$ | Column Address Set-Up Time | 0 | | 0 | | 0 | | ns |
| $t_{CAH}$ | Column Address Hold Time | 40 | | 45 | | 55 | | ns |
| $t_{AR}$ | Column Address Hold Time Referenced to $\overline{RAS}$ | 80 | | 95 | | 120 | | ns |
| $t_{RCS}$ | Read Command Set-Up Time | 0 | | 0 | | 0 | | ns |
| $t_{RCH}$ | Read Command Hold Time (Note 11) | 0 | | 0 | | 0 | | ns |
| $t_{OFF}$ | Output Buffer Turn-Off Delay (Note 15) | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| $t_{WP}$ | Write Command Pulse Width | 40 | | 45 | | 55 | | ns |
| $t_{WCS}$ | $\overline{WE}$ to $\overline{CAS}$ Set-Up Time (Note 16) | −10 | | −10 | | −10 | | ns |
| $t_{WCH}$ | Write Command Hold Time | 40 | | 45 | | 55 | | ns |
| $t_{WCR}$ | Write Command Hold Time Referenced to $\overline{RAS}$ | 80 | | 95 | | 120 | | ns |
| $t_{RWL}$ | Write Command to $\overline{RAS}$ Lead Time | 40 | | 45 | | 55 | | ns |
| $t_{CWL}$ | Write Command to $\overline{CAS}$ Lead Time | 40 | | 45 | | 55 | | ns |
| $t_{DS}$ | Data-In Set-Up Time | 0 | | 0 | | 0 | | ns |
| $t_{DH}$ | Data-In Hold Time | 40 | | 45 | | 55 | | ns |
| $t_{DHR}$ | Data-In Hold Time Referenced to $\overline{RAS}$ | 80 | | 95 | | 120 | | ns |
| $t_T$ | Transition Time (Rise and Fall) | 3 | 35 | 3 | 35 | 3 | 50 | ns |
| $t_{RRH}$ | Read Command Hold Time Referenced to $\overline{RAS}$ | 20 | | 20 | | 25 | | ns |
| $t_{REF}$ | Refresh Period | | 2 | | 2 | | 2 | ms |
| **READ-MODIFY-WRITE CYCLES** | | | | | | | | |
| $t_{RWD}$ | $\overline{RAS}$ to $\overline{WE}$ Delay | 90 | | 110 | | 145 | | ns |
| $t_{CWD}$ | $\overline{CAS}$ to $\overline{WE}$ Delay (Note 16) | 50 | | 60 | | 80 | | ns |
| $t_{RWC}$ | Read-Write-Cycle Time | 240 | | 270 | | 330 | | ns |
| **PAGE MODE CYCLES** | | | | | | | | |
| $t_{CP}$ | $\overline{CAS}$ Precharge Time (Note 10) | 50 | | 60 | | 80 | | ns |
| $t_{PC}$ | Page Mode Cycle Time | 150 | | 170 | | 225 | | ns |

**Note 6:** An initial pause of 100 μs is required after power-up, followed by any 8 RAS cycles, before proper device operation is achieved.
**Note 7:** Transition times are assumed to be 5 ns.
**Note 8:** Timing reference points are $V_{IH}$ (min) and $V_{IL}$ (max).
**Note 9:** If $t_{RCD}$ (min) < $t_{RCD}$ < $t_{RCD}$ (max) the access time is $t_{RAC}$ ($\overline{RAS}$ limited timing). If the $t_{RCD}$ exceeds $t_{RCD}$ (max) the access time is $t_{RCD}$ plus $t_{CAC}$ ($\overline{CAS}$ limited timing).
**Note 10:** $t_{CP}$ is necessary for $\overline{RAS}/\overline{CAS}$ cycles preceded by a $\overline{CAS}$ only cycle or page mode cycle.
**Note 11:** $t_{RCH}$ is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
**Note 12:** Load = 2 TTL loads and 100 pF.
**Note 13:** Assumes $t_{RCD}$ < $t_{RCD}$ (max) ($\overline{RAS}$ limited timing).
**Note 14:** Assumes $t_{RCD}$ > $t_{RCD}$ ($\overline{CAS}$ limited timing).
**Note 15:** $t_{OFF}$ max defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
**Note 16:** The placement of the negative going edge of $\overline{WE}$ with respect to the negative edge of $\overline{CAS}$ determines the type of write cycle. If $t_{WCS}$ is greater than $t_{WCS}$ (min) (negative edge of $\overline{WE}$ before the negative edge of $\overline{CAS}$) the memory is in an early write cycle and data out is TRI-STATE. If $t_{CWD}$ is greater than $t_{CWD}$ (min), the memory is in a read-write or read-modify-write cycle and data out is the original contents of the selected cell. If $\overline{WE}$ goes low between these two times, the cycle is a write cycle and data out is indeterminate.

## Switching Time Waveforms

### Read Cycle Timing

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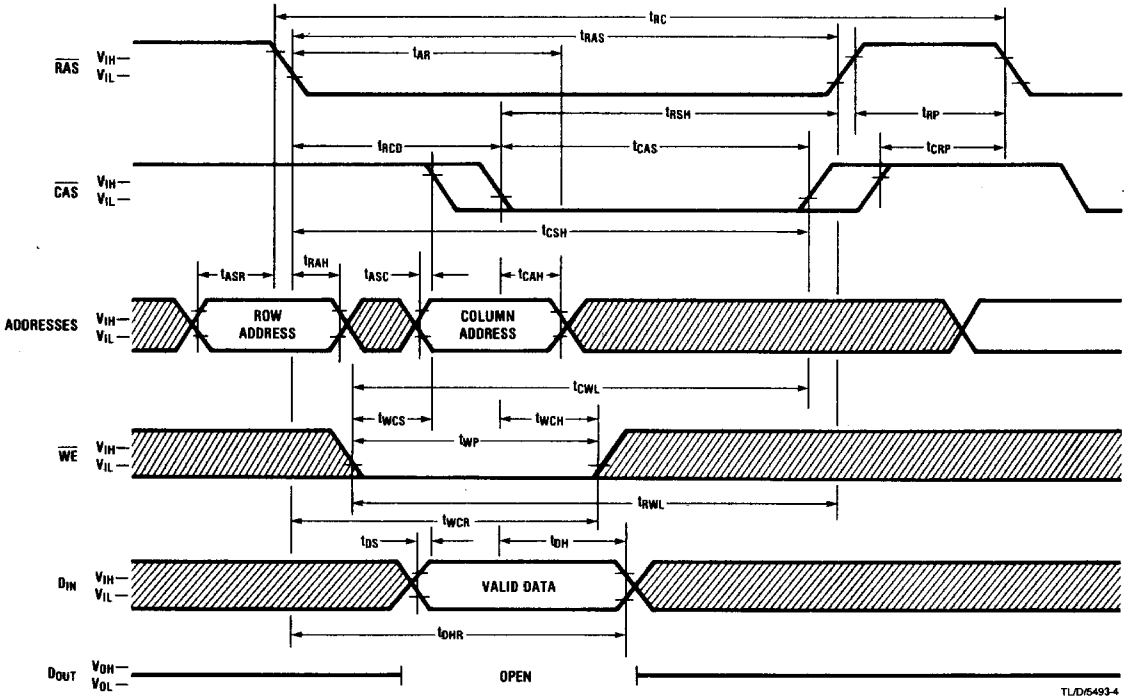
### Write Cycle Timing (Early Write)

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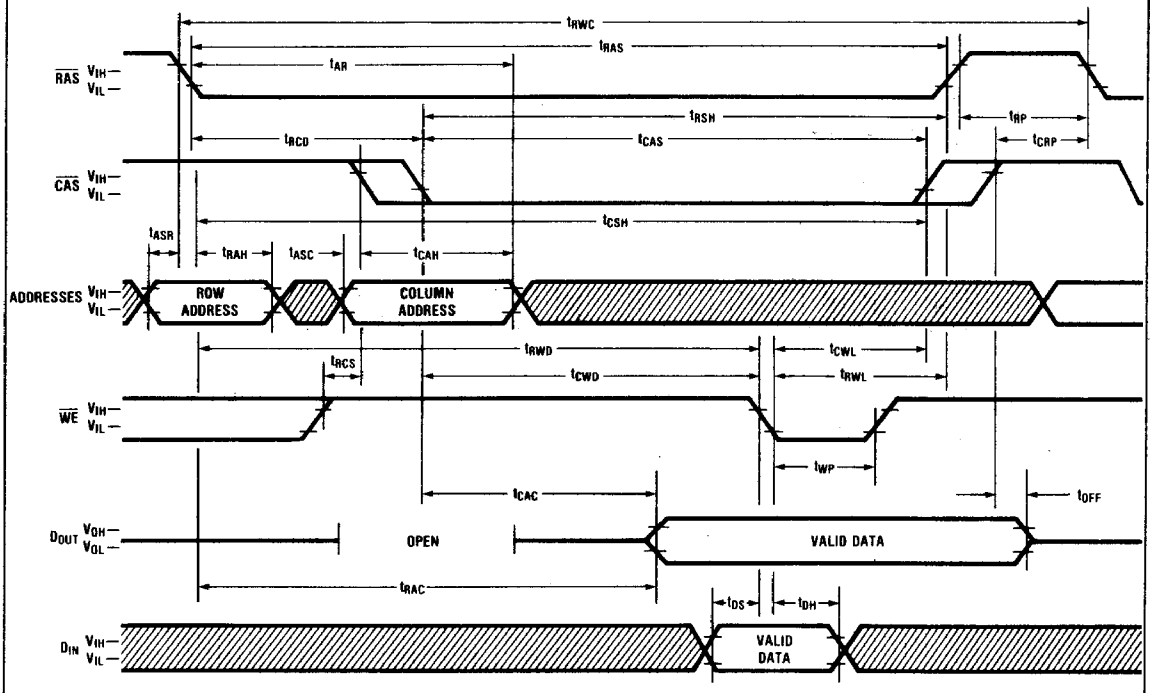
## Switching Time Waveforms (Continued)

### Read-Write/Read-Modify-Write Cycle

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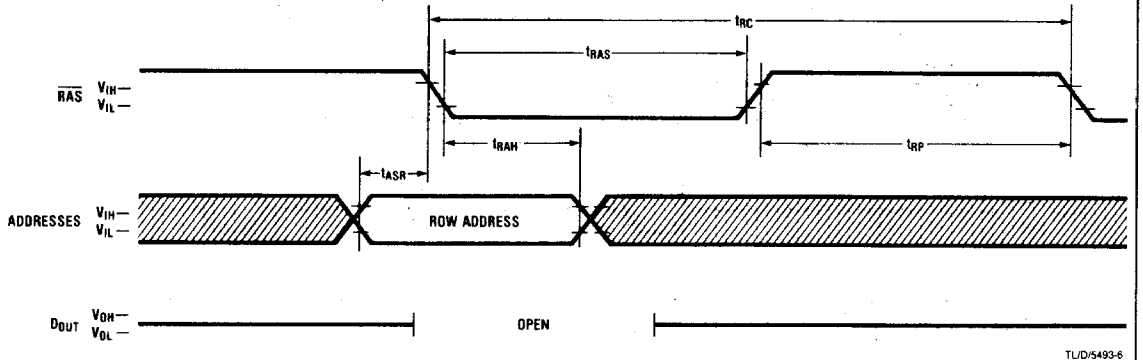
### RAS Only Refresh Timing

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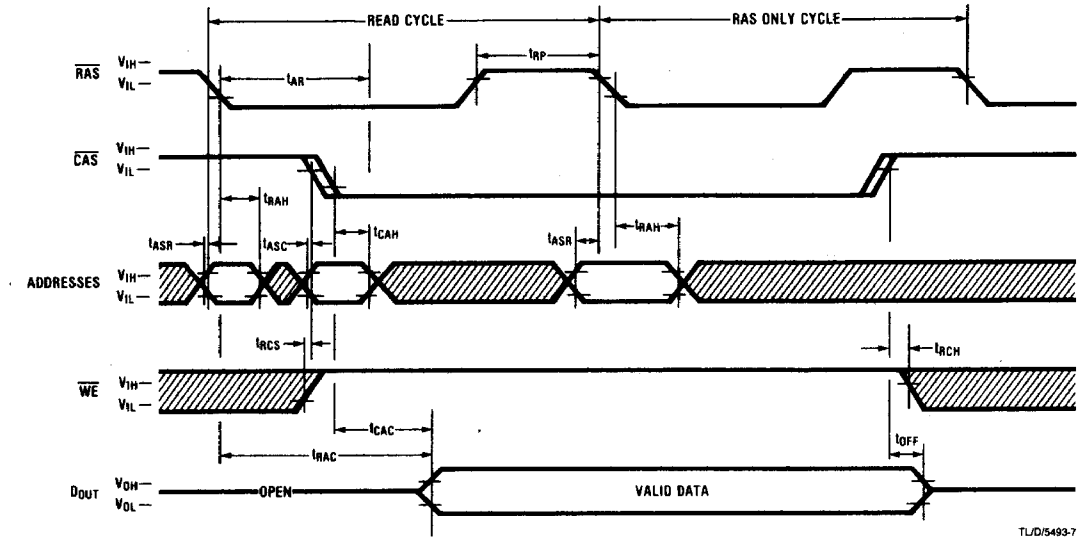
**Note:** CAS: $V_{IH}$, WE and $D_{IN}$: Don't care.

## Switching Time Waveforms (Continued)

### Hidden Refresh

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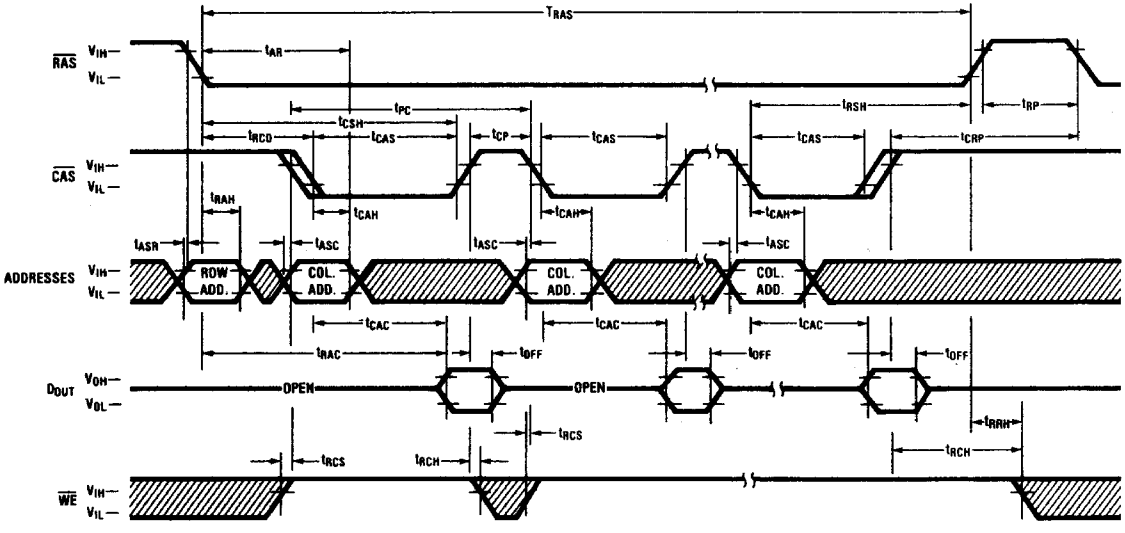
### Page Mode Read Cycle

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## Switching Time Waveforms (Continued)

### Page Mode Write Cycle