8502

Ethernet MII to AUI Interface Adapter

98210

Features

- **Single Chip Connecting MII and AUI Interfaces**
- **AUI Interface to Ethernet Transceiver**
- **MII Interface to Ethernet Controller**
- **MI Interface for Configuration & Status**
- **Few External Components**
- **Meets All Applicable IEEE 802.3 Standards**
- **Interface to External E^2PROM for Automatic Preloading of MI Serial Port Bits**
- **Many User Features and Options**
  - **Full Duplex**
  - **Powerdown**
  - **Transmitter Disable/Powerdown**
  - **Loopback**
  - **MII Disable**
  - **Link and Jabber Status Passthrough**
  - **Multiple Register Access**
- **LED Outputs**
  - **Activity, Transmit, Receive**
  - **Collision**
  - **Link**
  - **User Programmable**
- **44L PLCC**

Note: Check for latest Data Sheet revision before starting any designs.

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Description

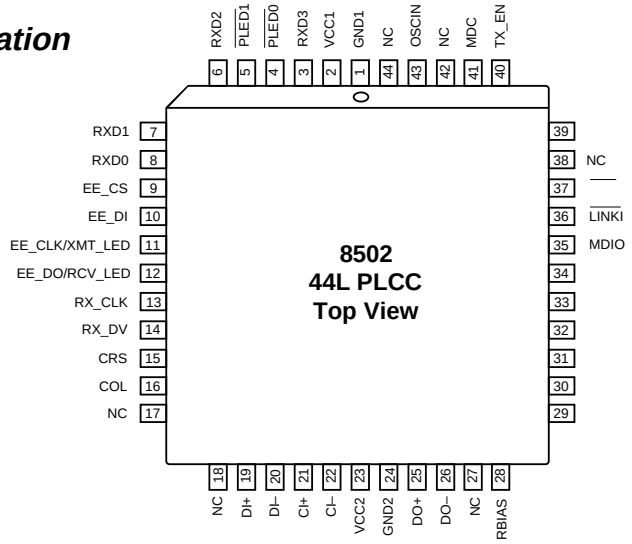
The 8502 is a interface IC that provides a single chip link between an Ethernet AUI (Attachment Unit Interface) and an Ethernet MII (Media Independent Interface). The 8502 is in a 44L package.

The 8502 consists of Manchester encoder, AUI transmitter, AUI receiver, Manchester decoder, Media Independent Interface (MII) to an external controller, and Management Interface (MI) serial port.

The 8502 can access five 16 bit registers though the MI serial port. These registers contain configuration inputs, status outputs, and device capabilities.

The 8502 is ideal for external PHY's that connect AUI or other media to MII. They are also ideal as an AUI interface to MII based Ethernet controllers in adapter cards, motherboards, and hubs.

Pin Configuration



MD400157/D

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5.0 Specifications

1.0 Pin Description

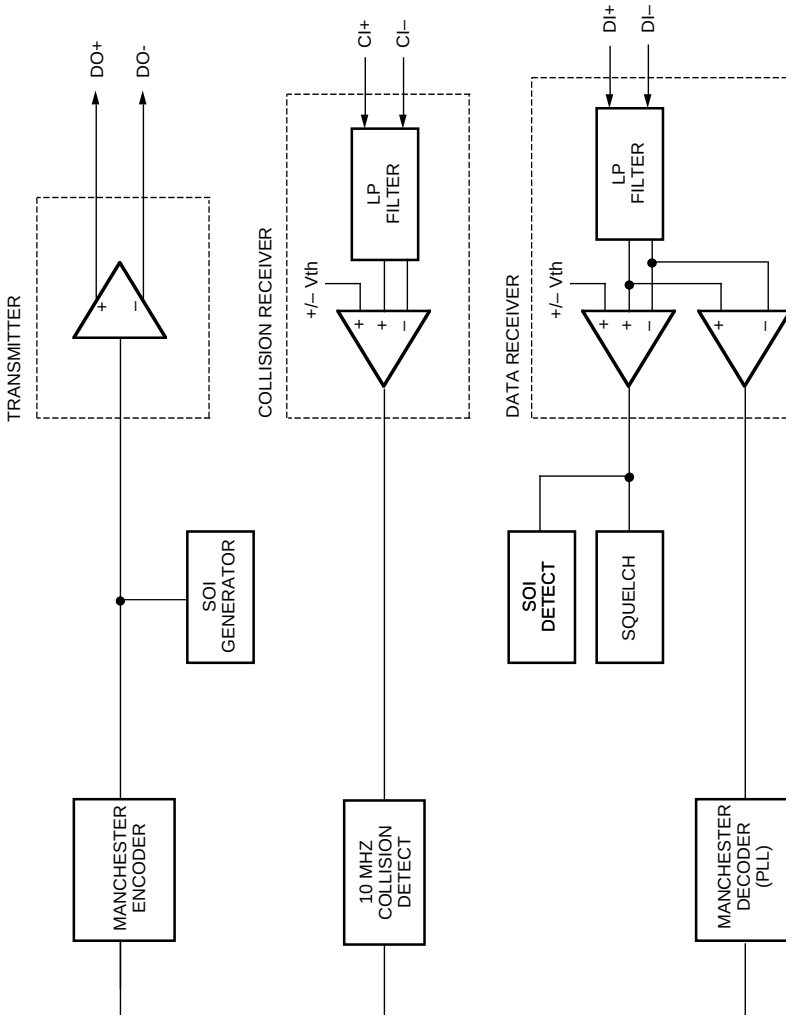
Pin # 44L 8502	Pin Name	I/O	Description
2 23	VCC2 VCC1	—	**Positive Supply.** +5 +/-5% Volts.
1 24	GND2 GND1	—	**Ground.** 0 Volts.
25	DO+	O	**AUI Transmit Output, Positive.**
26	DO-	O	**AUI Transmit Output, Negative.**
19	DI+	I	**AUI Receive Input, Positive.**
20	DI-	I	**AUI Receive Input, Negative.**
21	CI+	I	**AUI Collision Input, Positive.**
22	CI-	I	**AUI Collision Input, Negative.**
28	RBIAS	—	**Internal Bias Current Set.** An external resistor connected between this pin and GND will create a reference current for the internal bias circuits.
43	OSCIN	I	**Clock Oscillator Input.** There must be either a 20 MHz crystal or a 20 MHz clock tied between this pin and GND. TX_CLK output clock is generated from this input.
30	TX_CLK	O	**Transmit Clock Output.** This Media Independent Interface output provides a clock to the controller. Transmit data from the controller on TXD and TX_EN is clocked in on rising edges of TX_CLK and OSCIN.
40	TX_EN	I	**Transmit Enable Input.** This Media Independent Interface input has to be asserted active high to indicate that data on TXD is valid and is clocked in on rising edges of TX_CLK and OSCIN.
34 33 32 31	TXD3 TXD2 TXD1 TXD0	I	**Transmit Data Input.** These Media Independent Interface inputs contain input nibble data to be transmitted on the AUI outputs and are clocked in on rising edges of TX_CLK and OSCIN.
13	RX_CLK	O	**Receive Clock Output.** This Media Independent Interface output provides a clock to the controller. Receive data on RXD and RX_DV is clocked out to the controller on falling edges of RX_CLK.
15	CRS	O	**Carrier Sense Output.** This Media Independent Interface output is asserted when valid data is detected on the AUI inputs and is clocked out on falling edges of RX_CLK.
14	RX_DV	O	**Receive Data Valid Output.** This Media Independent Interface output is asserted active high when valid decoded data is present on the RXD outputs and is clocked out on falling edges of RX_CLK.
3 6 7 8	RXD3 RXD2 RXD1 RXD0	O	**Receive Data Output.** These Media Independent Interface outputs contain receive nibble data from the AUI input and are clocked out on falling edges of RX_CLK.

1.0 Pin Description continued

Pin # 44L 8502	Pin Name	I/O	Description
16	COL	O	**Collision Output.** This Media Independent Interface output is asserted when collision between transmit and receive data is detected.
41	MDC	I	**Management Interface Clock Input.** This Management Interface clock shifts serial data into and out of MDIO on rising edges.
35	MDIO	I/O	**Management Interface Data Input/Output.** This bidirectional pin contains serial Management Interface data that is clocked in and out on rising edges of the MDC clock.
36	$\overline{\text{LINKI}}$	I Pullup To VCC/2	**Link Input.** The value on this pin is either passed through to the internal MI serial port Link Status output bit In Register 1 or it enables the internal Link algorithm. 1 = Link Status Bit Is Set To 0 (Link Fail) float = Link Status Bit Determined By The Internal Link Algorithm 0 = Link Status Bit Is Set To 1 (Link Pass) In 28L 8501, the Link Status Bit is always forced to 1 (Link Pass).
37	$\overline{\text{JABI}}$	I Pullup	**Jabber Input.** The value on this pin is passed through to the internal MI serial port Jabber Detect output bit In Register 1. 1 = Jabber Detect Bit Is Set To 0 (No Jabber Detect) 0 = Jabber Detect Bit Is Set To 1 (Jabber Detect) In 28L 8501, the Jabber Detect Bit is always forced to 0 (No Jabber Detect).
9	EE_CS	O	**External EEPROM Chip Select Output.** During powerup or reset, this pin is a chip select output to an external EEPROM that can preload the MI serial port input bits to values other than the defaults.
11	EE_CLK/ XMT_LED	O	**External EEPROM Clock Output/Transmit LED.** During powerup or reset, this pin is serial data clock output to an external EEPROM that can preload the MI serial port input bits to values other than the defaults. Data is shifted in and out on EE_DI and EE_DO, respectively, on rising edges of the EE_CLK clock. During normal operation, this pin can be used as Transmit LED and can drive an LED to GND. 0 = No Detect 1 = Transmit Activity Detected, On for 50 mS
10	EE_DI	I Pullup	**External EEPROM Data Input.** During powerup or reset, this pin is a data input from an external EEPROM that can preload the MI serial port input bit to values other than the defaults.
12	EE_DO/ RCV_LED	O	**External EEPROM Data Output/Receive LED.** During powerup or reset, this pin is a data output to an external EEPROM that can preload the MI serial port input bit to values other than the defaults. During normal operation, this pin can be used as Receive LED and can drive an LED to GND. 0 = No Detect 1 = Receive Activity Detected, On for 50 mS

1.0 Pin Description continued

Pin # 44L 8502	Pin Name	I/O	Description
5	$\overline{\text{PLED1}}$ (MDA1)	I/O O.D. Pullup	**Programmable LED Output/Management Interface Address Input.** This pin can be programmed through the MI serial port to be either a Collision Detect output or a user select output. This pin can drive an LED from VCC. During powerup or reset, this pin is high impedance and the value on this pin is latched in as an address for the MI serial port. When programmed as Collision Detect Output: 1 = No Detect 0 = Collision Detected, On For 50 mS
4	$\overline{\text{PLED0}}$ (MDA0)	I/O O.D. Pullup	**Programmable LED Output/Management Interface Address Input.** This pin can be programmed through the MI serial port to be either a Activity Detect output or a user select output. This pin can drive an LED from VCC. During powerup or reset, this pin is high impedance and the value on this pin is latched in as an address for the MI serial port. When programmed as Activity Detect Output: 1 = No Detect 0 = Activity Detected, On For 50 mS
17 18 27 29 38 39 42	NC	—	**No Connect.** These pins are not connected but should be tied to GND to minimize noise.


TRANSMITTER
DO+
DO-
SOI GENERATOR
MANCHESTER ENCODER
COLLISION RECEIVER
CI+
CI–
LP FILTER
+/– Vth
10 MHZ COLLISION DETECT
DATA RECEIVER
DI+
DI–
LP FILTER
+/– Vth
SOI DETECT
SQUELCH
MANCHESTER DECODER (PLL)

3.0 Functional Description

3.1 GENERAL

The 8502 is a single chip interface IC's for connecting MII to AUI. MII and AUI are acronyms for Media Independent Interface and Attachment Unit Interface, respectively. Both of these interfaces are defined by IEEE 802.3 specifications.

The 8502 has six main sections: Media Independent Interface (MII), Manchester encoder, Manchester decoder, AUI transmitter, AUI receiver, and MI serial port.

On the transmit side, NRZ data is received on the MII from an external Ethernet controller per the MII format described in Figure 2. The NRZ data is then sent to the Manchester encoder for formatting. The Manchester encoded data is then sent to the AUI transmitter. The AUI transmitter shapes the output and drives a 78 ohm AUI cable. In addition, the transmitter generates start of idle (SOI) pulses.

On the receive side, the AUI receiver receives incoming Manchester encoded data from the AUI cable, removes high frequency noise from the input, determines if the input signal is a valid packet, and then converts the data from AUI levels to internal digital levels. The AUI receiver also detects start of idle (SOI) pulses and implements a squelch algorithm to reject invalid signals. The output of the AUI receiver then goes to the Manchester decoder which recovers a clock from the AUI data stream, recovers the data, and converts the data back to NRZ. The NRZ data is then transmitted to an external Ethernet controller through the MII using the format shown in Figure 2.

The MI (Management Interface) serial port is a two pin bidirectional port through which configuration inputs can be set, and device capabilities and status outputs can be read out.

A crystal oscillator generates a master clock for the device.

Each block plus the operating modes are described in more detail in the following sections. A block diagram of the 8502 is shown in Figure 1.

3.2 MEDIA INDEPENDENT INTERFACE (MII)

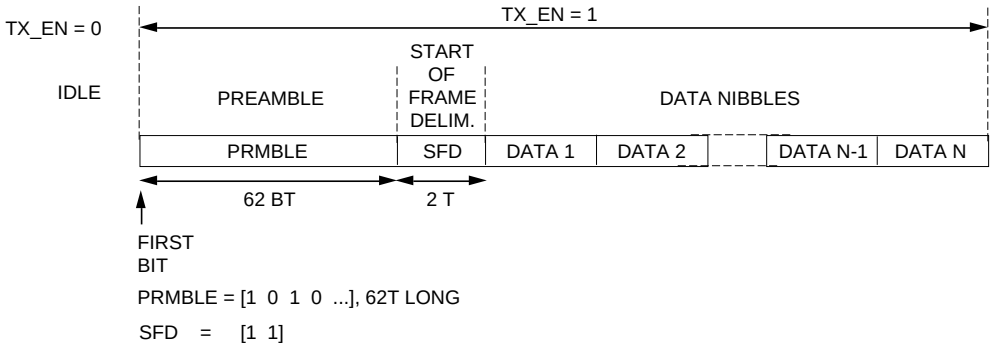
3.2.1 General

The Media Independent Interface, called MII, provides a standardized interface between the 8502 and an external Ethernet controller. The MII is a nibble wide packet data interface defined in IEEE 802.3 specifications and shown in Figure 2. The 8502 meets all the MII requirements outlined in IEEE 802.3 specifications. The 8502 can directly connect, without any external logic, to any Ethernet controllers which also comply with the IEEE 802.3 MII specifications.

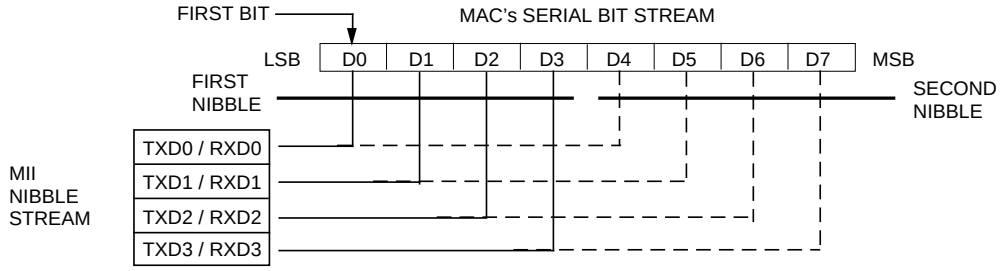
The MII consists of fourteen signals: four transmit data bits (TXD[3:0]), transmit clock (TX_CLK), transmit enable (TX_EN), four receive data bits (RXD[3:0]), receive clock (RX_CLK), carrier sense (CRS), receive data valid (RX_DV), and collision (COL). The transmit and receive clocks operate at 2.5 MHz.

On the transmit side, the TX_CLK output runs continuously. When no data is to be transmitted, TX_EN input is deasserted and any data on TXD[3:0] is ignored. When TX_EN is asserted on rising edge of TX_CLK, data on TXD[3:0] is clocked into the device on rising edges of the TX_CLK. TXD[3:0] input data is actually nibble wide packet data whose format needs to be the same as specified in IEEE 802.3 specifications and shown in Figure 2. When all the data on TXD[3:0] has been latched into the device, TX_EN is deasserted on rising edge of TX_CLK.

On the receive side, when invalid data is sensed on the AUI inputs, the receiver is idle. During idle, RX_CLK follows TX_CLK, RXD[3:0] is held low, and CRS and RX_DV are deasserted. When a valid packet is detected on the AUI receive inputs, CRS is asserted and the clock recovery process starts on the incoming data. After the receive clock has been recovered from the data, the RX_CLK is switched over to the recovered clock and the data valid signal RX_DV is asserted on a falling edge of RX_CLK. While RX_DV is asserted, valid data is clocked out of



a.) MII Frame Format



b.) MII Nibble Order

Signals	Bit Value																		
TXDO	X	X	1[1]	1	1	1	1	1	1	1	1	1	1	1	1	1	1[2]	1	D0[3]	D4[4]
TXD1	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
TXD2	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
TXD3	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
TX_EN	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

1. 1st preamble nibble transmitted.
2. 1st sfd nibble transmittted.
3. 1st data nibble transmitted.
4. D0 thru D7 are the first 8 bits of the data field.

c.) Transmit Preamble and SFD bits

Signals	Bit Value																			
RXDO	X	X	X	X	X	X	X	X	X	X	X	X	1[1]	1	1	1	1[2]	1	D0[3]	D4[4]
RXD1	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	D1	D5
RXD2	X	X	X	X	X	X	X	X	X	X	X	X	1	1	1	1	1	1	D2	D6
RXD3	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	1	D3	D7
RX_DV	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

1. 1st preamble nibble received. Device guaranteed to provide a minimum of 6 preamble nibbles.
2. 1st sfd nibble received.
3. 1st data nibble received.
4. D0 thru D7 are the first 8 bits of the data field.

d.) Receive Preamble and SFD Bits

Figure 2. MII Data Packet Format

RXD[3:0] on falling edges of the RX_CLK clock. The RXD[3:0] data has the same packet format as the TXD[3:0] data and is specified in IEEE 802.3 specifications as shown in Figure 2. When the end of packet is detected, CRS and RX_DV are deasserted. CRS and RX_DV also stay deasserted if the Link Detect bit in the MI serial port bit is set to the Link Fail state.

The collision output, COL, is asserted whenever the collision condition is detected.

3.2.2 MII Disable

The MII inputs and outputs can be disabled by setting the MII disable bit in the MI serial port Control register. When the MII is disabled, the MII inputs are ignored, the MII outputs are high impedance, and the AUI transmitter is idle. If the MI address lines, $\overline{MDA[1:0]}$, are pulled high during reset or powerup, the 8502 powers up and resets with the MII disabled. Otherwise, the 8501/8502 powers up and resets with the MII enabled.

3.3 MANCHESTER ENCODER

The Manchester encoder converts the NRZ nibble data from the MII into a single Manchester encoded serial data stream and adds a start of idle (SOI) pulse at the end of the packet as specified in the IEEE 802.3 specifications. The Manchester encoding process combines clock and data such that the first half of the data bit contains the complement of the data, and the second half of the data bit contains the true data, as described in IEEE 802.3 specifications. This guarantees that a transition always occurs in the middle of the data bit cell. Manchester encoding of the data from TXD occurs only when TX_EN is asserted.

3.4 MANCHESTER DECODER

The Manchester decoder converts the serial data stream from the AUI receiver into NRZ data for the MII. Thus, the Manchester decoder performs clock and data recovery from the Manchester encoded serial data stream. In Manchester encoded data, the first half of the data bit contains the complement of the data, and the second half of the data bit contains the true data.

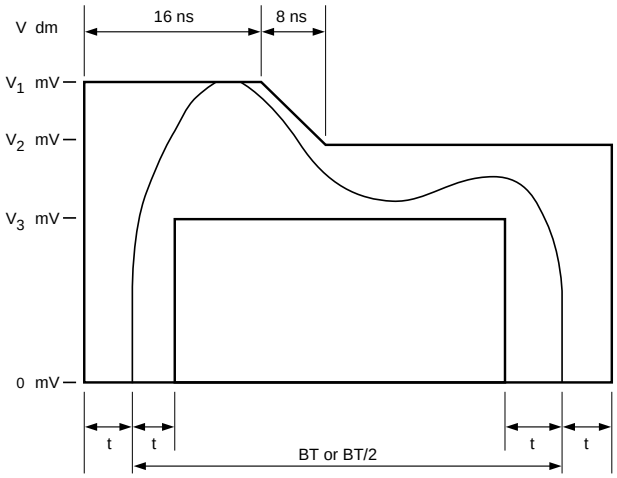
Clock recovery is done with a PLL. When valid data is not detected on the AUI input, an internal 10 MHz clock is applied to the input of the PLL. When valid data is detected on the AUI input, the PLL input is switched to the incoming AUI data. The PLL then recovers the clock by locking onto zero crossings of the preamble of the incoming signal from the AUI cable. The recovered clock frequency is 10 MHz. The PLL can lock onto the preamble signal in less than 12 transitions (bit times) and can reliably perform the data recovery process with up to ±18 nS of jitter on the AUI input. While the PLL is in the process of locking onto the preamble signal, some of the preamble data symbols are lost. The clock recovery process recovers enough preamble data symbols to pass at least 6 nibbles to the receive MII Media Independent Interface as shown in Figure 2.

Data recovery is performed by latching in data from the receiver with the recovered clock extracted by the PLL. The data is also converted from a single bit stream into nibble data according the format shown in Figure 2.

3.5 AUI TRANSMITTER

3.5.1 Transmitter

The AUI (Attachement Unit Interface) transmitter takes the Manchester encoded data, shapes it to meet the pulse template outlined in IEEE 802.3 and shown in Figure 3, adjusts the output voltage to meet the IEEE 802.3 required levels for AUI, and drives the 78 Ohm AUI cable.



t = 2.5 ns

V_1 < 1315 mV. V_3 > 450 mV

V_2 = 0.89 V_1

V_3 = 0.82 V_2

Figure 3. AUI Transmit Output Voltage Template

3.5.2 Transmit Activity Indication

Activity can be programmed to appear on the PLED0 pin by appropriately setting the programmable LED output select bits in the MI serial port Configuration register. When the PLED0 pin is programmed to be an activity detect output, this pin is asserted low for 50 mS every time a transmit or receive packet occurs. The PLED0 output is open drain with resistor pullup and can drive an LED from VCC or can drive another digital input.

XMT_LED is transmit activity output during normal operation. This pin is asserted high for 50 mS every time a transmit packet occurs. The XMT_LED output can drive an LED to GND or can drive another digital input.

3.5.3 Transmit Disable

The AUI transmitter can be disabled by setting the transmit disable bit in the MI serial port Configuration register. When the transmit disable bit is set, the AUI transmitter is forced into the idle state, and no data is transmitted regardless of the state of TX_EN.

3.5.4 Transmit Powerdown

The AUI transmitter can be powered down by setting the transmit powerdown bit in the MI serial port Configuration register. When the transmit powerdown bit is set, the AUI transmitter is powered down, the AUI transmit output is high impedance, and the rest of the device operates normally.

3.6 AUI RECEIVER

3.6.1 Receiver

The AUI (Attachement Unit Interface) receiver converts AUI levels to internal digital levels. There are two AUI receivers on the 8502, one for data (DI±) and one for collision (CI±).

The AUI inputs on the DI± pins are internally biased to about 3V by internal 10K bias resistors. The AUI inputs first pass through a low pass filter designed to eliminate high frequency noise on the input. The output of the receive filter then goes to two different types of comparators, threshold and zero crossing. The threshold comparator determines whether the signal is valid, and the zero crossing comparator is used to sense the actual data transitions once the signal is determined to be valid data. The output of the threshold comparator goes to the squelch circuit; the output of the zero crossing comparator is used for clock and data recovery.

The AUI inputs on the CI± pins are internally biased to about 3V by internal 10K bias resistors. The AUI inputs first pass through low pass filter designed to eliminate high frequency noise on the input. The output of the collision receive filter then goes to a collision threshold comparator which converts the CI± inputs to internal digital levels. The output of the collision threshold comparator then goes to the collision detect circuit.

3.6.2 Squelch

The squelch block determines if the data from the threshold comparators (and hence, AUI inputs) contains valid data. The threshold comparator compares the DI± and CI± inputs against a fixed negative threshold, called the AUI squelch level. If the input voltage to the threshold comparator does not exceed the fixed negative threshold level, the receiver is in the squelched state. If the input voltage exceeds the negative squelch level for more than 20 nS, the data is considered to be valid and the receiver now enters into the unsquelch state. In the unsquelch state, the AUI receive threshold level is reduced by approximately 30% for noise immunity reasons and is called the unsquelch level. While in the unsquelch state, the receive squelch circuit looks for SOI (Start Of Idle) pulse to locate the end of the packet. When the SOI signal is detected, the receive squelch is turned on again. The AUI receiver meets the AUI receive requirements defined in IEEE 802.3 Section 7.

3.6.3 Receive Activity Indication

Activity can be programmed to appear on the PLED0 pin by appropriately setting the programmable LED output select bits in the MI serial port Configuration register. When the PLED0 pin is programmed to be an activity detect output, this pin is asserted low for 50 mS every time a transmit or receive packet occurs. The PLED0 output is open drain with resistor pullup and can drive an LED from VCC or can drive another digital input.

RCV_LED is receive activity output during normal operation. This pin is asserted high for 50 mS every time a receive packet occurs. The RCV_LED output can drive an LED to GND or can drive another digital input.

3.7 COLLISION

3.7.1 General

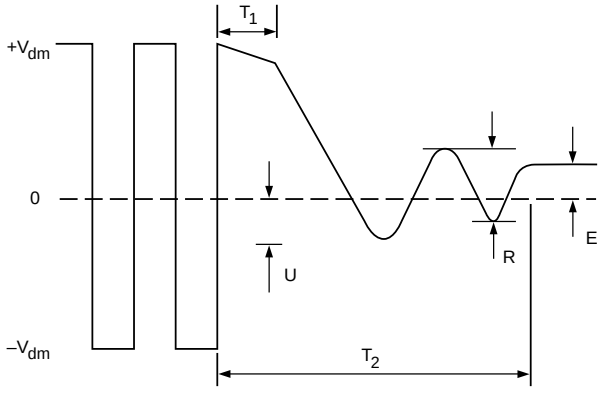
Collision is detected whenever the collision detect algorithm senses a valid 10 MHz signal on the CI± collision inputs. When collision is detected, the COL output is asserted, CRS is asserted, and RX_DV is deasserted. The collision function is disabled if the device is in the Full Duplex mode or if the Link Status bit in the MI serial port Status register is set to the Link Fail state.

3.7.2 Collision Detect Algorithm

The collision detect circuit looks for a valid 10 MHz signal by monitoring the period of the waveform from the CI± inputs. If the period of the input waveform on CI± is between 77-200 nS, the collision signal is considered to be valid and collision is asserted. If the period of the input waveform on CI± is less than 48 nS or greater than 400 nS, then collision is deasserted. Any high and low pulse widths less than 10 nS are rejected as noise.

3.7.3 Collision Indication

Collision detect can be programmed to appear on the PLED1 pin by appropriately setting the programmable LED output select bits in the MI serial port Configuration register. When the PLED1 pin is programmed to be a collision detect output, this pin is asserted low for 50 mS every time a collision occurs. The PLED1 output is open drain with resistor pullup and can drive an LED from VCC or can drive another digital input.



T_1 = 200 ns Minimum

T_2 = 8000 ns

U = –100 mV Maximum Undershoot

E = +/– 40 mV Max

R = <200 mV PK – PK

Figure 4. AUI Transmit SOI Output Voltage Template

3.7.4 Collision Test

The MII collision signal, COL, can be tested by setting the collision test bit in the MI serial port Control register. When this bit is set, TX_EN is looped back onto COL and the AUI trasmitter is forced to the idle state.

3.8 SOI (START OF IDLE)

The SOI pulse is a positive pulse inserted at the end of every transmitted packet to indicate the end of data transmission and the start of idle.

The AUI transmitter generates an SOI pulse at the end of data transmission when TX_EN is deasserted. The transmitted SOI output pulse meets the pulse template requirements specified in IEEE 802.3 Section 7 and shown in Figure 4.

The AUI receiver detects the SOI pulse by sensing missing data transitions. Once the SOI pulse is detected, data reception is ended and CRS is deasserted.

3.9 FULL DUPLEX MODE

Full Duplex mode allows transmission and reception to occur simultaneously without a collision being signalled. When Full Duplex mode is enabled, collision is disabled, COL is deasserted regardless of the input on CI±, and any loopback of TX_EN to CRS is disabled, if enabled.

The device can be forced into the Full Duplex Mode by setting the duplex bit in the MI serial port Control register.

3.10 LOOPBACK

Two different loopback modes are available on the 8502: (1) TX_EN to CRS Loopback, and (2) diagnostic loopback.

TX_EN to CRS Loopback is enabled by setting the TX_EN to CRS Loopback bit in the MI serial port Configuration register. When this loopback mode is enabled, TX_EN is looped back onto CRS during every transmit packet. This TX_EN to CRS Loopback is disabled during collision, when the device is placed in the Full Duplex mode, when the Link Status bit in the MI serial port Status register is in the Link Fail state, when the transmit disable bit is set in the MI serial port Configuration register, and any other conditions where the transmitter is disabled.

A diagnostic loopback mode can also be selected by setting the loopback bit in the MI serial port Control register. When diagnostic loopback is enabled, TXD[3:0] data is looped back onto RXD[3:0], TX_EN is looped back onto CRS, RX_DV operates normally, and the AUI receive and transmit paths are disabled.

3.11 LINK

3.11.1 General

The status of the link is reported with the link status bit in the MI serial port Status register. The Link Status bit (LINK bit) can either be controlled by an internal link algorithm or externally with the LINKI pin. The selection of the method to set the LINK bit is determined by the LINKI pin. The LINKI input pin is a three level pin. If LINKI =1 or 0, the 1 or 0 value is inverted and automatically passed through to the LINK bit in the MI serial port Status register. If the LINKI pin is left floating, the pin floats to VCC/2 and this level indicates to the device that the internal link algorithm should be used for setting the LINK bit.

3.11.2 Link Algorithm

The internal link algorithm is enabled by letting the LINKI pin float. The internal link algorithm starts by setting the LINK bit to the pass state when the device is powered up. This bit stays in the pass state until a packet is transmitted. When a packet is transmitted, the internal link algorithm expects a corresponding receive packet to arrive at the AUI inputs within 2 μS. If the expected receive packet arrives within 2 μS after the start of a transmission, the LINK bit stays in the Link Pass state. If the expected receive packet doesn't arrive within 2 μS, then the LINK bit goes to the Link Fail state. Since the LINK bit is an R/LL bit (see section 3.18.4), it latches itself whenever it goes low (Link Fail) and stays low until read out. Once it is read out, then it returns high to the Link Pass state.

3.11.3 Link Indication

Link Detect can be programmed to appear on the PLED1 pin by appropriately setting the PLED configuration bit and the programmable LED output select bits in the MI serial port Configuration register. When the PLED1 pin is programmed to be a link detect output, this pin is asserted low whenever the device is in the Link Pass State. The PLED1 output is open drain with resistor pullup and can drive an LED from VCC or can drive another digital input.

3.12 JABBER

The Jabber Detect bit in the MI serial port Status register is used to report the jabber condition. The 8502 does not have a jabber detect circuit, but the Jabber Detect bit (JAB bit) can be controlled externally with the JABI pin. Thus, if JABI =1 or 0, the 1 or 0 value is inverted and automatically passed through to the JAB bit in the MI serial port Status register.

3.13 RESET

The 8502 is reset when either VCC is applied to the device or when the reset bit is set in the MI serial port Control register. When reset bit is set to a 1, an internal power-on reset pulse is generated which resets all internal circuits, attempts to access an external EEPROM to load the MI serial port bits, forces the MI serial port bits to either their default values or to the contents of the external EEPROM, and latches in the MI physical address values on PLED[1:0]/MDA[1:0]. After the power-on reset pulse has finished, the reset bit in the MI serial port Control register is cleared to a 0 and the device is ready for normal operation 500 mS after the reset was initiated.

3.14 POWERDOWN

The 8502 can be powered down by setting the powerdown bit in the MI serial port Control register. In powerdown mode, the AUI outputs are in high impedance state, all functions are disabled except the MI serial port, and the power consumption is reduced to less than 10 mW. When the device goes from powerdown to powerup state, the device is ready for normal operation 500 mS after powerdown was deaserted (powerdown bit cleared).

3.15 OSCILLATOR

The 8502 requires a 20 MHz reference frequency for internal signal generation. This 20 MHz reference frequency can be generated by either connecting an external 20 MHz crystal between OSCIN and GND or an external 20 MHz clock on OSCIN.

3.16 LED DRIVERS

The PLED[1:0] outputs are open drain with a resistor pullup. These outputs can drive LED's tied to VCC.

The PLED[1:0] outputs can be individually programmed through the MI serial port to do 4 different functions: (1) Normal Function (2) On, (3) Off, and (4) Blink.

PLED[1:0] can be individually programmed by appropriately setting the LED output select bits in the MI serial port Configuration register. When PLED[1:0] are programmed for their Normal function, these outputs indicate the specific functions described in the MI serial port Configuration register shown on Table 9 (Collision, Activity, respectively). When PLED[1:0] are programmed to be On, the LED output drivers goes low, thus turning on the LED under user control. When PLED[1:0] are programmed to be Off, the LED output drivers will turn off, thus turning off

the LED under user control. When PLED[1:0] are programmed to Blink, the LED output drivers will continuously blink at a rate of 50 mS on, 50 mS off.

The default Normal functions for PLED1 and PLED0 are Collision Detect and Activity, respectively. The Normal function for PLED1 can be changed from Collision Detect to Link Detect by setting the PLED1 Configuration Select bit in the MI serial port Configuration register. When this bit is set, the Normal function for PLED1 changes from Collision to Link. That is, for PLED1 to be a Link Detect output, the PLED1 Configuration Select and PLED1 Output Select bits must all be high.

XMT_LED and RCV_LED outputs can drive LEDs to GND indicating transmit and receive activity respectively. They are asserted high for 50 mS every time a transmit or a receive packet occurs.

3.17 MI SERIAL PORT

3.17.1 Signal Description

The MI serial port has four pins, MDC, MDIO, and MDA[1:0]. MDC is the serial shift clock input. MDIO is a bidirectional data I/O pin. MDA[1:0] are address pins for the MI serial port.

MDA[1:0] inputs share the same pins as the PLED[1:0] outputs, respectively. At powerup or reset, the PLED[1:0] output drivers are high impedance for an interval towards the end of the poweron reset time. During this interval, the values on these pins are latched into the device, inverted, and used as the MI serial port addresses.

3.17.2 Timing

The MI serial port is idle when at least 32 continuous 1's are detected on MDIO, and it remains idle as long as continuous 1's are detected. During idle, MDIO is in the high impedance state. When the MI serial port is in the idle state, a 01 pattern on the MDIO pin initiates a serial shift cycle. Data on MDIO is then shifted in on the next 14 rising edges of MDC (MDIO is high impedance). If the multiple register access mode is not enabled, on the next 16 rising edges of MDC, data is either shifted in or out on MDIO, depending on whether a write or read cycle was selected with the bits READ and WRITE. After the 32 MDC cycles have been completed, one complete register has been read/written, the serial shift process is halted, data is latched into the device, and MDIO goes into high impedance state. Another serial shift cycle cannot be initiated until the the idle condition (at least 32 continuous 1's) is detected.

3.17.3 Multiple Register Access

Multiple registers can be accessed on a single MI serial port access cycle with the multiple register access feature. The multiple register access feature can be enabled by setting the multiple register access enable bit in the MI serial port Configuration register. When the multiple register access feature is enabled, multiple registers can be accessed on a single MI serial port access cycle by setting the register address to 11111 during the first 16 MDC clock cycles. There is no actual register residing in register address location 11111, so when the register address is then set to 11111, all five registers are accessed on the 80 rising edges of MDC that occur after the first 16 MDC clock cycles of the MI serial port access cycle. The registers are accessed in numerical order from 0 to 16. After all 96 MDC clocks have been completed, all the registers have been read/written, the serial shift process is halted, data is latched into the device, and MDIO goes into high impedance state. Another serial shift cycle cannot be initiated until the the idle condition (at least 32 continuous 1's) is detected.

3.17.4 Bit Types

Since the serial port is bidirectional, there are many types of bits. Write bits (W) are inputs during a write cycle and are high impedance during a read cycle. Read bits (R) are outputs during a read cycle and high impedance during a write cycle. Read/Write bits (R/W) are actually write bits which can be read out during a read cycle. R/WSC bits are R/W bits that clear themselves after a set period of time or after a specific event has completed. R/LL bits are read bits that latch themselves when they go low, and they stay latched low until read. After they are read, they are reset

high. R/LH bits are the same as R/LL bits except that they latch high. The bit type definitions are summarized in Table 1

Table 1. MI Register Bit Type Definition

Sym.	Name	Definition	
		Write Cycle	Read Cycle
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]

3.17.5 Frame Structure

The structure of the serial port frame is shown in Table 2 and a timing diagram of a frame is shown in Figure 5. Each serial port access cycle consists of 32 bits (or 96 bits if multiple register access is enabled and REGAD=11111), exclusive of idle. The first 16 bits of the serial port cycle are always write bits and are used for addressing. The last 16(80) bits are to or from one(all) of the five data registers.

The first 2 bits in Table 2 and Figure 5 are start bits and need to be written as a 01 for the serial port cycle to continue. The next 2 bits are a read and write bit which determine if the accessed data register bits will be read from or written to. The next 3 bits are upper device addresses and they must be written as 111 for the serial port access to continue. The next 2 bits are lower device address and must match the inverted values latched in from pins MDA[1:0] during the poweron reset time for the serial port access to continue. The next 5 bits are register address select bits which select one or all of the five data registers for access. The next 2 bits are turnaround bits which are not actual register bits but extra time to switch MDIO from write to read if necessary, as shown in Figure 5. The final 16 bits of the MI serial port cycle (or 80 bits if multiple register access is enabled and REGAD=11111) are to or from the data register designated in the register address bits REGAD[4:0].

3.17.6 Register Structure

The 8502 has five internal 16 bit registers. All five registers are available for setting configuration inputs and reading status outputs. A map of the registers is shown in Table 3. The five registers consist of four registers that are defined by the IEEE 802.3 specification (Registers 0-3) and one register that is unique to the 8502 (Register 16).

The structure and bit definition of the Control register is shown in Table 4. This register stores various configuration inputs and its bit definition complies with the IEEE 802.3 specifications.

The structure and bit definition of the Status register is shown in Table 5. This register contains device capabilities and status output information. and its bit definition complies with the IEEE 802.3 specifications.

The structure and bit definition of the PHY ID #1 and #2 registers is shown in Tables 6 and 7, respectively. These registers contain an identification code unique to the 8502 and their bit definition complies with the IEEE 802.3 specifications.

The structure and bit definition of the Configuration register is shown in Table 8. This register stores various configuration inputs.

3.17.7 Link Status Bit

The Link Status bit in the Status register is controlled by either the internal link algorithm or by direct pass through from the LINKI pin. Refer to the Link section for further details.

3.17.8 Jabber Detect Bit

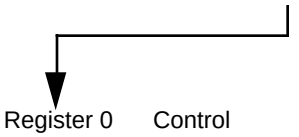
The Jabber Detect bit in the Status register is controlled by direct pass through from the JABI pin. Refer to the Jabber section for further details.

Figure 5. MI Serial Port Frame Timing Diagram

3.18 Register Description

Table 2. MI Serial Port Frame Structure

<Idle>	<Start>	<Read>	<Write>	<PHY Addr.>	<Reg. Addr.>	<Turnaround>	<Data> ....
IDLE	ST[1:0]	READ	WRITE	PHYAD[4:0]	REGAD[4:0]	TA[1:0]	D[15:0]....



Register 0	Control
Register 1	Status
Register 2	PHY ID #1
Register 3	PHY ID #2
Register 16	Configuration

Symbol	Name	Definition	R/W
IDLE	Idle Pattern	These Bits Are an Idle Pattern. Device Will Not Initiate An MI Cycle Until It Detects At Least 32 1's.	W
ST1 ST0	Start Bits	When ST[1:0]=01, A MI Serial Port Access Cycle Starts.	W
READ	Read Select	1 = Read Cycle	W
WRITE	Write Select	1 = Write Cycle	W
PHYAD[4:0]	Physical Device Address	When PHYAD[4:2]=000 and PHY[1:0]=$\overline{\text{MDA[1:0]}}$ Pins Inverted, The MI Serial Port Is Selected For Operation.	W
REGAD[4:0]	Register Address	If REGAD=00000-11111, These Bits Determine The Register From Which D[15:0] Is Read/Written. If Multiple Register Access Is Enabled And REGAD=11111, All Registers Are Read/Written.	W
TA1 TA0	Turnaround Time	These Bits Provide Some Turnaround Time For MDIO When READ=1, TA[1:0]=Z0 When WRITE=1, TA[1:0]=ZZ	R/W
D[15:0]....	Data	These 16 Bits Contain Data To/From One Of The Five Registers Selected By Register Address Bits REGAD[4:0].	Any

IDLE is shifted in first

ort Register Map

	x.7	x.6	x.5	x.4	x.3	x.2	x.1	x.0
X	COLTST	0	0	0	0	0	0	0
	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0
	0	CAP_SUPR	ANEG_ACK	REM_FLT	CAP_NWY	LINK	JAB	EXREG
	R 0	R 0	R 0	R 0	R 0	R/LL 1	R/LH 0	R 1
0	OUI11	OUI12	OUI13	OUI14	OUI15	OUI16	OUI17	OUI18
	R 0	R 0	R 0	R 1	R 0	R 1	R 1	R 0
T4	PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0
	R 0	R 0	R 1	R 0	R 0	R 0	R 0	R 0

Table 4. MI Register 0 (Control) Structure And Bit Definition

0.15	0.14	0.13	0.12	0.11	0.10	0.9	0.8
RST	LPBK	SPEED	ANEG_EN	PDN	MII_DIS	ANEG_RST	DPLX
R/WSC	R/W	R/W	R/W	R/W	R/W	R/W	R/W

0.7	0.6	0.5	0.4	0.3	0.2	0.1	0.0
COLTST	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
0.15	RST	Reset	1 = Reset 0 = Normal	R/W SC	0
0.14	LPBK	Loopback Enable	1 = Loopback Mode Enabled 0 = Normal	R/W	0
0.13	SPEED	Speed Select	0 = 10 Mbps Selected, No 100 Mbps Capability	R/W	0
0.12	ANEG_EN	AutoNegotiation Enable	0 = No Enable, No AutoNegotiation Capability	R/W	0
0.11	PDN	Powerdown Enable	1 = Powerdown 0 = Normal	R/W	0
0.10	MII_DIS	MII Interface Disable	1 = MII Interface Disabled, All MII Outputs Hi-z 0 = Normal	R/W	1[1]
0.9	ANEG_RST	AutoNegotiation Reset	0 = No Reset, No AutoNegotiation Capability	R/W	0
0.8	DPLX	Duplex Mode Select	1 = Full Duplex 0 = Half Duplex	R/W	0
0.7	COLTST	Collision Test Enable	1 = Collision Test Enabled 0 = Normal	R/W	0
0.6 thru 0.0			Reserved, Must Be 0	R/W	0

x.15 Bit Is Shifted First

1. If $\overline{\text{MDA}}$[1:0] Is Not =11 during reset, then the MII_DIS default value is changed to 0.

Table 5. MI Register 1 (Status) Structure and Bit Definition

1.15	1.14	1.13	1.12	1.11	1.10	1.9	1.8
CAP_T4	CAP_TXF	CAP_TXH	CAP_TF	CAP_TH	0	0	0
R	R	R	R	R	R	R	R

1.7	1.6	1.5	1.4	1.3	1.2	1.1	1.0
0	CAP_SUPR	ANEG_ACK	REM_FLT	CAP_ANEG	LINK	JAB	EXREG
R	R	R	R	R	R/LL	R/LH	R

Bit	Symbol	Name	Definition	R/W	Def.
1.15	CAP_T4	100BaseT4 Capable	0 = Not Capable of 100BaseT4 Operation	R	0
1.14	CAP_TXF	100BaseTX Full Duplex Capable	0 = Not Capable of 100BaseTX Full Duplex	R	0
1.13	CAP_TXH	100BaseTX Half Duplex Capable	0 = Not Capable of 100BaseTX Half Duplex	R	0
1.12	CAP_TF	10BaseT Full Duplex Capable	1 = Capable of 10 Mbps Full Duplex	R	1
1.11	CAP_TH	10BaseT Half Duplex Capable	1 = Capable of 10 Mbps Half Duplex	R	1
1.10 thru 1.7			Reserved	R	0
1.6	CAP_SUPR	MI Preamble Suppress Capable	0 = Not Capable of MI Preamble Suppression	R	0
1.5	ANEG_ACK	AutoNegotiation Acknowledgemnt	0 = No Acknowledgement, No AutoNegotiation Capability	R	0
1.4	REM_FLT	Remote Fault Detect	0 = No Remote Fault	R	0
1.3	CAP_ANEG	AutoNegotation Capable	0 = Not Capable of AutoNegotiation Operation	R	0
1.2	LINK	Link Status	1 = Link Pass 0 = Link Fail	R/LL	1[1]
1.1	JAB	Jabber Detect	1 = Jabber Detected 0 = Jabber Not Detected	R/LH	0[2]
1.0	EXREG	Extended Register Capable	1 = Extended Registers Exist	R	1

x.15 Bit is Shifted First

1. The Default Value of LINK Bit is Determined by the $\overline{\text{LINKI}}$ Pin.
2. The Default Value of JAB Bit is Determined by the JABI Pin.

Table 6. MI Register 2 (PHY ID #1) Structure and Bit Definition

2.15	2.14	2.13	2.12	2.11	2.10	2.9	2.8
OUI3	OUI4	OUI5	OUI6	OUI7	OUI8	OUI9	OUI10
R	R	R	R	R	R	R	R

2.7	2.6	2.5	2.4	2.3	2.2	2.1	2.0
OUI11	OUI12	OUI13	OUI14	OUI15	OUI16	OUI17	OUI18
R	R	R	R	R	R	R	R

Bit	Symbol	Name	Definition	R/W	Def.
2.15	OUI3	Company ID, Bits 3-18	SEEQ OUI = 00 – A0 – 7D	R	0
2.14	OUI4				0
2.13	OUI5				0
2.12	OUI6				0
2.11	OUI7				0
2.10	OUI8				0
2.9	OUI9				0
2.8	OUI10				0
2.7	OUI11				0
2.6	OUI12				0
2.5	OUI13				0
2.4	OUI14				1
2.3	OUI15				0
2.2	OUI16				1
2.1	OUI17				1
2.0	OUI18				0

x.15 Bit Is Shifted First

Table 7. MI Register 3 (PHY ID #2) Structure and Bit Definition

3.15	3.14	3.13	3.12	3.11	3.10	3.9	3.8
OUI19	OUI20	OUI21	OUI22	OUI23	OUI24	PART5	PART4
R	R	R	R	R	R	R	R

3.7	3.6	3.5	3.4	3.3	3.2	3.1	3.0
PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0
R	R	R	R	R	R	R	R

Bit	Symbol	Name	Definition	R/W	Def.
3.15 3.14 3.13 3.12 3.11 3.10	OUI19 OUI20 OUI21 OUI22 OUI23 OUI24	Company ID, Bits 19-24	SEEQ OUI = 00 – A0 – 7D	R	1 1 1 1 1 0
3.9 3.8 3.7 3.6 3.5 3.4	PART5 PART4 PART3 PART2 PART1 PART0	Manufacturer's Part Number	02_{16}	R	0 0 0 0 1 0
3.3 3.2 3.1 3.0	REV3 REV2 REV1 REV0	Manufacturer's Revision Number	0_{16}	R	0 0 0 0

x.15 Bit is Shifted First

Table 8. MI Register 16 (Configuration) Structure and Bit Definition

16.15	16.14	16.13	16.12	16.11	16.10	16.9	16.8
XMT_DIS	XMT_PDN	0	TXEN_CRS	MREG	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

16.7	16.6	16.5	16.4	16.3	16.2	16.1	16.0
PLED1_1	PLED1_0	PLED0_1	PLED0_0	PLED1_CFG	0	0	0
R/W or R/WSC	R/W or R/WSC	R/W or R/WSC	R/W or R/WSC	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
16.15	XMT_DIS	AUI Transmit Disable	1 = AUI Transmitter Disabled, Force To Idle 0 = Normal	R/W	0
16.14	XMT_PDN	AUI Transmit Powerdown	1 = AUI Transmitter Powered Down 0 = Normal	R/W	0
16.13			Reserved For Factory Use, Must Be 0	R/W	0
16.12	TXEN_CRS	TXEN To CRS Loopback Enable	1 = TX_EN Looped Back To CRS While Non-Idle 0 = No Loopback	R/W	0
16.11	MREG	Multiple Register Access Enable	1 = Multiple Register Access Feature Enabled 0 = No Multiple Register Access	R/W	0
16.10 16.9 16.8			Reserved For Factory Use, Must Be 0	R/W	0 0 0
16.7 16.6	PLED1_1 PLED1_0	Programmable LED Output Select, Pin $\overline{\text{PLED1}}$	11 = Collision ($\overline{\text{PLED1}}$ Is Low For 100 mS When Collision Occurs,Then Pin Returns High and Bit Clears Itself) 10 = LED Blink ($\overline{\text{PLED1}}$ Is Toggling 100 mS Low, 100 mS High) 01 = LED On ($\overline{\text{PLED1}}$ Is Low) 00 = LED Off ($\overline{\text{PLED1}}$ Is High)	R/W or R/W SC	1 1
16.5 16.4	PLED0_1 PLED0_0	Programmable LED Output Select, Pin $\overline{\text{PLED0}}$	11 = Activity ($\overline{\text{PLED0}}$ Is Low For 100 mS When Activity Occurs,Then Pin Returns High and Bit Clears Itself) 10 = LED Blink ($\overline{\text{PLED0}}$ Is Toggling 100 mS Low, 100 mS High) 01 = LED On ($\overline{\text{PLED0}}$ Is Low) 00 = LED Off ($\overline{\text{PLED0}}$ Is High)	R/W or R/W SC	1 1
16.3	PLED1_CFG	PLED1 Configuration Select	1 = $\overline{\text{PLED1}}$ Is Link Detect When PLED1_[1:0]=11 0 = $\overline{\text{PLED1}}$ Is Collision When PLED1_[1:0]=11	R/W	0
16.2			Reserved For Factory Use, Must Be 0	R/W	0
16.1			Reserved For Factory Use, Must Be 0	R/W	0
16.0			Reserved For Factory Use, Must Be 0	R/W	0

x.15 Bit is Shifted First

Figure 6. EEI Frame Timing Diagram

3.19 EXTERNAL EEPROM INTERFACE (EEI)

3.19.1 General

The default values of the MI serial port registers can be modified externally through the External EEPROM Interface, called EEI. The EEI will automatically fetch data stored in an external EEPROM (or equivalent) and use this data to overwrite the default values in the MI registers. This automatic fetch and write function is initiated when VCC is applied to the device or when the MI serial port reset bit is set. The EEI can overwrite all the bits in the MI registers including the read bits (with the exception of RESET, JAB, and LINK).

The EEI is intended to interface to the 9346 family of EEPROM's.

3.19.2 Signal Description

The EEI consists of four pins, EE_CS, EE_CLK, EE_DI, and EE_DO. EE_CS is a chip select output. EE_CLK is a serial shift clock output. EE_DI and EE_DO are the data in and data out pins, respectively.

3.19.3 Frame Structure

Each EEI frame consists of six individual accesses of the external EEPROM memory, called EE_CS cycles. A diagram of the frame structure is shown in Figure 6.

Each EE_CS cycle (exclusive of the first cycle) accesses one 16 bit register in the external EEPROM and moves the contents of that EEPROM register into one of the five MI registers. The correspondance of EE_CS cycle number to which EEPROM register is read to which MI register is written to is shown in Table 9 as well as Figure 6.

The first EE_CS cycle is used by the 8502 to determine if there is an EEPROM or equivalent connected to the EEI; it does not load any data into any MI register. This identification of an EEPROM or equivalent on the EEI is done by examination of a specific EEPROM register for a specific data pattern. If the contents of the first EEPROM register accessed (EEPROM register 000001) is $A07D_{16}$, then the remainder of the EEPROM data is fetched and written into the MI registers as described. If the content of EEPROM register 000001 is not $A07D_{16}$, the EEI frame is terminated, the contents of the EEPROM are not written into the MI registers, and the default values remain in the MI registers.

Table 9. EEI To MI Register Correspondance

EE_CS Cycle	EEI Register Read Out (REG[5:0])	MI Register Written To	
		Address	Name
1	000001	-----	-----
2	000011	00000	Control
3	000111	00001	Status
4	001111	00010	PHY ID #1
5	011111	00011	PHY ID #2
6	111111	10000	Configuration

3.19.4 EE_CS Cycle Structure

A description of the EE_CS cycle structure is shown in Table 10 and in Figure 6. Each EE_CS cycle consists of 25 bits. The first 9 bits of an EE_CS cycle are always read bits and are used to provide instructions and register addressing to the external EEPROM. The last 16 bits are write bits and are loaded from the external EEPROM into one of the MI registers per Table 9 and Figure 6.

The first bit in a EE_CS cycle is read out on the EEI as a 1 and instructs the external EEPROM to start an access cycle. The next two bits are read out as a 10 and contain the opcode instruction for the external EEPROM to execute a read cycle. The next 6 bits are one of six register addresses read out to the external EEPROM and contain the address of the 16 bit register in the external EEPROM where the data is to be fetched. On the same clock cycle that the last register address bit is read out to the external EEPROM, the external EEPROM may also send back a "0" on EE_DO. The 8502 ignores this "0" data. The next 16 bits are written into the 8502 from the EEPROM and are written into a specific MI register as shown in Table 9 and Figure 6.

There are three individual MI bits whose value will not be modified or should not be modified through the EII: (1) Reset, bit 0.15, (2) Link Detect, bit 1.2, and (3) Jabber Detect, 1.1. The Reset bit should not be modified through the EEI and should only be set to a 1 via a MI write to that bit; the Link Detect and Jabber Detect bits will not be modified by the EEI, so refer to the Link and Jabber sections for more details how these bits are set and reset.

3.19.5 Timing

The total EEI cycle consists of six individual EE_CS cycles, one for each register accessed over the EEI. Before a reset is initiated, the EEI is in the idle state. During idle, EE_CS=0, EE_DO is in the high impedance state, EE_DI is ignored, and EE_CLK clock output is held low. When a reset is initiated, then EE_CS is asserted high, EE_CLK clock output is enabled, and a serial shift cycle is initiated between the external EEPROM and the 8502. Data on EE_DO is then shifted out from the 8502 to the EEPROM on the first 9 falling edges of EE_CLK. On the next 16 falling edges of EE_CLK, data is shifted into the 8502 from the EEPROM on EE_DI (EE_DO is high impedance). After 25 EE_CLK cycles have been completed, EE_CS goes low, EE_DO goes to high impedance, EE_DI stops latching in data, the last 16 data bits shifted in are latched into the 8502, and the serial shifting process is halted. This process is repeated five more times, once for each of the five internal MI registers as shown in Tables 10 and 11 and Figure 6. Once all six EE_CS access cycles have been completed, then the EEI returns to the idle state.

Table 10. EEI EE_CS Cycle Structure

<1>	<10>	<Register Addr.>	<Data>
START	OP[1:0]	A[5:0]	D[15:0]

000001	Identification
000011	MI Register 0
000111	MI Register 1
001111	MI Register 2
011111	MI Register 3
111111	MI Register 16

Symbol	Name	Definition	R/W
START	Start Bit	1 Read Out To EEPROM On Every EE_CS Cycle	R
OP[1:0]	EEPROM Opcode Instruction	10 Read Out To EEPROM On Every EE_CS Cycle	R
A[5:0]	EEPROM Register Address	EEPROM Register Address Where Data Will Be Fetched on Each of the 6 EE_CS Cycles and Loaded into the MI Registers as Shown in Table 10 And Figure 6.	R
D[15:0]	MI Data	These 16 Bits Contain Data Written from the External EEPROM into the MI Registers According to Table 10. The First Register Written from Regad = 000001 must Contain $A07d_{16}$ for the Access to Continue.	W

START is Shifted Out First

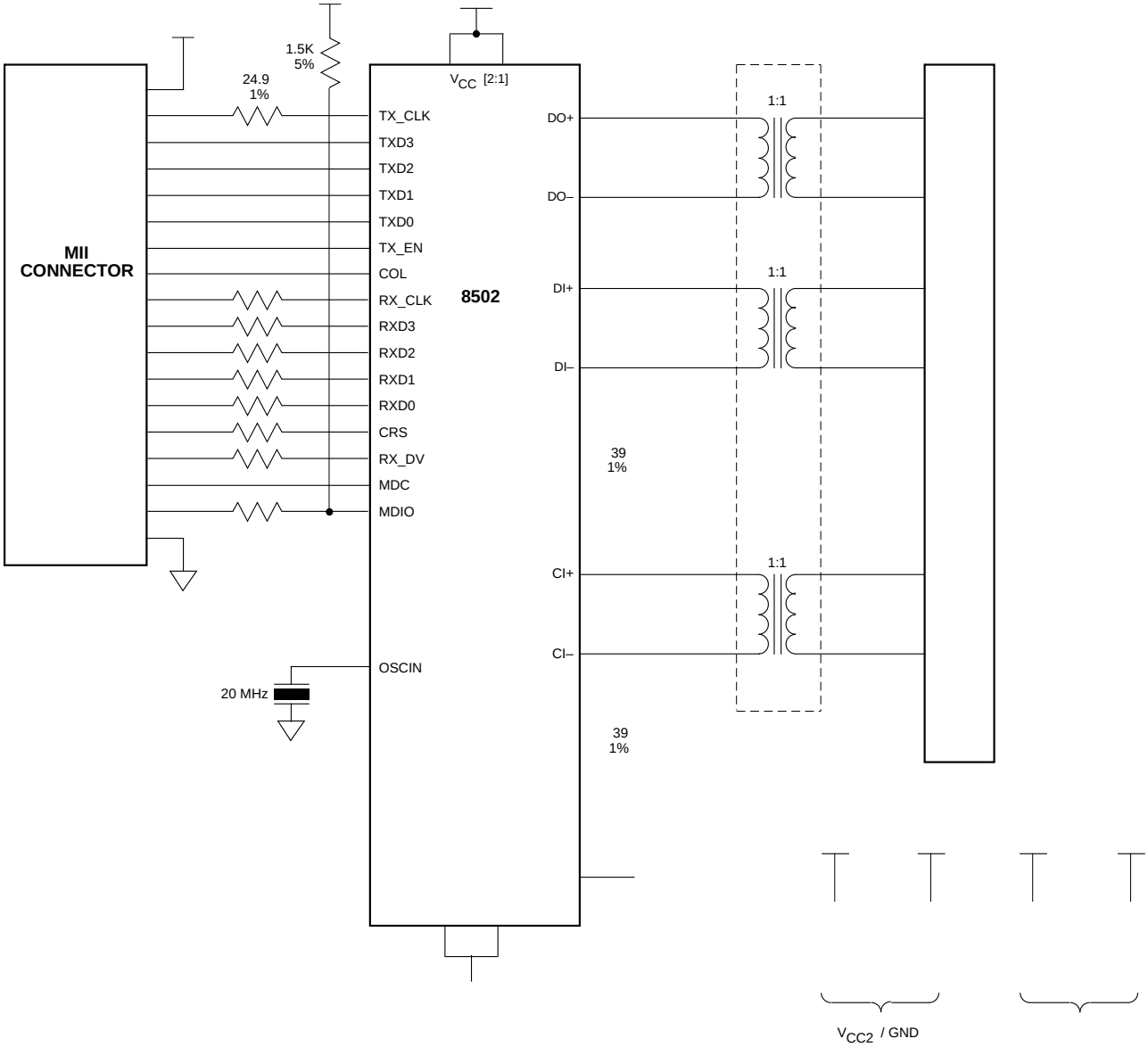


Figure 7. External MII-AUI Schematic Using 8502

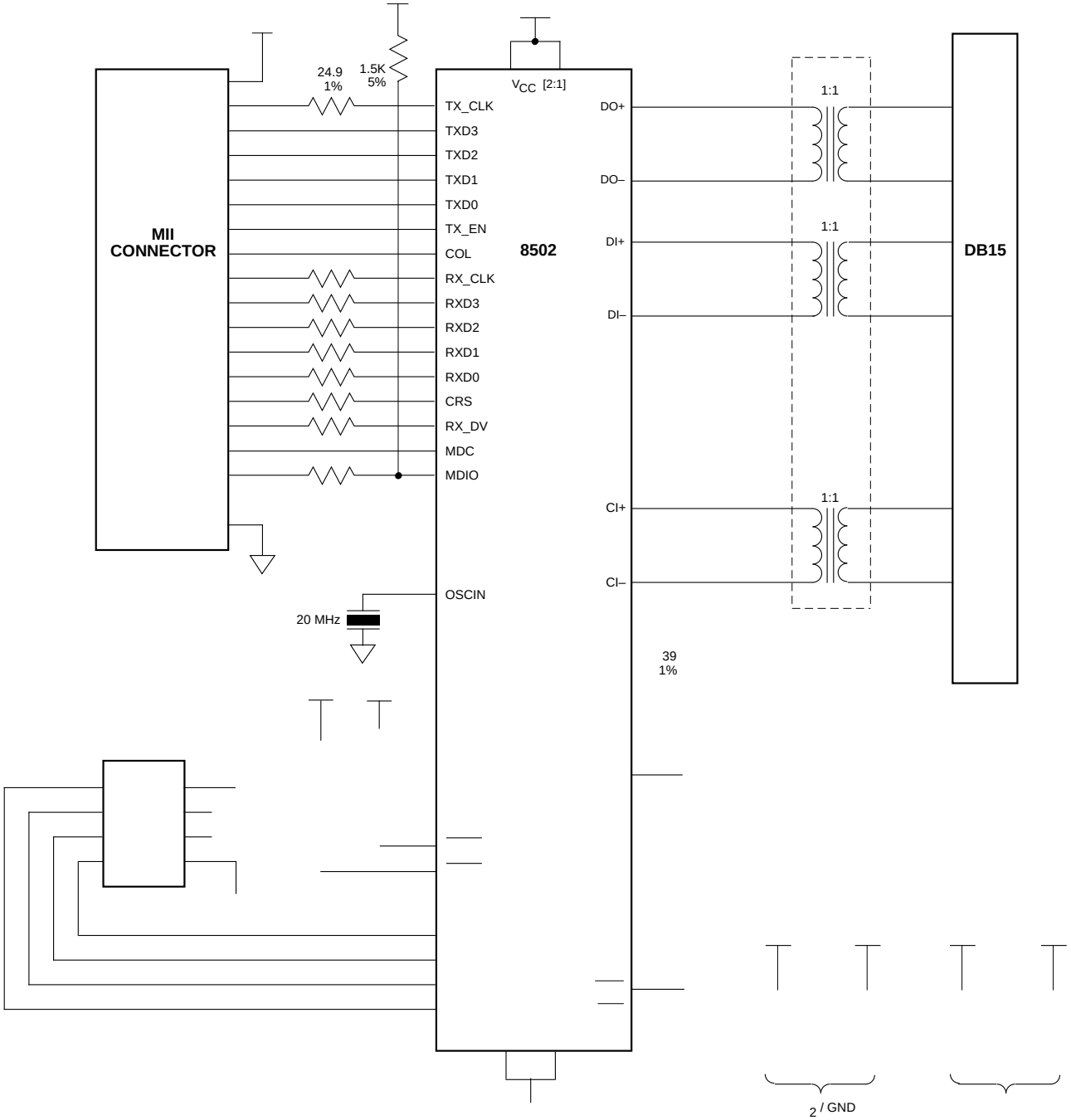


Figure 8. External MII-AUI Schematic Using 8502 with EEPROM and LED's

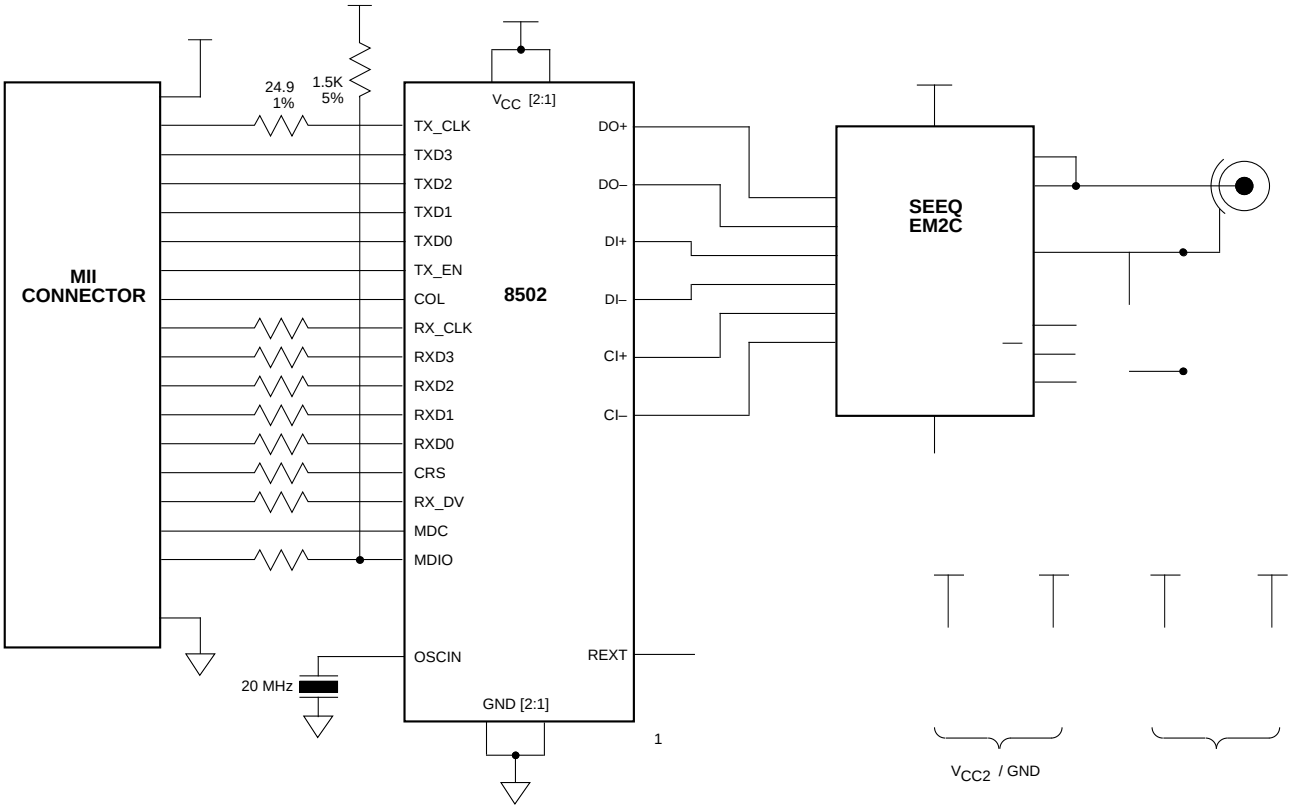


Figure 9. External MII-Coax PHY Schematic Using 8502

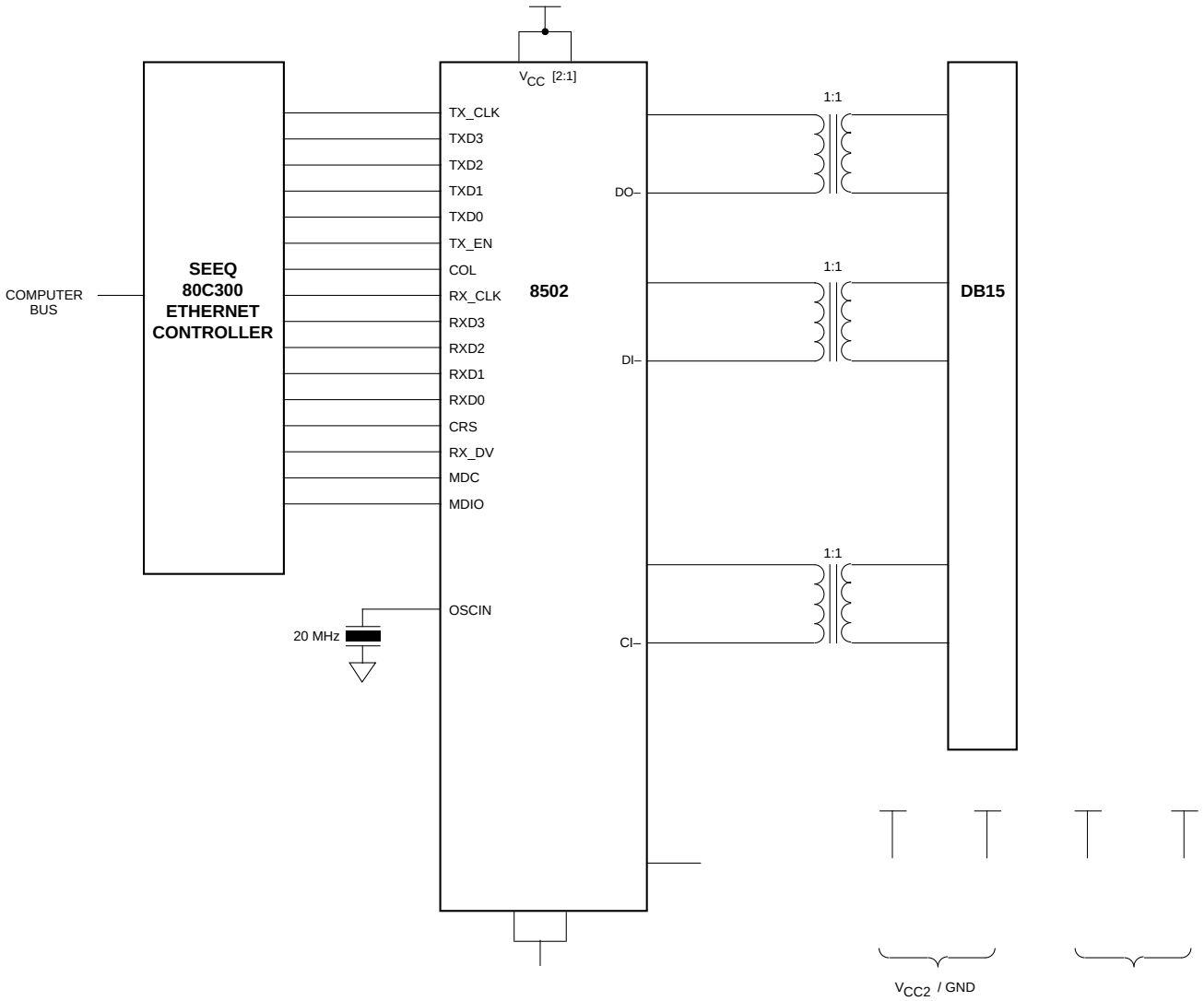


Figure 10. Network Interface Card Schematic Using 8502

4.0 APPLICATION INFORMATION

4.1 EXAMPLE SCHEMATICS

Typical examples of the 8502 used in external MII-AUI, external PHY, and Network Interface Card application are shown in Figures 7-10. Figure 7 is the 8502 used in an external MII-AUI application. Figure 8 is the 8502 used in an external MII-AUI application with LED's and external EEPROM. Figure 9 is the 8502 used in an external MII-COAX PHY application. Figure 10 is the 8502 in a Network Interface Card application.

4.2 AUI TRANSMIT INTERFACE

The interface between the AUI outputs on DO± and the AUI cable requires a transformer as shown in Figures 7-10. A 10K resistor is also needed between RBIAS pin and GND to provide internal bias for the transmitter. For proper AUI output levels, the DO± outputs must be connected to a 78 Ohm cable or some other 78 Ohm load. No other external components are required.

The AUI transformer specifications for the transmitter are shown in Table 11. Some sources for the AUI transformer are listed in Table 12, but most standard AUI transformers should meet these requirements.

Table 11. AUI Transformer Specification

Parameter	Specification
Turns Ratio	1:1
Inductance (µH Min)	75
Leakage Inductance (µH Max)	0.4
Capacitance (pF Max)	10
DC Resistance (Ohms Max)	0.25

To minimize noise pickup, the loading on DO± should be minimized and both outputs should always be loaded equally.

4.3 AUI RECEIVE INTERFACE

Receive data is typically transformer coupled into the receive inputs on DI± and terminated with an external resistor as shown in Figures 7-10.

The AUI transformer specifications for the receiver are shown in Table 11. Some sources for the AUI transformer are listed in Table 12, but most standard AUI transformers should meet these requirements.

Table 12. AUI Transformer Sources

Vendor	Part Number
Valor	ST7033
NanoPulse	5421-30
Pulse Engineering	PE65728
Belfuse	S553-1006-AE
PCA	EPA 1885-6

The receive input needs to be terminated with 78 Ohms in order to meet input impedance requirements of IEEE 802.3 Section 7. Notice that in Figures 7, 8 and 10 the receive input has this input termination resistor broken up into two 39 ohm 1% resistors with a 0.1µF capacitor tied between the center points and GND. This capacitor attenuates common mode input noise. The 0.1µF capacitor is optional and is only needed if the device is required to meet the receive common mode input AC voltage specification in IEEE 802.3 Section 7. The 0.1µF capacitors are not needed if the AUI is embedded, that is, restricted to a PCB or other piece of equipment where common mode noise is small on the AUI inputs. If the capacitor is not needed, then the two termination resistors can be lumped into one 78 Ohm 1% resistor across DI±.

In order to minimize noise pickup into the receive path, loading on DI± should be minimized and both inputs should be loaded equally.

4.4 CONTROLLER INTERFACE

4.4.1 General

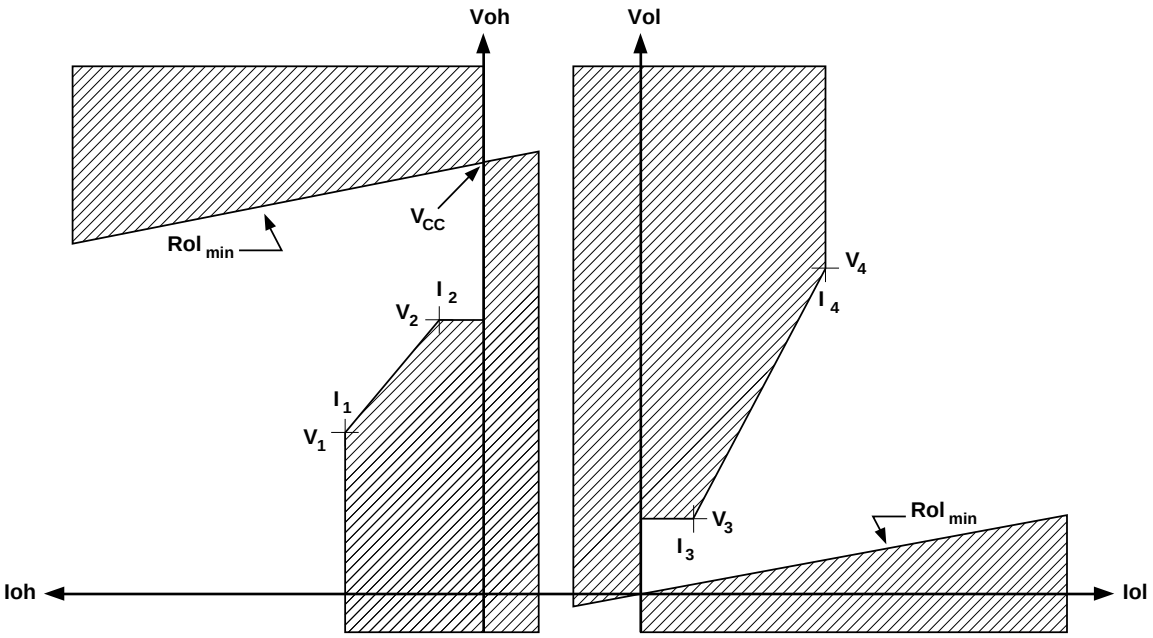
The 8502 will connect to any Ethernet controller without any glue logic provided that the external Ethernet controller has a MII interface that complies with IEEE 802.3.

4.4.2 Output Drivers

The digital outputs on the 8502 MII signals can meet the external MII driver characteristics specified in IEEE 802.3 and shown in Figure 11 if external 24.9 ohm 1% termination resistors are added. These termination resistors are only needed if the outputs have to drive a MII cable or other transmission line type load, such as in the external MII applications shown in Figures 7-10. If the 8502 is used in internal MII applications such as adapter cards or on a motherboard, then these termination resistors are not needed, as shown in the schematic in Figure 10.

4.4.3 MII Disable

The MII inputs and outputs can be disabled by setting the MII disable bit in the MI serial port Control register. When the MII is disabled, the MII inputs don't respond to any input signals and the MII outputs are placed in the high impedance state. The default value of this bit when the device powers up or is reset is dependent on the device address. If the device address latched into MDA[1:0] at reset is not 11, it is assumed that the device is being used in applications where it is the only device on the MII bus, like adapter card, and the device powers up with the MII enabled. If the device address latched into MDA[1:0] at reset is 11, it is assumed that the device is being used in application where many devices could be sharing the same MII bus, like an external PHY, and the device powers up with the MII disabled.



I - V	I (mA)	V (Volts)
I_1, V_1	–20	1.10
I_2, V_2	–4	2.4
I_3, V_3	4	0.40
I_4, V_4	43	3.05

Roh_{min} Rol_{min} equals 40 ohms

Figure 11. MII Output Driver Characteristics

4.5 MI SERIAL PORT

4.5.1 General

The 8502 has a MI serial port to set all of the devices's configuration inputs and read out the status outputs. Any external device that has a IEEE 802.3 compliant MI interface can connect directly to the 8502 without any glue logic, as shown in Figures 7-10.

As described earlier, the MI serial port consists of 4 lines: MDC, MDIO, and MDA[1:0]. However, only 2 lines, MDC and MDIO, are needed to shift data in and out. MDA[1:0] are provided for convenience only.

The MDA[1:0] addresses are inverted inside the 8502 before going to the MI serial port block. For example, the MDA[1:0] pins would have to be pin strapped to 11 externally in order to successfully match the MI physical address bits PHYAD[1:0]=00 internally.

4.5.2 Multiple Register Access

If the MI serial port needs to be constantly polled in order to monitor changes in status output bits, all registers can be accessed on a single MI serial port access cycle by setting the register address REGAD[4:0]=11111 with the multiple register access mode enabled. This eliminates the need to poll registers individually. Multiple register access is normally disabled but can be enabled by setting the multiple register access bit in the MI serial port Configuration register.

4.5.3 Serial Port Addressing

The device address for the MI serial port is selected by tying the MDA[1:0] pins to the desired value. MDA[1:0] share the same pins as the PLED[1:0] outputs, respectively, as shown in Figure 12a. At powerup or reset, the output drivers are high impedance for an interval called the poweron reset time. During the power on reset interval, the value on these pins is latched into the device, inverted, and used as the MI serial port address. The LED outputs are open drain with internal resistor pullup to VCC.

If an LED is desired on the LED outputs, then an LED and resistor are tied to VCC as shown in Figures 12b. If a high address is desired, then the LED to VCC automatically makes the latched address value a high. If a low value for the address is desired, then a 50K resistor to GND must be added as shown in Figure 12b.

If no LED's are needed on the LED outputs, the selection of addresses can be done without any external components as shown in Figure 12c. If a high address is desired, the pin should be left floating and the internal pullup will pull the pin high during power on reset and latch in a high address value. If a low address is desired, then the output pin should be tied to GND or tied to GND through an optional 10K resistor as shown in Figure 12c. The optional 10K resistor allows the pin to be used as a digital output under normal conditions.

4.6 RESET

The reset function in the 8502 resets all the internal timers, sets all the input configuration bits in the MI serial port to their default values, loads data into the MI from an external EEPROM (if connected), and latches in the physical address values for the serial port on MDA[1:0]. Reset can be initiated internally or externally.

An internal reset automatically occurs when VCC is applied to the 8502 or when the device comes out of the powerdown state.

An external reset can be initiated by setting the reset bit in the serial port Control register. Setting this bit will create a reset and this bit will clear itself automatically when the reset is completed.

It is not necessary to use the reset function in normal operation; it is available if external control of reset is desired.

4.7 EXTERNAL EEPROM

The EEI is intended as an inexpensive and convenient way to override the MI serial port default values with a user defined set. The EEI provides a glueless interface to the industry standard 9346 EEPROM. The 8502 can automatically detect whether an external EEPROM is present, so no configuration is necessary. The schematic in Figure 8 shows how an external 9346 EEPROM can be connected directly to the 8502. A device other than the 9346 can be connected to the EEI provided it complies with the timing and frame structure of the EEI.

One unique feature of the EEI is that it can modify the default values of the read bits in the MI. Normally, when the read bits are accessed through the MI, they can only be read out and cannot be written into. When the read bits are accessed through the EEI, however, they become write bits and can be overwritten by the contents of the EEPROM. This feature allows the user to modify the OUI and other capability bits to match the characteristics of the end equipment, not the 8502 itself.

If an external EEPROM or other device is used with the EEI to override the MI register default values, the EEPROM needs to be programmed according to the EEPROM memory map shown in Table 14. In Table 14, the names for individual bit locations correspond to the MI register bit names, and values in these register locations in the EEPROM will be automatically loaded into the corresponding MI bit locations when a reset is initiated.

Note that the value of the Reset bit should always be written as a 0 from the EEI; if it is written to a 1, the device will be resetting for eternity. Also note that the Link Detect and Jabber Detect bits are not overwritten by the EEI. Also note that there are some reserved bits in the Configuration register that must be written to specific values for the device to function properly.

4.8 OSCILLATOR

The 8502 requires a 20 Mhz reference frequency for internal signal generation. This 20 Mhz reference frequency can be generated by either connecting an external 20 MHz crystal between OSCIN and GND or by applying an external 20 MHz clock to OSCIN.

If the crystal oscillator is used, it needs only an external crystal, and no other external capacitors or other components are required. The crystal must have the characteristics shown in Table 13. The crystal must be placed as close as possible to OSCIN and GND so that parasitics on OSCIN are kept to a minimum.

Table 13. Crystal Specifications

Parameter	Spec
Type	Parallel Resonant
Frequency	20 Mhz +/- 0.01%
Equivelent Series Resistance	25 ohms max
Load Capacitance	18 pF typ
Case Capacitance	7 pF max
Power Dissipation	1mW max

4.9 PROGRAMMABLE LED DRIVERS

The $\overline{\text{PLED[1:0]}}$ outputs can drive LED's tied to VCC as shown in Figure 6. The $\overline{\text{PLED[1:0]}}$ outputs can be programmed through the MI serial port to do 4 different functions: (1) Normal Function (2) On, (3) Off, and (4) Blink. PLED[1:0] can be programmed by appropriately setting the LED output select bits in the MI serial port Configuration register. When $\overline{\text{PLED[1:0]}}$ is programmed for its Normal function, these outputs indicate the specific functions described in the MI serial port Configuration register shown on Table 10 (Collision, Activity). When $\overline{\text{PLED[1:0]}}$ is programmed to be On, the LED output driver goes low, thus turning on the LED under user control. When $\overline{\text{PLED[1:0]}}$ is programmed to be Off, the LED output driver will turn off, thus turning off the LED under user control. When $\overline{\text{PLED[1:0]}}$ is programmed to Blink, the LED output driver will continuously blink at a rate of 100 mS on, 100 mS off.

The normal function for $\overline{\text{PLED1}}$ can be changed from Collision to Link Detect by setting the PLED1 configuration select bit in the MI serial port Configuration register.

The On and Off functions allow the LED driver to be controlled directly through the MI serial port to indicate any function that is desired under external control. The Blink function allows the same external control of the LED driver and also offers the provision to blink the LED without the need for any external timers.

The $\overline{\text{PLED[1:0]}}$ outputs can also drive other digital inputs. Thus, $\overline{\text{PLED[1:0]}}$ can also be used as digital outputs whose function can be user defined and controlled through the MI serial port.

4.10 LINK PASSTHROUGH

The $\overline{\text{LINKI}}$ pin can be used to force the status reported on the MI serial port Link Status output bit. If $\overline{\text{LINKI}}$ is tied to the Link Status output pin from an external transceiver, the link status from the external transceiver will be inverted and passed through to and be reported on the Link Status bit in the MI Status register.

4.11 JABBER PASSTHROUGH

The $\overline{\text{JABI}}$ pin is can be used to force the status reported on the MI serial port Jabber Detect output bit. If $\overline{\text{JABI}}$ is tied to the Jabber Detect output pin from an external transceiver, the Jabber Detect status from the external transceiver will be inverted and passed through to and be reported on the Jabber Detect bit in the MI Status register.

4.12 POWER SUPPLY DECOUPLING

There are two VCC's on the 8502 (VCC[2:1]) and two GND's (GND[2:1]).

Both VCC's should be connected together as close as possible to the device with a large VCC plane. If the VCC's vary in potential by even a small amount, noise and latchup can result. The two VCC's should be kept to within 50 mV of each other.

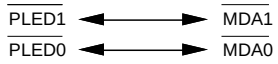
Both GND's should also be connected together as close as possible to the device with a large ground plane. If the GND's vary in potential by even a small amount, noise and latchup can result. The two VCC's should be kept to within 50 mV of each other.

A 0.01-0.1 μF decoupling capacitor should be connected between each VCC/GND set as close as possible to the device pins, preferably within 0.5". The value of the decoupling capacitor should be selected based on whether the noise on VCC-GND is high or low frequency. A conservative approach would be to use two decoupling

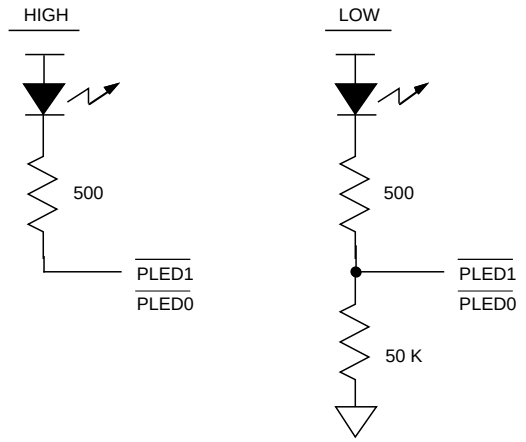
capacitors on each VCC/GND set, one 0.1µF for low freuqency and one 0.001µF for high frequency noise on the power supply.

The PCB layout and power supply decoupling discussed above should provide sufficient decoupling to acheive the following when measured at the device: (1) the resultant AC noise voltage measured across each VCC/GND set should be less than 100 mVpp, (2) all VCC's should be within 50 mVpp of each other, and (3) all GND's should be within 50 mVpp of each other.

a.) OUTPUT DRIVER / INPUT ADDRESS CORRESPONDENCE



b.) SETTING ADDRESS WITH LEDs



c.) SETTING ADDRESS WITHOUT LEDs

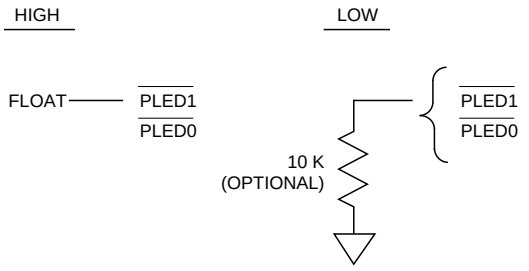


Figure 12. MI Serial Port Address Selection

5.0 Specifications

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limits beyond which may cause permanent damage to the device or affect device reliability. All voltages are specified with respect to GND, GND unless otherwise specified.

V_{CC} Supply Voltage ..... –3V to 7V

All Inputs and Outputs ..... –3V to V_{CC}+.3V

Input Latchup Current ..... +/-25 mA

Package Power Dissipation ..... 3 Watt @ 25°C

Storage Temperature ..... –65 to +150°C

Operating Temperature ..... –65 to +85°C

Lead Temperature (Soldering, 10 Sec) ..... 250°C

M Memory Map

	x.7	x.6	x.5	x.4	x.3	x.2	x.1	x.0
	0	1	1	1	1	1	0	1
X	COLTST	0	0	0	0	0	0	0
	0	CAP_SUPR	ANEG_ACK	REM_FLT	CAP_NWY	LINK	JAB	EXREG
0	OUI11	OUI12	OUI13	OUI14	OUI15	OUI16	OUI17	OUI18

DC Electrical Characteristics

Unless otherwise noted, all test conditions are as follows:

1. T_A = 0 to 70°C
2. V_{CC} = 5V +/-5%
3. 20 MHz +/- 0.01%
4. RBIAS = 10K +/- 1%, no load

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
VIL	Input Low Voltage			0.8	Volt	All except OSCIN, $\overline{\text{MDA[1:0]}}$, $\overline{\text{LINKI}}$
				V_{CC}–1.0	Volt	$\overline{\text{MDA[1:0]}}$
				1.5	Volt	OSCIN
				0.5	Volt	$\overline{\text{LINKI}}$
VIM	Input Intermediate Voltage	1.5		V_{CC}–1.5	Volt	$\overline{\text{LINKI}}$
VIH	Input High Voltage	2			Volt	All except OSCIN, $\overline{\text{MDA[1:0]}}$, $\overline{\text{LINKI}}$
		V_{CC}– 0.3			Volt	$\overline{\text{MDA[1:0]}}$
		3.5			Volt	OSCIN
		V_{CC}– 0.5			Volt	$\overline{\text{LINKI}}$
IIL	Input Low Current			-1	µA	VIN = GND All Except $\overline{\text{MDA[1:0]}}$, OSCIN, EE_DI, $\overline{\text{LINKI}}$
		-12		-50	µA	VIN = GND EE_DI
		- 5		-25	µA	VIN = GND $\overline{\text{MDA [1:0]}}$
				-150	µA	VIN = GND OSCIN, $\overline{\text{LINKI}}$
IIH	Input High Current			1	µA	VIN = VCC All Except OSCIN, $\overline{\text{LINKI}}$
				150	µA	VIN = VCC OSCIN, $\overline{\text{LINKI}}$
VOL	Output Low Voltage			0.4	Volt	IOL = 4mA All except $\overline{\text{PLED[1:0]}}$
				1	Volt	IOL = -20 mA $\overline{\text{PLED[1:0]}}$
VOH	Output High Voltage	V_{CC} - 1.0			Volt	IOH = 4 mA All except $\overline{\text{PLED[1:0]}}$, XMT_LED, RCV_LED
		V_{CC} - 1.0			Volt	IOH = 10 mA, XMT_LED, RCV_LED
		2.4			Volt	IOH = 4µA $\overline{\text{PLED[1:0]}}$
CIN	Input Capacitance		5		pF	
ICC	VCC Supply Current		85	110	mA	Transmitting
			1.3	3.06	mA	Powerdown Mode

AUI CHARACTERISTICS, TRANSMIT

Unless otherwise noted, all test conditions are as follows:

1. T_A = 0 to 70°C
2. V_{CC} = 5V +/-5%
3. 10 MHz +/- 0.01%
4. RBIAS = 10K +/- 1%
5. 78 ohm, 27µH load across DO±

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
TOV	DO± Differential Output Voltage	550		1200	mV pk	
TOVT	DO± Differential Output Voltage Template	See Figure 3				
TORF	DO± Output Rise And Fall Time			5	nS	t_r, t_f measured at –450 mV and +450 mV points
TOJ	Transmit Output Jitter			± 0.5	nS	
TOIV	DO± Differential Output Idle Voltage			+/– 40	mV	
TOVU	DO± Differential Output Undershoot During Idle			–100	mV	
TCMD	DO± Common Mode DC Output Voltage		$V_{CC}/4$ +0.5		mV pk	Voltage on Either DO+ or DO– Relative to GND

AUI CHARACTERISTICS, RECEIVE

Unless otherwise noted, all test conditions are as follows:

1. T_A = 0 to 70°C
2. V_{CC} = 5V +/-5%
3. 10 MHz +/- 0.01%
4. RBIAS = 10K +/- 1%
5. 10 MHz sinewave on DI±, C±

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
RST	DI±, CI± Squelch Threshold	–175		–325	mV	
RUT	DI±, CI± Unsquelch Threshold	–100		–225	mV	
ROCV	DI±, CI± Input Open Circuit Voltage		3.0 ±0.5		Volt	Voltage on Either DI+/CI+ or DI–/CI– Relative to GND.
RCMR	DI±, CI± Input Common Mode Voltage Range		ROCV ±0.5		Volt	
RDR	DI±, CI± Input Differential Voltage Range	GND		V_{CC}	Volt	Voltage on Either DI+/CI+ or DI–/CI– Relative to GND.
RIR	DI±, CI± Input Resistance	5K			Ohm	
RIC	DI±, CI± Input Capacitance		10		pF	

AC Test Timing Conditions

Unless otherwise noted, all test conditions are as follows:

1. T_A = 0 to 70°C
2. V_{CC} = 5V +/-5%
3. 20 MHz +/- 0.01%
4. RBIAS = 10K +/- 1%, no load
5. Input conditions:
   All Inputs: tr, tf <= 10nS, 20-80%
6. Output Loading
   DO±: 78 Ω, 27 µH
   Open Drain Outputs: 1K Ω Pullup, 50 pF
   All Other Digital Outputs: 50pF
7. Measurement Points:
   DO±, DI±, CI±: 0.0V During Data, ±0.3V at start/end of packet
   All other inputs and outputs: 1.5 Volts

20 MHz Clock Timing Charateristics

Refer To Figure 13 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_1	OSCIN Cycle Time	49.995	50	50.005	nS	
t_2	OSCIN High Time	15			nS	OSCIN Driven by External Clock
t_3	OSCIN Low Time	15			nS	OSCIN Driven by External Clock
t_4	OSCIN To TX_CLK Delay			20	nS	

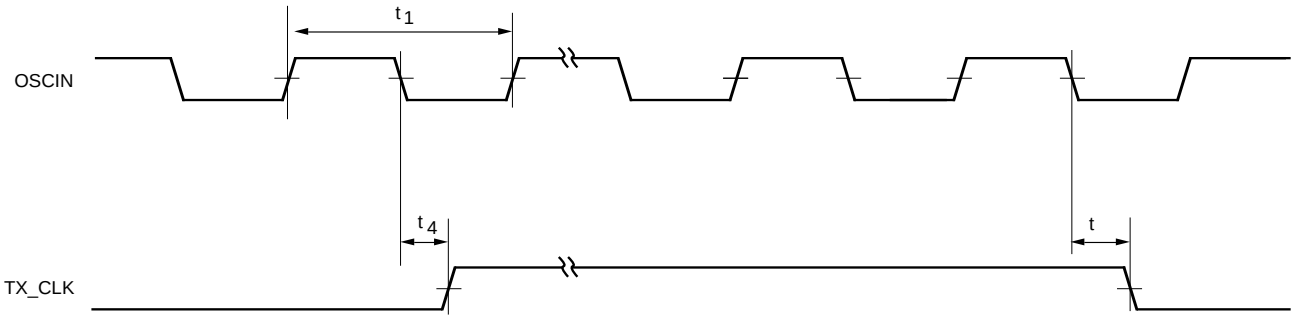
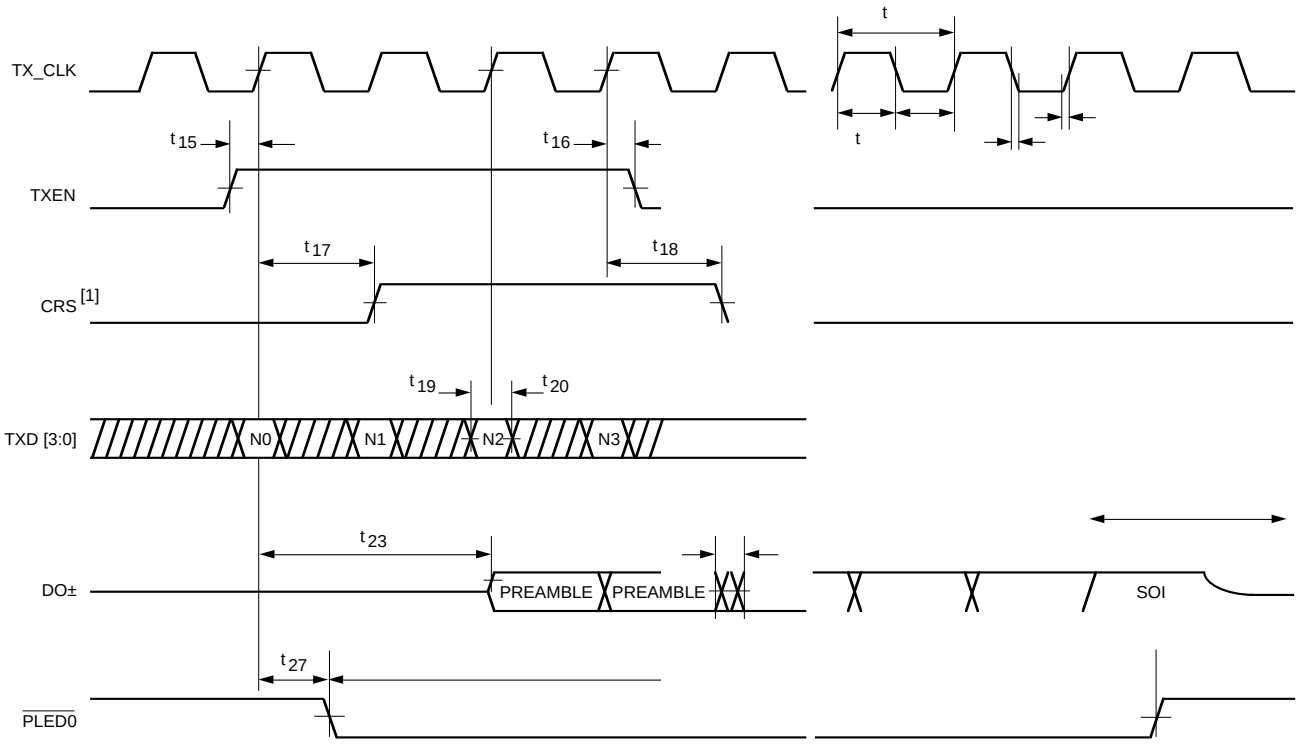


Figure 13. 20 MHz Clock Timing

Transmit Timing Charateristics

Refer To Figure 14 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{11}	TX_CLK Cycle Time	399.96	400	400.04	nS	
t_{12}	TX_CLK High Time	160	200	240	nS	
t_{13}	TX_CLK Low Time	160	200	240	nS	
t_{14}	TX_CLK Rise/Fall Time			10	nS	
t_{15}	TX_EN Setup Time	40			nS	
t_{16}	TX_EN Hold Time	0			nS	
t_{17}	CRS During Transmit Assert Time			40	nS	TXEN_CRS=1
t_{18}	CRS During Transmit Deassert Time			40	nS	
t_{19}	TXD Setup Time	40			nS	
t_{20}	TXD Hold Time	0			nS	
t_{23}	Transmit Propagation Delay			200	nS	
t_{24}	Transmit Output Jitter			$\pm$ 0.5	nS	
t_{25}	Transmit SOI Pulse Width To 0.3V	225		350	nS	
t_{26}	Transmit SOI Pulse Width to 40 mV			7000	nS	
t_{27}	$\overline{\text{PLED0}}$ Assert Time			55	mS	$\overline{\text{PLED0}}$ Programmed For Activity
t_{28}	$\overline{\text{PLED0}}$ Pulse Width	45		55	mS	$\overline{\text{PLED0}}$ Programmed For Activity



Note 1. CRS is asserted only when TX_EN to CRS Loopback select bit is programmed in MI Serial Port. Default is TX_EN to CRS Loopback Disabled.

Figure 14. Transmit Timing

Receive Timing Charateristics

Refer To Figures 15 And 16 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{31}	Start Of Packet To CRS Assert Delay			100	nS	
t_{32}	End Of Packet To CRS Deassert Delay			250	nS	
t_{33}	Start Of Packet To RX_DV Assert Delay			2000	nS	
t_{34}	End Of Packet To RX_DV Deassert Delay			900	nS	
t_{36}	Start Of Packet To First Data Nibble Delay			7300	nS	
t_{37}	RX_CLK To RX_DV, RXD Delay	0		25	nS	
t_{38}	RX_CLK High Time	180	200	220	nS	
t_{39}	RX_CLK Low Time	180	200	1200	nS	
t_{40}	Minimum SOI Pulse Width Required For Idle Detection	125		200	nS	Measure On DI± from last zero cross in Middle of Manchester Bit Cell to 0.3V point.
t_{41}	Receive Input Jitter			±18.0	nS	Data
				±12.0	nS	Preamble
t_{42}	$\overline{\text{PLED0}}$ Assert Time			55	mS	$\overline{\text{PLED0}}$ Programmed For Activity
t_{43}	$\overline{\text{PLED0}}$ Pulse Width	45		55	mS	$\overline{\text{PLED0}}$ Programmed For Activity
t_{44}	RX_CLK, RXD, CRS, RX_DV Output Rise And Fall Times			10	nS	

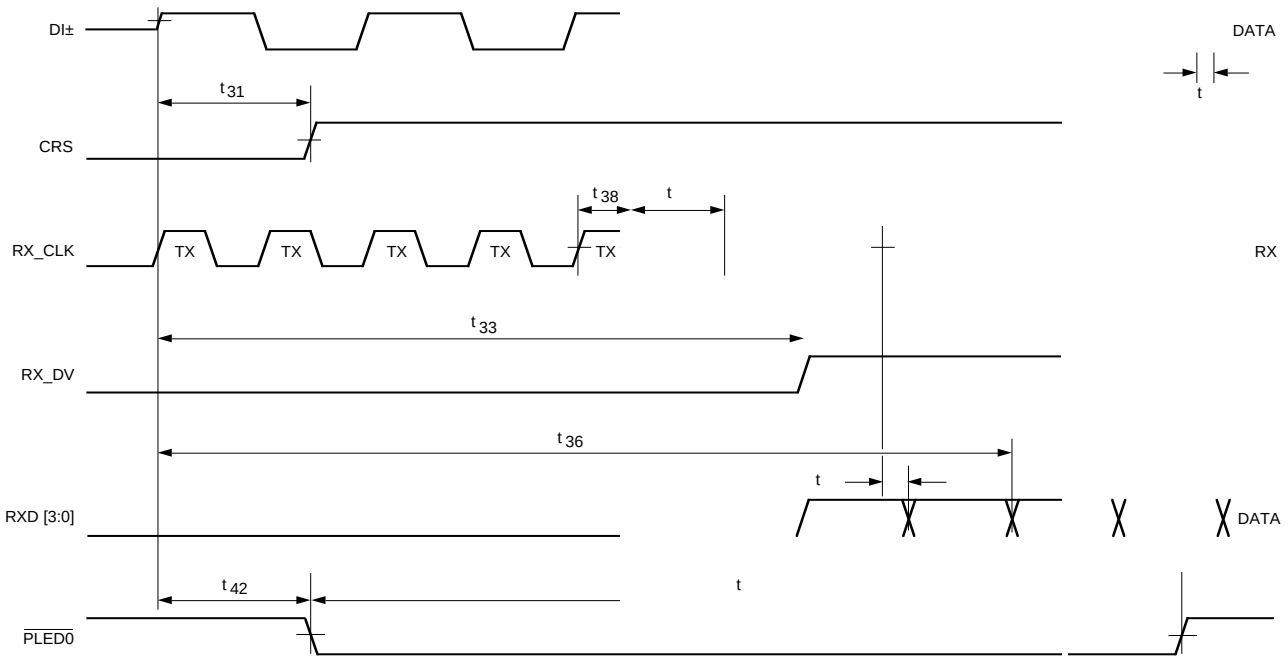


Figure 15. Receive Timing, Start of Packet

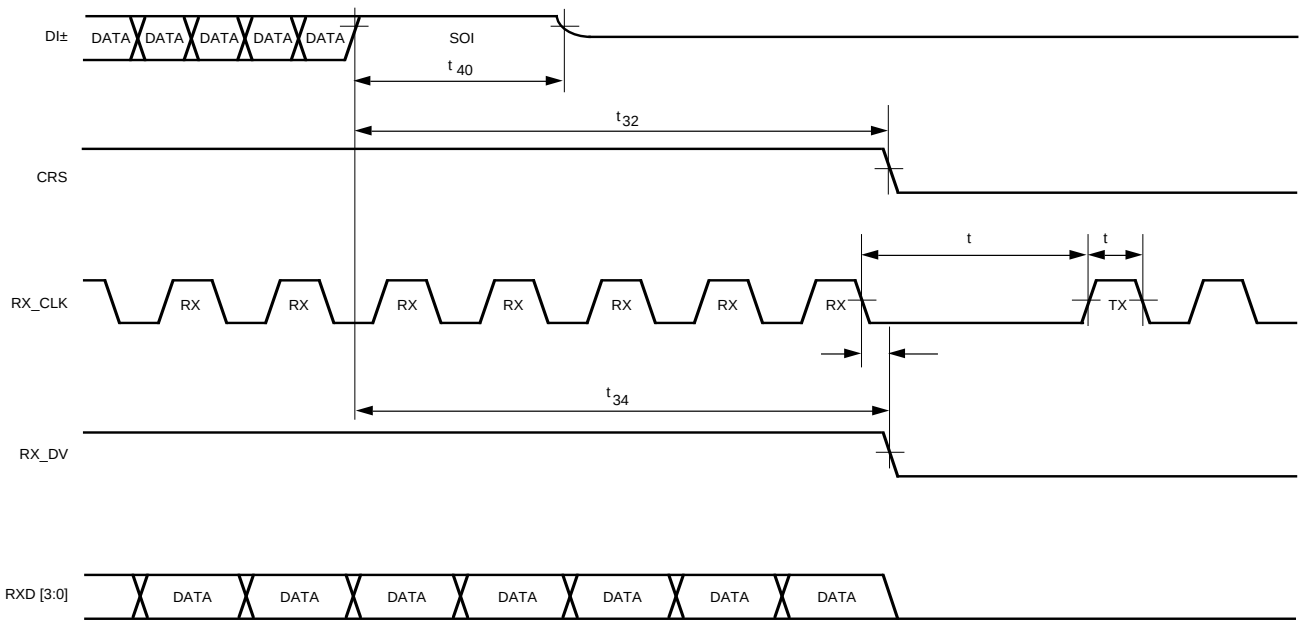


Figure 16. Receive Timing, End of Packet

Collision Timing Characteristics

Refer To Figures 17 and 18 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{51}	CI± Start To COL Assert Time			200	nS	
t_{52}	CI± Stop To COL Deassert Time			400	nS	
t_{53}	CI± Start To CRS Assert Time			200	nS	
t_{54}	Minimum CI± Pulse Width Required For Collision Detection	10		35	nS	
t_{55}	CI± Minimum Cycle Time Required For Collision Detection	48		77	nS	
t_{56}	CI± Maximum Cycle Time Required For Collision Detection	200		400	nS	
t_{57}	COL Rise And Fall Time			10	nS	
t_{58}	$\overline{\text{PLED1}}$ Assert Time			55	mS	$\overline{\text{PLED1}}$ Programmed For Collision
t_{59}	$\overline{\text{PLED1}}$ Pulse Width	45		55	mS	$\overline{\text{PLED1}}$ Programmed For Collision
t_{60}	Collision Test Assert Time			100	nS	
t_{61}	Collision Test Deassert Time			40	nS	

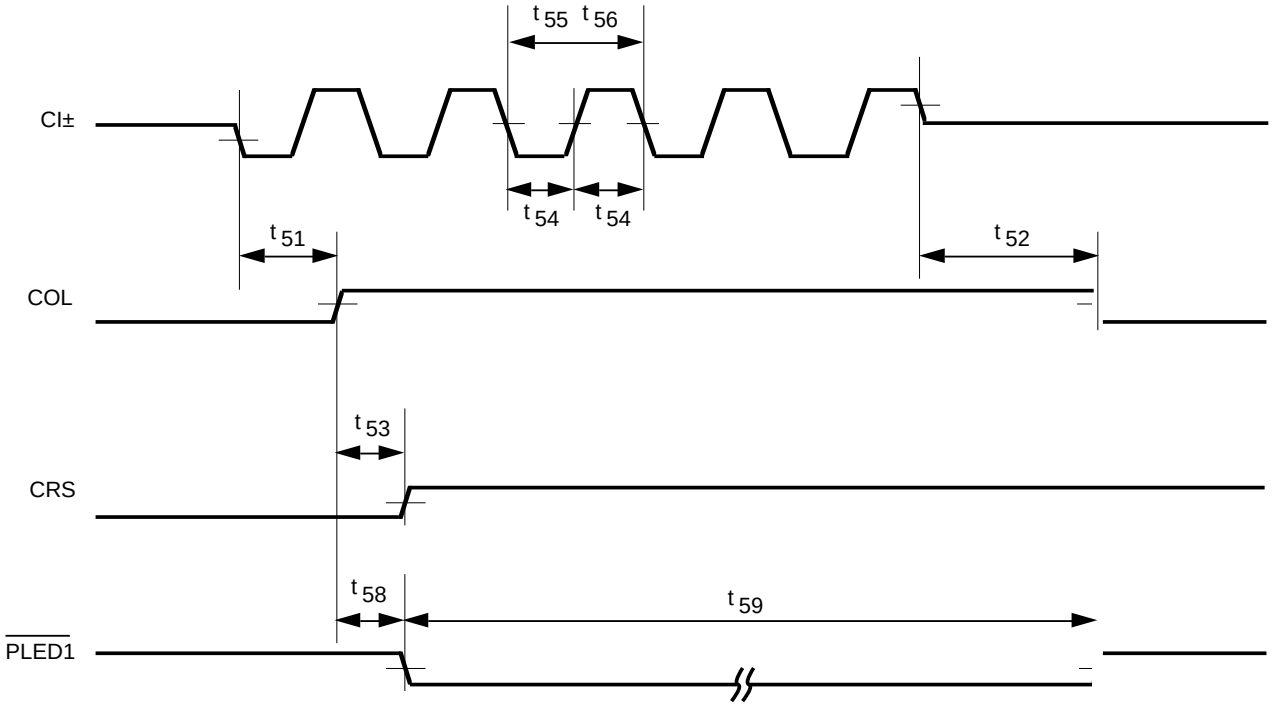


Figure 17. Collision Timing

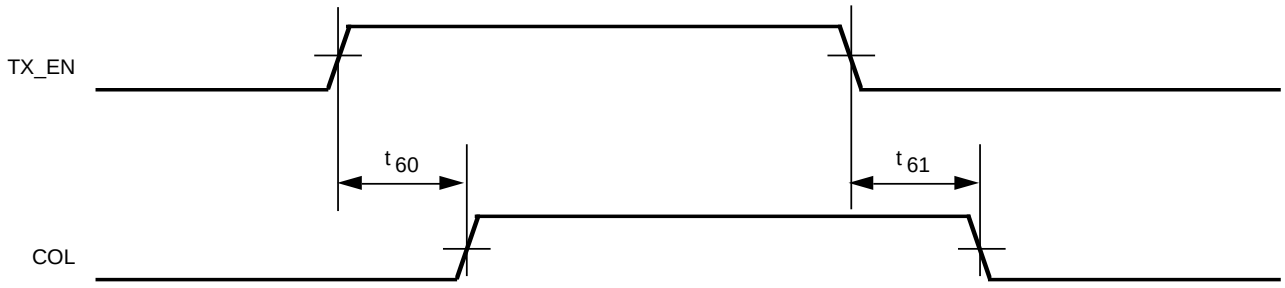


Figure 18. Collision Test Timing

LED Driver Timing Characteristics

Refer To Figure 19 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{66}	$\overline{\text{PLED}}$[1:0] XMT_LED, RCV_LED, On Time	45		55	mS	
t_{67}	$\overline{\text{PLED}}$[1:0] XMT_LED, RCV_LED, Off Time	45		55	mS	

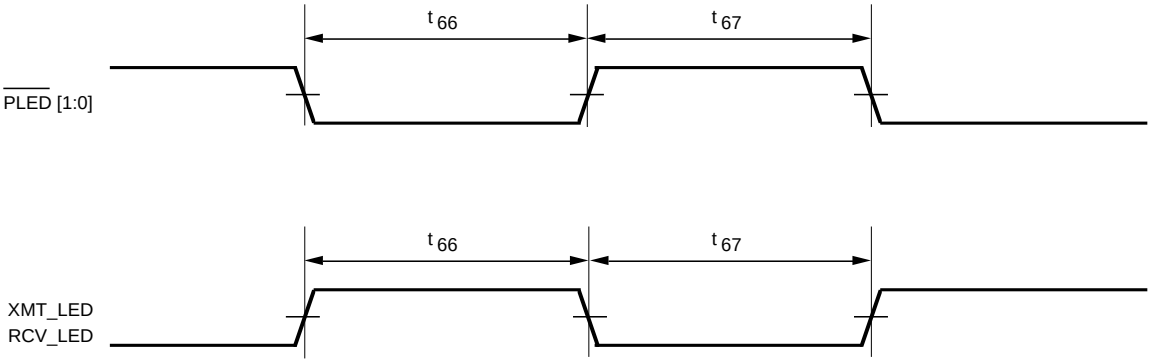


Figure 19. LED Driver Timing

MI Serial Port Timing Characteristics

Refer To Figure 20 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{71}	MDC High Time	20			nS	
t_{72}	MDC Low Time	20			nS	
t_{73}	MDIO Setup Time	10			nS	Write Bits
t_{74}	MDIO Hold Time	10			nS	Write Bits
t_{75}	MDC To MDIO Delay			20	nS	Read Bits
t_{76}	MDIO Hi-Z To Active Delay			20	nS	Write-Read Bit Transition
t_{77}	MDIO Active To HI-Z Delay			20	nS	Read-Write Bit Transition
t_{78}	Frame Delimiter (Idle)	32			Clocks	MDC Clocks With MDIO=1's

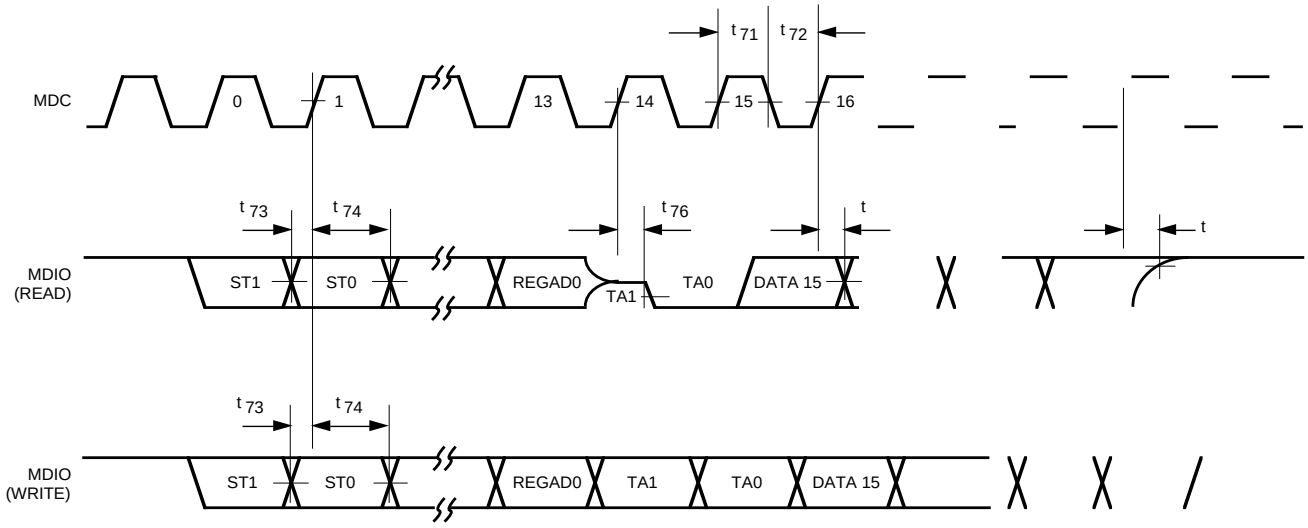


Figure 20. MI Serial Port Timing

EEI Timing Characteristics

Refer To Figure 21 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{81}	EE_CS Setup Time	1800			nS	
t_{82}	EE_CS Hold Time	50			nS	
t_{83}	EE_CLK High Time	3800	4000	4200	nS	
t_{84}	EE_CLK Low Time	3800	4000	4200	nS	
t_{85}	EE_CLK To EE_DO Delay			500	nS	Read Bits
t_{86}	EE_DI Setup Time	500			nS	Write Bits
t_{87}	EE_DI Hold Time	0			nS	Write Bits
t_{88}	EE_DO Hi-Z To Active Delay			500	nS	Write-Read Bit Transition
t_{89}	EE_DO Active To HI-Z Delay			500	nS	Read-Write Bit Transition
t_{90}	EE_CS Deassert Time	7600	8000	8400	nS	

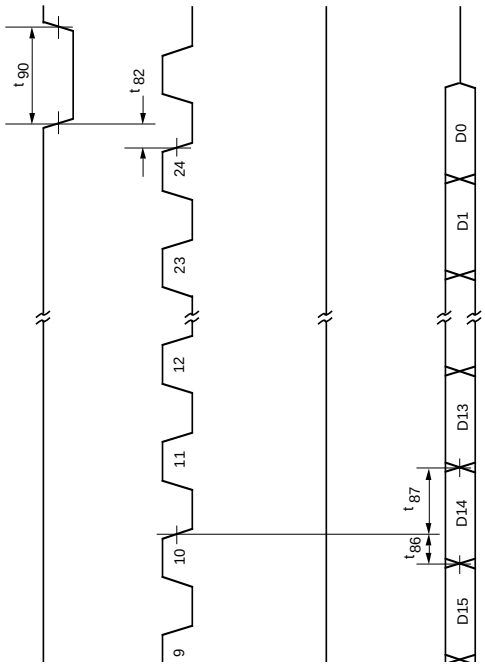
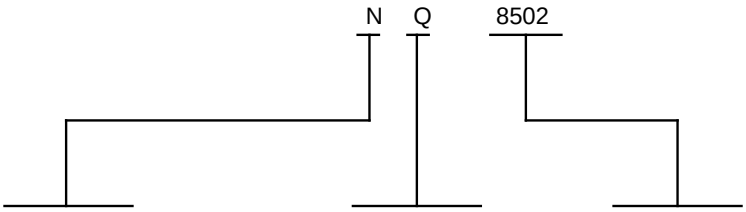


Figure 21. EEI Timing

Ordering Information



Revision History

9/23/96

Page 11, First Paragraph:
- Reference to 75-200 nS has been changed to 77-200 nS.
- Reference to 50 nS has been changed to 48 nS.
- Reference to 15 nS has been changed to 10 nS.

Page 26, Figure 7: References to 49 1 % resistors has changed to 39 1%.

Page 27, Figure 8: References to 49 1 % resistors has changed to 39 1%.
- Figure 8 Resistors 500 and LEDs have been flipped.

Page 29, Figure 10: References to 49 1 % resistors has changed to 39 1%.

Page 32, First column, last paragraph copy has been added, end of paragraph now reads:
- ...tied to GND or tied to GND through an optional 10K resistor as shown in Figure 12c. The optional 10K resistor allows the pin to be used as a digital output under normal conditions.

Page 34, Figure 12b. Resistors 500 and LEDs have been flipped.
- Figure 12c. Setting Address Without LEDs:
- 10K Resistor (Optional) has been added.

Page 36, DC Electrical Characteristics:
- VIL (max) 0.8 Conditions now reads, All except OSCIN, $\overline{\text{MDA}}$[1:0], $\overline{\text{LINKI}}$.
- VIL (max) 0.5, row has been added.
- VIM (max) has changed from 3.0 to VCC–1.5.
- VIH (min) 3.5 Conditions is now OSCIN.
- VIH (min) VCC–0.5, row has been added.
- VIH (min) VCC–0.5, row has been added.
- IIL (min) –12 Conditions is now VIN = GND, EE_DI.
- IIL (min) –5, row has been added.
- IIH Conditions has been changed from VIN = V_{CC} C to VIN = V_{CC}.
- VOH (min) 4 Conditions, has been changed from IOL = 4mA to IOH = 4mA.
- VOH (min) 2.4 Conditions, has changed from IOL = 12µA to IOH = 5µA.
- I_{CC} (max) has been changed from 85 to 70.
- I_{CC} (max) has been changed from 0.1 to 1.0.
- I_{CC} (max) 35 row has been deleted.

Revision History

Page 37, AUI Characteristics, Transmit:
- TOV (max) is now 1200.
- TOV (unit) is now mV pk.
- TCMD (min) $V_{CC}/3–0.5$ has been deleted.
- TCMD (typ) has changed $V_{CC}/3$ to $V_{CC}/4 \pm 0.5$.
- TCMD (max) $V_{CC}/3 + 0.5$ has been deleted.
- TCMD Conditions now reads; Voltage on Either DO+ or DO– Relative to GND.
- TCMA has been deleted.
- TOR has been deleted.
- TOC has been deleted.

Page 38, AUI Characteristics, Receive:
- ROCV Parameter now reads; DI±, CI± Input Open Circuit Voltage.
- ROCV (min) has been deleted.
- ROCV (typ) has changed from $V_{CC}/2$ to $V_{CC}2 \pm 0.5$.
- ROCV (max) has been deleted.
- ROCV Conditions is now; Voltage on Either DI+/CI+ or DI–/CI_ Relative to GND.
- RCMR (min) has been deleted.
- RCMR (typ) is now; $V_{CC}/2 \pm 1.0$.
- RCMR (max) has been deleted.
- RDR Conditions is now; Voltage on Either DI+/CI+ or DI–/CI– Relative to GND.

Page 39, 20 MHz Clock Timing Characteristics
- t_2 Conditions is now; OSCIN Driven by External Clock.
- t_3 Conditions is now; OSCIN Driven by External Clock.

Page 40, Transmit Timing Characteristics:
- t_{15} (min) has changed from 25 to 40.
- t_{19} (min) has changed from 25 to 40.
- t_{25} (min) has changed from 250 to 225.
- t_{27} (max) has changed from 105 to 55.
- t_{28} (min) has changed from 95 to 45.
- t_{28} (max) has changed from 105 to 55.

Page 43, Figure 15: RXD[3:0] has changed; additional DATA reference.

Page 44, Collision Timing Characteristics:
- t_{52} (max) has changed from 450 to 400.
- t_{53} Parameter now reads; CI± Start to CRS Assert Time.
- t_{53} (max) has changed from 400 to 200.
- t_{54} Parameter now reads; Minimum CI± Pulse Width Required for Collision Detection.
- t_{54} (min) has changed from 17.6 to 10.
- t_{55} (min) has changed from 50 to 48.
- t_{55} (max) has changed from 75 to 77.
- t_{58} (max) has changed from 105 to 55.
- t_{59} (min) has changed from 95 to 45.
- t_{59} (max) has changed from 105 to 55.
- t_{60} (max) has changed from 5.12 to 100.
- t_{60} (unit) has changed from µS to nS.

Page 45, Figure 17; CRS has changed.

Page 46, LED Driver Timing Characteristics:
- t_{66} (min) has changed from 95 to 45.
- t_{66} (max) has changed from 105 to 55.
- t_{67} (min) has changed from 95 to 45.
- t_{67} (max) has changed from 105 to 55.

Revision History

Page 48, EEI Timing Characteristics:
- t_{86} (min) is now 500.
- t_{86} (max) has been deleted.
- t_{87} (min) is now 0.
- t_{87} (max) has been deleted.

6/23/97

Document Revision Changed to MD400157/B

Page 1, Features:
- LED Outputs, Activity; has been changed to Activity, Transmit, Receive.
- NOTES 1. 8502 only, has been added. Refers to features, LED Outputs, and Interface to External E^2 PROM for Automatic Preloading of MI Serial Port Bits.
- Pin Configuration 8502 44 PLCC; Pin #11 EE_CLK has been changed to EE_CLK/XMT_LED, and Pin #12 EE_DO has been changed to EE_DO/RCV_LED.

Page 4, Pin Description continued:
- Pin #11, Pin Name; EE_CLK has been changed to EE_CLK/XMT_LED
- Pin #11, Description, copy change; External EEPROM Clock Output has been changed to External EEPROM Clock Output Transmit LED.
- Pin #11, Description, copy; During normal operation, this pin can be used as Transmit LED and can drive an LED to GND.

  0 = No Detect
  1 = Transmit Activity Detected, On for 50 mS.

  copy has been added.

- Pin #12, Pin Name; EE_DO has been changed to EE_DO/RCV_LED
- Pin #12, Description, copy change; External EEPROM Clock Output has been changed to External EEPROM Clock Output Receive LED.
- Pin #12, Description, copy; During normal operation, this pin can be used as Receive LED and can drive an LED to GND.

  0 = No Detect
  1 = Receive Activity Detected, On for 50 mS.

  copy has been added.

Page 5, 1.0 Pin Description continued:
- Pin #5 Description; reference to 100 mS has been changed to 50 mS.
- Pin #4 Description; reference to 100 mS has been changed to 50 mS.

Page 6, Figure 1. 8501, 8502 Block Diagram:
- References to EE_CLK has been changed to EE_CLK/XMT_LED and EE_DO has been changed to EE_DO/RCV _LED.

Page 10, Section 3.6.2 Transmit Activity Indication:
- First paragraph, reference to 100 mS has been changed to 50mS.
- New second paragraph copy; XMT_LED is transmit activity output during normal operation. This pin is asserted high for 50 mS every time a transmit packet occurs. The XMT_LED output can drive an LED to GND or can drive another digital input.
- Paragraph three copy has been changed from ... The $\overline{\text{PLED0}}$ pin is only available on the 8502 (44L) ... to... The $\overline{\text{PLED0}}$ and XMT_LED pins are only available on the 8502 (44L).
- Section 3.7.1 Receiver; Paragraphs 2, and 3 references to VCC/2 have been changed to, about 3.

Revision History

Page 10, Section 3.7.3 Receive Activity Indication; reference to 100 mS has been changed to 50 mS.
- New paragraph two copy; RCV_LED is receive activity output during normal operation. This pin is asserted high for 50 mS every time a receive packet occurs. The RCV_LED output can drive an LED to GND or can drive another digital input.
- Paragraph three copy has been changed from ...The $\overline{\text{PLED0}}$ pin is only available on the 8502 (44L)... to ...The $\overline{\text{PLED0}}$ and RCV_LED pins are only available on the 8502 (44L).

Page 11, Section 3.8.3 Collision Indication
- Reference to 100 mS has been changed to 50 mS.

Page 12, - Section 3.15 POWERDOWN; Reference to 0.5 mW has been changed to 10 mW.
- Section 3.17 LED DRIVERS; Paragraph 3, reference to 100 mS have been changed to 50 mS.
- New paragraph; XMT_LED and RCV_LED outputs can drive LEDs... has been added.

Page 13, Section 3.18.1 Signal Description second paragraph; copy has change from ...PLED[1:0] output drivers are high impedance for an interval called the poweron reset time. During the poweron reset interval... to ...PLED[1:0] output drivers are high impedance for an interval towards the end of the poweron reset time. During this interval,

Page 14, Section 3.18.5 Frame Structure, copy change, first paragraph; copy has been change from...The last 16/80 bits are from one/all of the five data registers... to ...The last 16(80) bits are to or from one(all) of the five data registers.
- Second paragraph, copy has been change from ...accessed data register bits will be read or write. The next 3 bits are upper device ... to ... accessed data register bits will be read from or written to. The next 3 bits are upper device...
- Second paragraph, copy has been change from ... The next 5 bits are register address select bits which select one of the five data registers for access ... to ... The next 5 bits are register address select bits which select one or all of the five data registers for access....
- Second paragraph, copy has been change from ... cycle (or 80 bits if multiple register access is enabled and REGAD=11111) come from the data register ... to ... cycle (or 80 bits if multiple register access is enabled and REGAD=11111) are to or from the data register ...
- Table 2. MI Register Bit Type Definition, R/WS C Definition; Clears Itself After Operation Completed, has been moved from Write Cycle to Read Cycle.

Page 15, Figure 5. MI Serial Port Frame Timing Diagram
- References to ST, OP, PHYAD, REGAD, TA, DATA have been changed to ST[1:0], OP[1:0], PHYAD[4:0], REGAD[4:0], TA[1:0], DATA[15:0]

Page 27, Figure 8. External MII -AUI Schematics Using 8502 with EEPROM and LED's
- References to EE/DO and EE_CLK have been changed to EE_DO/RCV_LED and EE_CLK/XMT_LED.
- 1K Resisters and LEDs have been added to EE_DO/RCV_LED and EE_CLK/XMT_LED.

Page 36, DC Electrical Characteristics
- IIL Conditions $\overline{\text{MDA}}$[1:0] has been changed to VIN = GND $\overline{\text{MDA}}$[1:0].
- IIL Conditions $\overline{\text{OSCIN}}$ LINKI has beeen changed to VIN = GND $\overline{\text{OSCIN}}$ LINKI.
- VOH Limit (Min) has been changed from 4 to VCC - 1.0.
- VOH Conditions, XMT_LED, RCV_LED have been added.
- New VOH Row, Limit (MIN) = VCC -1.0, Limit (UNIT) = Volt, Conditions IOH = 10µA XMT_LED, RCV_LED has been added.
- ICC Transmitting Limit (Typ) is now 85.
- ICC Transmitting Limit (Max) has been changed from 85 to 110.
- ICC Powerdown Mode Limit (Typ) is now 1.3.
- ICC Powerdown Mode Limit (Max) is now 3.06.

Page 38, AUI Characteristics Receive
- ROCV Limit (TYP) has changed from $V_{CC}/2 \pm 0.5$ to 3.0 ± 0.5.
- RCMR Limit (TYP) has changed from $V_{CC}/2 \pm 1.0$ to ROVC $\pm$ 0.5

Page 39, Figure 13. 20 MHz Clock Timing
- TX_CLK Timing has been changed.

20 MHz Clock Timing Characteristics
- t_4 Limit (Max) has been changed from 10 to 20.

Revision History

Page 45, Figure 18. Collision Test Timing
- Timing reference to t_{69} has been changed to t_{61}.

Page 46, LED Driver Timing Characteristics
- t_{66} Parameter, XMT_LED RCV_LED has been added.
- t_{67} Parameter, XMT_LED RCV_LED has been added.

Figure 19. LED Driver Timing
- XMT_LED RCV_LED, Timing has been added to illustration.

Page 47, Figure 20. MI Serial Port Timing
- MDIO(READ) and MDIO(WRITE), timing labels have changed.
- MDIO(WRITE) DATA 0 rising edge, is now rising falling.
- t_{74} reference now extends to MDC timing.

Page 55, 44 Pin PLCC Dimension Diagram has been added.
Page 56, 28 Pin PLCC Dimension Diagram has been added.

7/14/97

Document Revision Changed to MD400157/C

Page 5, Pin 4, Pin Name:
- Corrected error, ($\overline{MDA}$) changed to ($\overline{MDA0}$).

Page 22, Bit 16.5, 16.4, Definition
- Corrected error, reference to $\overline{PLED1}$ has been changed to $\overline{PLED0}$.

7/29/97

Document Revision Changed to MD400157/D

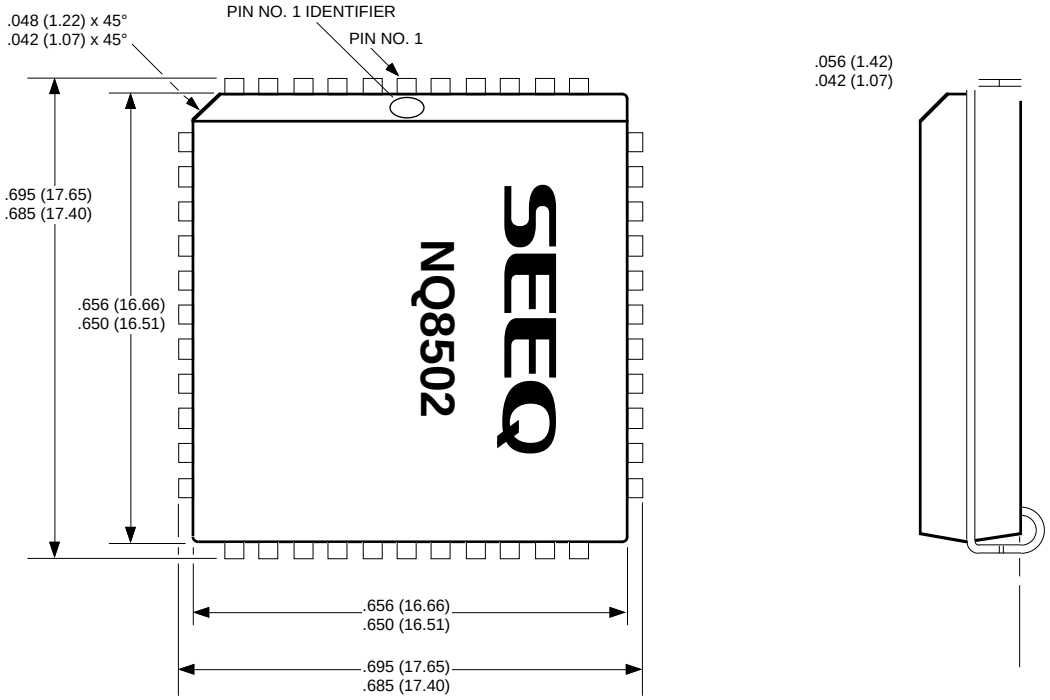
Global change: All references to $V_{CC} = 5 \pm 10\%$, has been changed to $V_{CC} = 5 \pm 5\%$.

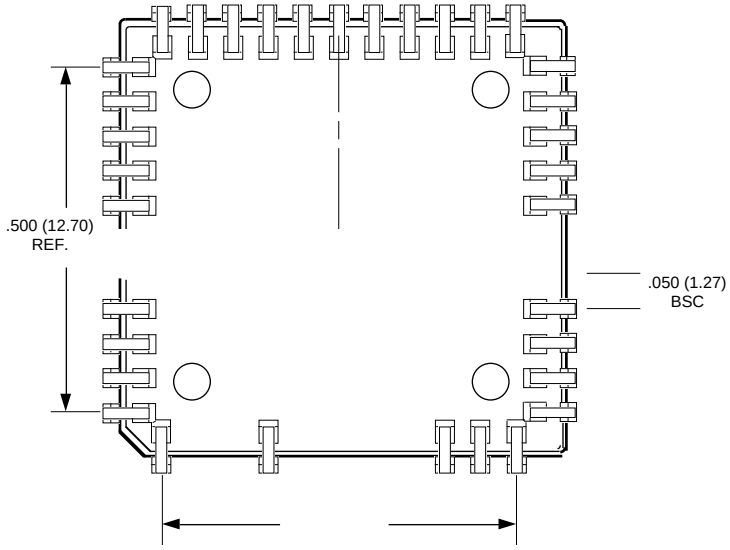
Global change: All references to 8501 have been deleted or changed to 8502.

Page 36, DC Electrical Characteristics, SYM VOH Conditions: Reference to IOH = 5µA has been changed to IOH 4µA.

Surface Mount Packages

44 Pin Plastic Leaded Chip Carrier





Notes

1. **All dimensions are in inches and (millimeters).**
2. **Dimensions do not include mold flash. Maximum allowable flash is .008 (.20).**
3. **Formed leads shall be planar with respect to one another within 0.004 inches.**