High-performance Regulator IC Series for PCs

FET Integrated Switching Regulators for DDR-SDRAM Cores

BD95513MUV

●Description

BD95513MUV is a switching regulator capable of supplying high current output (up to 3A) at low output voltages (0.7V~5.0V) over a broad range of input voltages (4.5V~28V). The regulator features an internal N-MOSFET power transistor for high efficiency and low space consumption, while incorporating ROHM's proprietary H^3Reg^{TM} control mode technology, yielding the industry's fastest transient response time against load changes. SLLM (Simple Light Load Mode) technology is also integrated to improve efficiency when powering lighter loads, as well as soft start, variable frequency, short-circuit protection with timer latch, over-voltage protection, and REF functions. This regulator is suited for PC applications.

●Features

1) Internal low ON-resistance power N-MOSFET
2) Internal 5V linear voltage regulator
3) Integrated H^3Reg^{TM} DC/DC converter controller
4) Selectable Simple Light Load Mode (SLLM), Quiet Light Load Mode (QLLM) and forced continuous mode
5) Built-in thermal shutdown, low input, current overload, output over- and under-voltage protection circuitry
6) Soft start function to minimize rush current during startup
7) Adjustable switching frequency (f = 200 kHz ~ 1000 kHz)
8) Built-in output discharge function
9) VQFN032-V5050 package size
10) Tracking function
11) Internal bootstrap diode

●Applications

Mobile PCs, desktop PCs, LCD-TV, digital household electronics

Sep. 2008

●Absolute Maximum Ratings (T_a = 25 °C)

Parameter	Symbol	Value	Unit
Input Voltage 1	V_{CC}	7 *1	V
Input Voltage 2	V_{DD}	7 *1	V
Input Voltage 3	V_{IN}	30 *1	V
External V_{CC} Voltage	$EXTV_{CC}$	7 *1	V
BOOT Voltage	BOOT	35	V
BOOT-SW Voltage	BOOT-SW	7 *1	V
Output Feedback Voltage	FB	VCC	V
SS/FS/MODE Voltage	SS/FS/MODE	VCC	V
V_{REG} Voltage	VREG	VCC	V
EN/CTL Input Voltage	EN/CTL	7 *1	V
PGOOD Voltage	PGOOD	7 *1	V
Output Current (Average)	I_{SW}	3 *1	A
Power Dissipation 1	P_{d1}	0.38 *2	W
Power Dissipation 2	P_{d2}	0.88 *3 *6	W
Power Dissipation 3	P_{d3}	2.06 *4 *6	W
Power Dissipation 4	P_{d4}	4.56 *5 *6	W
Operating Temperature Range	T_{opr}	-10 ~ +100	°C
Storage Temperature Range	T_{stg}	-55 ~ +150	°C
Junction Temperature	T_{jmax}	+150	°C

*1 Do not exceed Pd.
*2 $T_a \geqq$ 25 °C (IC only), power dissipated at 3.0 mW / °C.
*3 $T_a \geqq$ 25 °C (single-layer board, 20.2 mm^2 copper heat dissipation pad), power dissipated at 7.0 mW / °C.
*4 $T_a \geqq$ 25 °C (4-layer board, 10.29 mm^2 copper heat dissipation pad on top layer, 5505 mm^2 pad on 2nd and 3rd layer), power dissipated at 16.5 mW / °C.
*5 $T_a \geqq$ 25 °C (4-layer board, all layers with 5505 mm^2 copper heat dissipation pads), power dissipated at 36.5 mW / °C.
*6 Values observed with chip backside soldered. When unsoldered, power dissipation is lower.

●Operating Conditions (T_a = 25 °C)

Parameter	Symbol	Min	Max	Unit
Input Voltage 1	V_{CC}	4.5	5.5	V
Input Voltage 2	V_{DD}	4.5	5.5	V
Input Voltage 3	V_{IN}	4.5	28	V
External V_{CC} Voltage	$EXTV_{CC}$	4.5	5.5	V
BOOT Voltage	BOOT	4.5	33	V
SW Voltage	SW	-0.7	28	V
BOOT-SW Voltage	BOOT-SW	4.5	5.5	V
MODE Input Voltage	MODE	0	5.5	V
EN/CTL Input Voltage	EN/CTL	0	5.5	V
PGOOD Voltage	PGOOD	0	5.5	V
Minimum On Time	t_{onmin}	-	100	ns

★This product is not designed for use in a radioactive environment.

●Electrical Characteristics

(Unless otherwise noted, T_a =25°C, AV_{IN} =12V, V_{CC} =V_{DD} =V_{REG}, EN/CTL=5V, MODE=0V, R_{FS} =180kΩ)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
[Whole Device]						
AVIN Bias Current 1	IIN1	-	1200	1800	μA	
AVIN Bias Current 2	IIN2	-	150	250	μA	EXTVCC=5V
AVIN Standby Current	IINstb	-	0	10	μA	CTL=EN=0V
EN Low Voltage	ENlow	GND	-	0.8	V	
EN High Voltage	ENhigh	2.3	-	5.5	V	
EN Bias Voltage	IEN	-	12	20	μA	
CTL Low Voltage	CTLlow	GND	-	0.8	V	
CTL High Voltage	CTLhigh	2.3	-	5.5	V	
CTL Bias Current	ICTL	-	1	6	μA	
[5V Regulator]						
VREG Input Voltage	VREG	4.90	5.00	5.10	V	VIN=6.0 to 25V IREG=0 to 100mA
Maximum Current	IREG	100	-	-	mA	
[5V Switch]						
EXTVCC Input Threshold Voltage	EVCC_UVLO	4.2	4.4	4.6	V	EXTVCC:Sweep up
Switch Resistance	REVCC	-	1.0	2.0	Ω	
[Under-Voltage Lockout Protection]						
AVIN Threshold Voltage	AVIN_UVLO	4.1	4.3	4.5	V	VCC:Sweep up
AVIN Hysteresis Voltage	dAVIN_UVLO	100	160	220	mV	VCC:Sweep down
VREG Threshold Voltage	VREG_UVLO	4.1	4.3	4.5	V	VREG:Sweep up
VREG Hysteresis Voltage	dVREG_UVLO	100	160	220	mV	VREG:Sweep down
[H^3REG^{TM} Control Block]						
ON Time	ton	400	500	600	nsec	
MAX ON Time	tonmax	10.0	22.0	40.0	μsec	
MIN OFF Time	toffmin	-	450	550	nsec	
[FET Block]						
High-side ON Resistance	Ron_high	-	120	200	mΩ	
Low-side ON Resistance	Ron_low	-	120	200	mΩ	
[SCP Block]						
SCP Startup Voltage	VSCP	0.420	0.490	0.560	V	When VFB: 30% down
Delay	tSCP	-	1	-	ms	
[Over-Voltage Protection Block]						
OVP Detect Voltage	VOVP	0.812	0.840	0.868	V	When VFB: 20% up
[Soft Start Block]						
Charge Current	Iss	1.4	2.2	3.0	μA	
Standby Voltage	Vss_stb	-	-	100	mV	
[Current Regulation Block]						
Maximum Output Current	IOCP	3	-	-	A	
[Voltage Detection Block]						
Feedback Terminal Voltage 1	VFB1	0.693	0.700	0.707	V	
Feedback Terminal Voltage 2	VFB2	0.690	0.700	0.710	V	T_a =-10°C to 100°C I_{out} = 0A to 3A
Feedback Terminal Bias Current	IFB	-100	0	100	nA	
[MODE Block]						
SLLM Condition	VthSLLM	VCC-0.5	-	VCC	V	SLLM Longest low-gate off time: ∞
Forced Continuous Mode	VthCONT	GND	-	0.5	V	Continuous mode
[Power Good Block]						
VFB Power Good Low Voltage	VFB PL	0.605	0.63	0.655	V	When VFB: 10% down
VFB Power Good High Voltage	VFB PH	0.745	0.77	0.795	V	When VFB: 10% up

●Reference Data

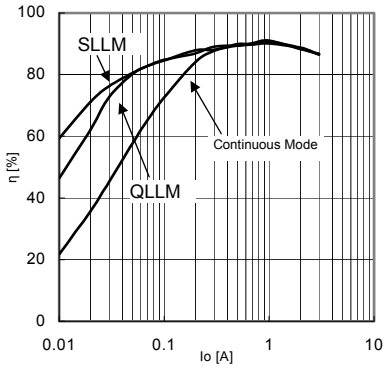


Fig.1 Io-Efficiency
(VIN=7V,VOUT=2.5V)

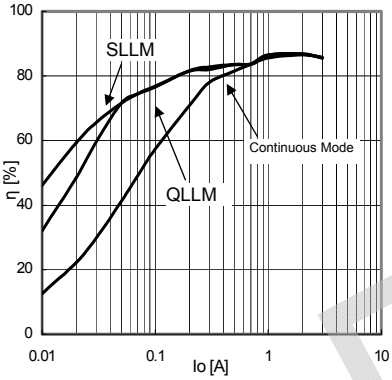


Fig.2 Io-Efficiency
(VIN=12V,VOUT=2.5V)

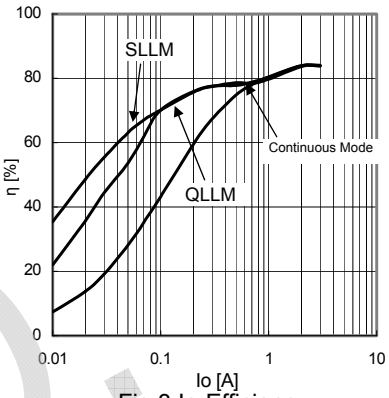


Fig.3 Io-Efficiency
(VIN=19V,VOUT=2.5V)

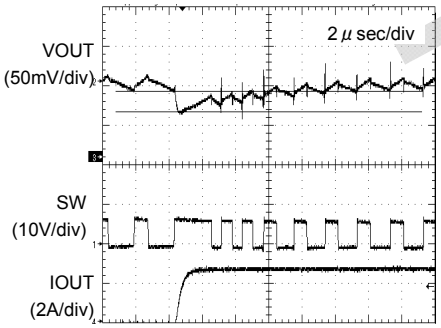


Fig.4 Transient Response
(VIN=7V, VOUT=2.5V)

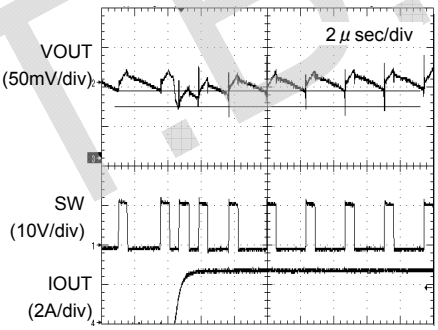


Fig.5 Transient Response
(VIN=12V, VOUT=2.5V)

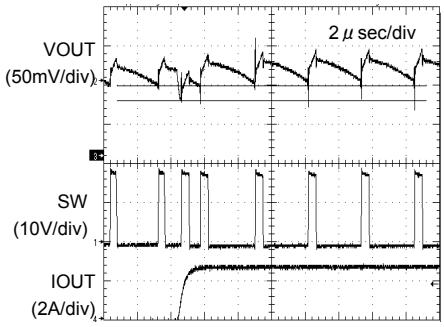


Fig.6 Transient Response
(VIN=19V, VOUT=2.5V)

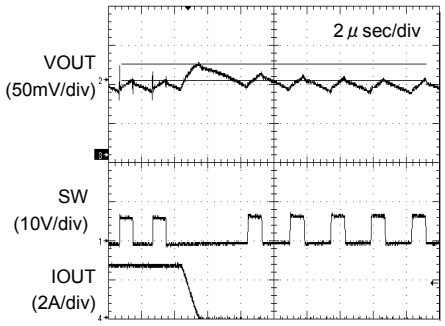


Fig.7 Transient Response
(VIN=7V, VOUT=2.5V)

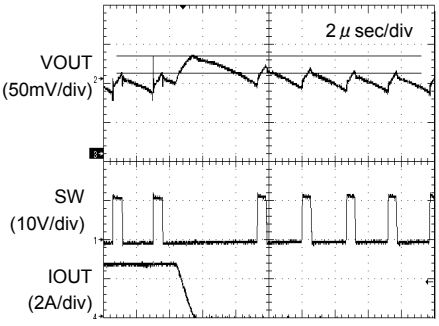


Fig.8 Transient Response
(VIN=12V, VOUT=2.5V)

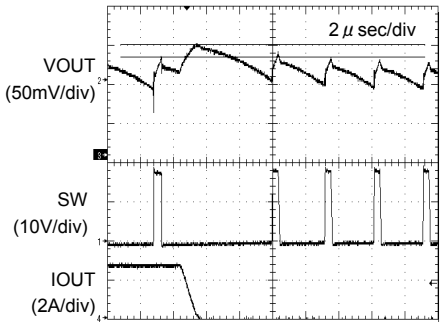


Fig.9 Transient Response
(VIN=19V, VOUT=2.5V)

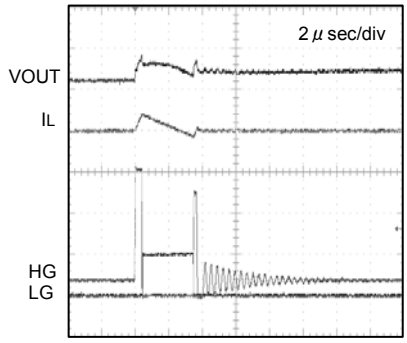


Fig.10 SLLM Mode
(IOUT=0A)

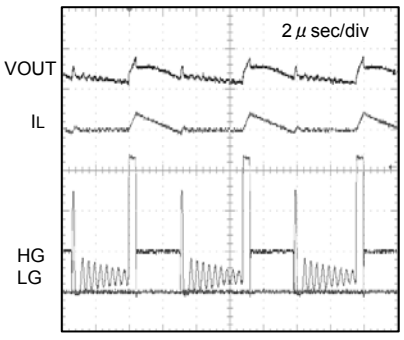


Fig.11 SLLM Mode
(IOUT=0.4A)

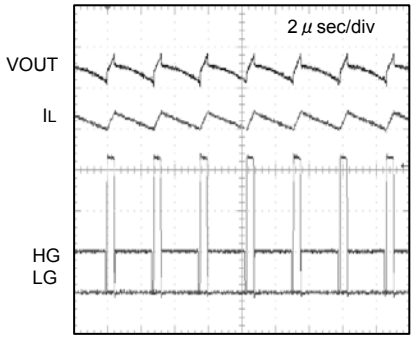


Fig.12 1 SLLM Mode
(IOUT=1A)

●Reference Data

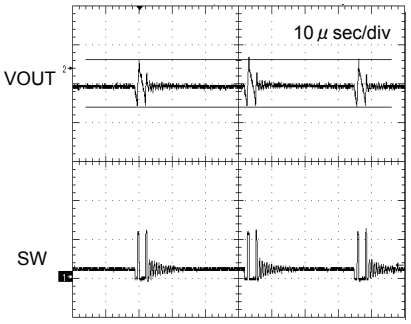


Fig.13 QLLM Mode
(I_{OUT}=0A)

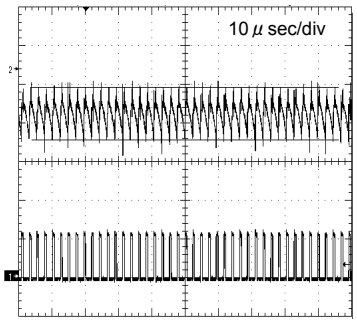


Fig.14 QLLM Mode
(I_{OUT}=1A)

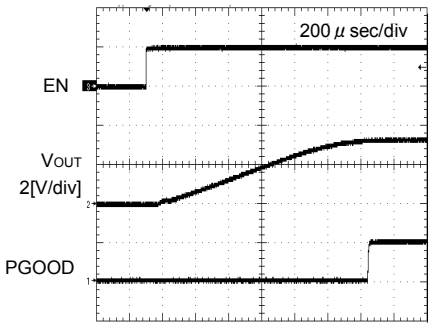


Fig.15 PGOOD Rising Waveform

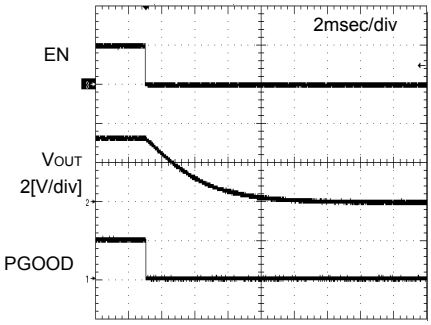


Fig.16 PGOOD Falling Waveform

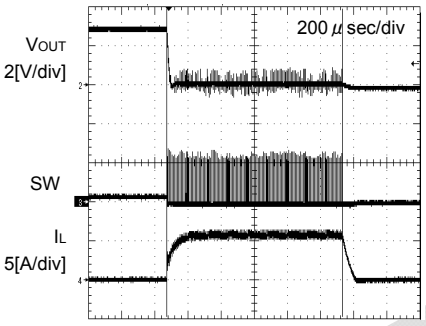


Fig.17 SCP Timer Latch Waveform

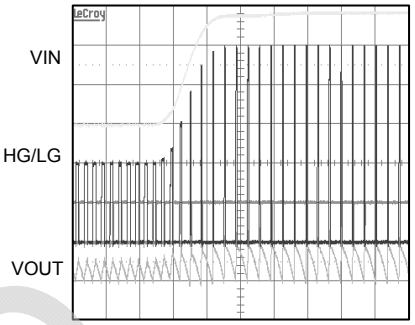


Fig.18 V_{IN} change
(5→19V)

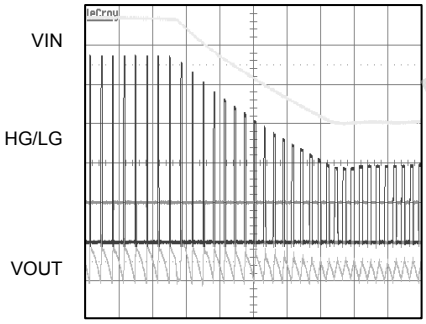


Fig.19 V_{IN} change
(19→5V)

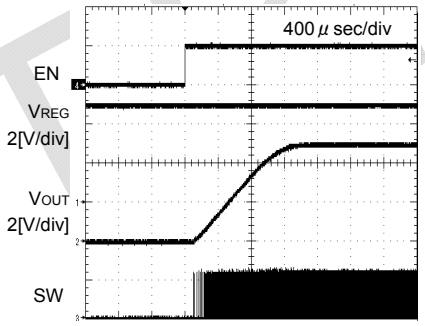
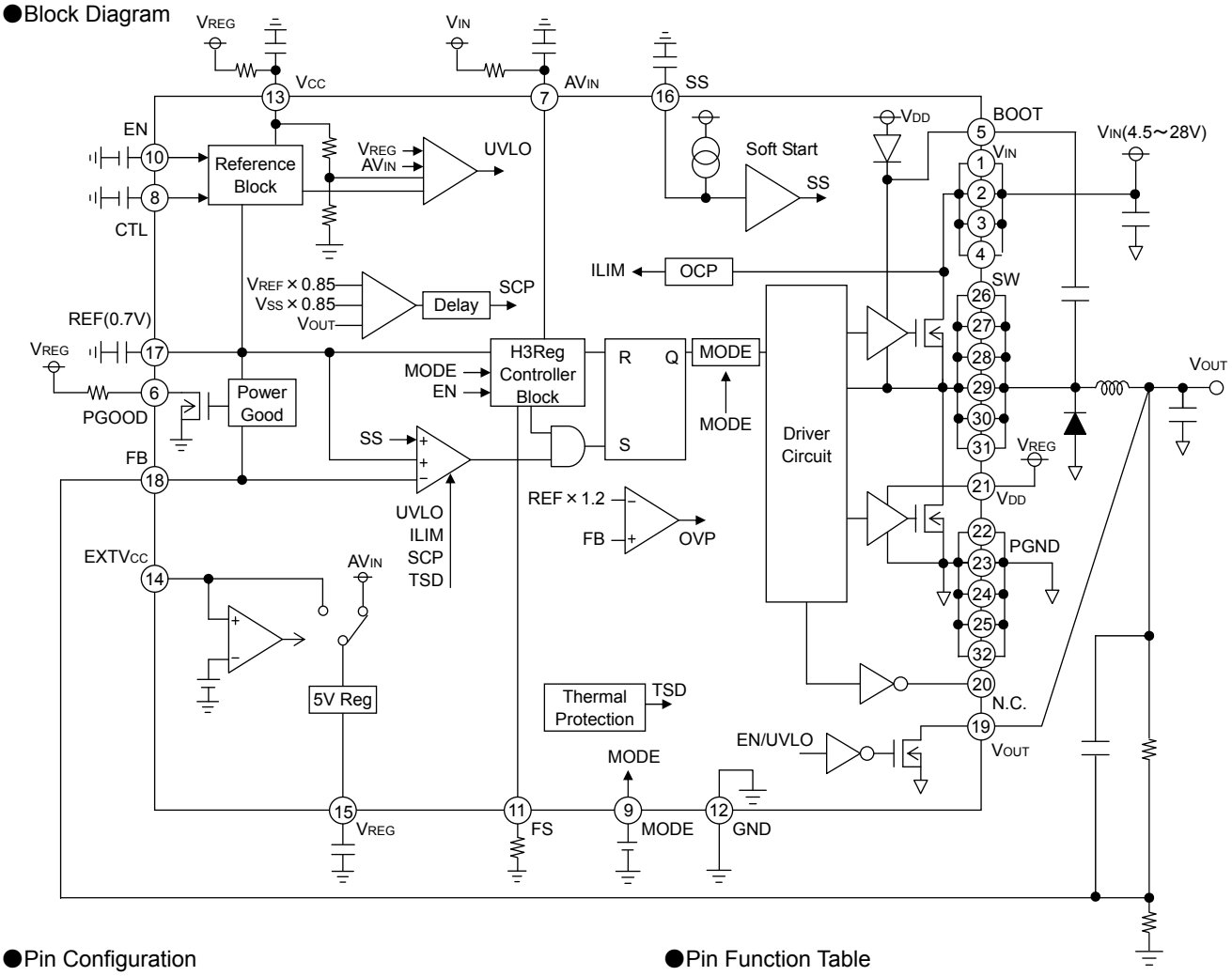
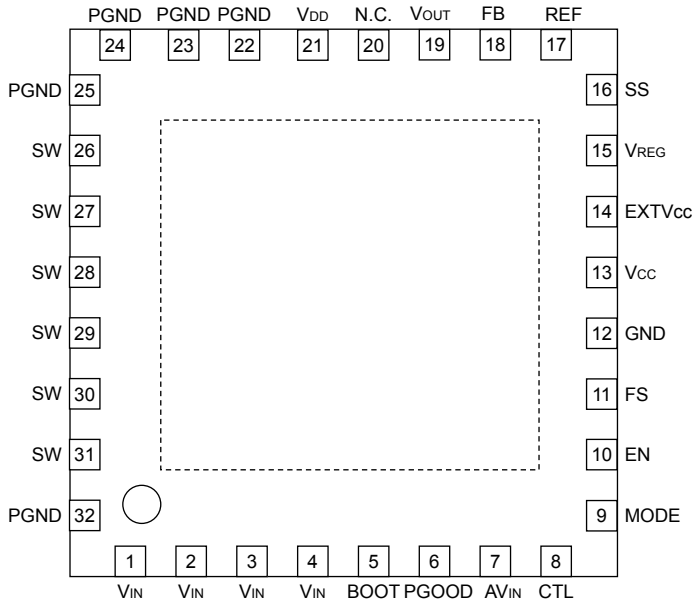


Fig.20 EN wake up

●Block Diagram



●Pin Configuration



*Connect the underside (FIN) to the ground terminal

●Pin Function Table

PIN No.	PIN Name	PIN Function
1-4	VIN	Battery voltage input (4.5 ~ 28 V)
5	BOOT	HG driver power supply
6	PGOOD	Power good output (high when output ±10% of regulation)
7	AVIN	Battery voltage sense
8	CTL	Linear regulator on/off (high = 5.0V, low = off)
9	MODE	Control mode selection GND : Continuous Mode 3.0V : QLLM VCC : SLLM
10	EN	Enable output (high when VOUT ON)
11	FS	Switching frequency adjustment (RFS = 30 k ~ 100 kΩ)
12	GND	Sense ground
13	VCC	Power supply input
14	EXTVCC	External power supply input
15	VREG	IC reference voltage (5.0V / 200mA)
16	SS	Soft start condenser input
17	REF	Output reference voltage (0.7 V)
18	FB	Feedback input (0.7 V)
19	VOUT	Voltage discharge output
20	N.C.	-
21	VDD	Power supply input (5 V)
22-25	PGND	Power ground
26-31	SW	Output to inductor
32	PGND	Power ground
Underside	FIN	Substrate connection

●Pin Descriptions

・V_{CC}

This pin supplies power to the IC's internal circuitry, excluding the FET driver. The input supply voltage range is 4.5 to 5.5 V, with a maximum current draw of 900 µA. This pin should be bypassed with a capacitance of approximately 0.1 µF.

・EN

Enables or disables the switching regulator. When the voltage on this pin reaches 2.3 V or higher, the internal switching regulator is turned on. At voltages less than 0.8 V, the regulator is turned off.

・V_{DD}

This pin supplies power to the low side of the FET driver, as well as to the bootstrap diode. As the diode draws its peak current when switching on or off, this pin should be bypassed with a capacitance of approximately 1 µF.

・V_{REG}

Output pin from the 5 V linear regulator. This pin also supplies power to the internal driver and control circuitry. V_{REG} standby function is controlled by the CTL pin. The output supplies 5V at 100 mA and should be bypassed to ground using a 10 µF capacitor with a rating of X5R or X7R.

・$EXTV_{CC}$

External power supply input for the linear regulator. When the voltage on the $EXTV_{CC}$ pin exceeds 4.4 V, the regulator uses it in conjunction with other power sources to supply V_{REG}. Leave the $EXTV_{CC}$ pin floating when not in use.

・REF

Reference voltage output pin. The reference voltage is set internally by the IC to 0.7 V, and the IC works to keep V_{REF} approximately equal to V_{FB}. Variations in voltage levels on this pin affect the output voltage, so the pin should be bypassed with a 100 pF ~ 0.1 µF ceramic capacitor.

・SS

Soft start/stop pin. When EN is set high, the capacitor between the internal current source and SS-GND controls the startup time of the IC. When the voltage on the SS pin is lower than the REF output voltage (0.7 V), the output voltage is held at the same voltage as the SS pin.

・AV_{IN}

The BD95513MUV controls the duty cycle and output voltage based upon the input voltage at this pin, so voltage variations or oscillations on this line can cause operation to become unstable. This pin also acts as the voltage input for the switching block, so insufficient coupling impedance can also cause operation to become unstable. Therefore, this line should be bypassed with either a power capacitor or RC filter.

・FS

Frequency-adjusting resistance input pin. Attaching a resistance of 30 k ~ 100 kΩ adjusts the switching frequency from 200 kHz ~ 1 MHz.

・BOOT

This pin serves as the power source for the high side of the FET driver. A bootstrap diode is integrated within the IC. The maximum voltage on this pin should not exceed +30 V vs. GND or +7 V vs. SW. When operating the switching regulator, the operation of the bootstrap circuitry causes the BOOT voltage to swing from (V_{IN} + V_{DD}) ~ V_{DD}.

・PGOOD

Power good indicator. This open-drain output should be connected via a 100 kΩ pull-up resistor.

・MODE

Mode selection pin. When low, the IC functions in forced-continuous mode; at voltages from 0V ~ 3V, QLLM mode; when high, SLLM mode.

・CTL

Linear regulator control pin. When voltage is 2.3 V or higher, a logic HIGH is recognized and the internal regulator (V_{REG} = 5 V) is switched on. At voltages of 0.8 V or lower, a logic LOW is recognized and the regulator is switched off. However, even if EN is logic HIGH, the switching regulator will not operate if CTL is logic LOW.

・FB

Output voltage feedback input. V_{FB} is held at 0.7 V by the IC.

・SW

Output from the switching regulator to the inductor. This output swings from V_{IN} ~ GND. The trace from the output to the inductor should be as short and wide as possible.

・V_{OUT}

Voltage output discharge pin. When EN is off, this output is pulled low.

・V_{IN}

Power supply input. The IC can accept any input from 4.5 V to 28 V. This pin should be bypassed directly to ground by a power capacitor.

・PGND

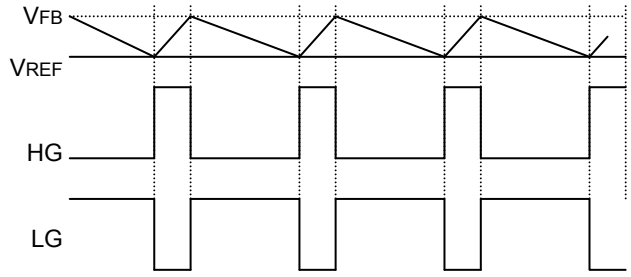
Power ground terminal.

●Operation

The BD95513MUV is a switching regulator incorporating ROHM's proprietary H^3Reg CONTROLLA control system. When V_{OUT} drops suddenly due to changes in load, the system quickly restores the output voltage by extending the t_{on} time interval. This improves the regulator's transient response. When light-load mode is activated, the IC employs the Simple Light Load Mode (SLLM) controller, further improving system efficiency.

H^3Reg^{TM} Control

(Normal Operation)

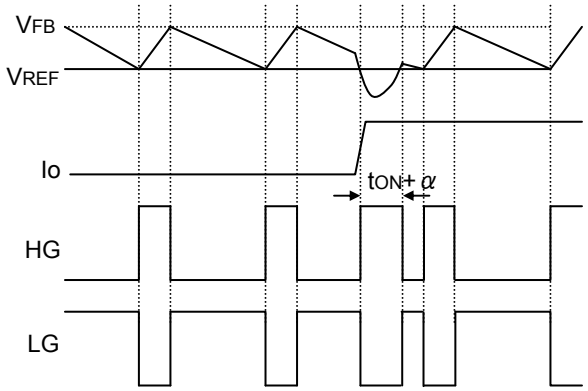


When V_{FB} falls below the reference voltage (0.7 V), the H^3Reg CONTROLLA is activated;

$$t_{ON} \quad \frac{V_{REF}}{V_{IN}} \times \frac{1}{f} \text{ [sec]} \cdot \cdot \cdot (1)$$

High gate output is determined by the above formula.

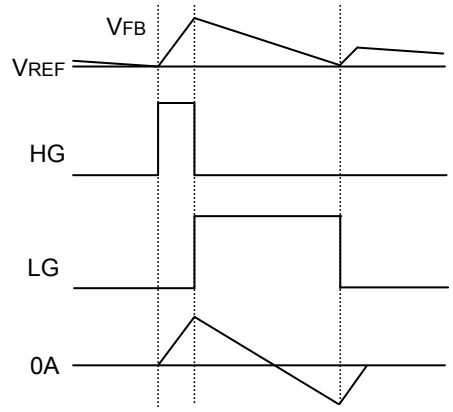
(Rapid Changes in Load)



When V_{OUT} drops due to a sudden change in load and the voltage remains below V_{REF} after the preprogrammed t_{ON} time interval has elapsed, the system quickly restores V_{OUT} by extending the t_{ON} time, thereby improving transient response.

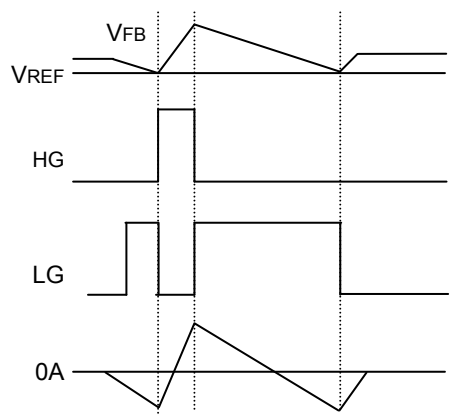
Light Load Control

(SLLM Mode)



SLLM mode is enabled by setting the MODE pin to logic high. When the low gate is off and the current through the inductor is 0 (current flowing from V_{OUT} to SW), the SLLM function is activated, disabling high gate output.
If V_{FB} falls below V_{REF} again, the high gate is switched back on, lowering the switching frequency of the regulator and yielding higher efficiency when powering light loads.

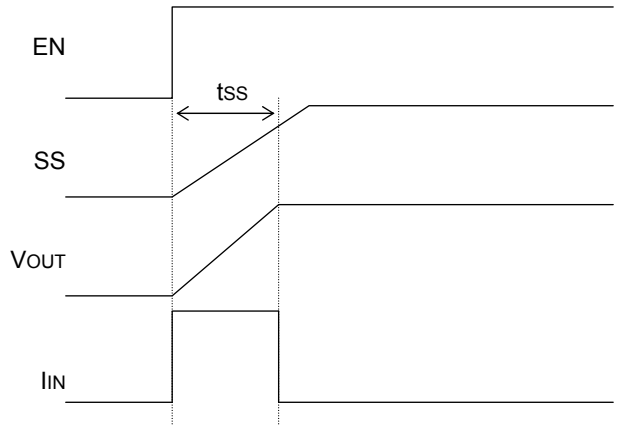
(QLLM Mode)



QLLM mode is enabled by setting the MODE pin to HiZ or middle voltage. When the lower gate is off and the current through the inductor is 0 (current flowing from VOUT to SW), QLLM mode is activated, disabling high gate output.
If VFB falls below VREF within a programmed time interval (typ. 40 µs), the high gate is switched on, but if VFB does not fall below VREF, the lower gate is forced on, dropping VFB and switching the high gate back on.
The minimum switching frequency is set to 25 kHz (T = 40 µS), which keeps the regulator's frequency from entering the audible spectrum but yields less efficient results than SLLM mode.

●Timing Chart

・Soft Start Function



The soft start function is enabled when the EN pin is set high. Current control circuitry takes effect at startup, yielding a moderate “ramping start” in output voltage. Soft start timing and incoming current are given by equation (2) and (3) below:

Soft start period:

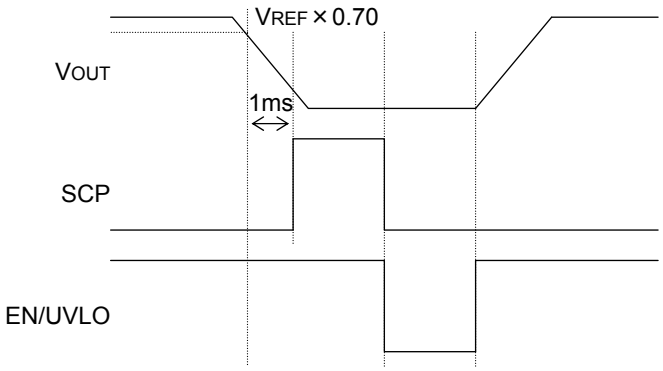
$$t_{SS} = \frac{V_{REF} \times Css}{2\,\mu A(typ)} \text{ [sec]} \quad \cdot\cdot\cdot (2)$$

Rush current:

$$I_{IN}(ON) = \frac{Co \times V_{OUT}}{tss} \text{ [A]} \quad \cdot\cdot\cdot (3)$$

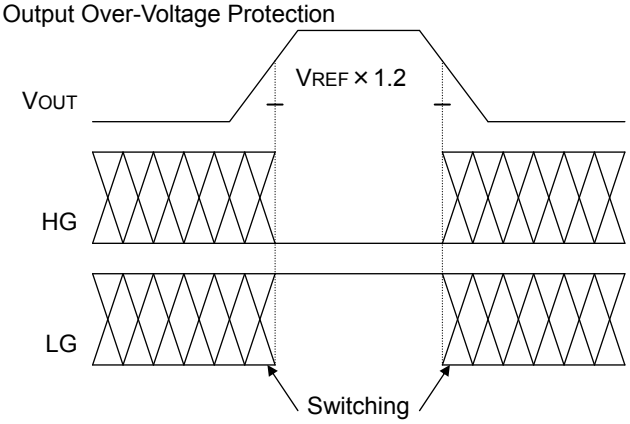
(Css: soft start capacitor; Co: output capacitor)

・Timer Latch-type Short Circuit Protection



When output voltage falls to V_{REF} x 0.70 or less, the output short circuit protection engages, turning the IC off after a set period of time to prevent internal damage. When EN is switched back on or when UVLO is cleared, output continues. The time period before shutting off is set internally at 1 ms.

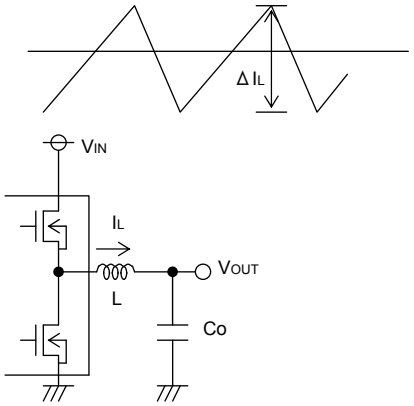
・Output Over-Voltage Protection



When output reaches or exceeds V_{REF} x 1.2, the output over-voltage protection is engaged, turning the low-side FET completely on to reduce the output (low gate on, high gate off). When the output falls, it returns to standard mode.

●External Component Selection

1. Inductor (L) Selection



Output ripple current

The inductor's value directly influences the output ripple current. As formula (4) indicates below, the greater the inductance or switching frequency, the lower the ripple current:

$$\Delta I_L = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{L \times V_{IN} \times f} \text{ [A]} \cdot \cdot \cdot (4)$$

The proper output ripple current setting is about 30% of maximum output current.

$$\Delta I_L = 0.3 \times I_{OUT}\text{max. [A]} \cdot \cdot \cdot (5)$$

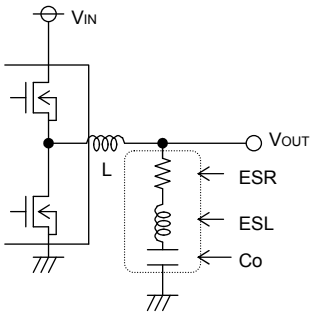
$$L = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{IN} \times f} \text{ [H]} \cdot \cdot \cdot (6)$$

(ΔI_L: output ripple current, f: switching frequency)

※ Passing a current larger than the inductor's rated current will cause magnetic saturation in the inductor and decrease system efficiency. In selecting the inductor, be sure to allow enough margin to assure that peak current does not exceed the inductor's rated current value.

※ To minimize possible inductor damage and maximize efficiency, choose an inductor with a low DCR and ACR resistance.

2. Output Capacitor Selection (C_O)



Output Capacitor

When determining the proper output capacitor, be sure to factor in the equivalent series resistance (ESR) and equivalent series inductance (ESL) required to set the output ripple voltage at 20 mV or more.

When selecting the limit of the inductor, be sure to allow enough margin for the output voltage. Output ripple voltage is determined by formula (7) below:

$$\Delta V_{OUT} = \Delta I_L \times ESR + ESL \times \Delta I_L / T_{ON} \cdot \cdot \cdot (7)$$

(ΔI_L: Ouput ripple current, ESR: equivalent series resistance, ESL: equivalent series inductance)

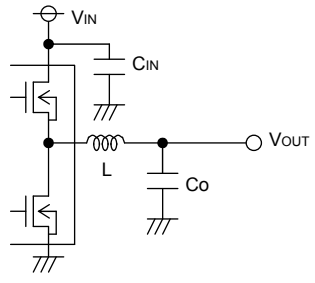
Give special consideration to the conditions of formula (7) for output capacitance. Also, keep in mind that the output rise time must be established within the soft start timeframe.

$$Co \leqq \frac{tss \times (I_{limit}-I_{OUT})}{V_{OUT}} \cdot \cdot \cdot (8)$$

tss: Soft start timeframe (see p. 10, equation (2))
I_{limit}: Maximum output current

Choosing a capacitance that is too large can cause startup malfunctions, or in some cases, may engage the short circuit protection.

3. Input Capacitor Selection (C_{IN})



Input Capacitor

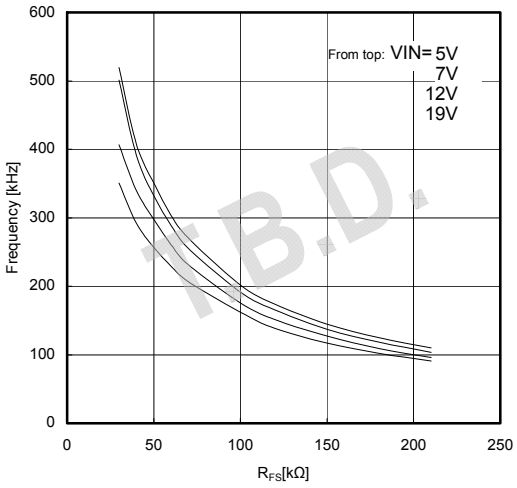
In order to prevent extreme over-current conditions, the input capacitor must have a low enough ESR to fully support a large ripple in the output. The formula for RMS ripple current (I_{RMS}) is given by equation (9) below:

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{IN}(V_{IN}-V_{OUT})}}{V_{IN}} \text{ [A]} \cdot \cdot \cdot (9)$$

When $V_{IN} = 2 \times V_{OUT}$, $I_{RMS} = \frac{I_{OUT}}{2}$

A low-ESR capacitor is recommended to reduce ESR loss and maximize efficiency.

4. Frequency Adjustment



The resistance connected to the FS terminal adjusts the on-time (t_{ON}) during normal operation as illustrated to the left. When t_{ON}, input voltage and VREF voltage are known, the switching frequency can be determined by the following formula:

$$F = \frac{V_{REF}}{V_{IN} \times t_{ON}} \quad \cdot\cdot\cdot (10)$$

However, real-life considerations (such as external MOSFET gate capacitance and switching time) must be factored in as they affect the overall switching rise and fall time. This leads to an increase in t_{ON}, lowering the total frequency slightly.

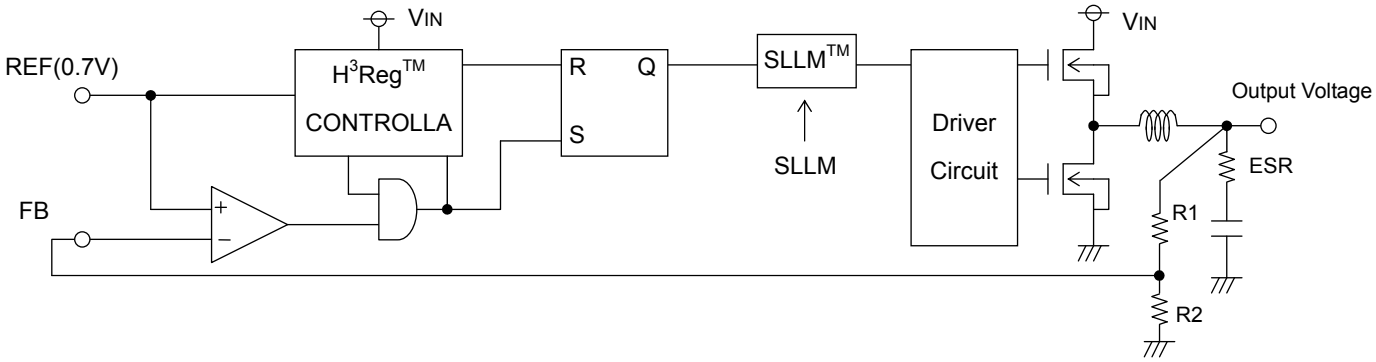
Additionally, when output current lingers around 0A in continuous mode, this “dead time” also has an effect upon t_{ON}, further lowering the switching frequency. Confirm the switching frequency by measuring the current through the coil (at the point where current does not flow backwards) during normal operation.

The BD95513MUV operates by feeding the output voltage back through a resistive voltage divider. The output voltage is set by the following equation (see schematic below):

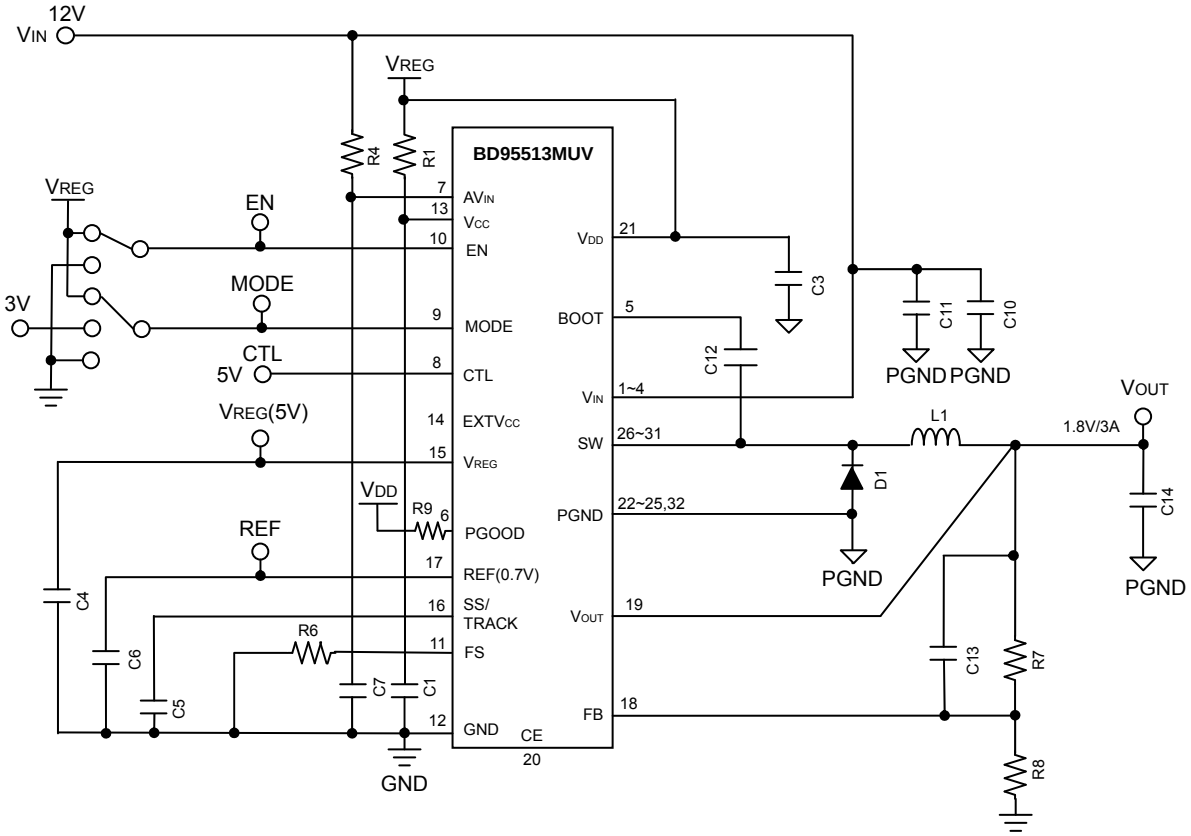
$$\text{Output Voltage} = \frac{R1+R2}{R2} \times V_{REF}\,(0.7V) + \frac{1}{2} \times \Delta I_L \times ESR \quad \cdot\cdot\cdot (11)$$

The switching frequency is also amplified by the same resistive voltage divider network:

$$f_{sw} = \frac{R1+R2}{R2} \times (\text{frequency set by } R_{FS})\ [Hz] \quad \cdot\cdot\cdot (12)$$



●Evaluation Board Circuit (Frequency=300kHz Continuous Mode/QLLM/SLLM Example Circuit)



●Evaluation Board Parts List

Part No	Value	Company	Part name
U1		ROHM	BD95513MUV
D1		ROHM	RB051L-40
C1	1uF	KYOCERA	CM105B105K06A
C3	1uF	KYOCERA	CM105B105K16A
C4	10uF	KYOCERA	CM316B106K06A
C5	1000pF	MURATA	GRM39X7R102K50
C6	0.1uF	KYOCERA	CM105B104K06A
C7	1uF	KYOCERA	CM105B105K16A
C11	10uF	KYOCERA	CM316B106M16A
C12	0.1uF	KYOCERA	CM05B104K25A
C13	220pF	MURATA	GRM39C0G221J50

Part No	Value	Company	Part name
R1	10Ω	ROHM	MCR03
R4	10Ω	ROHM	MCR03
R6	68KΩ	ROHM	MCR03
R7	31kΩ	ROHM	MCR03
R8	20kΩ	ROHM	MCR03
R9	100kΩ	ROHM	MCR03
L1	1.8uH	SUMIDA	CDEP104-1R8ML
C14	470uF	SANYO	2R5TPE470ML
C15	1uF	KYOCERA	CM105B105K06A
C16	1uF	KYOCERA	CM105B105K06A

●Operation Notes

(1) Absolute maximum ratings

Exceeding the absolute maximum ratings (such as supply voltage, temperature range, etc.) may result in damage to the device. In such cases, it may be impossible to identify problems such as open circuits or short circuits. If any operational values are expected to exceed the maximum ratings for the device, consider adding protective circuitry (such as fuses) to eliminate the risk of damaging the IC.

(2) Power supply polarity

Connecting the power supply in reverse polarity can cause damage to the IC. Take precautions when connecting the power supply lines. An external power diode can be added.

(3) Power supply lines

The PCB layout pattern should be designed to provide the IC with low-impedance GND and supply lines. To minimize noise on the supply and GND lines, ground and power supply lines of analog and digital blocks should be separated. For all power lines supplying ICs, connect a bypass capacitor between the power supply and the GND terminal. If using electrolytic capacitors, keep in mind that their capacitance is reduced at lower temperatures.

(4) GND voltage

The potential of the GND pin must be the minimum potential in the system in all operating conditions.

(5) Thermal design

Use thermal design techniques that allow for a sufficient margin for power dissipation in actual operating conditions.

(6) Inter-pin shorts and mounting errors

Use caution when positioning he IC for mounting on PCBs. The IC may be damaged if there are any connection errors or if pins are shorted together.

(7) Operation in strong electromagnetic fields

Exercise caution when using the IC in the presence of strong electromagnetic fields as doing so may cause the IC to malfunction.

(8) ASO

When using the IC, set the output transistor so that it does not exceed either absolute maximum ratings or ASO.

(9) Thermal shutdown circuit

The IC incorporates a built-in thermal shutdown circuit (TSD circuit), which is designed to shut down the IC only to prevent thermal overloading. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC if this circuit is activated, or in environments in which activation of this circuitry can be assumed.

	TSD ON Temp. [°C] (typ.)	Hysteresis Temp. [°C] (typ.)
BD95513MUV	175	15

(10) Testing on application boards

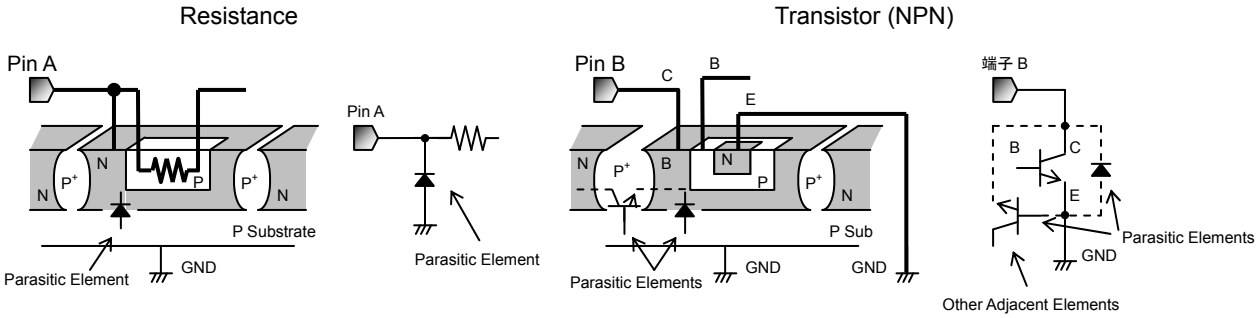
When testing the IC with application boards, connecting capacitors directly to low-impedance terminals can subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should be turned off completely before connecting it to or removing it from a jig or fixture during the evaluation process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

(11) Regarding IC input pins

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. PN junctions are formed at the intersection of these P layers with the N layers of other elements, creating parasitic diodes and/or transistors. For example (refer to the figure below):

- When GND > Pin A and GND > Pin B, the PN junction operates as a parasitic diode
- When GND > Pin B, the PN junction operates as a parasitic transistor

Parasitic diodes occur inevitably in the structure of the IC, and the operation of these parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

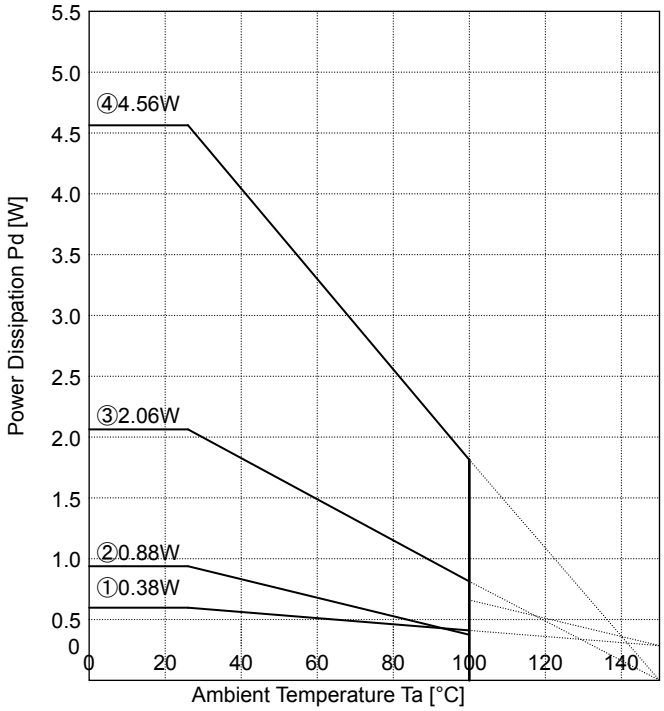


Example of IC Structure

(12) Ground wiring traces

When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground potential within the application in order to avoid variations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on GND voltage.

●Power Dissipation



VQFN032-V5050

① IC Only

$\Theta_{j\text{-}a}$ = 328.9 °C/W

② IC mounted on 1-layer board (with 20.2 mm^2 copper thermal pad)

$\Theta_{j\text{-}a}$ = 142.0 °C/W

③ IC mounted on 4-layer board (with 20.2 mm^2 pad on top layer, 5502 mm^2 pad on layers 2,3)

$\Theta_{j\text{-}a}$ = 60.7 °C/W

④ IC mounted on 4-layer board (with 5505mm^2 pad on all layers)

$\Theta_{j\text{-}a}$ = 27.4 °C/W

●Ordering Instructions

B	D	9	5	5	1	3	M	U	V	–	E	2

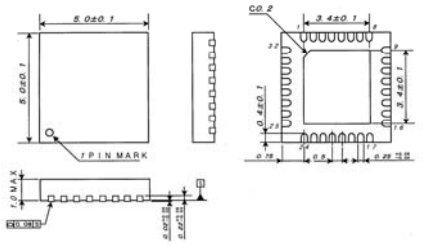
Product name
- **BD955X**

Package Type
- **MUV : VQFN032-V5050**

Taping type name
E2= Embossed carrier tape

VQFN032-V5050

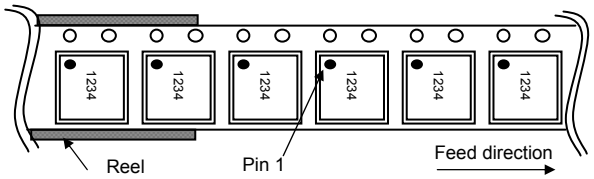
<Dimensions>



(Unit:mm)

<Packing Specifications>

Tape	Embossed carrier tape (with dry-pack)
Quantity	2500 pcs
Feed Direction	**E2** Pin 1 is located on the upper-left corner when the reel is held on the left and fed out to the right



※ Please place orders in quantities of full reels.

Contact us for further information about the products.

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Chicago	TEL: +1-847-368-1006	FAX: +1-847-368-1008
Dallas	TEL: +1-469-287-5366	FAX: +1-469-362-7973
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Detroit	TEL: +1-248-348-9920	FAX: +1-248-348-9942
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Stuttgart	TEL: +49-711-7272-370	FAX: +49-711-7272-3720
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