PLESSEY Semiconductors — CLA2000 series

MICROGATE-C

CLA2000 SERIES

Microgate-C is a semi-custom design technique for the production of gate arrays on Plessey Semiconductors high speed, low power Isoplanar CMOS process. The CLA2000 series gate arrays consist of a matrix of array elements and peripheral cells that are customised by the use of two layers of metallisation and the interlayer via holes.

The simple design procedure requires no specialised semiconductor experience and may be undertaken by any logic or PCB designer accustomed to thinking in traditional MSI/SSI terms.

Table 1 gives details of the CLA2000 series of arrays.

The cell library currently consists of over 30 logic functions, including gates, latches, decoders, shift registers, arithmetic elements, input buffers and output buffers.

Type No.	No.of gates	No.of available pads	Min. package size
CLA21XX	840	44	16 pins
CLA23XX	1440	56	22 pins
CLA25XX	2400	68	22 pins

1 Gate = 4 CMOS transistors (which may be arranged as a 2 input NAND gate) = 1 basic array element (Fig.1).
1 Array Block = 4 array elements.

Table 1 CLA 2000 series

CLA2000 SERIES DESIGN

The CLA2000 series consists of rows of array elements and blocks with interconnect highways between each row (Fig.3). On the edges of the chip surrounding the array elements, are peripheral cells (Fig.2) which buffer signals into and out of the chip. A simplified schematic of a CLA2000 series layout is shown in Fig.3 .

The customer's circuit is built up using standard fully characterised cells selected from the comprehensive library. Each cell is constructed from one or more of the array elements (or from the peripheral cells).

The cells are joined together using the interconnection highways. The interconnections required within the cells are held on the Plessey Semiconductors computer graphics system and are automatically added to the customer's interconnection pattern when called up by their code names.

INTERCONNECTION HIGHWAYS

A maximum of 12 first layer metals may run in the highways between the rows of cells. Up to 10 metals may run across each array block, at right angles to the first layer metals. Interconnection between the two layers may take place wherever they cross by the use of a via hole.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	-55°C to +150°C
Package temperature	-55°C to +125°C
DC input voltage	V_{SS} -0.3V to V_{DD} +0.3V
Operating voltage range (V_{DD}-V_{SS})	3V to 6V

FEATURES

- Manufactured using High Speed Silicon Gate Isoplanar CMOS Technology
- All Inputs and Outputs are TTL/CMOS Compatible and Static Protected
- Available to Commercial, Industrial and Military Specifications
- Low Power Dissipation (3μW per Gate per MHz at 5V)
- Single Supply Voltage (3V to 6V, Ideal for Battery-Powered Applications)
- Gives Competitive Protection of Customer's Design
- Full Interactive Logic Simulation using Plessey Semiconductors 'CLASSIC' Program. A Full Library is Available
- 90% Utilisation Achievable because of Well Planned Interconnection Highways
- Auto-routing from Logic Simulation Connect File

ELECTRICAL CHARACTERISTICS (SEE ALSO INDIVIDUAL CHARACTERISTICS FOR GA NAND2 AND GA DTRS)

Test conditions (unles otherwise stated):

V_{DD} = +5V, V_{SS} = 0V, T_{amb} = +25° C

Static Characteristics

Characteristic	Value Min.	Value Max.	Units	Conditions
High level output voltage, V_{OH}	4		V	I_{OH} = -1.6mA } Note 1
Low level output voltage, V_{OL}		0.4	V	I_{OL} = 3.2mA } Note 1
Low level input voltage, V_{IL}		1.0	V	
High level input voltage, V_{IH}	4		V	} Note 2
Input capacitance, C_{IN}		7	pF	Any input

NOTES
1. Refers to a 'type D' output stage. Increase drive capability is available in 'type Q'.
2. Refers to inverter type input stage.

Dynamic Characteristics at 0° C to +70° C, 5V ± 10 %

Characteristic	Value Min.	Value Max.	Units	Definition
Propagation delay	1.75	7.0	ns	2-input NAND gate, fan-out = 2 + 2mm of track
System clock rate		14	MHz	$\frac{1}{10(\text{Gate Delays})}$
Toggle rate		35	MHz	$\frac{1}{4(\text{Gate Delays})}$

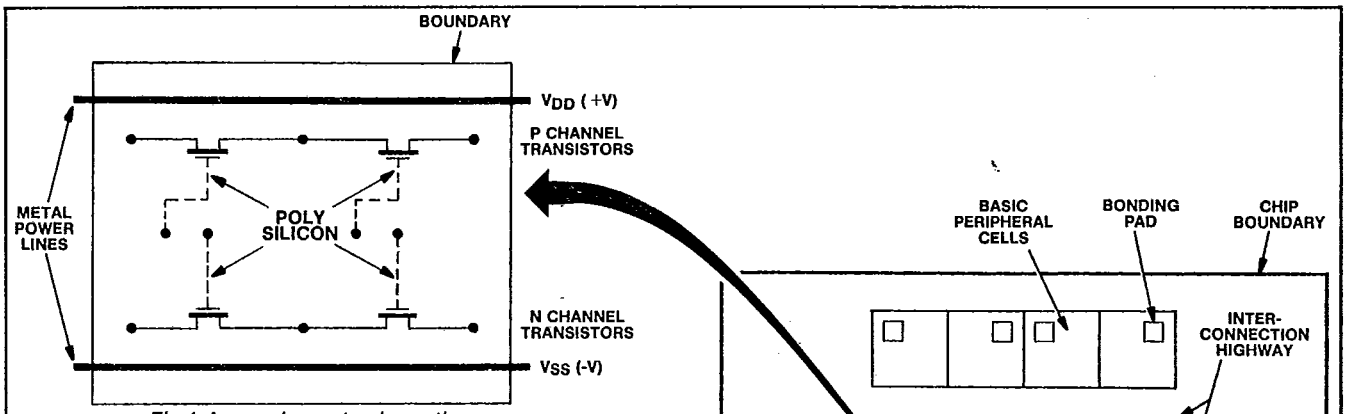


Fig.1 Array element schematic

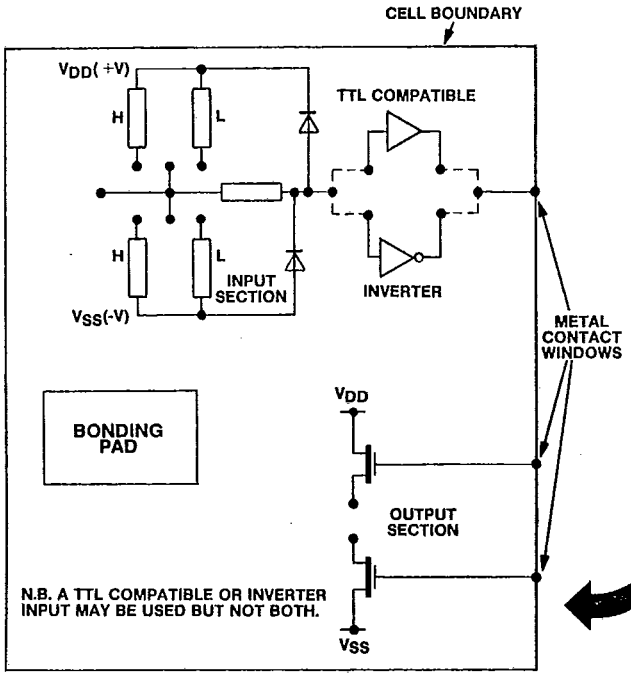


Fig.2 Peripheral cell schematic

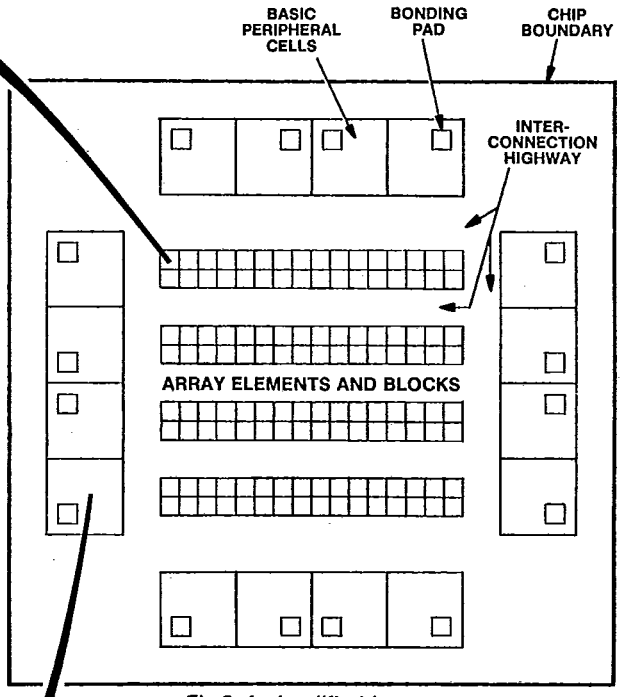
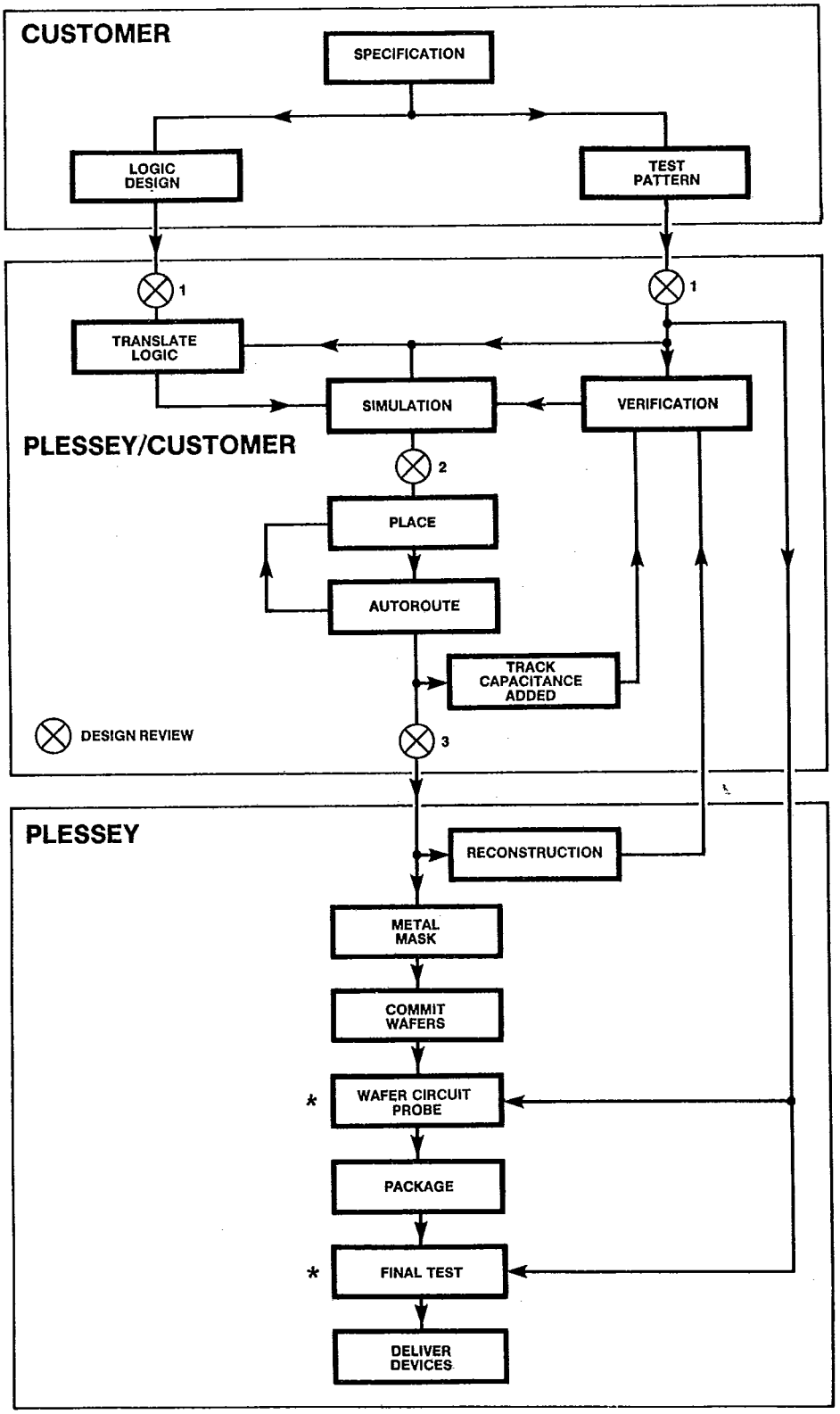


Fig.3 A simplified layout



* MAY BE OMITTED FOR INITIAL SAMPLE DEVICES

Fig.4 Typical design route for CLA2000

ELECTRICAL CHARACTERISTICS - GA NAND2

Characteristic	Value			Units
	Min.	Typ.	Max.	
Output rise time				
Intrinsic delay	0.8	1.6	3.2	ns
Delay per load	0.5	1.0	2.0	ns/LU
Output fall time				
Intrinsic delay	0.6	1.3	2.5	ns
Delay per load	0.2	0.5	0.9	ns/LU
Input loading A			1.0	LU
Input loading B			1.0	LU
Drive capability	8			LU

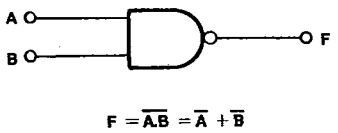


Fig.5 GA NAND2 two input gate

ELECTRICAL CHARACTERISTICS - GA DTRS

Characteristic	Value			Units
	Min.	Typ.	Max.	
Output rise time				
Intrinsic delay CK-Q	2.4	4.8	9.6	ns
Intrinsic delay CK-$\overline{Q}$	4.4	8.7	17.4	ns
Intrinsic delay SET-Q	1.3	2.6	5.2	ns
Intrinsic delay RESET-$\overline{Q}$	1.8	3.6	7.2	ns
Delay/load $\overline{Q}$ output	0.5	1.0	2.0	ns/LU
Delay/load Q output	0.5	1.0	2.0	ns/LU
Output fall time				
Intrinsic delay CK-Q	3.5	7.0	13.9	ns
Intrinsic delay CK-$\overline{Q}$	2.6	5.1	10.2	ns
Intrinsic delay SET-$\overline{Q}$	2.4	4.8	9.5	ns
Intrinsic delay RESET-Q	3.1	6.2	12.4	ns
Delay/load $\overline{Q}$ output	0.2	0.5	0.9	ns/LU
Delay/load Q output	0.2	0.5	0.9	ns/LU
Input loading CK			2.0	LU
Input loading $\overline{CK}$			2.0	LU
Input loading data			2.0	LU
Input loading SET			1.0	LU
Input loading RESET			1.0	LU
Drive capability Q	8			LU
Drive capability $\overline{Q}$	8			LU

NOTE
LU (Load Unit) is the input capacitance of one basic inverter.

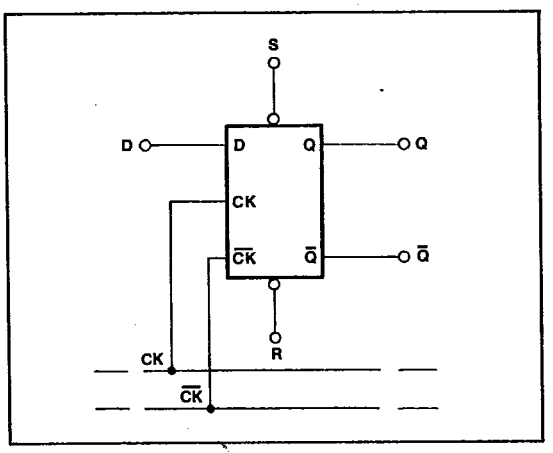


Fig.6 GA DTRS set-reset master slave 'D'-type

Further information is obtainable from Plessey Semiconductors.

Name	Description	No. of array elements
-	Basic Inverter	-
-	Inverter (M)	-
-	Inverter (H)	-
GA 21NV	Dual Inverter	1
GA 1NV4	Powerful Inverter	2
GA 1NV8	Powerful Inverter	4
GA NAND2	2 Input NAND Gate	1
GA NAND3	3 Input NAND Gate	2
GA NAND4	4 Input NAND Gate	2
GA NOR2	2 Input NOR Gate	1
GA NOR3	3 Input NOR Gate	2
GA NOR4	4 Input NOR Gate	2
GA AO1	AND-NOR/OR Gate	2
GA OA1	OR-NAND/AND Gate	2
GA 2ANOR	Dual AND-NOR Gate	2
GA 2ONAND	Dual OR-NAND Gate	2
GA EXNOR	Exclusive NOR Gate	4
GA EXOR	Exclusive OR Gate	4
GA HADD	Half Adder	4
GA FADD	Full Adder	8
GA CKA	Clock Driver 1	2
GA CKA+	Clock Driver 1	2
GA CKA-	Clock Driver 1	2
GA CKB	Clock Driver 2	4
GA RS1	NOR Set/Reset Latch	2
GA RS2	NAND Set/Reset Latch	2
GA 2DL	Dual 'D' Latch	4
GA 2DLRS	Dual Set/Reset 'D' Latch	6
GA DT	Master/Slave 'D' type flip-flop	4
GA DTRS	Set/Reset Master/Slave 'D' type flip-flop	6
GA TRID	Tristate Driver	4
GA 2TM1	2 Transmission Gates + Inverters	2
GA 2TM2	2 Transmission Gates + NAND Gate	2
GA 2TM3	2 Transmission Gates (Buffered)	2
GA 4TM	4 Transmission Gates	2
GA IPS	Input with TTL-Compatible Circuitry	-
GA IPSL-	Input with TTL-Compatible Circuitry and low value pull-down R	-
GA IPSL+	Input with TTL-Compatible Circuitry and low value pull-up R	-
GA IPSH-	Input with TTL-Compatible Circuitry and high value pull-down R	-
GA IPSH+	Input with TTL-Compatible Circuitry and high value pull-up R	-
GA IPI	Inverter Input	-
GA IPIL-	Inverter Input with low value pull-down R	-
GA IPIL+	Inverter Input with low value pull-up R	-
GA IPIH-	Inverter Input with high value pull-down R	-
GA IPIH+	Inverter Input with high value pull-up R	-
GA OPD	Output Inverter (Dual Drive)	-
GA OPQ	Output Inverter (Quad Drive)	-
GA OPS	Output Inverter (Single Drive)	-
GA OPTRD	Tristate Output (Type D)	-
GA OPTRQ	Tristate Output (Type Q)	-
GA OPODD	Open Drain Output (Type D)	-
GA OPODQ	Open Drain Output (Type Q)	-
GA OSC	Oscillator Maintaining Circuit	-
GA 2BD	Dual Buffer Drivers	-
GA V-	Dual Buffer Drivers with additional negative supply pad	-
GA V+	Dual Buffer Drivers with additional positive supply	-

Table 2 CLA2000 series cell library