EL7661C
100V Full Bridge Driver

Features

- 100V High Side Voltage
- Programmable Delay
- Direct Coupled
- No Start Up Ambiguity
- Rail to Rail Output
- 1 MHz Operation
- 1.0 Amp Peak Current
- Improved Response Times
- Matched Rise and Fall Times
- Low Supply Current
- Low Output Impedance
- Low Input Capacitance

Applications

- Uninterruptible Power Supplies
- Distributed Power Systems
- IGBT Drive
- DC-DC Converters
- Motor Control
- Power MOSFET Drive
- Switch Mode Power Supplies

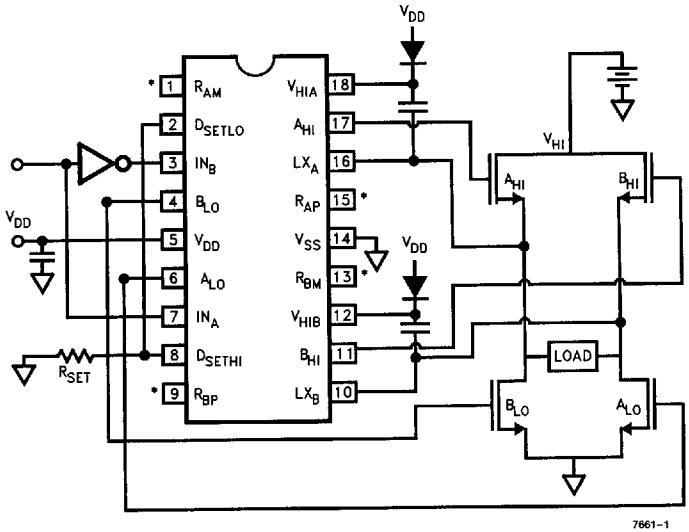
Ordering Information

Part No.	Temp. Range	Package	Outline #
EL7661CN	−40°C to +85°C	18-Pin P-DIP	MDP0031

General Description

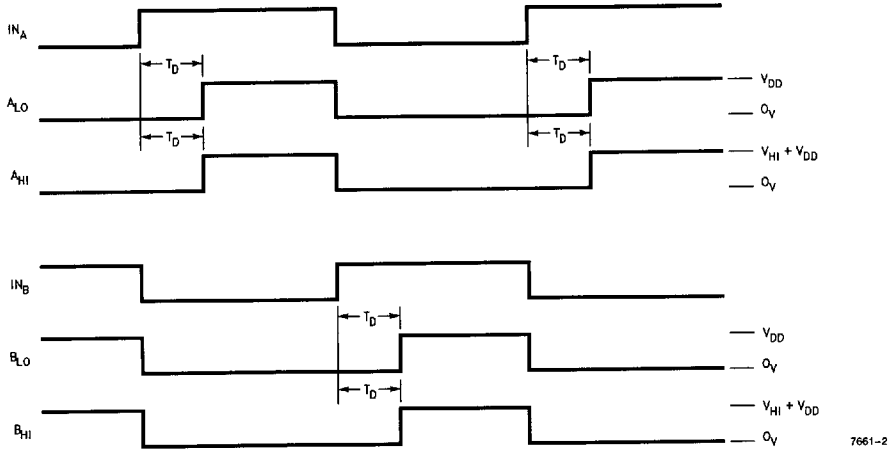
The EL7661 provides a low cost solution to many full bridge applications. The EL7661 is DC coupled so that there are no start up problems associated with AC coupled schemes. A single resistor from the D_{SET} pins to V_{SS} provides "dead time" programmability. Shorting the D_{SET} pins to V_{DD} gives the minimum delay (~100 ns).

Connection Diagram



*Pins 1, 9, 13, 15 must be open.

Timing Diagram



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Absolute Maximum Ratings (T_A = 25°C)

Supply (V_{HIA} and V_{HIB} to V_{SS})	100V	Storage Temperature Range	−65°C to +150°C
Supply (V_{DD} to GND)	16.5V	Ambient Operating Temperature	−40°C to +85°C
Input Pins	−0.3V below V_{SS}, +0.3V above V_{DD}	Power Dissipation PDIP	1600 mW
Operating Junction Temperature	125°C		
Combined Peak Output Current	4A		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

(T_A = 25C, V_{DD} = 15V, V_{SS} = 0V, C_{LOAD} = 1000 pF, unless otherwise specified)

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input/Output							
V_{IL}	Logic "1" Input Voltage		3.0	2.4		I	V
I_{IH}	Logic "1" Input Current			0.1	10.0	I	µA
V_{IL}	Logic "0" Input Voltage			1.8	0.8	I	V
V_{HYS}	Input Hysteresis			0.5		IV	V
I_{IL}	Logic "0" Input Current			0.1	10.0	I	µA
R_{OH}	Pull-Up Resistance	I_{OUT} = −100 mA		5.0	10.0	I	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100 mA		5.0	10.0	I	Ω
I_{PK}	Peak Output Current			1.0		IV	A
I_{DC}	Continuous Output Current Source/Sink		50.0			IV	mA
Power Supply							
I_{DD}	Supply Current into V_{DD}	R_{SET} = 5.1k Inputs = 15V			15.0	I	mA
I_{HIA}	Supply Current into V_{HIA}				4.0	I	mA
I_{HIB}	Supply Current into V_{HIB}				4.0	I	mA
V_{DD}	Operating Voltage		4.5		15.0	I	V

AC Electrical Characteristics

(T_A = 25C, V_{DD} = 15V, V_{SS} = 0V, C_{LOAD} = 1000 pF, unless otherwise specified)

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 500 pF C_L = 1000 pF		15.0 20.0	40.0	IV	ns
t_F	Fall Time	C_L = 500 pF C_L = 1000 pF		15.0 20.0	40.0	IV	ns
$t_{D\ ON\ HI}$	High Side Turn On Delay Time	D_{SET} = V_{DD} R_{SET} = 5.1k R_{SET} = 200k	50.0 75.0 750.0	100.0 125.0 1150.0	150.0 200.0 1500.0	IV I I	ns
$t_{D\ ON\ LO}$	Low Side Turn On Delay Time	D_{SET} = V_{DD} R_{SETLO} = 5.1k R_{SETLO} = 200k	50.0 75.0 750.0	100.0 125.0 1150.0	150.0 200.0 1500.0	IV I I	ns
$t_{D\ OFF\ HI}$	High Side Turn Off Delay Time	D_{SET} = V_{DD}		100.0	150.0	IV	ns
$t_{D\ OFF\ LO}$	Low Side Turn Off Delay Time	D_{SET} = V_{DD}		100.0	150.0	IV	ns
$t_{D\ MISMATCH}$	A_{HI} to A_{LO} Delay Mismatch	D_{SET} = 200k			+/-10.0	I	%
$t_{D\ MISMATCH}$	B_{HI} to B_{LO} Delay Mismatch	D_{SET} = 200k			+/-10.0	I	%
$t_{D\ MISMATCH}$	A_{HI} to B_{HI} Delay Mismatch	D_{SET} = 200k			+/-10.0	I	%
$t_{D\ MISMATCH}$	A_{LO} to B_{LO} Delay Mismatch	D_{SET} = 200k			+/-10.0	I	%

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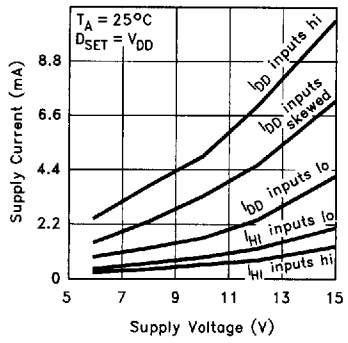
EL7661 Pin Description

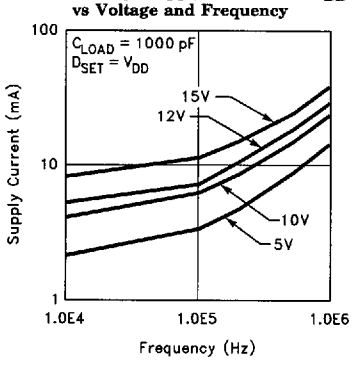
Pin #	Name	Description
1	R_{AM}	Internal circuit connection. This pin swings from V_{SS} to V_{DD}. This pin is out of phase with IN_A. Normally this pin should be unconnected to any external circuitry.
2	D_{SETLO}	Connection for the delay setting resistor. This pin must be connected externally to the D_{SETHI} pin. This pin is connected internally to a PMOS diode referenced to V_{DD}.
3	IN_B	Digital input for the "B" drivers. Its polarity is non-inverting with respect to the "B" outputs.
4	B_{LO}	"B" lo-side output. Swings from V_{SS} to V_{DD}.
5	V_{DD}	Positive supply for the lo-side circuitry.
6	A_{LO}	"A" lo-side output. Swings from V_{SS} to V_{DD}.
7	IN_A	Digital input for the "A" drivers. Its polarity is non-inverting with respect to the "A" outputs.
8	D_{SETHI}	Connection for the delay setting resistor. This pin must be connected externally to the D_{SETLO} pin. This pin is connected internally to a PMOS diode referenced to V_{DD}.
9	R_{BP}	Internal circuit connection. This pin swings from V_{SS} to V_{DD}. It is in phase with IN_B. Normally this pin should be unconnected to any external circuitry.
10	LX_B	Negative supply for the "B" hi-side driver.
11	B_{HI}	"B" hi-side output. Swings from LX_B to V_{HIB}.
12	V_{HIB}	Positive supply for the "B" hi-side driver.
13	R_{BM}	Internal circuit connection. This pin swings from V_{SS} to V_{DD}. It is out of phase with IN_B. Normally this pin should be unconnected to any external circuitry.
14	V_{SS}	Negative supply for lo-side circuitry.
15	R_{AP}	Internal circuit connection. This pin swings from V_{SS} to V_{DD}. It is in phase with IN_A. Normally this pin should be unconnected to any external circuitry.
16	LX_A	Negative supply for the "A" hi-side driver.
17	A_{HI}	"A" hi-side output. Swings from LX_A to V_{HIA}.
18	V_{HIA}	Positive supply for the "A" hi-side driver.

Typical Performance Curves

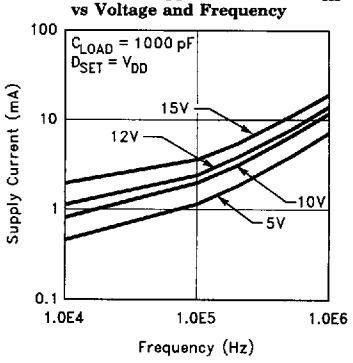
Quiescent Supply Current vs Supply Current



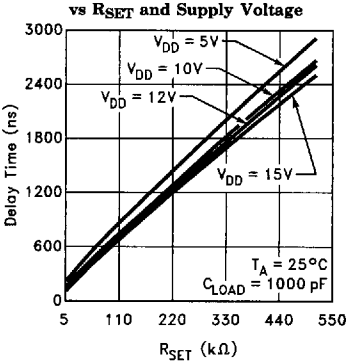
Average Supply Curent into V_{DD} vs Voltage and Frequency



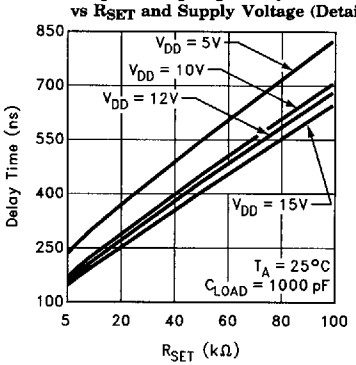
Average Supply Curent into V_{HI} vs Voltage and Frequency



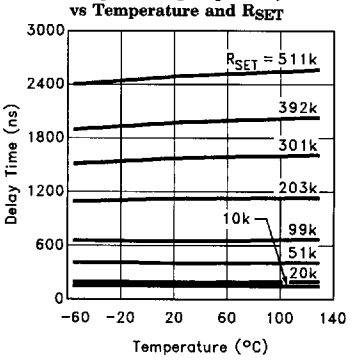
Output Rising Edge Delay vs R_{SET} and Supply Voltage



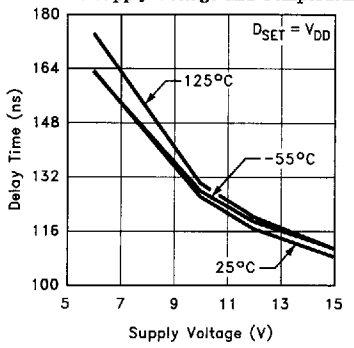
Output Rising Edge Delay vs R_{SET} and Supply Voltage (Detail)



Output Rising Edge Delay vs Temperature and R_{SET}

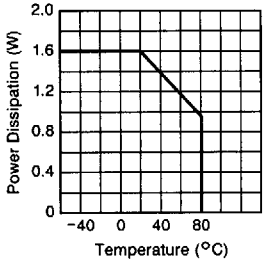


Output Falling Edge Delay vs Supply Voltage and Temperature

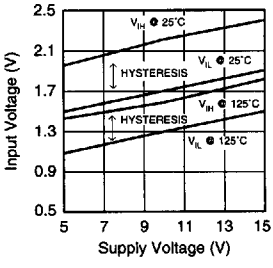


Typical Performance Curves — Contd.

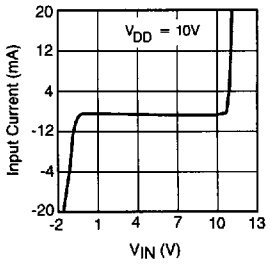
Power Dissipation vs Temperature



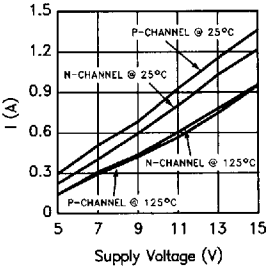
Input Threshold vs Supply Voltage



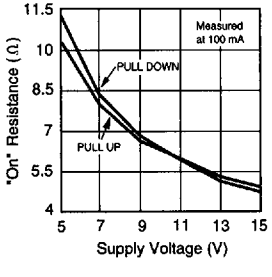
Input Current vs Input Voltage



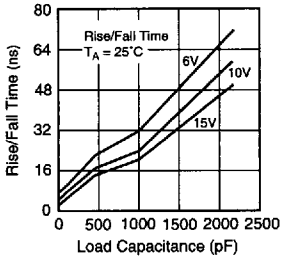
Peak Drive vs Supply Voltage



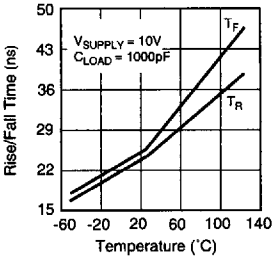
"On" Resistance vs Supply Voltage



Rise/Fall Time vs Load and Supply



Rise/Fall Time vs Temperature



7661-10

EL7661C

Theory of Operation

The EL7661 consists of, among other things, 4 CMOS super inverter output stages. The super inverter configuration minimizes the possibility of simultaneous conduction of the two output complementary MOS devices. Each output stage can source or sink up to 1 amp of peak current. The state of the two output stages denoted "A_{LO}" and "A_{HI}" is determined by the input "IN_A". In a like manner the state of the two output stages denoted "B_{LO}" and "B_{HI}" is determined by the input "IN_B". The lo-side output stages, "A_{LO}" and "B_{LO}" have V_{SS} as their negative supply and V_{DD} as their positive supply. The negative supply of the "A_{HI}" output stage is LX_A. The positive supply of the "A_{HI}" output stage is V_{HIA}. Similarly, the positive and negative supplies of the "B_{HI}" output stage are denoted V_{HIB} and LX_B. The hi-side supplies, LX_A, LX_B, V_{HIA}, and V_{HIB} can float with respect to V_{SS}. In fact the hi-side supplies can easily be 100V higher than V_{SS}. However, the differential voltage between V_{HIA} and LX_A, and between V_{HIB} and LX_B, should never exceed 15V.

The input signals, IN_A and IN_B, are level shifted from their quasi TTL levels to V_{SS} to V_{DD} voltages. After the level shift stage the rising edge of the signal is delayed some amount determined by the value of the resistor at the D_{SET} pin. (The falling edge of the signal has no extra delay added to it at this stage.) The delayed signal then drives its respective output drivers. The signals which drive the hi-side drivers are level shifted up to the appropriate levels while the signals which drive the lo-side drivers have an additional delay added to mimic the delay inherent in the hi-side level shift circuitry.

The circuitry which produces the resistor controlled delay of the rising edge of the output reduces down to a simple RC time constant. The R is provided by the user and the C is built into the delay circuitry. Ideally the delay would have no dependency on supply voltage or temperature since the R and C are well controlled, however, due to nonidealities of the exact implementation, the delay times are a weak function of supply voltage and temperature.

EL7661C
100V Full Bridge Driver

Macromodel

```
****EL7661 model****
*** top level circuit starts here ***
*                    a-input
*                    |    b-input
*                    |    |    a lo-side output
*                    |    |    |    b lo-side output
*                    |    |    |    |    a hi-side output
*                    |    |    |    |    |    b hi-side output
*                    |    |    |    |    |    |    a hi-side neg supply
*                    |    |    |    |    |    |    |    b hi-side neg supply
*                    |    |    |    |    |    |    |    |    lo-side neg supply
*                    |    |    |    |    |    |    |    |    |    a hi-side pos supply
*                    |    |    |    |    |    |    |    |    |    |    b hi-side pos supply
*                    |    |    |    |    |    |    |    |    |    |    |    lo-side pos supply
*                    |    |    |    |    |    |    |    |    |    |    |    |
.subckt M7661        ina  inb  alo  blo  ahi  bhi  lxa  lxb  vss  vhia vhib vdd
****top level subcircuit calls****
xdela ina outa vss delay
xdelb inb outb vss delay
xalo alo outa vdd vss vss outstg
xblo blo outb vdd vss vss outstg
xahi ahi outa vhia lxa vss outstg
xbhi bhi outb vhib lxb vss outstg
.ends M7661
****put in value of rset resistor here****
.param rset = 50e3
****comparator subcircuit****
.subckt comp10 out inp inm vss
el out vss table {(v(inp)-v(inm))*5000} (0,0,15,15)
rout out vss 10meg
rinp inp vss 10meg
rinm inm vss 10meg
.ends comp10
```

Macromodel — Contd.

```
****input, delay, and level shift subcircuit****
.subckt delay vin compout vss
vinref vinref vss 1.8
x1 n1 vin vinref vss comp10
rslow n1 n5 {rset}
rnom n5 n2 25k
cdelay n2 vss 7.5p
ddelay n4 n1 modd
rfast n4 n2 110k
rdiv1 vddint n3 1k
rdiv2 n3 vss 1k
x2 compout n3 n2 vss comp10
vddint vddint vss 15
.model modd d is=1e-7
.ends delay
****5 ohm output stage subcircuit****
.subckt outstg out gate vhi lx vss
sp vhi out gate vss spmod
sn out lx gate vss snmod
.model spmod vswitch ron=5 roff=2meg von=2.5 voff=4.5
.model snmod vswitch ron=5 roff=2meg von=7.5 voff=5.5
.ends outstg
```

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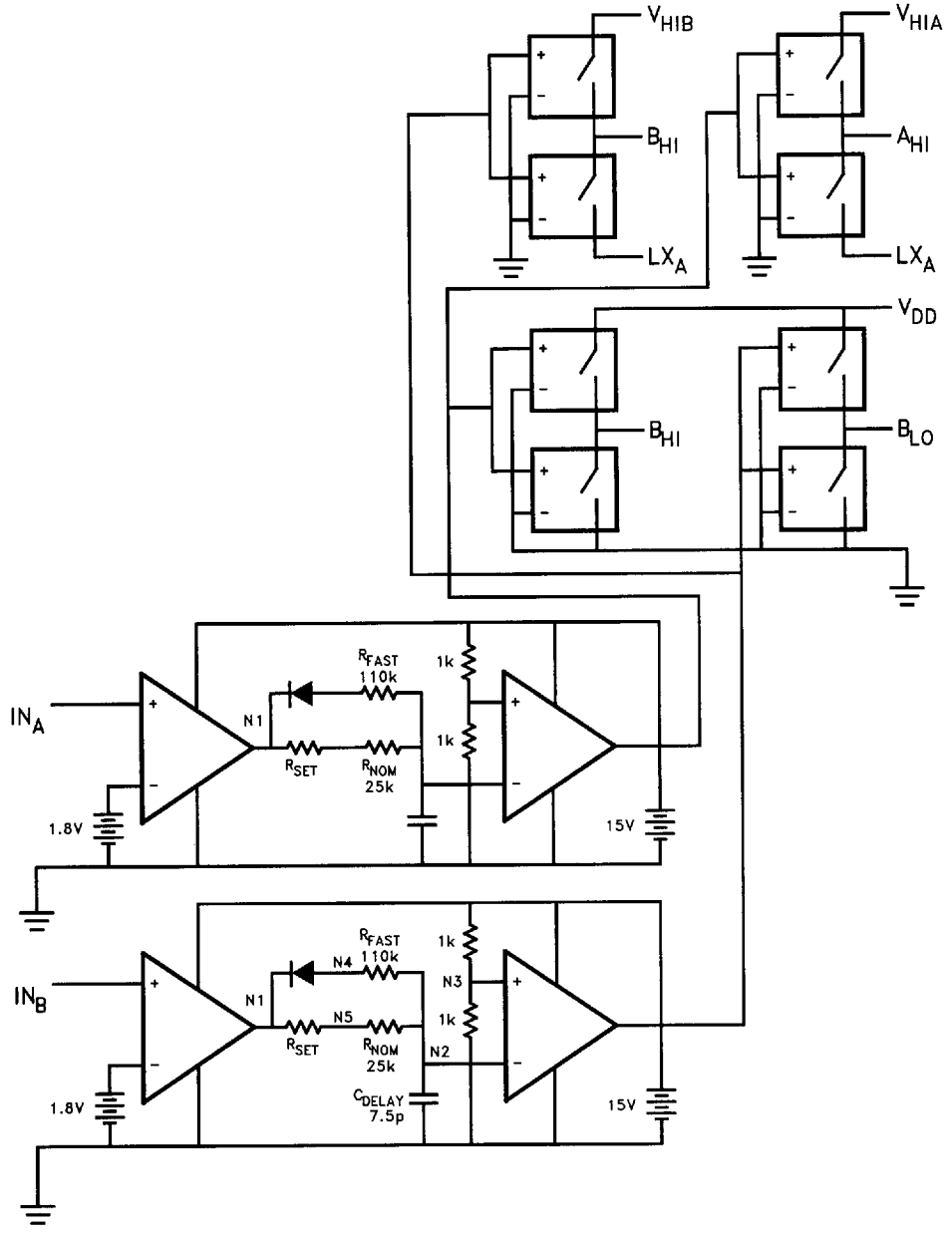
EL7661C
100V Full Bridge Driver

Macromodel — Contd.

EL7661 Macromodel Schematic



Soldering Packages to PC Boards

DIP Packages

Wave soldering is recommended for DIP packages. Solder plated boards are recommended. Rosin mildly activated (RMA) flux is needed. Wave soldering using a dual wave system at 250°C ±10°C for two seconds per wave is preferable. Thorough cleaning of boards after soldering is required.

Hand soldering, Elantec's DIP packages will survive a peak temperature of 300°C (at leads) for a maximum period of 10 seconds.

Surface Mount Packages

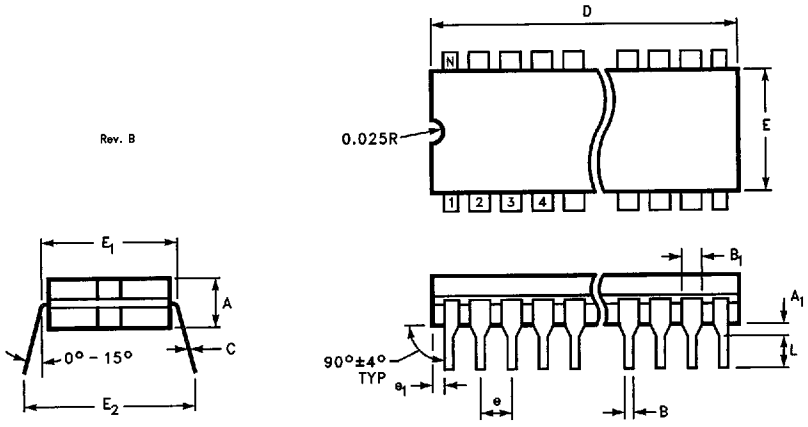
Wave soldering and vapor phase or infrared (IR) reflow can be used for soldering surface mount packages to PC boards. Solder plated boards are recommended for wave soldering and vapor phase or IR reflow methods.

Wave Soldering: Adhesive is used to hold components on the boards during wave soldering. Place components on the board and cure adhesive before wave soldering. Rosin mildly activated (RMA) flux or organic flux is needed. Wave soldering using a dual wave system at 250°C ±10°C for a maximum of two seconds per wave is preferable. Thorough cleaning of boards after soldering is required.

Reflow Soldering: Screen solder paste on board and attach components to board. Solder paste with RMA flux is recommended. Bake boards at 65°C–90°C for 15 minutes. Preheat boards to within 60°C–70°C of the solder temperature. To reflow solder paste with vapor phase method, the solder paste temperature must be maintained at or above 200°C for at least 30 seconds. The components temperature can not exceed 215°C. For the IR reflow method, the solder paste temperature must be maintained at or above 200°C for at least 30 seconds. The components temperature can not exceed 220°C. The temperature/time ramp-up during vapor phase or IR reflow shall be no greater than 2°C/sec.

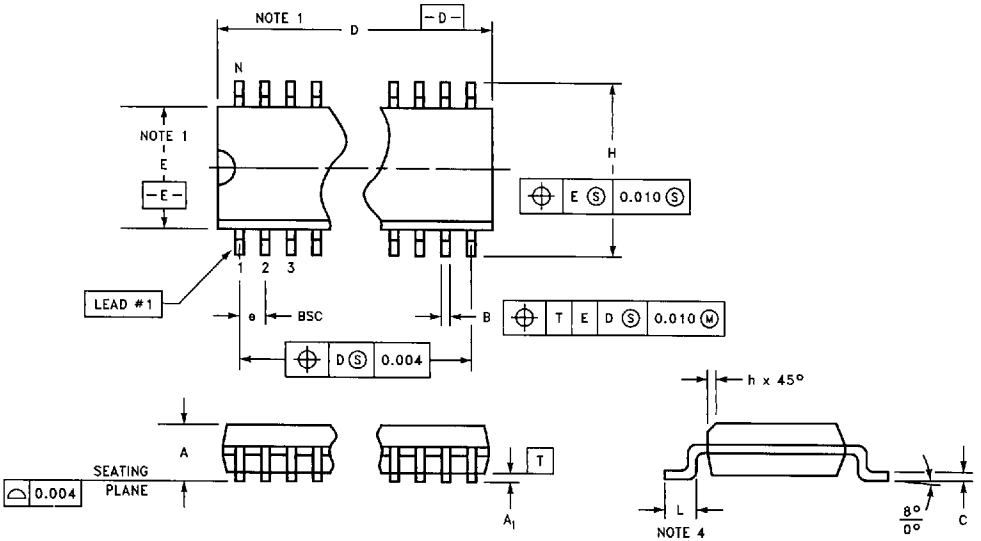
Hand soldering, Elantec's surface mount packages will survive a peak temperature of 260°C (at leads) for a maximum period of 10 seconds.

Package Outlines



MDP0016 Rev. B
CerDIP Package
Lead Finish (Coml)—Tin Plate or Hot Solder DIP
Lead Finish (Mil)—Hot Solder DIP

Common Dimensions	Min	Max	Min	Max	Min	Max	Min	Max
A	0.140	0.160	0.140	0.160	0.140	0.160	0.140	0.160
A_1	0.115	0.055	0.020	0.050	0.015	0.060	0.020	0.050
B	0.016	0.023	0.016	0.021	0.014	0.026	0.016	0.021
B_1	0.050	0.065	0.050	0.060	0.038	0.068	0.050	0.060
C	0.008	0.012	0.008	0.012	0.008	0.018	0.008	0.012
D	0.375	0.395	0.760	0.785	0.940	0.960	1040.925	1.060
E	0.245	0.265	0.220	0.291	0.220	0.310	0.2780	0.298
E_1	0.300	0.320	0.300	0.320	0.290	0.320	0.300	0.320
E_2	0.340	0.390	0.340	0.390	0.360	0.410	0.340	0.390
e	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
e_1	0.020	0.055	0.078	0.098	0.068	0.098	0.078	0.098
L	0.125	0.150	0.125	0.150	0.125	0.150	0.130	0.150
N	8-Lead		14-Lead		18-Lead		20-Lead	



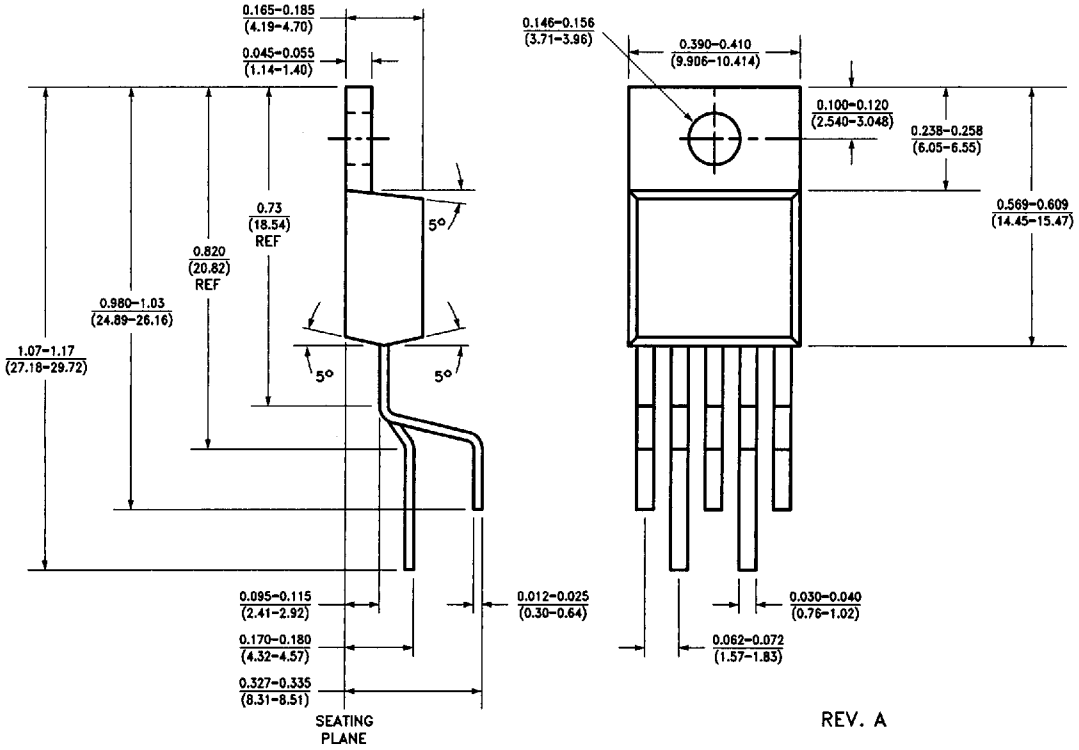
REV. C

Note 1: These dimensions do not include mold flash or protrusions. Mold flash protrusion shall not exceed .006" on any side.
Note 2: SO-8, SO-14, S0-16 packages are narrow body (0.150").
Note 3: Dimensions and tolerancing per ANSI Y14.5M-1982.
Note 4: Flat area of lead foot.
Note 5: SOL-24T2 (thermal package) has 2 fused leads on each side of package.
Note 6: SOL-20T (thermal package) has 4 fused leads on each side of package.
Note 7: SOL-28T contains a thermal metal slug.

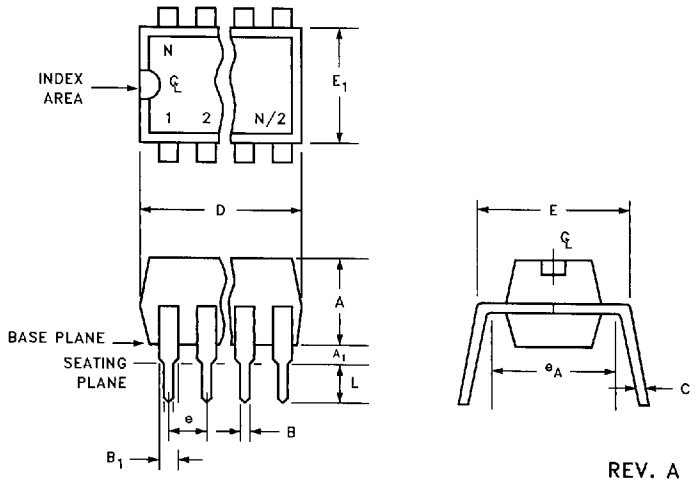
MDP0027 Rev. C
Package Outline—SOIC
Lead Finish—Solder Plate

Symbol	Lead Count													
	SOL-28		SOL-20		SOL-16		SO-16		SO-14		SO-8		SOL-24	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.096	0.104	0.096	0.104	0.096	0.104	0.061	0.068	0.061	0.068	0.061	0.068	0.096	0.104
A_1	0.004	0.011	0.004	0.011	0.004	0.011	0.004	0.010	0.004	0.010	0.004	0.010	0.004	0.011
B	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019
C	0.009	0.012	0.009	0.012	0.009	0.012	0.008	0.010	0.008	0.010	0.008	0.010	0.009	0.012
D	0.696	0.712	0.498	0.510	0.397	0.430	0.386	0.394	0.337	0.344	0.189	0.196	0.598	0.614
E	0.291	0.299	0.291	0.299	0.291	0.299	0.150	0.157	0.150	0.157	0.150	0.157	0.291	0.299
e	0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC	
H	0.398	0.414	0.398	0.414	0.398	0.414	0.230	0.244	0.230	0.244	0.230	0.244	0.398	0.414
h	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016
L	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024

Package Outlines



MDP0028 Rev. A
5-Lead TO-220
Lead Finish—Solder Plate



MDP0031 Rev. A
Plastic Package
Lead Finish—Hot Solder DIP

Common Dimensions	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A_1	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
A	0.125	0.145	0.125	0.145	0.125	0.145	0.125	0.145	0.125	0.145
B	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020	0.015	0.021
B_1	0.050	0.070	0.050	0.070	0.050	0.070	0.050	0.070	0.050	0.070
C	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
D	0.350	0.385	0.745	0.755	0.745	0.755	0.875	0.905	0.925	1.045
E	0.295	0.320	0.295	0.320	0.295	0.320	0.295	0.320	0.295	0.320
E_1	0.245	0.255	0.245	0.255	0.245	0.255	0.245	0.255	0.245	0.255
e	0.100 Typ		0.100 Typ		0.100 Typ		0.100 Typ		0.100 Typ	
e_A	0.300 Ref		0.300 Ref		0.300 Ref		0.300 Ref		0.300 Ref	
L	0.115	0.135	0.115	0.135	0.115	0.135	0.115	0.135	0.115	0.135
N	8		14		16		18		20	

Note: Package outline exclusive of any mold flashes. Mold flash protrusion shall not exceed 0.006" on any side.