Integrated Device Technology, Inc.

512K/256K x 16 CMOS STATIC RAM MODULE

IDT7MP4047
IDT7MP4046

FEATURES:

- High-speed 8/4 megabit (pin compatible) CMOS static RAM modules
- Fast access time: 70ns (max.)
- Low power consumption
  - — Active: 220mA max.
  - — CMOS Standby: 850µA max.
  - — Data retention: 450µA max. (Vcc= 2V)
- Surface mounted small outline plastic packages on a 45 pin FR-4 SIP (Single In-line Package)
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

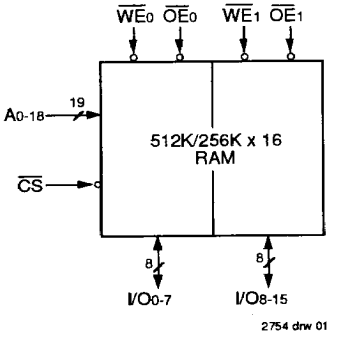
DESCRIPTION:

The IDT7MP4047/4046 is a 512K/256K x 16 CMOS static RAM module constructed on a multilayer epoxy laminate (FR-4) substrate using eight or four 128K x 8 static RAMs in small outline plastic packages and a one-of-four decoder. Availability of two Write Enables and two Output Enables provides byte access and output control flexibility. The IDT7MP4047/4046 is available with access times as fast as 70ns with a maximum operating current of 220mA. For battery backup applications, a very low data retention current is available.

The IDT7MP4047/4046 is packaged in a 45 pin FR-4 SIP (Single In-line Package). This results is a package 4.6 inches in length and less than 0.2 inches in thickness.

All inputs and outputs of the IDT7MP4047/4046 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



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COMMERCIAL TEMPERATURE RANGE

APRIL 1992

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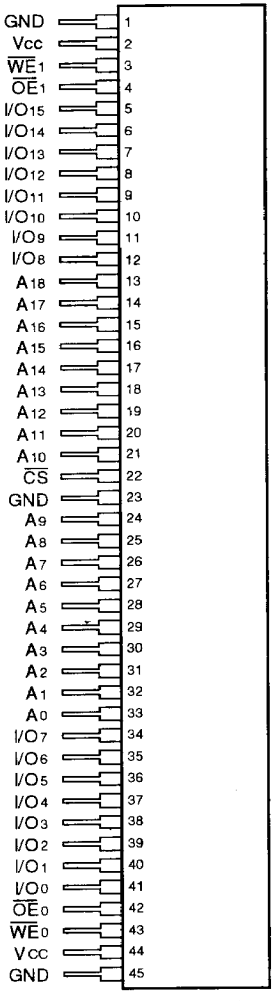
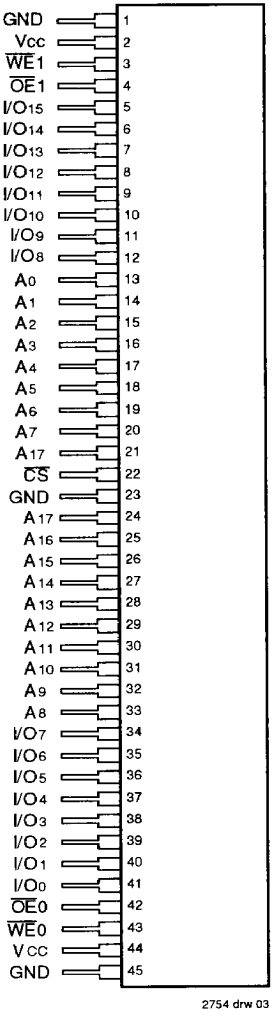
PIN CONFIGURATION — 7MP4047



2754 drw 02

PIN CONFIGURATION[1] — 7MP4046

SIP
FRONT VIEW



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NOTE:
1. For proper operation of the 7MP4046 module, pins 21 and 24 must be tied together.

PIN NAMES - 7MP4047

I/O0–I/O15	Data Inputs/Outputs
A0–A18	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}_{0-1}$	Write Enables
$\overline{OE}_{0-1}$	Output Enables
Vcc	Power
GND	Ground

2754 tbl 03

PIN NAMES - 7MP4046

I/O0–I/O15	Data Inputs/Outputs
A0–A17	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}_{0-1}$	Write Enables
$\overline{OE}_{0-1}$	Output Enables
Vcc	Power
GND	Ground

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2754 tbl 05

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	High Z	Active

2754 tbl 06

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2754 tbl 07

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

2754 tbl 08

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	7MP4046 Max.	7MP4047 Max.	Unit
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	4	8	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	4	8	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2mA	—	0.4	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -1mA	2.4	—	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}, f = f_{MAX}, Output Open	—	220	220	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS} \geq V_{IH}$, V_{CC} = Max., f = f_{MAX}, Ouput Open	—	12	24	mA
I_{SB1}	Full Standby Supply Current (CMOS Levels)	$\overline{CS} \geq V_{HC}$, $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$ V_{CC} = Max., Output Open	—	450	850	µA

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DATA RETENTION CHARACTERISTICS

(T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition	Min.	7MP4046/4047 Max. @ 2.0V	Unit
V_{DR}	V_{CC} for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ - 0.2V	—	250/450	µA
t_{CDR}(2)	Chip Deselect to Data Retention Time	$V_{IN} \leq V_{CC}$ - 0.2V	0	—	ns
t_R(2)	Operation Recovery Time	$V_{IN} \geq$ - 0.2V	t_{RC}(1)	—	ns

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NOTES:
1. t_{RC} = Read Cycle Time.
2. This parameter is guaranteed by design, but not tested.

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2754 tbl 11

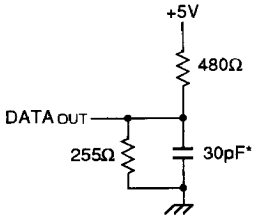

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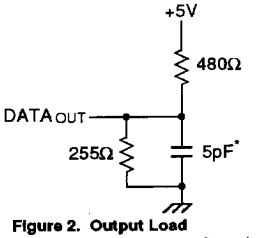
Figure 1. Output Load



2754 drw 05

Figure 2. Output Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, and tWHZ)

*Including scope and jig

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

		7MP4046/4047LxxS								
		-70		-85		-100		-120		
Symbol	Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE										
tRC	Read Cycle Time	70	—	85	—	100	—	120	—	ns
tAA	Address Access Time	—	70	—	85	—	100	—	120	ns
tACS	Chip Select Access Time	—	70	—	85	—	100	—	120	ns
tOE	Output Enable to Output Valid	—	45	—	48	—	50	—	60	ns
tOHZ(1)	Output Disable to Output in High Z	—	30	—	33	—	35	—	40	ns
tOLZ(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	ns
tCLZ(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
tCHZ(1)	Chip Deselect to Output in High Z	—	40	—	43	—	45	—	50	ns
tOH	Output Hold from Address Change	10	—	10	—	10	—	10	—	ns
WRITE CYCLE										
tWC	Write Cycle Time	70	—	85	—	100	—	120	—	ns
tWP	Write Pulse Width	55	—	65	—	75	—	90	—	ns
tAS	Address Set-up Time	0	—	2	—	5	—	5	—	ns
tAW	Address Valid to End of Write	65	—	82	—	90	—	100	—	ns
tCW	Chip Selection to End of Write	65	—	80	—	85	—	100	—	ns
tDS	Data Set-up Time	35	—	38	—	40	—	45	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tWHZ(1)	Write Enable to Ouput in High Z	—	30	—	33	—	35	—	40	ns
tOW(1)	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

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NOTE:
1. This parameter is guaranteed by design, but not tested.

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CAPACITANCE[1] - 7MP4047

(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
$C_{IN(C)}$	Input Capacitance($\overline{CS}$)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	35	pF

2754 tbl 01

NOTE:
1. This parameter is guaranteed by design, but not tested.

CAPACITANCE[1] - 7MP4046

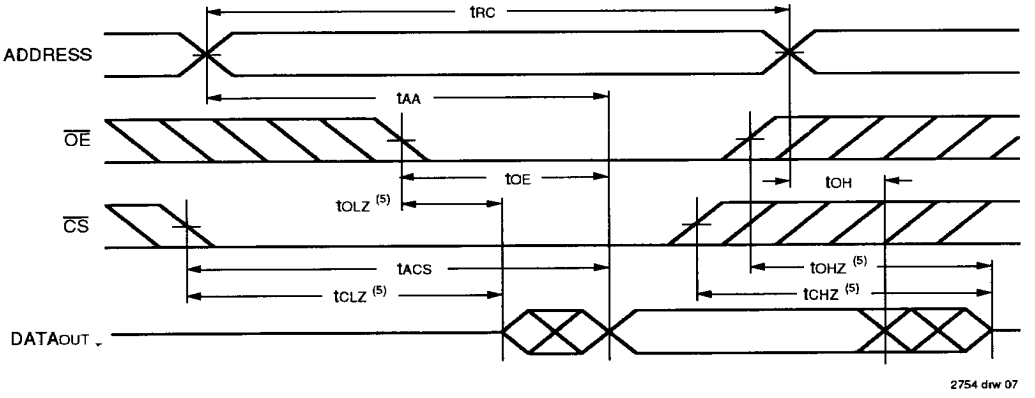
(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	30	pF
$C_{IN(C)}$	Input Capacitance($\overline{CS}$)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	20	pF

2754 tbl 02

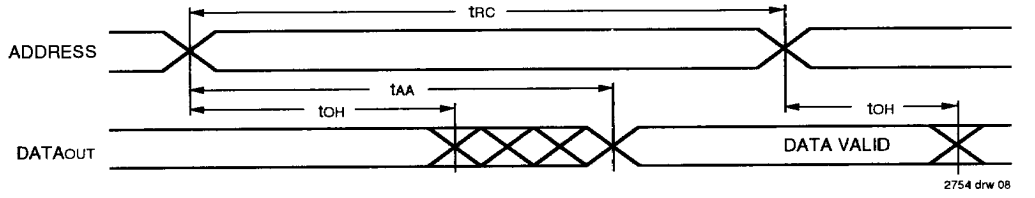
NOTE:
1. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



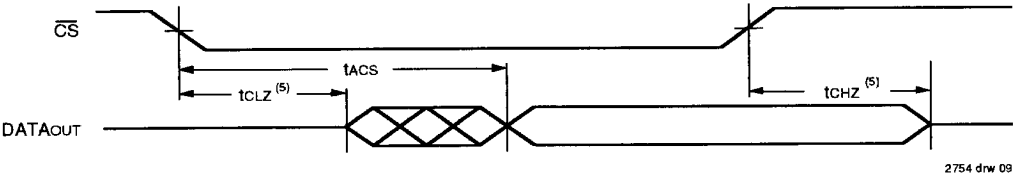
2754 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]



2754 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4]



2754 drw 09

NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed, but not tested.

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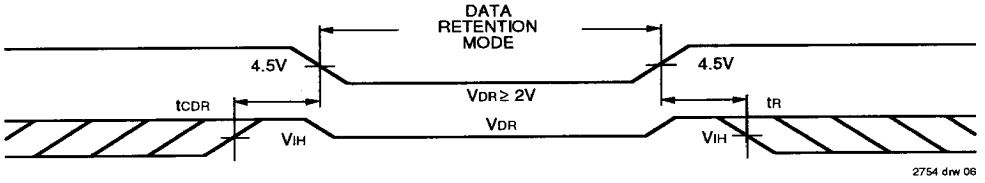
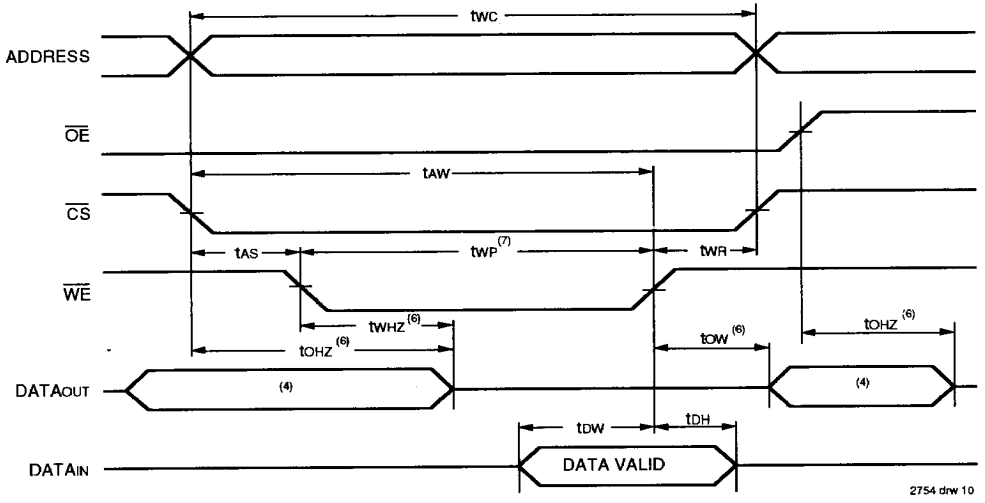
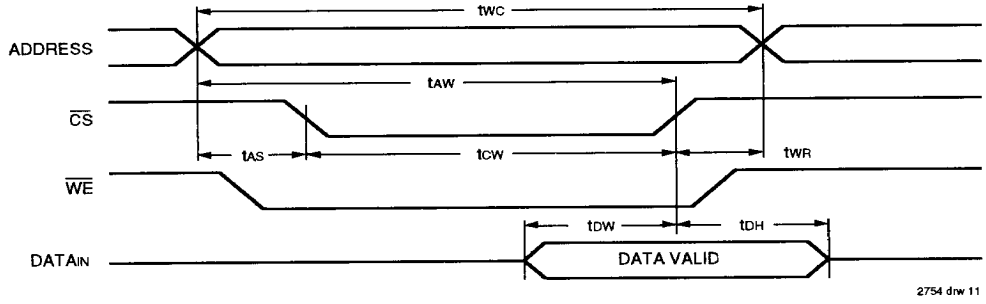
DATA RETENTION WAVEFORM



TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state and inputs signals must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transitions, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).. This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tWD. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

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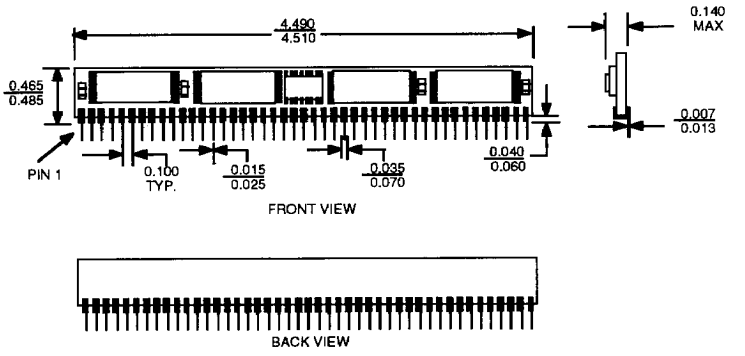
PACKAGE DIMENSIONS

7MP4046



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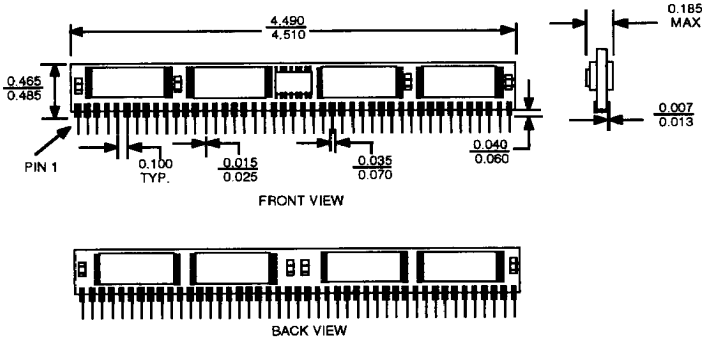
7MP4047



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