Rockwell

RC144ACFL and RC144ATFL
Low Power, Integrated High Speed Data/Fax/Voice Modem Device Set for Portable Applications

INTRODUCTION

The Rockwell RC144ACFL and RC144ATFL integrated data/fax/voice modem device set supports high speed data and high speed fax modem operation in the US or world-wide over a dial-up telephone line and, for US versions, a cellular phone. (Table 1 lists the models).

Low profile, small PQFP or TQFP packages and very low power consumption make this device set ideal for laptop, notebook, and palmtop applications using parallel or serial interface (E39 MCU) or PCMCIA interface (P39 MCU).

The modem operates at line speeds up to 14400 bps and supports fax Group 3 send and receive and T.30 protocol.

RC144ATFL models require no external RAM or ROM. Models are available to support either a parallel 16550A UART-compatible interface host or a serial EIA/TIA-232-E logic-compatible DTE interface.

RC144ACFL models perform error correction and data compression (ECC) in the modem using 32k bytes of external RAM. ECC increases data throughput typically by a factor of four.

RC144ATFL models support ECC performed by the host CPU and communications software for Windows using the enhanced Rockwell Windows Protocol Interface (RPI+™) and WinRPI host software module.

RC144ATFLW and RC144ACFLW models use an external EPROM to support single country (8k bytes) or multiple countries (128k bytes).

In voice mode, enhanced ADPCM coding and decoding supports efficient digital storage of voice using 2-bit or 4-bit compression and decompression at 7200 bps. Coder silence deletion and decoder silence interpolation is available to significantly increase compression rates.

Voice models operating with the parallel host bus support business audio and the Integrated Communications System (ICS) program. These models support applications such as digital answering machine, voice annotation, audio file play/record, and text-to-speech conversion.

In voice/business audio mode and in data modem modes, the modem supports data throughput in excess of 176 kbps utilizing the Rockwell High Speed Interface (RHSI). RHSI allows slower PCs such as 16 MHz 386-based computers to sustain data rates of 115.2 kbps and higher.

Cellular direct connect operation is supported by licensed firmware unique to a specific cellular phone type.

AccelerATor kits and reference designs are available to minimize application design time and costs.

FEATURES

- Data modem throughput up to 57.6 kbps
  - V.32 bis, V.32, V.22 bis, V.22A/B, V.23, and V.21; Bell 212A and 103
- RC144ACFL performs ECC in the modem
  - V.42 LAPM and MNP 2-4 error correction
  - V.42 bis and MNP 5 data compression
  - MNP 10 data throughput enhancement
  - MNP 10EC™ enhanced cellular performance
  - Cellular direct connect
- RC144ATFL supports ECC performed in the host
  - V.42 LAPM and MNP 2-4 error correction
  - V.42 bis and MNP 5 data compression
- Enhanced Rockwell Protocol Interface (RPI+) supported by WinRPI host software module
- Backward compatible with software that supports RPI
- Hayes AutoSync (option)
- Fax modem send and receive rates up to 14400 bps
  - V.17, V.29, V.27 ter, and V.21 channel 2
- Voice mode (option)
  - Enhanced ADPCM compression/decompression
  - Tone detection/generation and call discrimination
  - Concurrent DTMF detection
- Business audio mode (with parallel bus interface)
  - Record or playback mono data using 8-bit or 16-bit audio data encoding at 11.025 kHz or 7200 Hz
  - Concurrent DTMF/tone detection
- VoiceView alternating voice and data (AVD) (option)
- Rockwell High Speed Interface (RHSI)
- World-class operation (option)
  - Call progress, blacklisting, multiple countries
- AT, fax class 1, and voice/audio commands
- NVRAM directory, stored profiles, and CIS table configuration (option)
- Built-in DTE interfaces (DTE speed to 57.6 kbps)
  - Parallel 16550A UART interface
  - Serial CCITT V.24 (EIA/TIA-232-E)
- Fax and RPI data buffers
- Automatic format/speed sensing to 57.6 kbps
- Flow control and speed buffering
- Serial sync/async data; parallel async data
- Auto dial and auto answer; tone and pulse dialing
- Calling Number Delivery (Caller ID) detect
- Flexible packaging options
  - E39 MCU: One 80-pin PQFP or one 100-pin TQFP
  - P39 MCU: One 128-pin TQFP
  - MDP: One 100-pin PQFP or one 128-pin TQFP
- +5V operation; typical power consumption:

Mode	E39 MCU	P39 MCU
Operating:	345 mW	375 mW
Sleep mode:	21.0 mW	21.0 mW
Stop mode	10.8 mW	10.8 mW

Data Sheet
(Preliminary)

Order No. MD130
Rev. 1, January 24, 1995

Table 1. Modem Models and Functions

Model	ECC	Supported Functions						External Memory Required	
		Fax	MNP 10/ MNP 10EC/ Cellular &	Voice/ Business Audio	VoiceView	W-Class	Country Support	32k-Byte RAM	ROM
RC144ACFLD-x	Modem	-	S	-	-	-	US/Canada	Y	N
RC144ACFL(/A)-x	Modem	S	S	-	-	-	US/Canada	Y	N
RCV144ACFL(/A)-x	Modem	S	S	S	S	-	US/Canada	Y	N
RC144ACFLWD-x	Modem	-	S	-	-	S	Multiple	Y	128k-byte
RC144ACFLW-x	Modem	S	S	-	-	S	Multiple	Y	128k-byte
RCV144ACFLW-x	Modem	S	S	S	S	S	Multiple	Y	128k-byte
RC144ACFLWD-x	Modem	-	S	-	-	S	Single	Y	8k-byte
RC144ACFLW-x	Modem	S	S	-	-	S	Single	Y	8k-byte
RCV144ACFLW-x	Modem	S	S	S	S	S	Single	Y	8k-byte
RC144ATFLD-x	Host	-	-	-	-	-	US/Canada	N	N
RC144ATFL-x	Host	S	-	-	-	-	US/Canada	N	N
RCV144ATFL-x	Host	S	-	S	-	-	US/Canada	N	N
RC144ATFLWD-x	Host	-	-	-	-	S	Multiple	N	128k-byte
RC144ATFLW-x	Host	S	-	-	-	S	Multiple	N	128k-byte
RCV144ATFLW-x	Host	S	-	S	-	S	Multiple	N	128k-byte
RC144ATFLWD-x	Host	-	-	-	-	S	Single	N	8k-byte
RC144ATFLW-x	Host	S	-	-	-	S	Single	N	8k-byte
RCV144ATFLW-x	Host	S	-	S	-	S	Single	N	8k-byte

Notes:

1. ECC
   - Host — ECC performed by host CPU and commercially available windows software.
   - Modem — ECC performed by the modem MCU hardware and firmware.
2. Model options:
   - x — Host/DTE interface (P = Parallel host; S = Serial DTE)
   - (/A) — Optional Hayes AutoSync.
   - D — Data only (no fax).
   - V — Voice (including business audio for parallel interface)
   - W — World class support.
3. Supported functions (S = Supported; – = Not supported):
   - Fax — Fax class 1 command functions.
   - Cellular — Cellular direct connect and MNP 10/MNP 10EC functions.
   - Voice — Voice and business audio command functions.
   - VoiceView — VoiceView alternating voice and data (AVD)
   - W-Class — World class functions supporting multiple country requirements.

TECHNICAL SPECIFICATIONS

GENERAL DESCRIPTION

The modem device set, consisting of separate microcontroller (MCU) and modem data pump (MDP) devices, provides the processing core for a complete modem design. The OEM adds a two crystals, discrete components, and a digital access arrangement (DAA) and/or a cellular interface circuit to complete the modem system.

The modem is the full-featured, self-contained data/fax solution shown in Figure 1. No external microcontroller for data or fax control functions is required. Dialing, call progress, and telephone line interface functions are fully supported and controlled through the AT command set.

Data modes perform complete handshake and data rate negotiations. All tone and pattern detection required by the applicable CCITT or Bell standard are supported.

Fax modes support Group 3 fax requirements. Fax data transmission and reception performed by the modem is controlled and monitored through the fax EIA-578 Class 1 command interface. Full HDLC formatting, zero insertion/deletion, and CRC generation/checking is provided.

Both transmit and receive fax data are buffered within the modem. Data transfer to and from the DTE is flow controlled by XON/XOFF.

Modem Data Pump (MDP)

The MDP is a Rockwell RC144DPFL data/fax/voice modem data pump packaged in a 100-pin PQFP or a 128-pin TQFP. The crystal frequency is 35.2512 MHz.

As a data modem, the MDP can operate in 2-wire, full-duplex, synchronous/asynchronous modes at line rates up to 14400 bps.

As a fax modem, the MDP fully supports Group 3 facsimile send and receive speeds of 14400, 12000, 9600, 7200, 4800, or 2400 bps.

ADPCM voice processing in the MDP is supported in RC144ACFL models supporting voice commands.

Microcontroller (MCU)

The MCU is a Rockwell E39 or P39 microcomputer. The MCU performs the command processing and host interface functions. The crystal frequency is 8.064 MHz.

The MCU connects to the MDP via dedicated lines and the external bus. The MCU external bus also connects to OEM-supplied RAM (32k bytes, 70 ns) for RC144ACFL models and to OEM-supplied ROM (8k or 128k bytes, 70 ns) for W-class models.

For all models, a 256-byte or 2048-byte NVRAM can optionally be connected to the MCU over a dedicated serial interface.

E39 MCU. The E39 MCU connects to the host via a V.24 (EIA/TIA-232-E) serial interface or a parallel microcomputer bus depending on the installed MCU firmware. In parallel interface operation, the MCU can connect to a PCMCIA connector using a Rockwell PCMCIA Interface Control Adapter (PICA) device (see data sheet Order No. MD99) and a PCMCIA Card Information Structure (CIS) memory device.

The E39 MCU is packaged in an 80-pin PQFP or 100-pin TQFP.

P39 MCU. The P39 MCU performs all the functions as the E39 MCU and, in addition, incorporates a built-in PCMCIA interface and CIS memory allowing the P39 MCU to directly connect to the PCMCIA 68-pin Card Connector (socket) without requiring external PICA and CIS devices. In addition to the PCMCIA interface functions, the P39 MCU includes all the features of the E39 MCU.

The internal 512-byte CIS provides the host with PC Card specific information including card type, address range decoding capability, and control requirements to complete host link establishment with the PC card.

Four single-byte Card Configuration Registers provide the PC with the capability to configure and control the P39 MCU and receive status from the P39 MCU.

The P39 MCU is packaged in an 128-pin TQFP.

The P39 PCMCIA interface features include:

- PCMCIA interface logic and memory
  - Card Configuration Registers
  - 512-byte Card Information Structure (CIS)
  - Address decode logic
  - Digital speaker pass-through
- PCMCIA Card Configuration Registers
  - Configuration Option Register (full support)
  - Card Configuration and Status Register (full support)
  - Pin Replacement Register (RRdy/-Bsy and CRdy/-Bsy functions)
  - Extended Status Register (ReqAttn and RAEnab functions)
  - Supports the decoding for four standard COM ports in Overlapping I/O Address Mode
  - Supports Independent I/O Address Mode
- Supports unrestricted CIS Table access
- CIS Table configurable from ROM/flash memory (default) or from NVRAM (option)
- Performs power-down mode control
- Supports two ring handling methods
  - Extended Status Register
  - Ring Indicate pass-through to Status Change

MCU Firmware

MCU firmware in internal ROM performs processing of general modem control and command sets. Separate modem models support parallel host interface or serial DTE interface operation.

SUPPORTED INTERFACES

The major hardware signal interfaces of the modem device set are illustrated in Figure 1.

Parallel Host Bus Interface (E39 MCU with Parallel Host Interface Only)

A 16550A UART-compatible parallel interface is provided depending upon modem model. Eight data lines, three address lines, four control/status lines, and a reset line are supported.

In addition, a 512-byte fax data buffer and a 256-byte RPI data buffer are used to provide reliable performance in a multi-tasking environment.

DTE Serial Interface and Indicator Outputs (E39 MCU with DTE Serial Interface Only)

A V.24/EIA/TIA-232-E logic-compatible DTE serial interface is supported. A clock stop signal is also provided which can be used to turn off transmitter and receiver clocks to the DTE in asynchronous modes.

Four indicator outputs are also supported.

Built-in PCMCIA Interface (P39 MCU Only)

The built-in PCMCIA interface and CIS memory allows the P39 MCU to connect directly to the PCMCIA connector without requiring external PICA and CIS devices.

NVRAM Interface

A serial interface to an optional OEM-supplied non-volatile RAM (NVRAM) is provided. Data stored in NVRAM can take precedence over the factory default settings. A 256-byte NVRAM can store up to two user-selectable configurations and can store up to four 35-digit dial strings. When the P39 MCU is used, a 2048-byte NVRAM can also store the 512-byte CIS table (optional).

Speaker Interface

A speaker output, controlled by AT commands, is provided for an optional OEM-supplied speaker circuit.

External Bus Interface

For all models, the MCU external bus connects to the MDP. For ACFL and ACFLW models, the external bus connects to OEM-supplied 32k-byte, 70 ns RAM. For ACFLW and ATFLW models, the external bus also connects to OEM-supplied 8k-byte (single country support) or 128k-byte (multiple country support), 70 ns ROM.

This non-multiplexed bus supports eight bidirectional data lines and 17 address output lines. Read enable, write enable and chip select (MDP select, ROM select, and RAM select) outputs are also supported.

Telephone Line Interface

MCU. Wireline operation is selected when a DAA interface is indicated on the DAA/CELL input or when a cellular interface is indicated on the DAA/CELL input but no cellular firmware driver is loaded.

Four relay control outputs to the line interface are supported. These outputs may be used to control relays such as off-hook, pulse, mute, A/A1, earth, and talk/data. The MCU accepts ring signal and line current sense from the line interface.

MDP. A receive analog input, two transmit analog outputs, two relay driver outputs, and a ring signal input are supported. The relay outputs may be used to drive Caller ID and voice relays.

Cellular Phone Interface

MCU. Cellular operation is selected when a cellular interface is indicated on the DAA/CELL input and a cellular firmware driver is loaded. Signals supported are two encoded control outputs (CTRL0 and CTRL1), a bidirectional serial data line (CELDATA), a data clock input (CELCLK), a cellular busy output (CELBSY), and a cellular busy input (~CELBSY).

MDP. A receive analog input, two transmit analog outputs, two relay driver outputs, and a ring signal input are supported.

Eye Pattern Generator Interface

Eye pattern data, clock, and sync interface signals are provided to allow an external eye pattern generator circuit to be easily added in order to observe data modem performance relative to line impairments.

Microsoft Windows Interface

Rockwell High Speed Interface (RHSI). Business audio operation features data rates in excess of 115.2 kbps and requires higher DTE/DCE throughput than can be supported by the standard communications driver supplied with Microsoft Windows. The Rockwell High Speed Interface (RHSI) host software is provided to overcome these predefined communication port speed limitations and enables business audio operation. The Rockwell RHSICOMM.DRV driver replaces and is downward compatible with the standard Microsoft Windows communications driver COMM.DRV.

Enhanced Rockwell Protocol Interface (RPI+) and WinRPI Host Software Module. The RC144ATFL modem incorporates the enhanced Rockwell Protocol Interface (RPI+) and provides error correction and data compression (ECC) in conjunction with a provided host software module (WinRPI).

WinRPI allows implementation of high performance PC-based error correction and data compression with full compatibility to existing Windows-based communications applications.

The RC144ATFL with RPI+ is also backwards compatible to applications software currently shipping with Rockwell's host-based ECC module based upon the original version of the Rockwell Protocol Interface (RPI.

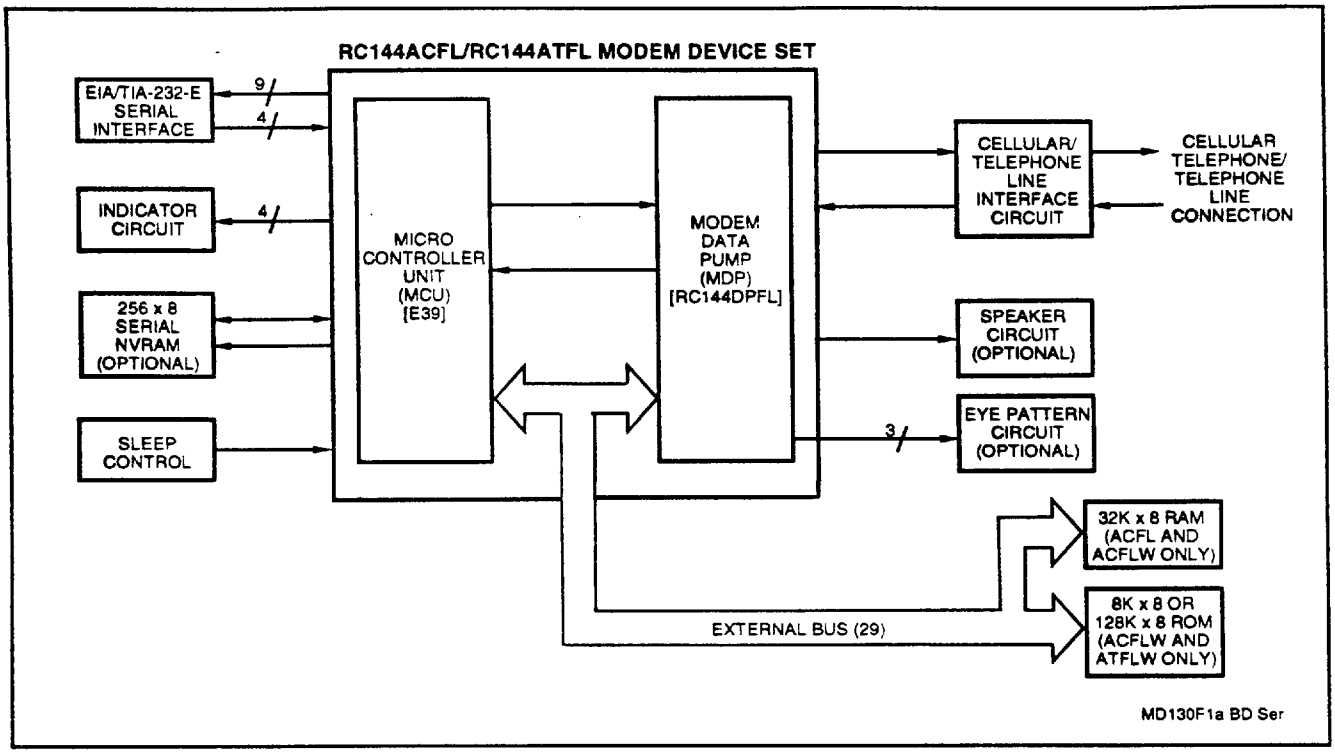


Figure 1a. Block Diagram - Serial Interface

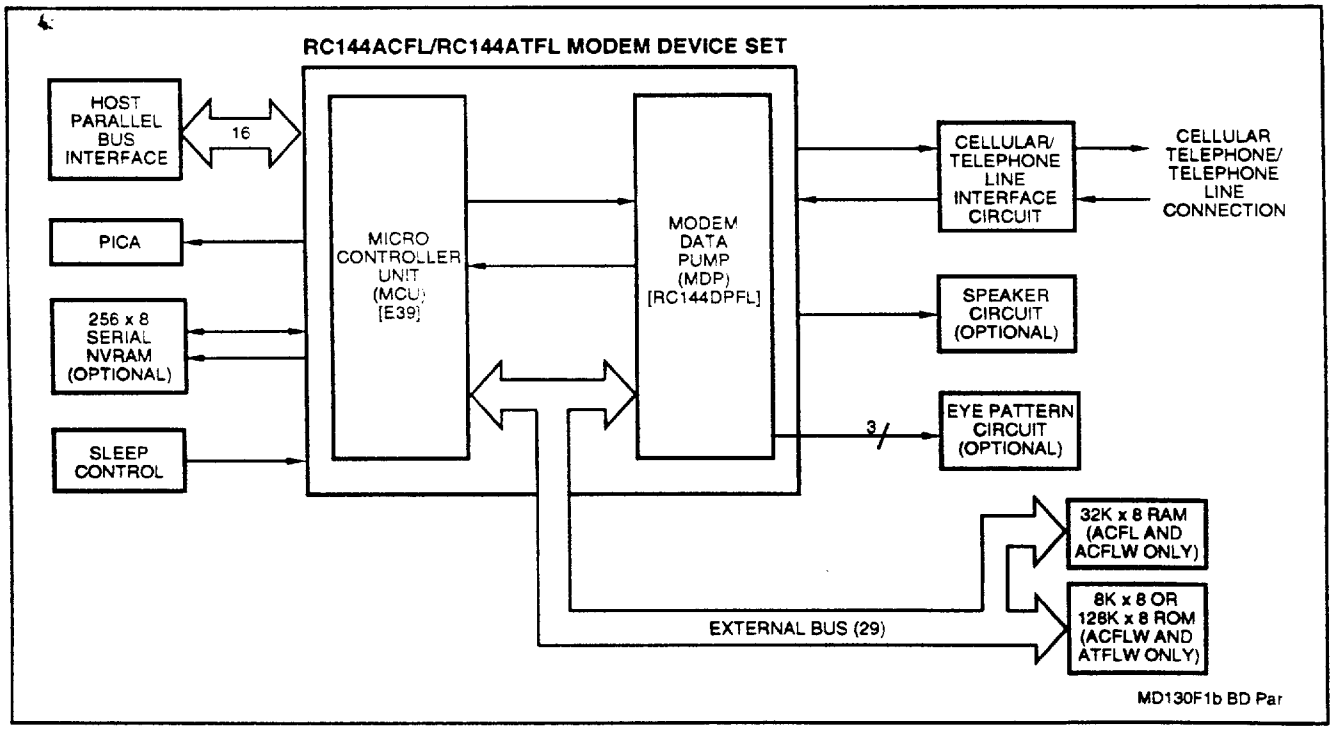


Figure 1b. Block Diagram - Parallel Interface

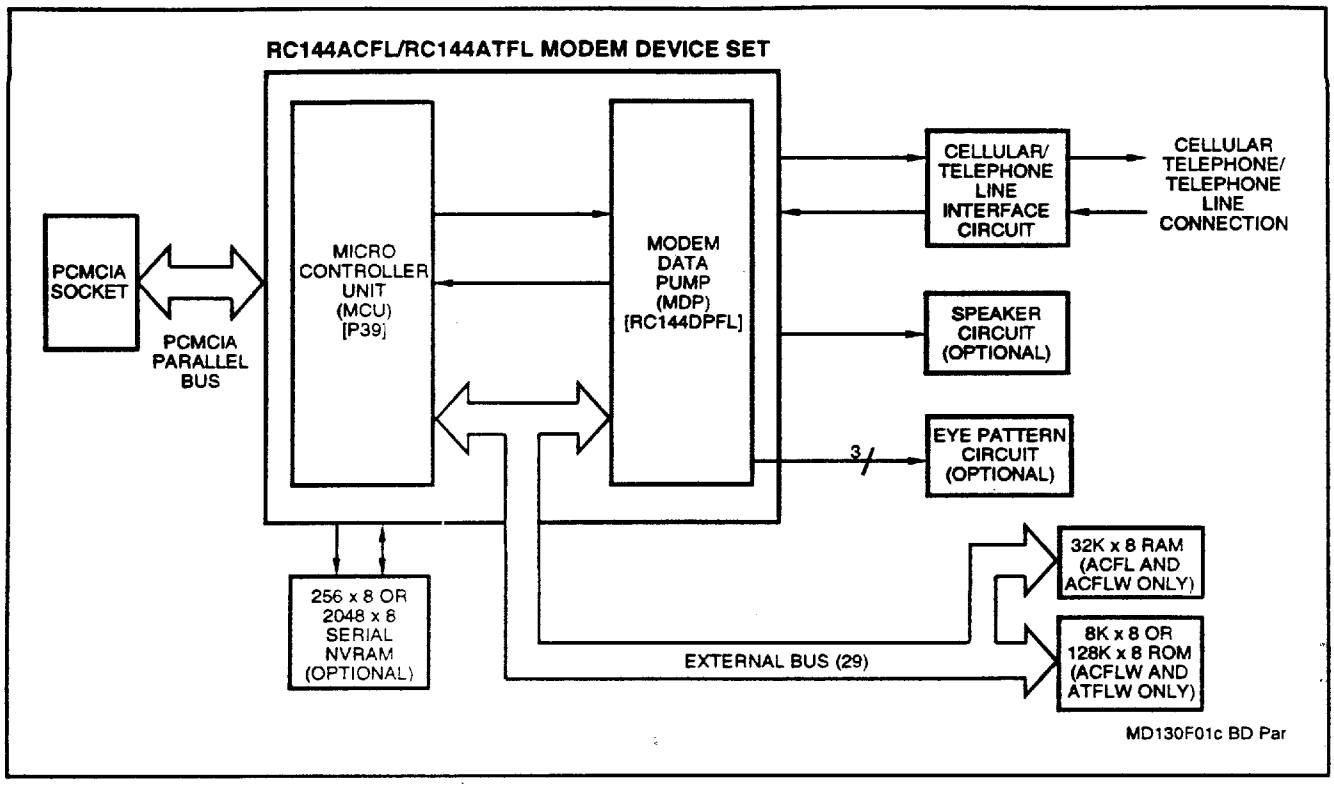


Figure 1c. Block Diagram - Parallel PCMCIA Interface

COMMANDS

The modem supports data modem, fax class 1 modem, voice/audio, MNP 10, and VoiceView commands, and S Registers in accordance with modem model options (see Tables 2 and 3, respectively).

Data Modem Operation. Data modem functions operate in response to the AT commands when +FCLASS=0. Default parameters support US/Canada operation.

MNP 10 Operation. MNP 10 functions operate in response to MNP 10 commands.

AutoSync Operation. AutoSync operates in response to the &Q4 command.

Fax Modem Operation. Fax modem functions operate in response to fax class 1 commands when +FCLASS=1 or #CLS=1.

Voice Operation. Voice mode functions operate in response to voice/audio commands when #CLS=8 and either #VBS=2 or #VBS=4 is selected.

Audio Operation. Audio mode functions operate in response to voice/audio commands when #CLS=8 and either #VBS=8 or #VBS=16 is selected.

Cellular Operation. Cellular functions operate when a cellular phone driver is loaded and a cellular phone interface is detected.

World Class (W-Class) Operation. Models supporting W-class functions operate in response to W-class AT commands.

VoiceView Operation. VoiceView alternating voice and data functions operate in response to VoiceView commands.

Table 2. AT Commands

Command	Function	ACFL/ACFLD/ ACFLW/ACFLWD	ATFL/ATFLD/ ATFLW/ATFLWD
	Basic Commands		
A/	Re-execute command	X	X
A	Answer a call	X	X
Bn	Set CCITT or Bell Mode	X	X
Cn	Carrier control	X	X
Dn	Dial (originate a call)	X	X
E	Command echo	X	X
Fn	Select line modulation	X	X
Hn	Disconnect (hang-up)	X	X
In	Identification	X	X
Ln	Speaker volume	X	X
Mn	Speaker control	X	X
Nn	Automode enable	X	X
On	Return to on-line data mode	X	X
P	Set pulse dial default	X	X
Qn	Quiet results codes control	X	X
Sn=x	Write to S Register	X	X
Sn?	Read S Register	X	X
T	Set tone dial default	X	X
Vn	Result code form	X	X
Wn	Error correction message control	X	X
Xn	Extended result codes	X	X
Yn	Long space disconnect	X	X
Zn	Soft reset and restore profile	X	X

Table 2. AT Commands (Cont'd)

Command	Function	ACFL/ACFLD/ ACFLW/ACFLWD	ATFL/ATFLD/ ATFLW/ATFLWD
&Cn	RLSD (DCD) option	X	X
&Dn	DTR option	X	X
&F	Restore factory configuration (profile)	X	X
&Gn	Select guard tone	X	X
&Jn	Telephone jack control	X	X
&Kn	Flow control	X	X
&Mn	Asynchronous/synchronous mode selection	X	X
&Pn	Select pulse dial make/break ratio	X	X
&Qn	Asynchronous/synchronous mode selection	X	X
&Rn	RTS/CTS option	X	X
&Sn	DSR override	X	X
&Tn	Test and diagnostic	X	X
&V	Display current configuration & profiles	X	X
&Wn	Store current configuration	X	X
&Xn	Select synchronous clock source	X	X
&Yn	Designate a default reset profile	X	X
&Zn=x	Store phone number	X	X
%En	Enable/disable line quality monitor	X	X
%L	Report line signal level	X	X
%Q	Report line signal quality	X	X
%TTn	PTT testing utilities	X	X
\Kn	Break control	X	X
\Nn	Operating mode	X	X
#CID	Caller ID detection and reporting	X	X
+Hn	Enable/disable RPI and DTE speed	X	X
**	Download to flash memory	X	X
	Cellular Commands		
^C2	Download Cellular Phone Driver	X	-
^I	Identify Cellular Phone Driver	X	-
^T6	Indicate Status Of Cellular Phone	X	-
T	**ECC Commands**		
%C	Select data compression	X	X
\An	Maximum MNP block size	X	-
\Bn	Transmit BREAK to remote	X	-
	MNP 10 Commands		
)Mn	Enable/disable cellular power level adjust	X	-
* Hn	Set link negotiation speed	X	-
-Kn	MNP extended services	X	-
-Qn	Enable fallback to V.22 bis/V.22	X	-
@Mn	Select initial transmit level	X	-
:E	Compromise equalizer enable	X	-
	W-Class Commands		
*B	Display blacklisted numbers	W only	W only
*D	Display delayed numbers	W only	W only
*NCnn	Country select	W only	W only

Table 2. AT Commands (Cont'd)

Command	Function	ACFL/ACFLD/ ACFLW/ACFLWD	ATFL/ATFLD/ ATFLW/ATFLWD
	Fax Class 1 Commands		
+FCLASS=n	Service class	X (except D)	X (except D)
+FAE	Data/fax auto answer	X (except D)	X (except D)
+FTS=n	Stop transmission and wait	X (except D)	X (except D)
+FRS=n	Receive silence	X (except D)	X (except D)
+FTM=n	Transmit data	X (except D)	X (except D)
+FRM=n	Receive data	X (except D)	X (except D)
+FTH=n	Transmit data with HDLC framing	X (except D)	X (except D)
+FRH=n	Receive data with HDLC framing	X (except D)	X (except D)
	Voice Commands		
#BDR	Select baud rate	V only	V only
#CLS	Select data, fax, or voice	V only	V only
#MDL?	Identify model	V only	V only
#MFR?	Identify manufacturer	V only	V only
#REV?	Identify revision level	V only	V only
#VBQ?	Query buffer size	V only	V only
#VBS	Bits per sample	V only	V only
#VBT	Beep tone timer	V only	V only
#VCI?	Identify compression method	V only	V only
#VLS	Voice line select	V only	V only
#VRA	Ringback goes away timer (originate)	V only	V only
#VRN	Ringback never came timer (originate)	V only	V only
#VRX	Voice receive mode	V only	V only
#VSD	Enable silence deletion	V only	V only
#VSK	Buffer skid setting	V only	V only
#VSP	Silence detection period (voice receive)	V only	V only
#VSR	Sampling rate selection	V only	V only
#VSS	Silence detection tuner (voice receive)	V only	V only
#VTD	DTMF/tone reporting	V only	V only
#VTS	Generate tone signals	V only	V only
#VTX	Voice transmit mode	V only	V only
	VoiceView Commands		
+FCLASS=n	Service class	V only	-
-SVV	Originate VoiceView data mode	V only	-
-SAC	Accept data mode request	V only	-
-SIP	Initialize VoiceView parameters	V only	-
-SIC	Reset capabilities data to default setting	V only	-
-SSQ	Initiate capabilities query	V only	-
-SDA	Originate modem data mode	V only	-
-SFX	Originate FAX data mode	V only	-
-SMT	Mute telephone	V only	-
-SDS	Disable switchhook status monitoring	V only	-
-SQR	Capabilities query response control	V only	-
-SCD	Capabilities data	V only	-
-SER?	Error status (read only)	V only	-
-SSP	VoiceView transmission speed	V only	-
-SSR	Start sequence response control	V only	-
+FLO	Flow control select	V only	-
+FPR	Serial port rate control	V only	-
-SSV	VoiceView data mode start sequence event	V only	-
-SFA	Facsimile data node start sequence event	V only	-
-SMD	Modem data mode start sequence event	V only	-
-SRA	Receive ADSI response event	V only	-
-SRQ	Receive capabilities query event	V only	-
-SRC:	Receive capabilities information event	V only	-
-STO	Talk-off event	V only	-

Table 3. S Registers

Register	Function	ACFL/ACFLD/ ACFLW/ACFLWD	ATFL/ATFLD/ ATFLW/ATFLWD
S0	Rings to auto-answer	X	X
S1	Ring counter	X	X
S2	Escape character	X	X
S3	Carriage return character	X	X
S4	Line feed character	X	X
S5	Backspace character	X	X
S6	Maximum time to wait for dial tone	X	X
S7	Wait for carrier	X	X
S8	Pause time for dial delay modifier	X	X
S9	Carrier detect response time	X	X
S10	Carrier loss disconnect time	X	X
S11	DTMF tone duration	X	X
S12	Escape code guard time	X	X
S13	Reserved	X	X
S14	General bit mapped options	X	X
S15	Reserved	X	X
S16	Test mode bit mapped options (&T)	X	X
S17	Reserved	X	X
S18	Test timer	X	X
S19	AutoSync Bit Mapped Options	/A or W Only	/A or W Only
S20	AutoSync HDLC Addr or BSC Sync Char	/A or W Only	/A or W Only
S21	V24/general bit mapped options	X	X
S22	Speaker/results bit mapped options	X	X
S23	General bit mapped options	X	X
S24	Sleep inactivity timer	X	X
S25	Delay to DTR (CT108) off	X	X
S26	RTS-to-CTS (CT105-to-CT106) delay	X	X
S27	General bit mapped options	X	X
S28	General bit-mapped options	X	X
S29	Flash modifier time	X	X
S30	Inactivity timer	X	X
S31	General bit-mapped options	X	X
S32	XON character	X	X
S33	XOFF character	X	X
S34-S35	Reserved	X	X
S37	Line connection speed	X	X
S38	Delay before forced hangup	X	X
S39	Flow control	X	X
S40	General bit-mapped options	X	X
S41	General bit-mapped options	X	X
S42-S45	Reserved	X	X
S91	PSTN transmit attenuation level	X	X
S92	Fax transmit attenuation level	X	X
S95	Result code messages control	X	X
	ECC S Registers		
S36	LAPM failure control	X	X
S46	Data compression control	X	X
S48	V.42 negotiation control	X	X
S82	Break handling control	X	-
S86	Call failure reason code	X	-
	Cellular Registers		
S201	Cellular transmit level	X	-

DTE SERIAL INTERFACE OPERATION

Command Mode and Data Modem Mode - Automatic Speed/Format Sensing. The modem can automatically determine the speed and format of the data sent from the DTE. The modem can sense speeds of 300, 600, 1200, 2400, 4800, 7200, 9600, 12000, 14400, 19200, 38400, and 57600 bps and the following data formats:

Parity	Data Length (No. of Bits)	No. of Stop Bits	Character Length (No. of Bits)
None	7	2	10
Odd	7	1	10
Even	7	1	10
None	8	1	10
Odd	8	1	11*
Even	8	1	11*

* 11-bit characters are sensed, but the parity bits are stripped off during data transmission in Normal and Error Correction modes. Direct mode does not strip off the parity bits.

The modem can speed sense data with mark or space parity and configures itself as follows:

DTE Configuration	Modem Configuration
7 mark	7 none
7 space	8 none
8 mark	8 none
8 space	8 even

Fax Modem Mode. The DTE to modem data rate is 19200 bps.

HOST PARALLEL BUS INTERFACE OPERATION

Command Mode and Data Modem Mode. The modem can operate at rates up to 57600 bps by programming the Divisor Latch in the parallel interface registers.

Fax Modem Mode. The host to modem data rate is 19200 bps.

ESTABLISHING DATA MODEM CONNECTIONS

Telephone Number Directory

The modem supports four telephone number entries in a directory that can be saved in a serial NVRAM. Each telephone number can be up to 35 characters in length. A telephone number can be saved using the &Zn=x command, and a saved telephone number can be dialed using the DS=n command.

Dialing

DTMF Dialing. DTMF dialing using DTMF tone pairs is supported in accordance with CCITT Q.23. The transmit tone level complies with Bell Publication 47001.

Pulse Dialing. Pulse dialing is supported in accordance with EIA/TIA-496-A.

Blind Dialing. The modem can blind dial in the absence of a dial tone if enabled by the X0, X1, or X3 command.

Modem Handshaking Protocol

If a tone is not detected within the time specified in the S7 register after the last digit is dialed, the modem aborts the call attempt.

Call Progress Tone Detection

Ringback, equipment busy, and progress tones can be detected in accordance with the applicable standard.

Answer Tone Detection

Answer tone can be detected over the frequency range of 2100 ± 40 Hz in CCITT modes and 2225 ± 40 Hz in Bell modes.

Ring Detection

A ring signal can be detected from a TTL-compatible 15.3 Hz to 68 Hz square wave input.

Billing Protection

When the modem goes off-hook to answer an incoming call, both transmission and reception of data are prevented for 2 seconds (data modem) or 4 seconds (fax adaptive answer) to allow transmission of the billing signal.

Connection Speeds

The possible data connection modes/speeds are in Table 4.

Two methods of establishing a connection are supported: use of the F command and use of N command, speed sense, and S37 register combination.

Table 4. Connection Speed Options

Configuration	Rate (bps)
V.32 bis	14400 (RC144ACFL/ATFL), 12000 (RC144ACFL/ATFL), 9600, 7200, or 4800
V.32	9600 or 4800
V.22 bis	2400 or 1200
V.22	1200
V.23	1200Tx/75Rx or 75TX/1200Rx
V.21	0-300
Bell 212A	1200
Bell 103	0-300

Automode

Automode detection can be enabled by the N1 or F0 commands to allow the modem to connect to a remote modem in accordance with EIA/TIA-PN2330.

DATA MODE

Data mode exists when a telephone line or cellular phone connection has been established between modems and all handshaking has been completed.

Speed Buffering (Normal Mode)

Speed buffering allows a DTE to send data to, and receive data from, a modem at a speed different than the line speed. The modem supports speed buffering at all line speeds.

Flow Control

DTE-to-Modem Flow Control. If the modem-to-line speed is less than the DTE-to-modem speed, the modem supports XOFF/XON or RTS/CTS flow control with the DTE to ensure data integrity.

Escape Sequence Detection

The "+++" escape sequence can be used to return control to the command mode from the data mode. Escape sequence detection is disabled by an S2 Register value greater than 127. Escape sequence detection is disabled in synchronous mode.

BREAK Detection

The modem can detect a BREAK signal from either the DTE or the remote modem. The \Kn command determines the modem response to a received BREAK signal.

Telephone Line Monitoring

GSTN Cleardown (V.32 bis, V.32). Upon receiving GSTN Cleardown from the remote modem in a non-error correcting mode, the modem cleanly terminates the call.

Loss of Carrier. If carrier is lost for a time greater than specified by the S10 register, the modem disconnects.

Receive Space Disconnect. If selected by the Y1 command in non-error-correction mode, the modem disconnects after receiving 1.6 ± 10% seconds of continuous SPACE.

Send SPACE on Disconnect

If selected by the Y1 command in non-error-correction mode, the modem sends 4 ± 10% seconds of continuous SPACE when a locally commanded hang-up is issued by the &Dn or H command.

Fall Forward/Fallback (V.32 bis/V.32)

During initial handshake, the modem will fallback to the optimal line connection within V.32 bis/V.32 mode depending upon signal quality if automode is enabled by the N1 command.

When connected in V.32 bis/V.32 mode, the modem will fall forward or fallback to the optimal line speed within V.32 bis/V.32 mode depending upon signal quality if fall forward/fallback is enabled by the %E2 command.

Retrain

The modem may lose synchronization with the received line signal under poor line conditions. If this occurs, retraining may be initiated to attempt recovery depending on the type of connection.

The modem initiates a retrain if line quality becomes unacceptable if enabled by the %E command. The modem continues to retrain until an acceptable connection is achieved, or until 30 seconds elapse resulting in line disconnect.

Programmable Inactivity Timer

The modem disconnects from the line if data is not sent or received for a specified length of time. In normal or error-correction mode, this inactivity timer is reset when data is received from either the DTE or from the line. This timer can be set to a value between 0 and 2550 seconds by using register S30. A value of 0 disables the inactivity timer.

Synchronous Data Mode (Serial Interface Only)

The modem can establish a synchronous connection in accordance with the &Mn or &Qn commands. Upon completing the physical handshake, the modem enters synchronous data mode. The inactivity timer is not used during synchronous data mode.

Direct Mode (Serial Interface Only)

The Direct mode allows data to be transmitted and received directly from the DTE and remote modem. The Direct mode is selected with the &Q0 or \N1 command. In Direct mode, no flow control characters are recognized or transmitted, the modem cannot execute error correction, and the inactivity timer is not used.

DTE Signal Monitoring (Serial Interface Only)

~DTR. When ~DTR is asserted, the modem responds in accordance with the &Dn and &Qn commands.

~RTS. ~RTS is used for flow control if enabled by the &K command in normal or error-correction mode or to affect the ~CTS output if enabled by the &R command in synchronous mode.

ERROR CORRECTION AND DATA COMPRESSION (ACFL AND ACFLW ONLY)

V.42 Error Correction

V.42 supports two methods of error correction: LAPM and, as a fallback, MNP 4. The modem provides a detection and negotiation technique for determining and establishing the best method of error correction between two modems.

MNP 2-4 Error Correction

MNP 2-4 is a data link protocol that uses error correction algorithms to ensure data integrity. Supporting stream mode, the modem sends data frames in varying lengths depending on the amount of time between characters coming from the DTE.

V.42 bis Data Compression

V.42 bis data compression mode, enabled by the %Cn command or S46 register, operates when a LAPM or MNP 10 connection is established.

The V.42 bis data compression employs a "string learning" algorithm in which a string of characters from the DTE is encoded as a fixed length codeword. Two 2k-byte dictionaries are used to store the strings. These dictionaries are dynamically updated during normal operation.

MNP 5 Data Compression

MNP 5 data compression mode, enabled by the %Cn command, operates during an MNP connection.

In MNP 5, the modem increases its throughput by compressing data into tokens before transmitting it to the remote modem, and by decompressing encoded received data before sending it to the DTE.

MNP 10 DATA THROUGHPUT ENHANCEMENT (ACFL AND ACFLW ONLY)

MNP 10 protocol, cellular functionality, and MNP Extended Services enhance performance under adverse channel conditions such as those found in rural, long distance, or cellular environments. An MNP 10 connection is established when an MNP 2-4 connection is negotiated with a remote modem supporting MNP 10. MNP 10 functions include:

Robust Auto-Reliability. A higher connection success rate is achieved by attempting to overcome channel interference during the modem negotiation phase while maintaining backward compatibility with non-MNP 10 modems.

Negotiated Speed Upshift. Initial connection and MNP handshake is performed at the most dependable speed, then the connection upshifts to the highest supported modem/channel speed. This function is particularly useful for channel conditions with high connection failure rates.

Aggressive Adaptive Packet Assembly. Frame size is dynamically changed to quickly adapt to varying levels of interference.

Dynamic Speed Shifting. Connection speed is shifted upward or downward to optimize data throughput for the channel conditions by continuously monitoring the line quality and link performance.

Dynamic Transmit Level Adjustment (DTLA). When enabled by the)M1 command, transmit level is dynamically adjusted to adapt to the varying cellular network environment, and to prevent "clipping" which causes data corruption due to the Preemphasis and Compander effect.

MNP Extended Services. The modem can revert from V.42 bis/LAPM operation to MNP operation when MNP extended services is enabled by the local and remote modems.

MNP 10EC™ ENHANCED CELLULAR CONNECTION (ACFL AND ACFLW ONLY)

A traditional landline modem, when used for high-speed cellular data transmission, typically encounters frequent signal interference and degradation in the connection due to the characteristics of the analog cellular network. In this case, cellular-specific network impairments, such as non-linear distortion, fading, hand-offs, and high signal-to-noise ratio, contribute to an unreliable connection and lower data transfer performance. Implementations relying solely on protocol layer methods, such as MNP 10, generally cannot compensate for the landline modem's degraded cellular channel performance.

The RC144ACFL/RC144ATFL modem achieves higher cellular performance by implementing enhanced cellular connection techniques at both the physical and protocol layers, depending on modem model. The RC144DPFL MDP, used in all RC144ACFL/RC144ATFL modem models, enhances the physical layer within the modulation by optimizing its responses to sudden changes in the cellular connection. For the RC144ACFL/ACFLW modem models, the MNP 10EC protocol layer implemented in the MCU firmware improves data error identification/correction and maximizes data throughput by dynamically adjusting speed and packet size based on signal quality and data error performance.

AUTOSYNC

Hayes AutoSync mode, when used with communications software incorporating the Hayes Synchronous Interface (HSI), provides synchronous communication capabilities from an asynchronous data terminal. In AutoSync, the modem places the call asynchronously then automatically switches to synchronous operation once the telephone connection has been established. AutoSync allows communication from an asynchronous DTE (typically a personal computer) to synchronous DTE (typically a mainframe computer or minicomputer).

FAX CLASS 1 OPERATION

The modem operates as a facsimile (fax) DCE whenever the +FCLASS=1 command is active. In the fax mode, the on-line behavior of the modem is different from the data (non-fax) mode. After dialing, modem operation is controlled by fax commands. Some AT commands are still valid but may operate differently than in data modem mode.

Calling tone is generated in accordance with T.30.

VOICE/AUDIO MODE

Voice and audio functions are supported by the Voice Mode. Voice Mode includes three submodes: Online Voice Command Mode, Voice Receive Mode, and Voice Transmit Mode (Table 2).

Online Voice Command Mode. This mode results from the connection to the telephone line or a voice/audio I/O device (e.g., microphone, speaker, or handset) through the use of the #CLS=8 and #VLS commands. After mode entry, AT commands can be entered without aborting the connection.

Voice Receive Mode. This mode is entered when the #VRX command is active in order to record voice or audio data input at the RXA pin, typically from a microphone/handset or the telephone line.

Received analog voice samples are converted to digital form and compressed for reading by the host. AT commands control the codec bits-per-sample rate and, optionally, select silence deletion including silence detection period adjustment.

Received analog mono audio samples are converted to digital form and formatted into 8-bit unsigned linear PCM or 16-bit signed linear PCM format for reading by the host. AT commands control the bit length and sampling rate. Concurrent DTMF/tone detection is available at the 7200 Hz sample rate.

Voice Transmit Mode. This mode is entered when the #VTX command is active in order to playback voice or audio data to the TXA1/TXA2 output pins, typically to a speaker/handset or to the telephone line.

Digitized voice data is decompressed and converted to analog form at the original compression quantization sample-per-bits rate then output to the TXA1/TXA2 pins. Optional silence interpolation is enabled if silence deletion was selected for voice compression.

Digitized audio data is converted to analog form then output to the TXA1/TXA2 pins.

VOICEVIEW

Voice and data can alternately sent and received in a time-multiplexed fashion over the telephone line whenever the +FCLASS=80 command is active. This command and other VoiceView commands embedded in host communications software control modem operation. Most VoiceView commands use an extended syntax starting with the characters "-S", which signifies the capability to switch between voice and data.

CALLER ID

Caller ID can be enabled/disabled using the #CID command. When enabled, caller ID information (date, time, caller code, and name) can be passed to the DTE in formatted or unformatted form. Inquiry support allows the current caller ID mode and mode capabilities of the modem to be retrieved from the modem.

CELLULAR DIRECT CONNECT

In US models, the modem provides defined hardware and firmware interfaces for connection to a cellular telephone. The modem controls downloading and execution of a cellular phone driver firmware into MCU RAM to support direct connection to a cellular phone. Different drivers are required to support different cellular phones or phone models as required by the phone manufacturer.

Cellular Interface Signals

The following MCU ports are assigned to cellular phone interface signals:

MCU Port	Cellular Use		Non-Cellular Use	
	Signal	I/O	DTE Serial Interface	Host Parallel Interface
PE0	CTRL0	O	~OH	~OH
PE1	CTRL1	O	~PULSE	~PULSE
PE2	CELBSY	O	~MUTE, ~A/A1	~MUTE, ~A/A1
PE5	CELDATA	I/O	~CLKSTOP	None
PE7	DAA/CELL	I	IDID*	IDID*
PA3	~CELBSY	I	None	None
PA4	CELCLK	I	None	None
* Used during reset initialization only.				

Support for these signals is supplied by the cellular driver. When the cellular driver is loaded and a cellular phone interface is indicated on the DAA/CELL input line, the cellular signals are used instead of the wireline signals assigned to the same lines. When the cellular driver is not loaded or when a cellular phone interface is not indicated on the DAA/CELL line when a cellular driver is loaded, the wireline signals are supported.

The cellular and wireline signals are supported in an AccelerATor Kit design and are routed to a standard 15-pin connector which connects to a cable from the cellular phone.

Cellular AT Commands

The modem supports three cellular AT commands that can be used to load the cellular driver and to provide cellular phone identification and status.

^C2 - Download Cellular Phone Driver. The ^C2 command initiates download of the cellular phone driver into MCU RAM.

^I - Identify Cellular Phone Driver. The ^I command. reports the identification of the loaded cellular phone driver.

^T6 - Indicates Status Of Cellular Phone. The ^T6 command reports the status of the cellular phone connection to the modem. Status such as phone receiving an incoming call, phone in use, phone locked, no phone service, phone powered on, driver initialized, and cellular cable detected is reported.

The information obtained by issuing the ^T6 can be used to determine if the loading of the cellular phone driver is necessary by the host software. Download of the cellular phone driver is not required if a cellular interface cable is not connected to the modem (DAA/CELL = high). A download is necessary when a cellular cable is detected (DAA/CELL = low), which implies a cellular phone is also connected, before operation of the phone. Once a driver is downloaded, the modem can operate in wireline mode or cellular mode based on the connection of a cellular cable.

Operation

Once the cellular driver is loaded and the modem is connected to the cellular phone and the phone is powered on, dial/answer functions will be routed through the phone instead of the wireline DAA. No special commands are needed to place or answer cellular calls and the same AT commands and software packages that are used for wireline communication sessions can be used. If a V.42 bis connection is established in wireline mode, the cellular phone driver is removed from MCU RAM so that the V.42 bis dictionaries can be increased to their full size.

Result Messages

While the modem is being used with a cellular phone, result messages are changed from wireline operation status to reflect cellular operation status as follows:

NO DIALTONE - Indicates that cellular service is not currently available or the cellular phone is powered off.

RING - Indicates that the cellular phone is receiving an incoming call.

WORLD CLASS COUNTRY SUPPORT (ACFLW AND ATFLW ONLY)

The W-class models include functions which support modem operation in multiple countries. The following capabilities are provided in addition the data modem functions previously described. Country dependent parameters are all programmable by ConfigurACE.

Dialing

Dial Tone Detection. Dial tone detection levels and frequency ranges are programmable by ConfigurACE.

DTMF Dialing. Transmit output level, DTMF signal duration, and DTMF interdigit interval parameters are programmable by ConfigurACE.

Pulse Dialing. Parameters such as make/break times, set/clear times, and dial codes are programmable by ConfigurACE.

Ring Detection. The frequency range is programmable by ConfigurACE.

Blind Dialing. Blind dialing may be disabled by ConfigurACE.

Carrier Transmit Level

The carrier transmit level can be programmed through S91 for data and S92 for fax. The maximum, minimum, and default values can be defined by ConfigurACE to match specific country and DAA requirements.

Calling Tone

Calling tone is generated in accordance with V.25. Calling tone may be toggled (enabled/disabled) by inclusion of a "^" character in a dial string. It may also be disabled by programming a country specific parameter using ConfigurACE.

Call Progress Tone Detection

Frequency and cadence of tones for busy, ringback, congested, dial tone 1, and dial tone 2 are programmable by ConfigurACE.

Answer Tone Detection

The answer tone detection period is programmable by ConfigurACE.

Blacklist Parameters

The modem can operate in accordance with requirements of individual countries to prevent misuse of the network by limiting repeated calls to the same number when previous call attempts have failed. Call failure can be detected for reasons such as no dial tone, number busy, no answer, no ringback detected, voice (rather than modem) detected, and key abort (dial attempt aborted by user). Actions resulting from such failures can include specification of minimum inter-call delay, extended delay between calls, and maximum numbers of retries before the number is permanently forbidden ("blacklisted"). Up to six such numbers may be tabulated. The blacklist parameters are established by ConfigurACE.

Relay Control

On-hook/off-hook, make/break, and set/clear relay control parameters are programmable by ConfigurACE.

DIAGNOSTICS

Commanded Tests

Diagnostics are performed in response to &T commands per V.54.

Analog Loopback (&T1 Command). Data from the local DTE is sent to the modem, which loops the data back to the local DTE.

Analog Loopback with Self Test (&T8 Command). An internally generated test pattern of alternating 1s and 0s (reversals) is sent to the modem. An error detector within the modem checks for errors in the string of reversals.

Remote Digital Loopback (RDL) (&T6 Command). Data from the local DTE is sent to the remote modem which loops the data back to the local DTE.

Remote Digital Loopback with Self Test (&T7 Command). An internally generated pattern is sent from the local modem to the remote modem, which loops the data back to the local modem.

Local Digital Loopback (&T3 Command). When local digital loop is requested by the local DTE, two data paths are set up in the local modem. Data from the local DTE is looped back to the local DTE (path 1) and data received from the remote modem is looped back to the remote modem (path 2).

Power On Reset Tests

Upon power on or receipt of the Z command, the modem performs tests of the MDP, RAM, ROM, and NVRAM.

If a MDP, RAM, or ROM test fails, the ~TMIND output is pulsed (serial interface version) or the DCD bit in the parallel interface register is pulsed (parallel interface version) as follows:

RAM test fails: One pulse every two seconds.
ROM test fails: Two pulses every two seconds.
MDP test fails: Three pulses every two seconds.

If the NVRAM test fails (due to NVRAM failure or if NVRAM is not installed), the test failure is reported by AT commands that normally use the NVRAM, e.g., the &V command.

LOW POWER SLEEP AND STOP MODES

Sleep Mode Entry. The modem enters the low power *sleep mode when no line* connection exists and no host activity occurs for the period of time specified in the S24 register. All MCU circuits are turned off except the internal MCU clock circuitry in order to consume reduced power while being able to immediately wake up and resume normal operation.

Stop Mode Entry. The modem enters the low power stop mode when the ~STPMODE input is asserted. All MCU circuits are turned off including the internal MCU clock circuitry in order to consume lower power than sleep mode. The modem will enter stop mode immediately, terminating a line connection, terminating any test in process, and allowing any data in the Receive Buffer Register to clear.

~STPMODE must be returned high before the modem can wake-up.

Wake-up. Wakeup occurs when a ring is detected on the telephone line, the host writes to the modem (parallel interface version), or the DTE sends a character to the modem (serial interface version). Since the modem requires more time to attain normal operation when waking up from stop mode than sleep mode, the host must send any character to the modem before issuing the first AT command.

ADDITIONAL INFORMATION

Additional information is described in the RC144ACFL Designer's Guide (Order No. 1052) and in the AT Command Reference Manual (Order No. 883).

CONFIGURACE UTILITY PROGRAM

The PC-based ConfigurACE utility program allows the OEM to customize the modem firmware for external ROM models to suit specific application and country requirements. ConfigurACE allows programming of functions such as:

- Loading of multiple sets of country parameters
- Loading of NVRAM factory profiles
- Call progress and blacklisting parameters
- Entry of S register maximum/minimum values
- Limitation of transmit levels
- Modification of result codes
- Modification of factory default values
- Customization of the ATI4 response
- Customization of fax OEM messages

This program modifies the hex object code which can be programmed directly into the system EPROM. Lists of the generated parameters can be displayed or printed.

Rockwell-provided country parameter files allow a complete set of country-specific call progress and blacklisting parameters to be selected.

HARDWARE INTERFACES

The modem hardware interface signals for the DTE seri interface using the E39 MCU is shown in Figure 2.

The modem hardware interface signals for the host parallel interface using the E39 MCU is shown in Figure 3.

The modem hardware interface signals for PCMCIA interface using the P39 MCU is shown in Figure 4.

The E39 MCU pin assignments for the 80-pin PQFP are shown in Figure 5 and are listed in Table 5.

The E39 MCU pin assignments for the 100-pin TQFP are shown in Figure 6 and are listed in Table 6.

The P39 MCU pin assignments for the 128-pin TQFP are shown in Figure 7 and are listed in Table 7.

The MDP pin assignments for the 100-pin PQFP are shown in Figure 8 and are listed in Table 8.

The MDP pin assignments for the 128-pin TQFP are shown in Figure 9 and are listed in Table 9.

The MCU hardware interface signals are defined in Table 10.

The MDP hardware interface signals are defined in Table 11.

The digital electrical characteristics for the hardware interface signals are listed in Table 12.

The analog electrical characteristics for the hardware interface signals are listed in Table 13.

The current and power requirements are listed in Table 14

The absolute maximum ratings are listed in Table 15.

Table 16 shows the parallel interface registers and the corresponding bit assignments.

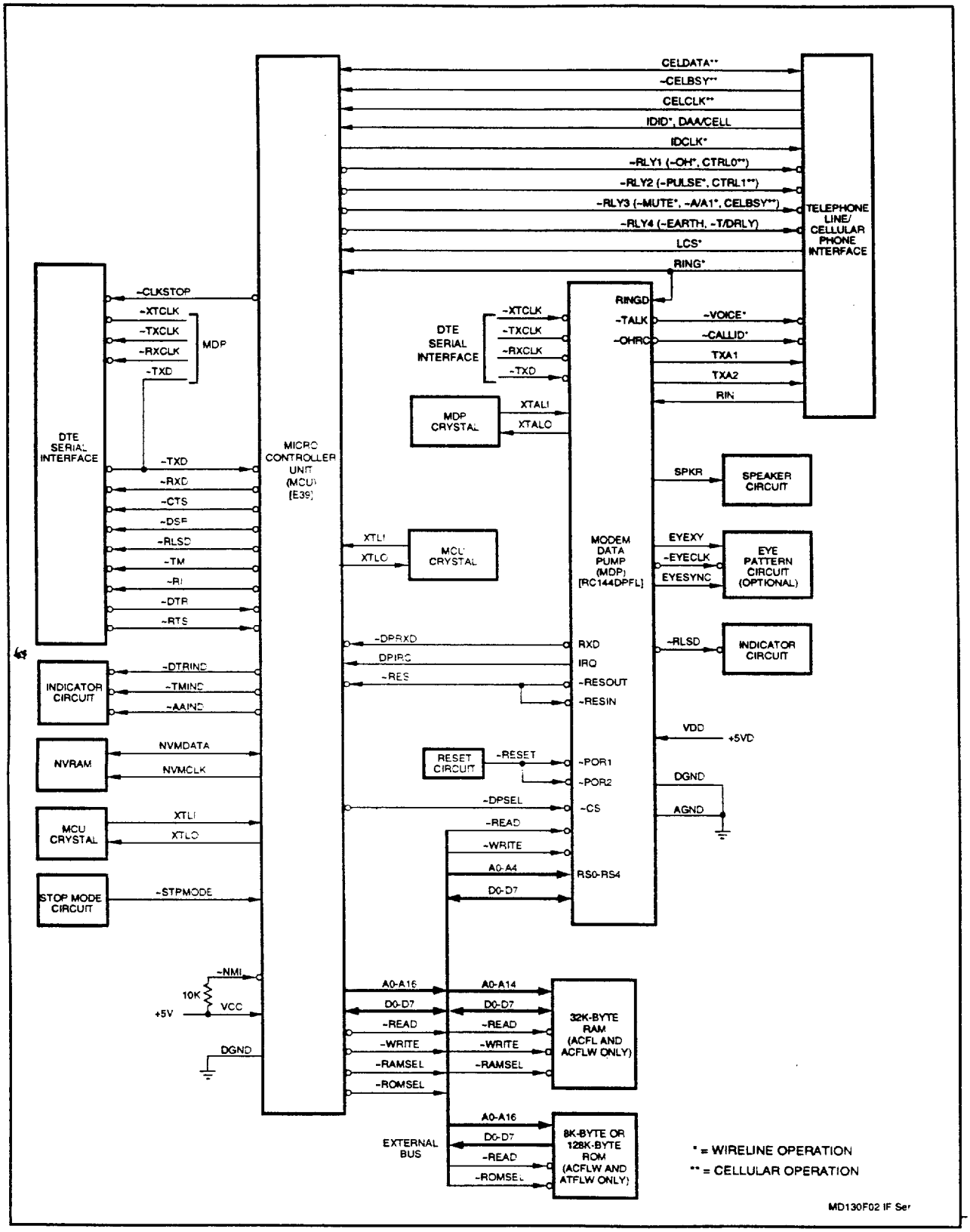


Figure 2. Hardware Interface Signals - Serial Interface

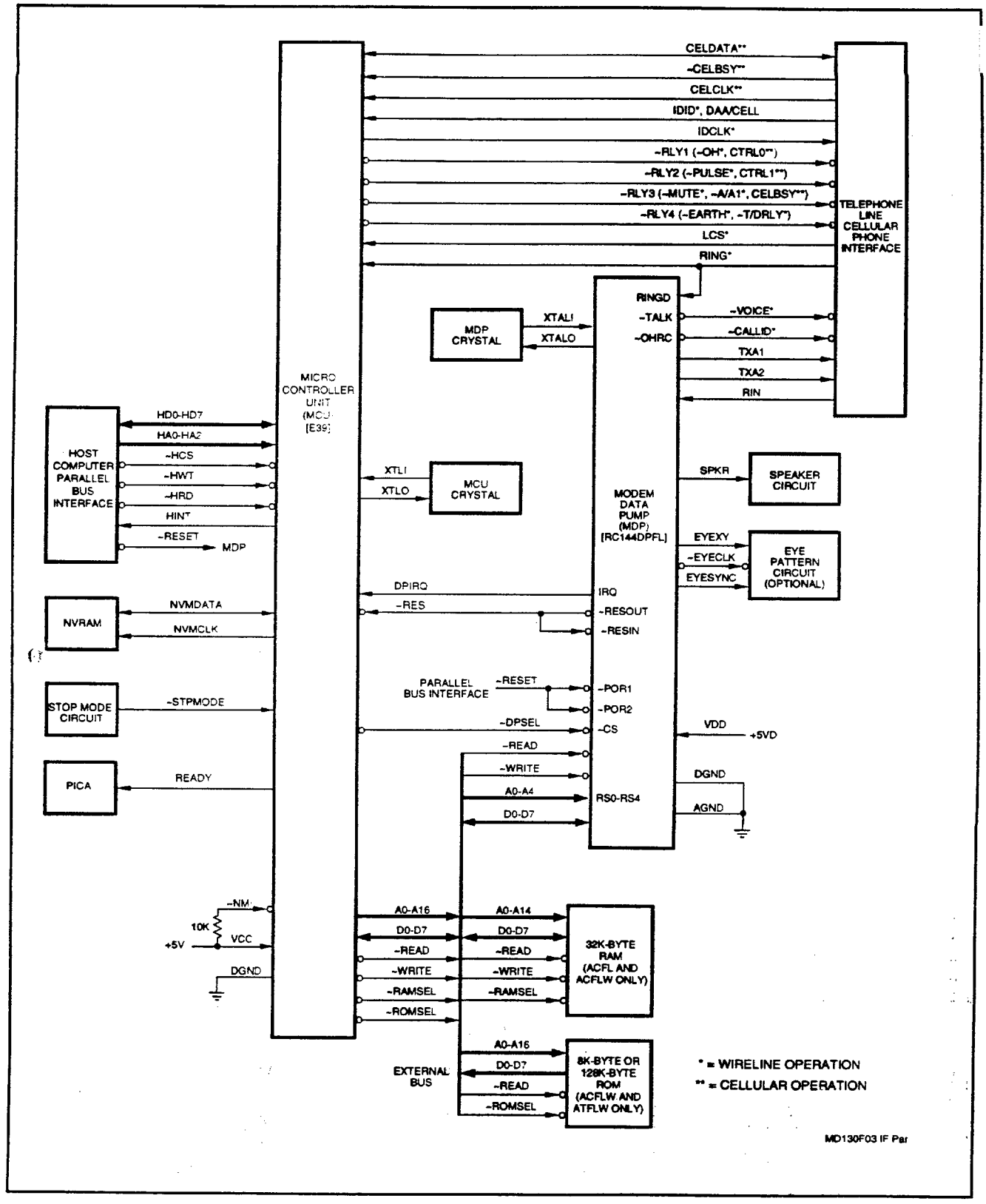


Figure 3. Hardware Interface Signals - Parallel Interface

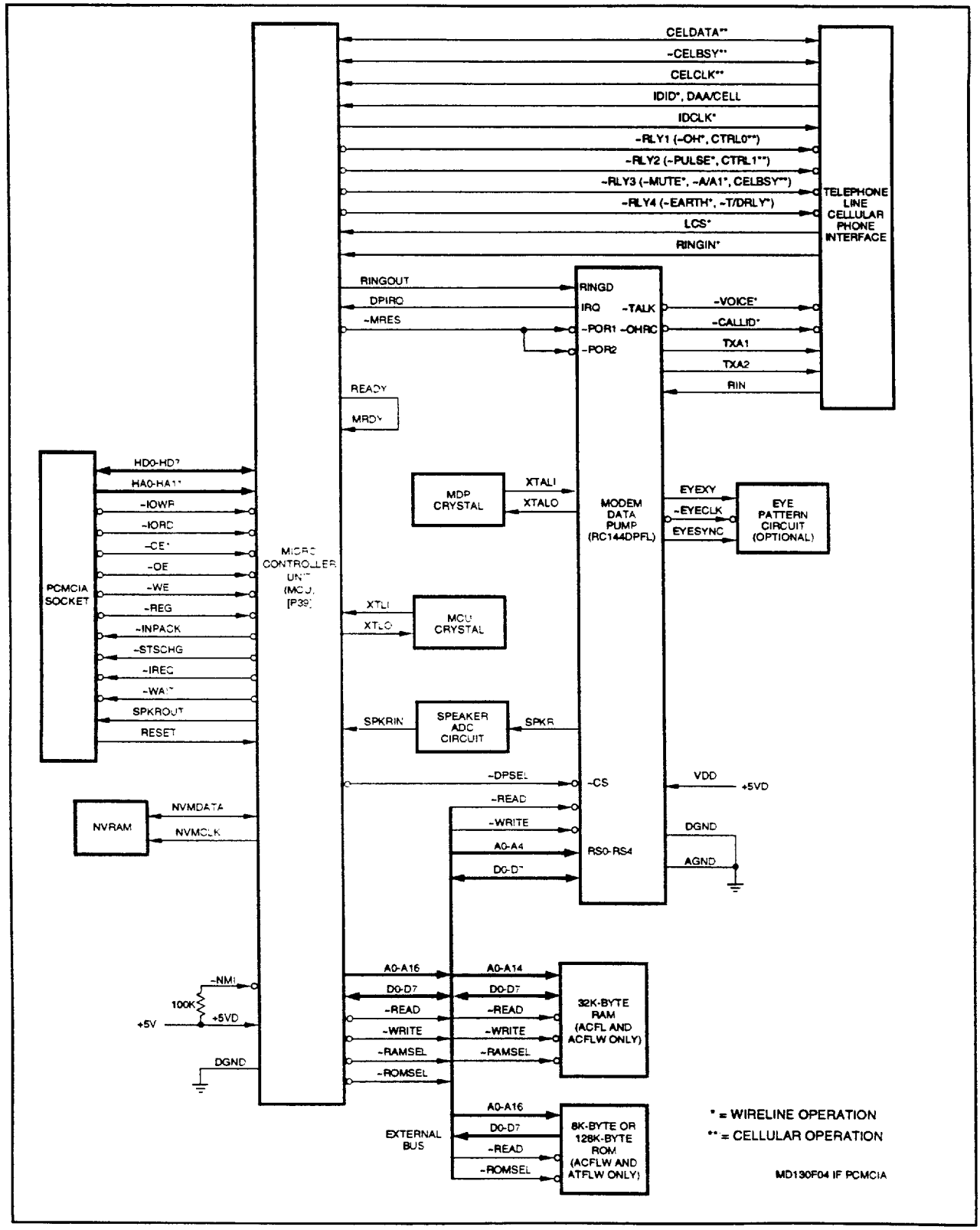


Figure 4. Hardware Interface Signals - PCMCIA Interface

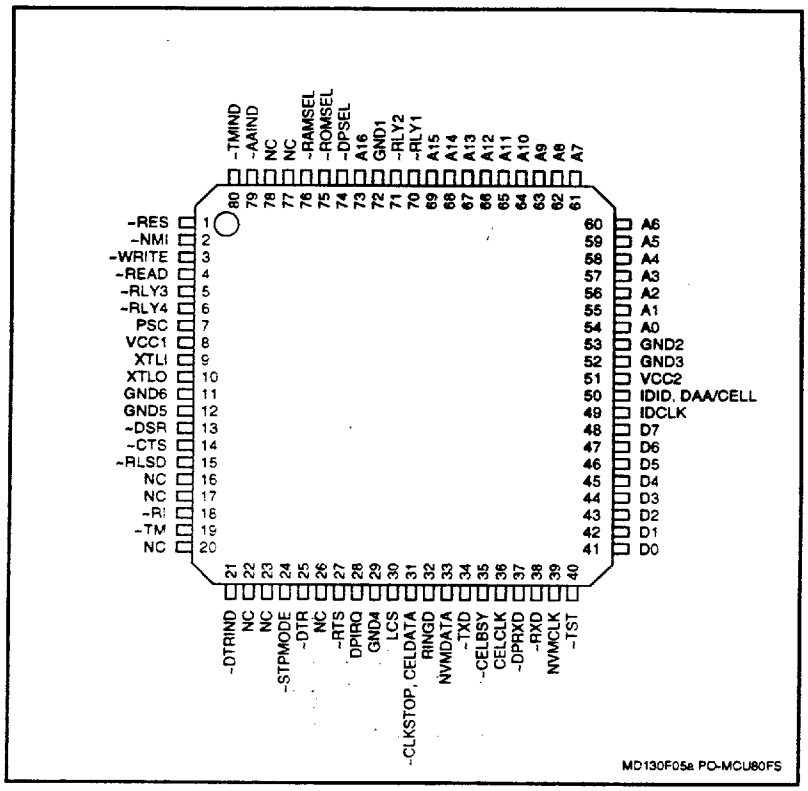


Figure 5a. E39 MCU Pin Signals- 80-Pin PQFP - Serial Interface

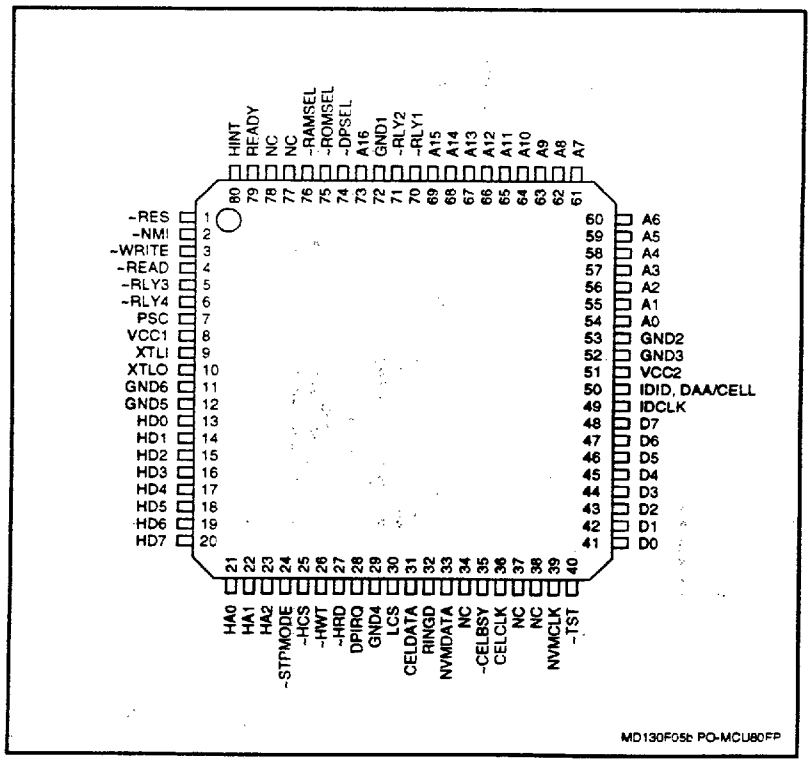


Figure 5b. E39 MCU Pin Signals- 80-Pin PQFP - Parallel Interface

Table 5a. E39 MCU Pin Signals - 80-Pin PQFP - Serial Interface

Pin	Signal Label	I/O Type	Interface	Pin	Signal Label	I/O Type	Interface
1	~RES	IC	MDP: ~RESOUT	41	D0	IA/OA	EB: D0
2	~NMI	MI	Note 4	42	D1	IA/OA	EB: D1
3	~WRITE	OA	EB: ~WRITE	43	D2	IA/OA	EB: D2
4	~READ	OA	EB: ~READ	44	D3	IA/OA	EB: D3
5	(PE2) ~RLY3	OA	WL: DAA: A/A1, ~MUTE, Cellular: CELBSY	45	D4	IA/OA	EB: D4
6	(PE3) ~RLY4	OA	WL: DAA: ~T/DRLY, ~EARTH	46	D5	IA/OA	EB: D5
7	PSC	IA	NC	47	D6	IA/OA	EB: D6
8	VCC1	PWR	VCC	48	D7	IA/OA	EB: D7
9	XTLI	IE	Crystal/Clock Circuit	49	(PE6) IDCLK	OA	WL: DAA: IDCLK
10	XTLO	OE	Crystal/Clock Circuit	50	(PE7) IDID Cellular: DAA/CELL	IA	WL: DAA: IDID Cellular: DAA/CELL
11	GND6	GND	GND	51	VCC2	PWR	VCC
12	GND5	GND	GND	52	GND3	GND	GND
13	(PC0) ~DSR	OA	DTE IF: ~DSR	53	GND2	GND	GND
14	(PC1) ~CTS	OA	DTE IF: ~CTS	54	A0	OA	EB: A0
15	(PC2) ~RLSD	OA	DTE IF: ~RLSD	55	A1	OA	EB: A1
16	(PC3) NC		NC	56	A2	OA	EB: A2
17	(PC4) NC		NC	57	A3	OA	EB: A3
18	(PC5) ~RI	OA	DTE IF: ~RI	58	A4	OA	EB: A4
19	(PC6) ~TM	OA	DTE IF: ~TM	59	A5	OA	EB: A5
20	(PC7) NC		NC	60	A6	OA	EB: A6
21	(PD0) ~DTRIND	OA	Indicator Circuit	61	A7	OA	EB: A7
22	(PD1) NC		NC	62	A8	OA	EB: A8
23	(PD2) NC		NC	63	A9	OA	EB: A9
24	(PD3) ~STPMODE	IA	Stop Mode Circuit	64	A10	OA	EB: A10
25	(PD4) ~DTR	IA	DTE IF: ~DTR	65	A11	OA	EB: A11
26	(PD5) NC		NC	66	A12	OA	EB: A12
27	(PD6) ~RTS	IA	DTE IF: ~RTS	67	A13	OA	EB: A13
28	(PD7) DPIRQ	IA	MDP: IRQ	68	A14	OA	EB: A14
29	GND4	GND	GND	69	A15	OA	EB: A15
30	(PE4) WL: LCS	IA	WL: DAA: LCS	70	(PE0) ~RLY1	OA	WL: DAA: ~OH Cellular: CTRL0
31	(PE5) WL: ~CLKSTOP Cellular: CELDATA	OA IA/OA	WL: DTE IF: ~CLKSTOP Cellular: CELDATA	71	(PE1) ~RLY2	OA	WL: DAA: ~PULSE Cellular: CTRL1
32	(PA0) RINGD	IA	DAA : RINGD	72	GND1	GND	GND
33	(PA1) NVMDATA	IA/OA	NVRAM: SDA (Note 4)	73	(PB0) A16	OA	EB: A16
34	(PA2) ~TXD	IA	DTE IF: ~TXD	74	(PB1) ~DPSEL	OA	EB: MDP: ~CS
35	(PA3) ~CELBSY	IA	Cellular: ~CELBSY	75	(PB2) ~ROMSEL	OA	EB: ROM: ~CE
36	(PA4) CELCLK	IA	Cellular: CELCLK	76	(PB3) ~RAMSEL	OA	EB: RAM: ~CS
37	(PA5) ~DPRXD	MI	MDP: RXD	77	(PB4) NC	OA	NC
38	(PA6) ~RXD	OA	DTE IF: ~RXD	78	(PB5) NC	OA	NC
39	(PA7) NVMCLK	OA	NVRAM: SCL	79	(PB6) ~AAIND	OA	Indicator Circuit
40	~TST	MI	NC (Note 5)	80	(PB7) ~TMIND	OA	Indicator Circuit

Notes:

1. I/O types:
   - MI = Modem interconnect.
   - IA, IB, IC, IE = Digital input.
   - OA, OB, OE = Digital output.
2. NC = No external connection.
3. NU = Not used; connect as noted.
4. Connect to VCC through 10K ohms.
5. Leave open to allow internal MCU ROM use; connect to GND through 10K ohms to force external ROM use only.
6. Connect to GND through 10K ohms.
7. Connect to GND through 100K ohms.

Table 5b. E39 MCU Pin Signals- 80-Pin PQFP - Parallel Interface

Pin	Signal Label	Type	Interface	Pin	Signal Label	Type	Interface
1	~RES	IC	MDP: ~RESOUT	41	D0	IA/OA	EB: D0
2	~NMI	MI	Note 4	42	D1	IA/OA	EB: D1
3	~WRITE	OA	EB: ~WRITE	43	D2	IA/OA	EB: D2
4	~READ	OA	EB: ~READ	44	D3	IA/OA	EB: D3
5	(PE2) ~RLY3	OA	WL: DAA: A/A1, ~MUTE Cellular: CELBSY	45	D4	IA/OA	EB: D4
6	(PE3) ~RLY4	OA	WL: DAA: ~T/DRLY, ~EARTH	46	D5	IA/OA	EB: D5
7	PSC	IA	NC	47	D6	IA/OA	EB: D6
8	VCC1	PWR	VCC	48	D7	IA/OA	EB: D7
9	XTLI	IE	Crystal/Clock Circuit	49	(PE6) IDCLK	OA	WL: DAA: IDCLK
10	XTLO	OE	Crystal/Clock Circuit	50	(PE7) IDID Cellular: DAA/CELL	IA	WL: DAA: IDID Cellular: DAA/CELL
11	GND6	GND	GND	51	VCC2	PWR	VCC
12	GND5	GND	GND	52	GND3	GND	GND
13	(PC0) HD0	IA/OA	HB: HD0	53	GND2	GND	GND
14	(PC1) HD1	IA/OA	HB: HD1	54	A0	OA	EB: A0
15	(PC2) HD2	IA/OA	HB: HD2	55	A1	OA	EB: A1
16	(PC3) HD3	IA/OA	HB: HD3	56	A2	OA	EB: A2
17	(PC4) HD4	IA/OA	HB: HD4	57	A3	OA	EB: A3
18	(PC5) HD5	IA/OA	HB: HD5	58	A4	OA	EB: A4
19	(PC6) HD6	IA/OA	HB: HD6	59	A5	OA	EB: A5
20	(PC7) HD7	IA/OA	HB: HD7	60	A6	OA	EB: A6
21	(PD0) HA0	IA	HB: HA0	61	A7	OA	EB: A7
22	(PD1) HA1	IA	HB: HA1	62	A8	OA	EB: A8
23	(PD2) HA2	IA	HB: HA2	63	A9	OA	EB: A9
24	(PD3) ~STPMODE	IA	Stop Mode Circuit	64	A10	OA	EB: A10
25	(PD4) ~HCS	IA	HB: ~CS	65	A11	OA	EB: A11
26	(PD5) ~HWT	IA	HB: ~WT	66	A12	OA	EB: A12
27	(PD6) ~HRD	IA	HB: ~RD	67	A13	OA	EB: A13
28	(PD7) DPIRQ	IA	MDP: IRQ	68	A14	OA	EB: A14
29	GND4	GND	GND	69	A15	OA	EB: A15
30	(PE4) WL: LCS	IA	WL: DAA: LCS	70	(PE0) ~RLY1	OA	WL: DAA: ~OH Cellular: CTRL0
31	(PE5) CELDATA	IA/OA	Cellular: CELDATA	71	(PE1) ~RLY2	OA	WL: DAA: ~PULSE Cellular: CTRL1
32	(PA0) RINGD	IA	PIF: DAA: RINGD; PCMCIA: PICA: RINGOUTB	72	GND1	GND	GND
33	(PA1) NVMDATA	IA/OA	NVRAM: SDA (Note 4)	73	(PB0) A16	OA	EB: A16
34	(PA2) NC		NC	74	(PB1) ~DPSEL	OA	EB: MDP: ~CS
35	(PA3) ~CELBSY	IA	Cellular: ~CELBSY	75	(PB2) ~ROMSEL	OA	EB: ROM:: ~CE
36	(PA4) CELCLK	IA	Cellular: CELCLK	76	(PB3) ~RAMSEL	OA	EB: RAM: ~CS
37	(PA5) NC		NC	77	(PB4) NC	OA	NC
38	(PA6) NC		NC	78	(PB5) NC	OA	NC
39	(PA7) NVMCLK	OA	NVRAM: SCL	79	(PB6) READY	OA	PICA: MRDY
40	~TST	MI	NC (Note 5)	80	(PB7) HINT	OA	HB: HINT

Notes:

1. I/O types:
   - MI = Modem interconnect.
   - IA, IB, IE = Digital input.
   - OA, OB, OE = Digital output.
2. NC = No external connection.
3. NU = Not used; connect as noted.
4. Connect to VCC through 10K ohms.
5. Leave open to allow internal MCU ROM use; connect to GND through 10K ohms to force external ROM use only.
6. Connect to HB: RESET through inverter.

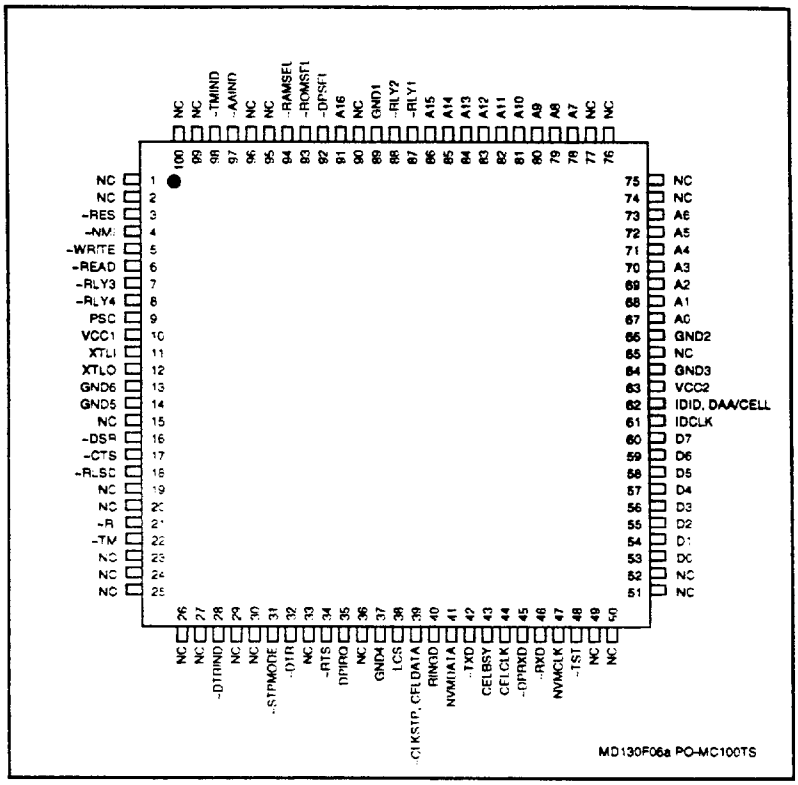


Figure 6a. E39 MCU Pin Signals- 100-Pin TQFP - Serial Interface

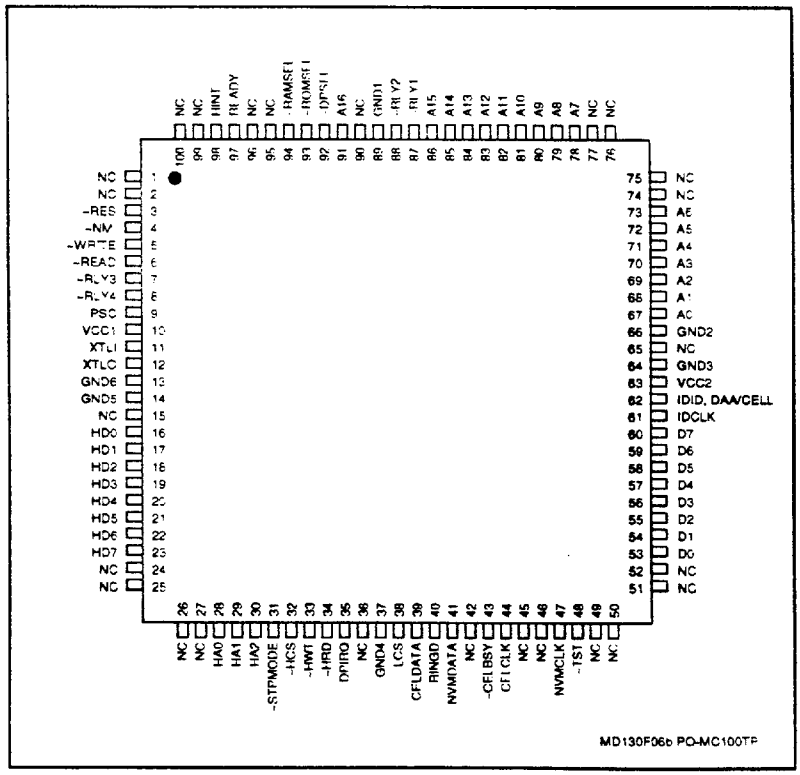


Figure 6b. E39 MCU Pin Signals- 100-Pin TQFP - Parallel Interface

Table 6a. E39 MCU Pin Signals- 100-Pin TQFP - Serial Interface

Pin	Signal Label	I/O Type	Interface	Pin	Signal Label	I/O Type	Interface
1	NC		NC	51	NC		NC
2	NC		NC	52	NC		NC
3	~RES	IC	MDP: ~RESOUT	53	D0	IA/OA	EB: D0
4	~NMI	MI	Note 4	54	D1	IA/OA	EB: D1
5	~WRITE	OA	EB: ~WRITE	55	D2	IA/OA	EB: D2
6	~READ	OA	EB: ~READ	56	D3	IA/OA	EB: D3
7	(PE2) ~RLY3	OA	WL: DAA: A/A1, ~MUTE, Cellular: CELBSY	57	D4	IA/OA	EB: D4
8	(PE3) ~RLY4	OA	WL: DAA: ~T/DRLY, ~EARTH	58	D5	IA/OA	EB: D5
9	PSC	IA	NC	59	D6	IA/OA	EB: D6
10	VCC1	PWR	VCC	60	D7	IA/OA	EB: D7
11	XTLI	IE	Crystal/Clock Circuit	61	(PE6) IDCLK	OA	WL: DAA: IDCLK
12	XTLO	OE	Crystal/Clock Circuit	62	(PE7) IDID Cellular: DAA/CELL	IA	WL: DAA: IDID Cellular: DAA/CELL
13	GND6	GND	GND	63	VCC2	PWR	VCC
14	GND5	GND	GND	64	GND3	GND	GND
15	NC		NC	65	NC		NC
16	(PC0) ~DSR	OA	DTE IF: ~DSR	66	GND2	GND	GND
17	(PC1) ~CTS	OA	DTE IF: ~CTS	67	A0	OA	EB: A0
18	(PC2) ~RLSD	OA	DTE IF: ~RLSD	68	A1	OA	EB: A1
19	(PC3) NC		NC	69	A2	OA	EB: A2
20	(PC4) NC		NC	70	A3	OA	EB: A3
21	(PC5) ~RI	OA	DTE IF: ~RI	71	A4	OA	EB: A4
22	(PC6) ~TM	OA	DTE IF: ~TM	72	A5	OA	EB: A5
23	(PC7) NC		NC	73	A6	OA	EB: A6
24	NC		NC	74	NC		NC
25	NC		NC	75	NC		NC
26	NC		NC	76	NC		NC
27	NC		NC	77	NC		NC
28	(PD0) ~DTRIND	OA	Indicator Circuit	78	A7	OA	EB: A7
29	(PD1) NC		NC	79	A8	OA	EB: A8
30	(PD2) NC		NC	80	A9	OA	EB: A9
31	(PD3) ~STPMODE	IA	Stop Mode Circuit	81	A10	OA	EB: A10
32	(PD4) ~DTR	IA	DTE IF: ~DTR	82	A11	OA	EB: A11
33	(PD5) NC		NC	83	A12	OA	EB: A12
34	(PD6) ~RTS	IA	DTE IF: ~RTS	84	A13	OA	EB: A13
35	(PD7) DPIRQ	IA	MDP: IRQ	85	A14	OA	EB: A14
36	NC		NC	86	A15	OA	EB: A15
37	GND4	GND	GND	87	(PE0) ~RLY1	OA	WL: DAA: ~OH Cellular: CTRL0
38	(PE4) WL: LCS	IA	WL: DAA: LCS	88	(PE1) ~RLY2	OA	WL: DAA: ~PULSE Cellular: CTRL1
39	(PE5) WL: ~CLKSTOP Cellular: CELDATA	OA IA/OA	WL: DTE IF: ~CLKSTOP Cellular: CELDATA	89	GND1	GND	GND
40	(PA0) RINGD	IA	DAA : RINGD	90	NC		NC
41	(PA1) NVMDATA	IA/OA	NVRAM: SDA (Note 4)	91	(PB0) A16	OA	EB: A16
42	(PA2) ~TXD	IA	DTE IF: ~TXD	92	(PB1) ~DPSEL	OA	EB: MDP: ~CS
43	(PA3) ~CELBSY	IA	Cellular: ~CELBSY	93	(PB2) ~ROMSEL	OA	EB: ROM: ~CE
44	(PA4) CELCLK	IA	Cellular: CELCLK	94	(PB3) ~RAMSEL	OA	EB: RAM: ~CS
45	(PA5) ~DPRXD	MI	MDP: RXD	95	(PB4) NC	OA	NC
46	(PA6) ~RXD	OA	DTE IF: ~RXD	96	(PB5) NC	OA	NC
47	(PA7) NVMCLK	OA	NVRAM: SCL	97	(PB6) ~AAIND	OA	Indicator Circuit
48	~TST	MI	NC (Note 5)	98	(PB7) ~TMIND	OA	Indicator Circuit
49	NC		NC	99	NC		NC
50	NC		NC	100	NC		NC

Notes:

1. I/O types:
   - MI = Modem interconnect.
   - IA, IB, IC, IE = Digital input.
   - OA, OB, OE = Digital output.
2. NC = No external connection.
3. NU = Not used; connect as noted.
4. Connect to VCC through 10K ohms.
5. Leave open to allow internal MCU ROM use; connect to GND through 10K ohms to force external ROM use only.
6. Connect to GND through 10K ohms.
7. Connect to GND through 100K ohms

Table 6b. E39 MCU Pin Signals- 100-Pin TQFP - Parallel Interface

Pin	Signal Label	I/O Type	Interface	Pin	Signal Label	I/O Type	Interface
1	NC		NC	51	NC		NC
2	NC		NC	52	NC		NC
3	~RES	IC	MDP: ~RESOUT	53	D0	IA/OA	EB: D0
4	~NMI	MI	Note 4	54	D1	IA/OA	EB: D1
5	~WRITE	OA	EB: ~WRITE	55	D2	IA/OA	EB: D2
6	~READ	OA	EB: ~READ	56	D3	IA/OA	EB: D3
7	(PE2) ~RLY3	OA	WL: DAA: A/A1, ~MUTE, Cellular: CELBSY	57	D4	IA/OA	EB: D4
8	(PE3) ~RLY4	OA	WL: DAA: ~T/DRLY, ~EARTH	58	D5	IA/OA	EB: D5
9	PSC	IA	NC	59	D6	IA/OA	EB: D6
10	VCC1	PWR	VCC	60	D7	IA/OA	EB: D7
11	XTLI	IE	Crystal/Clock Circuit	61	(PE6) IDCLK	OA	WL: DAA: IDCLK
12	XTLO	OE	Crystal/Clock Circuit	62	(PE7) IDID Cellular: DAA/CELL	IA	WL: DAA: IDID Cellular: DAA/CELL
13	GND6	GND	GND	63	VCC2	PWR	VCC
14	GND5	GND	GND	64	GND3	GND	GND
15	NC		NC	65	NC		NC
16	(PC0) HD0	IA/OA	HB: HD0	66	GND2	GND	GND
17	(PC1) HD1	IA/OA	HB: HD1	67	A0	OA	EB: A0
18	(PC2) HD2	IA/OA	HB: HD2	68	A1	OA	EB: A1
19	(PC3) HD3	IA/OA	HB: HD3	69	A2	OA	EB: A2
20	(PC4) HD4	IA/OA	HB: HD4	70	A3	OA	EB: A3
21	(PC5) HD5	IA/OA	HB: HD5	71	A4	OA	EB: A4
22	(PC6) HD6	IA/OA	HB: HD6	72	A5	OA	EB: A5
23	(PC7) HD7	IA/OA	HB: HD7	73	A6	OA	EB: A6
24	NC		NC	74	NC		NC
25	NC		NC	75	NC		NC
26	NC		NC	76	NC		NC
27	NC		NC	77	NC		NC
28	(PD0) HA0	IA	HB: HA0	78	A7	OA	EB: A7
29	(PD1) HA1	IA	HB: HA1	79	A8	OA	EB: A8
30	(PD2) HA2	IA	HB: HA2	80	A9	OA	EB: A9
31	(PD3) ~STPMODE	IA	Stop Mode Circuit	81	A10	OA	EB: A10
32	(PD4) ~HCS	IA	HB: ~CS	82	A11	OA	EB: A11
33	(PD5) ~HWT	IA	HB: ~WT	83	A12	OA	EB: A12
34	(PD6) ~HRD	IA	HB: ~RD	84	A13	OA	EB: A13
35	(PD7) DPIRQ	IA	MDP: IRQ	85	A14	OA	EB: A14
36	NC		NC	86	A15	OA	EB: A15
37	GND4	GND	GND	87	(PE0) ~RLY1	OA	WL: DAA: ~OH Cellular: CTRL0
38	(PE4) WL: LCS	IA	WL: DAA: LCS	88	(PE1) ~RLY2	OA	WL: DAA: ~PULSE Cellular: CTRL1
39	(PE5) WL: ~CLKSTOP Cellular: CELDATA	OA IA/OA	WL: ~CLKSTOP Cellular: CELDATA	89	GND1	GND	GND
40	(PA0) RINGD	IA	PIF: DAA: RINGD; PCMCIA: PICA: RINGOUTB	90	NC		NC
41	(PA1) NVMDATA	IA/OA	NVRAM: SDA (Note 4)	91	(PB0) A16	OA	EB: A16
42	(PA2) NC		NC	92	(PB1) ~DPSEL	OA	EB: MDP: ~CS
43	(PA3) ~CELBSY	IA	Cellular: ~CELBSY	93	(PB2) ~ROMSEL	OA	EB: ROM: ~CE
44	(PA4) CELCLK	IA	Cellular: CELCLK	94	(PB3) ~RAMSEL	OA	EB: RAM: ~CS
45	(PA5) NC		NC	95	(PB4) NC	OA	NC
46	(PA6) NC		NC	96	(PB5) NC	OA	NC
47	(PA7) NVMCLK	OA	NVRAM: SCL	97	(PB6) READY	OA	PICA: MRDY
48	~TST	MI	NC (Note 5)	98	(PB7) HINT	OA	HB: HINT
49	NC		NC	99	NC		NC
50	NC		NC	100	NC		NC

Notes:

1. I/O types:
   - MI = Modem interconnect.
   - IA, IB, IE = Digital input.
   - OA, OB, OE = Digital output.
2. NC = No external connection allowed
3. NU = Not used; connect as noted.
4. Connect to VCC through 10K ohms.
5. Leave open to allow internal MCU ROM use: connect to GND through 10K ohms to force external ROM use only.
6. Connect to HB: RESET through inverter.

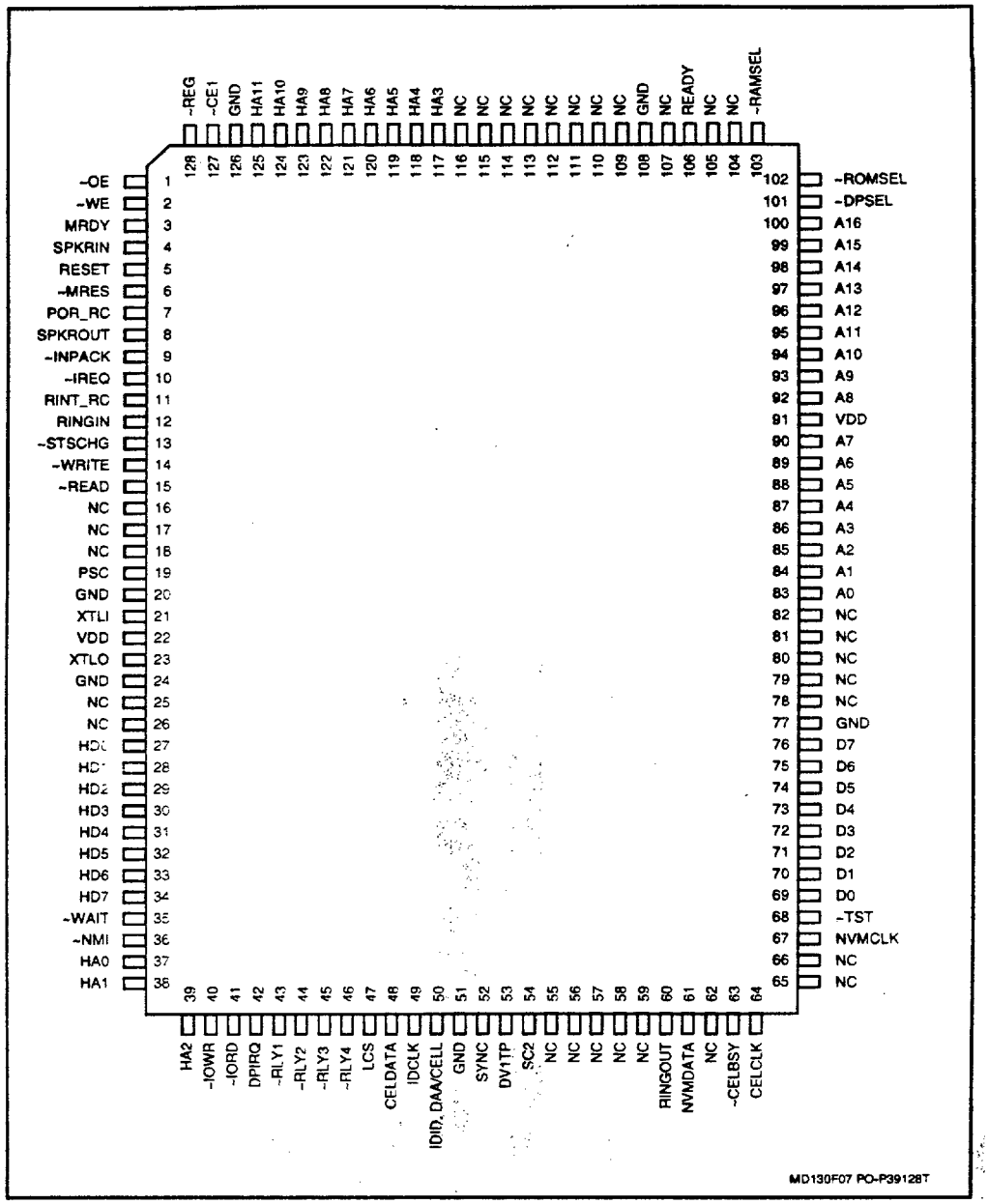


Figure 7. P39 MCU Pin Signals - 128 Pin TQFP

Table 7. P39 MCU Pin Signals- 128-Pin TQFP

Pin	Signal Label	I/O Type	Interface	Pin	Signal Label	I/O Type	Interface
1	~OE	IA	HB: ~OE	65	(PA5) NC		NC
2	~WE	IA	HB: ~WE	66	(PA6) NC		NC
3	MRDY	IA	READY (Note 9)	67	(PA7) NVMCLK	OA	NVRAM: SCL
4	SPKRIN	IA	Digital Speaker Circuit	68	~TST	MI	NC (Note 5)
5	RESET	IA	HB: ~RESET (Note 4)	69	D0	IA/OA	EB: D0
6	~MRES	IC	MDP: ~POR1 & ~POR2	70	D1	IA/OA	EB: D1
7	POR_RC	I	POR RC Circuit (Note 6)	71	D2	IA/OA	EB: D2
8	SPKROUT	OA	HB: SPKROUT	72	D3	IA/OA	EB: D3
9	~INPACK	OA	HB: ~INPACK	73	D4	IA/OA	EB: D4
10	~IREQ	OA	HB: ~IREQ	74	D5	IA/OA	EB: D5
11	RINT_RC		RINT RC Network (Note 7)	75	D6	IA/OA	EB: D6
12	RINGIN	IA	DAA: Ring Detect Circuit	76	D7	IA/OA	EB: D7
13	~STSCHG	OA	HB: ~STSCHG	77	GND	GND	GND
14	~WRITE	OA	EB: ~WRITE	78	NC		NC
15	~READ	OA	EB: ~READ	79	NC		NC
16	NC		NC	80	NC		NC
17	NC		NC	81	NC		NC
18	NC		NC	82	NC		NC
19	PSC	IA	NC	83	A0	OA	EB: A0
20	GND	GND	GND	84	A1	OA	EB: A1
21	XTLI	IE	Crystal/Clock Circuit	85	A2	OA	EB: A2
22	VDD	PWR	VCC	86	A3	OA	EB: A3
23	XTLO	OE	Crystal/Clock Circuit	87	A4	OA	EB: A4
24	GND	GND	GND	88	A5	OA	EB: A5
25	NC		NC	89	A6	OA	EB: A6
26	NC		NC	90	A7	OA	EB: A7
27	(PC0) HD0	IA/OA	HB: HD0	91	VDD	PWR	VCC
28	(PC1) HD1	IA/OA	HB: HD1	92	A8	OA	EB: A8
29	(PC2) HD2	IA/OA	HB: HD2	93	A9	OA	EB: A9
30	(PC3) HD3	IA/OA	HB: HD3	94	A10	OA	EB: A10
31	(PC4) HD4	IA/OA	HB: HD4	95	A11	OA	EB: A11
32	(PC5) HD5	IA/OA	HB: HD5	96	A12	OA	EB: A12
33	(PC6) HD6	IA/OA	HB: HD6	97	A13	OA	EB: A13
34	(PC7) HD7	IA/OA	HB: HD7	98	A14	OA	EB: A14
35	~WAIT	OA	HB: ~WAIT	99	A15	OA	EB: A15
36	~NMI	MI	VCC (Note 4)	100	(PB0) A16	OA	EB: A16
37	(PD0) HA0	IA	HB: HA0	101	(PB1) ~DPSEL	OA	MDP: ~CS
38	(PD1) HA1	IA	HB: HA1	102	(PB2) ~ROMSEL	OA	ROM: ~CE
39	(PD2) HA2	IA	HB: HA2	103	(PB3) ~RAMSEL	OA	RAM: ~CS
40	(PD5) ~IOWR	IA	HB: ~IOWR (Note 4)	104	(PB4) NC	OA	NC
41	(PD6) ~IORD	IA	HB: ~IORD (Note 4)	105	(PB5) NC	OA	NC
42	(PD7) DPIRQ	IA	MDP: DPIRQ	106	(PB6) READY	OA	MRDY
43	(PE0) ~RLY1	OA	WL: DAA: ~OH Cellular: CTRL0	107	(PB7) HINT	OA	NC
44	(PE1) ~RLY2	OA	WL: DAA: ~PULSE Cellular: CTRL1	108	GND	GND	GND
45	(PE2) ~RLY3	OA	WL: DAA: A/A1, ~MUTE Cellular: CELBSY	109	NC		NC
46	(PE3) ~RLY4	OA	WL: DAA: ~T/DRLY, ~EARTH	110	NC		NC
47	(PE4) WL: LCS	IA	WL: DAA: LCS	111	NC		NC
48	(PE5) CELDATA	IA/OA	Cellular: CELDATA	112	NC		NC
49	(PE6) IDCLK	OA	WL: DAA: IDCLK	113	NC		NC
50	(PE7) IDID, DAA/CELL	IA	WL: DAA: IDID Cellular: DAA/CELL	114	NC		NC

Table 7. P39 MCU Pin Signals- 128-Pin TQFP (Cont'd)

Pin	Signal Label	I/O Type	Interface	Pin	Signal Label	I/O Type	Interface
51	GND	GND	GND	115	NC		NC
52	SYNC		NC	116	NC		NC
53	DV1TP		NC	117	HA3	IA	HB: HA3
54	SC2		NC	118	HA4	IA	HB: HA4
55	NC		NC	119	HA5	IA	HB: HA5
56	NC		NC	120	HA6	IA	HB: HA6
57	NC		NC	121	HA7	IA	HB: HA7
58	NC		NC	122	HA8	IA	HB: HA8
59	NC		NC	123	HA9	IA	HB: HA9
60	(PA0) RINGOUT	OA	MDP: RINGD	124	HA10	IA	HB: HA10
61	(PA1) NVMDATA	IA/OA	NVRAM: SDA (Note 8)	125	HA11	IA	HB: HA11
62	(PA2) NC		NC	126	GND	GND	GND
63	(PA3) ~CELBSY	IA	Cellular: ~CELBSY	127	~CE1		HB: ~CE1 (Note 4)
64	(PA4) CELCLK	IA	Cellular: CELCLK	128	~REG	IA	HB: ~REG (Note 4)

Notes:

1. I/O types:
   MI = Modem interconnect.
   IA, IB, IC, IE = Digital input.
   OA, OB, OE = Digital output.
2. NC = No external connection.
3. NU = Not used; connect as noted.
4. Connect to VCC through 100K ohms.
5. Leave open to allow internal MCU ROM use: connect to GND through 10K ohms to force external ROM use only.
6. Connect to POR RC Network (180K ohms to VCC; 0.1 µF to GND).
7. Connect to RINT C Network (0.1 µF in parallel with 0.1 µF to GND.)
8. Connect to VCC through 10K ohms.
9. Connect to GND through 20K ohms.

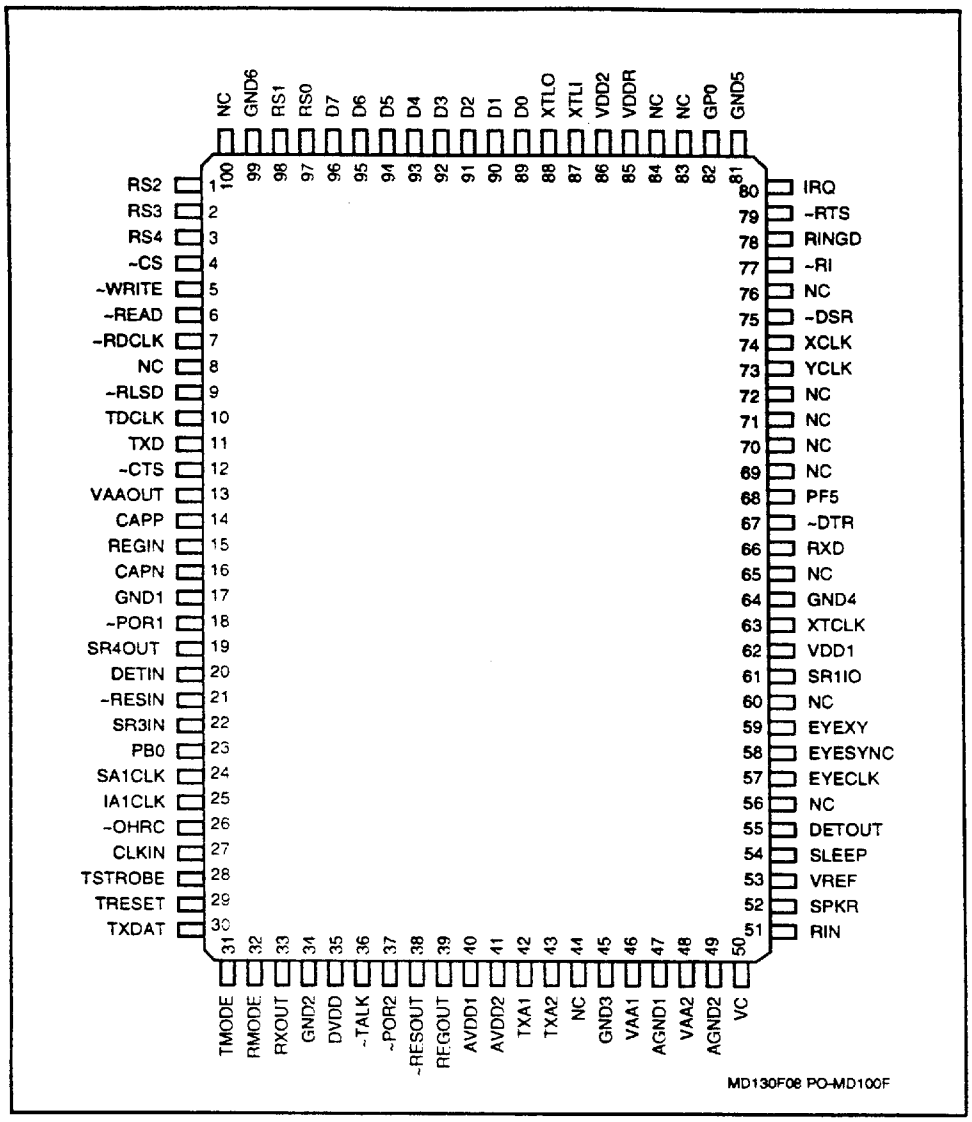


Figure 8. MDP Pin Signals - 100-Pin PQFP

Table 8. MDP Pin Signals - 100-Pin PQFP

Pin	Signal Label	I/O Type	Interface[3]	Pin	Signal Label	I/O Type	Interface
1	RS2	IA	MCU: A2	51	RIN	I(DA)	DAA: RIN
2	RS3	IA	MCU: A3	52	SPKR	O(DF)	Speaker Circuit
3	RS4	IA	MCU: A4	53	VREF	MI	VC through capacitors
4	~CS	IA	MCU: ~DPSEL	54	SLEEP	MI	PF5 (68)
5	~WRITE	IA	MCU: ~WRITE	55	DETOUT	MI	NC
6	~READ	IA	MCU: ~READ	56	NC		NC
7	~RDCLK	OA	PIF: NC SIF: DTE IF: ~RXCLK	57	~EYECLK	OA	NC
8	NC		NC	58	EYESYNC	OA	NC
9	~RLSD	OA	PIF: NC; SIP: Indicator Circuit	59	EYEXY	OA	NC
10	TDCLK	OA	PIF: NC SIF: DTE IF: ~TXCLK	60	NC		NC
11	TXD	IA	PIF: NC SIF: DTE IF & MCU TXD	61	SR1IO	MI	TMODE (31)
12	~CTS	OA	NC	62	VDD1	PWR	VCC
13	VAAOUT	MI	VAA1 and VAA2	63	XTCLK	IA	PIF: NC SIF: DTE IF: ~XTCLK
14	CAPP	MI	NC	64	GND4	GND	GND
15	REGIN	MI	GND	65	NC		NC
16	CAPN	MI	NC	66	RXD	OA	PIF: NC; SIF: MCU: ~DPRXD
17	GND1	GND	GND	67	~DTR	IA	VCC (Note 4)
18	~POR1	IA	PIF: ~RESET; P39 MCU /PICA: ~MRES	68	PF5	MI	SLEEP (54)
19	SR4OUT	MI	TXDAT (30)	69	NC		NC
20	DETIN	MI	VCC	70	NC		NC
21	~RESIN	MI	~RESOUT (38)	71	NC		NC
22	SR3IN	MI	RXOUT (33)	72	NC		NC
23	PB0	MI	CLKIN (27)	73	YCLK	O	NC
24	SA1CLK	MI	TRESET (29)	74	XCLK	O	NC
25	IA1CLK	MI	TSTROBE (28)	75	~DSR	OA	NC
26	~OHRC	OD	WL: DAA: Caller ID Relay	76	NC		NC
27	CLKIN	MI	PB0 (23)	77	~RI	OA	NC
28	TSTROBE	MI	IA1CLK (25)	78	RINGD	IA	SIF or PIF: DAA: RINGD; PCMCIA: PICA: RINGOUTB
29	TRESET	MI	SA1CLK (24)	79	~RTS	IA	VCC (Note 4)
30	TXDAT	MI	SR4OUT (19)	80	IRQ	OA	MCU: DPIRQ
31	TMODE	MI	RMODE (32)	81	GND5	GND	GND
32	RMODE	MI	TMODE (31)	82	GP0	MI	EYESYNC
33	RXOUT	MI	SR3IN (22)	83	NC		NC
34	GND2	GND	GND	84	NC		NC
35	DVDD	PWR	VCC	85	VDDR	MI	VCC
36	~TALK	OD	WL: DAA: Voice Relay	86	VDD2	PWR	VCC
37	~POR2	IA	~POR1	87	XTLI	I	Crystal/Clock Circuit
38	~RESOUT	IA	~RESIN (21); E39 MCU: ~RES	88	XTLO	O	Crystal/Clock Circuit
39	REGOUT	MI	NC	89	D0	IA/OA	MCU: D0
40	AVDD1	PWR	VCC	90	D1	IA/OA	MCU: D1
41	AVDD2	PWR	VCC with RC filter	91	D2	IA/OA	MCU: D2
42	TXA1	O(DD)	DAA: TXA1	92	D3	IA/OA	MCU: D3
43	TXA2	O(DD)	DAA: TXA2	93	D4	IA/OA	MCU: D4
44	NC		NC	94	D5	IA/OA	MCU: D5
45	GND3	GND	GND	95	D6	IA/OA	MCU: D6
46	VAA1	PWR	VAAOUT	96	D7	IA/OA	MCU: D7
47	AGND1	GND	AGND	97	RS0	IA	MCU: A0
48	VAA2	PWR	VAAOUT	98	RS1	IA	MCU: A1
49	AGND2	GND	AGND	99	GND6	GND	GND
50	VC	MI	AGND through capacitors	100	NC		NC

Notes:

1. I/O types:
   - MI = Modem interconnect.
   - IA, IB = Digital input.
   - OA, OB = Digital output.
   - I(DA)] = Analog input.
   - O(DD), O(DF) = Analog output
2. NC = No external connection allowed.
3. Interface Legend:
   - PIF = Host Parallel Interface Configuration
   - SIF = DTE Serial Interface Configuration
   - WL = Wireline.
   - DTE = Data Terminal Equipment.
4. Connect to VCC through 20K ohms.

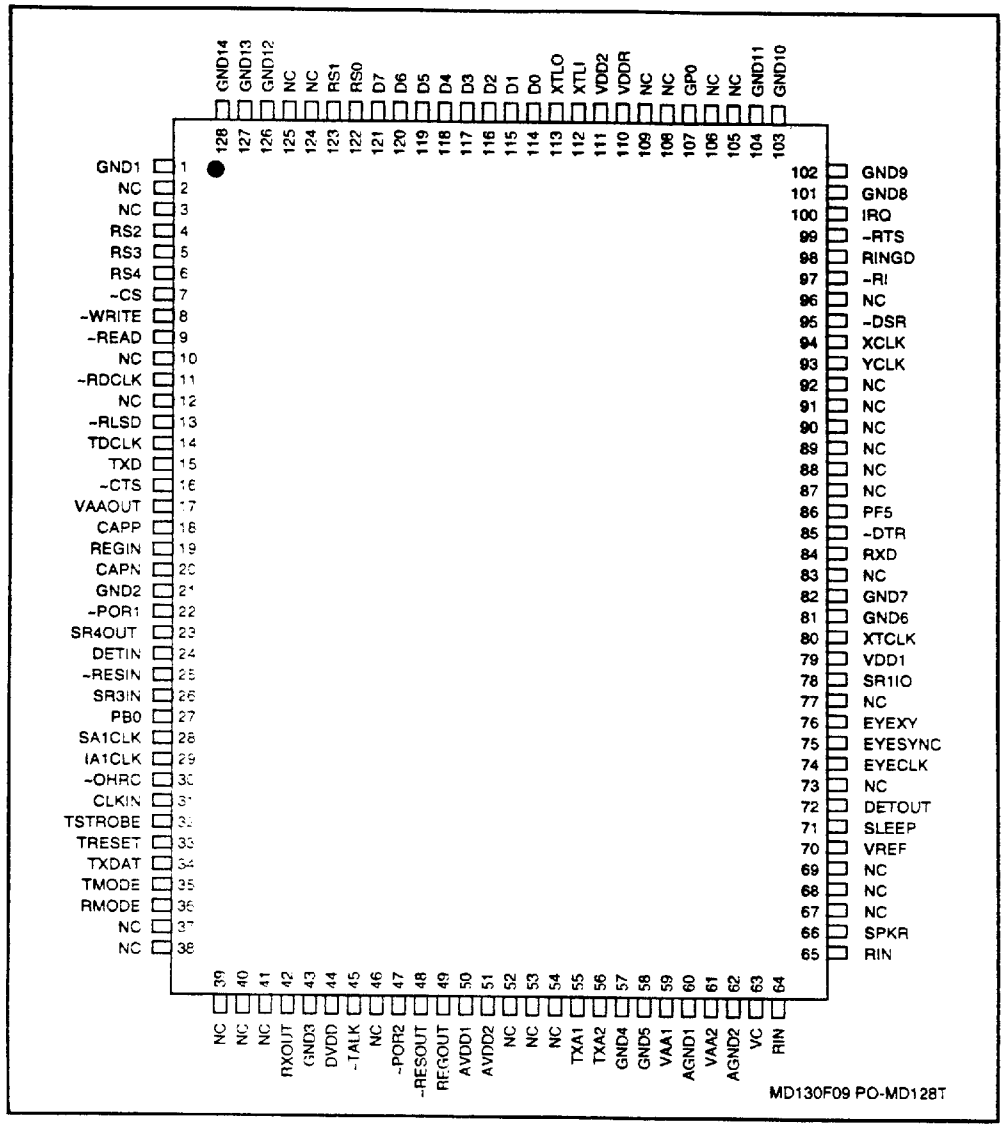


Figure 9. MDP Pin Signals - 128-Pin TQFP

Table 9. MDP Pin Signals - 128-Pin TQFP

Pin	Signal Label	I/O Type	Interface[3]	Pin	Signal Label	I/O Type	Interface
1	GND1	GND	GND	65	RIN	I(DA)	DAA: RIN
2	NC		NC	66	SPKR	O(DF)	Speaker Circuit
3	NC		NC	67	NC		NC
4	RS2	IA	MCU: A2	68	NC		NC
5	RS3	IA	MCU: A3	69	NC		NC
6	RS4	IA	MCU: A4	70	VREF	MI	VC through capacitors
7	~CS	IA	MCU: ~DPSEL	71	SLEEP	MI	PF5 (86)
8	~WRITE	IA	MCU: ~WRITE	72	DETOUT	MI	NC
9	~READ	IA	MCU: ~READ	73	NC		NC
10	NC		NC	74	~EYECLK	OA	NC
11	~RLSD	OA	PIF: NC; SIP: Indicator Circuit	75	EYESYNC	OA	NC
12	NC		NC	76	EYEXY	OA	NC
13	~RLSD	OA	NC	77	NC		NC
14	TDCLK	OA	PIF: NC SIF: DTE IF: ~TXCLK	78	SR1IO	MI	TMODE (35)
15	TXD	IA	PIF: NC SIF: DTE IF & MCU TXD	79	VDD1	PWR	VCC
16	~CTS	OA	NC	80	XTCLK	IA	DTE Serial Interface
17	VAAOUT	MI	VAA1 and VAA2	81	GND6	GND	GND
18	CAPP	MI	NC	82	GND7	GND	GND
19	REGIN	MI	GND	83	NC		NC
20	CAPN	MI	NC	84	RXD	OA	PIF: NC; SIF: MCU: ~DPRXD
21	GND2	GND	GND	85	~DTR	IA	VCC (Note 4)
22	~POR1	IA	PIF: ~RESET; P39 MCU /PICA: ~MRES	86	PF5	MI	SLEEP (71)
23	SR4OUT	MI	TXDAT (34)	87	NC		NC
24	DETIN	MI	VCC	88	NC		NC
25	~RESIN	MI	~RESOUT (48)	89	NC		NC
26	SR3IN	MI	RXOUT (42)	90	NC		NC
27	PB0	MI	CLKIN (31)	91	NC		NC
28	SA1CLK	MI	TRESET (33)	92	NC		NC
29	IA1CLK	MI	TSTROBE (32)	93	YCLK	O	NC
30	~OHRC	OD	WL: DAA: Caller ID Relay	94	XCLK	O	NC
31	CLKIN	MI	PB0 (27)	95	~DSR	OA	NC
32	TSTROBE	MI	IA1CLK (29)	96	NC		NC
33	TRESET	MI	SA1CLK (28)	97	~RI	OA	NC
34	TXDAT	MI	SR4OUT (23)	98	RINGD	IA	SIF or PIF: DAA: RINGD; PCMCIA: PICA: RINGOUTB
35	TMODE	MI	RMODE (36)	99	~RTS	IA	VCC (Note 4)
36	RMODE	MI	TMODE (35)	100	IRQ	OA	MCU: DPIRQ
37	NC		NC	101	GND8	GND	GND
38	NC		NC	102	GND9	GND	GND
39	NC		NC	103	GND10	GND	GND
40	NC		NC	104	GND11	GND	GND
41	NC		NC	105	NC		NC
42	RXOUT	MI	SR3IN (26)	106	NC		NC
43	GND3	GND	GND	107	GP0	MI	EYESYNC
44	DVDD	PWR	VCC	108	NC		NC
45	~TALK	OD	WL: DAA: Voice Relay	109	NC		NC
46	NC		NC	110	VDDR	MI	VCC
47	~POR2	IA	~POR1	111	VDD2	PWR	VCC
48	~RESOUT	IA	~RESIN (25); E39 MCU: ~RES	112	XTLI	I	Crystal/Clock Circuit
49	REGOUT	MI	NC	113	XTLO	O	Crystal/Clock Circuit
50	AVDD1	PWR	VCC	114	D0	IA/OA	MCU: D0
51	AVDD2	PWR	VCC with RC filter	115	D1	IA/OA	MCU: D1
52	NC		NC	116	D2	IA/OA	MCU: D2
53	NC		NC	117	D3	IA/OA	MCU: D3
54	NC		NC	118	D4	IA/OA	MCU: D4
55	TXA1	O(DD)	DAA: TXA1	119	D5	IA/OA	MCU: D5
56	TXA2	O(DD)	DAA: TXA2	120	D6	IA/OA	MCU: D6
57	GND4	GND	GND	121	D7	IA/OA	MCU: D7
58	GND5	GND	GND	122	RS0	IA	MCU: A0
59	VAA1	PWR	VAAOUT	123	RS1	IA	MCU: A1
60	AGND1	GND	AGND	124	NC		NC

Table 9. MDP Pin Signals - 128-Pin TQFP (Cont'd)

Pin	Signal Label	I/O Type	Interface[3]	Pin	Signal Label	I/O Type	Interface
61	VAA2	PWR	VAAOUT	125	NC		NC
62	AGND2	GND	GND	126	GND12	GND	GND
63	VC	MI	AGND through capacitors	127	GND13	GND	GND
64	RIN	I(DA)	DAA RIN	128	GND14	GND	GND

Notes:

1. I/O types:
   - MI = Modem interconnect.
   - IA, IB = Digital input.
   - OA, OB = Digital output.
   - I(DA)] = Analog input.
   - O(DD), O(DF) = Analog output.
2. NC = No external connection allowed.
3. Interface Legend:
   - PIF = Host Parallel Interface Configuration.
   - SIF = DTE Serial Interface Configuration.
   - WL = Wireline.
   - DTE = Data Terminal Equipment.
4. Connect to VCC through 20K ohms

Table 10. MCU Signal Definitions

Label	I/O Type	Signal Name/Description
UNIQUE TO E39 MCU		
SYSTEM OVERHEAD		
XTLI, XTLO	IE, OE	**MCU Crystal/Clock In and Crystal Out.** Connect XTLI and XTLO to an external crystal circuit consisting of a 8.064 MHz crystal and a capacitance network.
~RES	IC	**MCU Reset.** The active low ~RES input resets the MCU logic, and restores the saved configuration from NVRAM or returns the modem to the factory default values if NVRAM is not present. For serial interface, the ~RES input is typically connected to a reset switch circuit and MDP ~POR. For parallel interface, connect ~RES input to the host bus RESET line through an inverter and to MDP ~POR. For PCMCIA interface, connect ~RES to the MDP ~RESOUT.
DPIRQ	IA	**MDP Interrupt Request.** Connect to the MDP IRQ output.
~DPRXD	MI	**MDP Received Data.** Connect to the MDP RXD output (serial DTE interface only).
VCC1-VCC2	PWR	**+ 5V Digital Supply.** +5V ± 5%.
GND1-GND6	GND	**Digital Ground.** Connect to ground.
TELEPHONE LINE INTERFACE (WIRELINE OPERATION ONLY)		
RINGD	IA	**Ring Frequency.** A high-going edge on the RINGD input initiates an internal ring frequency measurement. The RINGD input from an external ring detect circuit is monitored to determine when to wake up from sleep or stop mode. The RINGD input is typically connected to the output of an optoisolator or equivalent. The idle state (no ringing) output of the ring detect circuit should be low. For PCMCIA operation, connect the RINGD input to the PICA RINGOUTB pin.
STOP MODE CIRCUIT		
~STPMODE	IA	**Stop Mode.** ~STPMODE low causes the modem to enter the stop mode immediately after terminating a line connection if connected, terminating any test in process, and allowing any data in the receive buffer to clear. ~STPMODE must be high before the modem can attain normal operation after power turn-on, reset, or wake-up from sleep or stop mode. For PCMCIA interface, connect ~STPMODE to the PICA -PWRDWN output. **NOTE:** Stop mode is available only when a dedicated MCU crystal circuit is used.
PARALLEL HOST INTERFACE (E39 MCU WITH PARALLEL INTERFACE) The parallel interface emulates a 16550A UART-compatible interface. The parallel interface is compatible with communications software designed to operate with a 16550A interface.		
HA0-HA2	IA	**Host Bus Address Lines 0-2.** During a host read or write operation with ~HCS low, HA0-HA2 select an internal MCU 16550A-compatible register.
HD0-HD7	IA/OA	**Host Bus Data Lines 0-7.** HD0-HD7 are comprised of eight three-state input/output lines providing bidirectional communication between the host and the MCU. Data, control words, and status information are transferred over HD0-HD7.
~HCS	IA	**Host Bus Chip Select.** ~HCS input low selects the host bus. For PCMCIA interface, connect ~HCS to the PICA -MCS output.
~HRD	IA	**Host Bus Read.** ~HRD is an active low, read control input. When ~HCS is low, ~HRD low allows the host to read status information or data from a selected MCU register. For PCMCIA interface, connect ~HRD to the PICA MODEMRD output.
~HWT	IA	**Host Bus Write.** ~HWT is an active low, write control input. When ~HCS is low, ~HWT low allows the host to write data or control words into a selected MCU register. For PCMCIA interface, connect ~HWT to the PC Socket -IOWR pin.
HINT	OA	**Host Bus Interrupt.** HINT output is set high when the receiver error flag, received data available, transmitter holding register empty, or modem status interrupt is asserted. HINT is reset low upon the appropriate interrupt service or master reset operation. For PCMCIA interface, connect HINT to the PICA HINT pin.

Table 10. MCU Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
UNIQUE TO E39 MCU (CONTINUED)		
V.24 (EIA/TIA-232-E) DTE SERIAL INTERFACE (E39 MCU WITH SERIAL INTERFACE)		
These signals correspond functionally to V.24/EIA/TIA-232-E signals with TTL levels and are inverted from V.24/EIA/TIA-232-E levels.		
~TXD	IA	**Transmitted Data (EIA BA/CCITT CT103).** The DTE uses the ~TXD line to send data to the modem for transmission over the telephone line or to transmit commands to the modem.
~RXD	OA	**Received Data (EIA BB/CCITT CT 104).** The modem uses the ~RXD line to send data received from the telephone line to the DTE and to send modem responses to the DTE. During command mode, ~RXD data represents the modem responses to the DTE.
~CTS	OA	**Clear To Send (EIA CB/CCITT CT106).** ~CTS output ON (low) indicates that the DTE is ready to accept data from the DTE. In asynchronous operation, in error correction or normal mode, ~CTS is always ON (low) unless RTS/CTS flow control is selected by the &Kn command. In synchronous operation, the modem also holds ~CTS ON during asynchronous command state. The modem turns ~CTS OFF immediately upon going off-hook and holds ~CTS OFF until both ~DSR and ~RLSD are ON and the modem is ready to transmit and receive synchronous data. The modem can also be commanded by the &Rn command to turn ~CTS ON in response to an ~RTS OFF-to-ON transition.
~DSR	OA	**Data Set Ready (EIA CC/CCITT CT107).** ~DSR indicates modem status to the DTE. ~DSR OFF (high) indicates that the DTE is to disregard all signals appearing on the interchange circuits except Ring Indicator (~RI). ~DSR output is controlled by the AT&Sn command.
~RLSD	OA	**Received Line Signal Detector (EIA CF/CCITT CT109).** When AT&C0 command is not in effect, ~RLSD output is ON when a carrier is detected on the line or OFF when carrier is not detected.
~TM	OA	**Test Mode Indicate (EIA TM/CCITT CT142).** The ~TM output indicates the modem is in test mode (low) or in any other mode (high).
~RI	OA	**Ring Indicator (EIA CE/CCITT CT125).** ~RI output ON (low) indicates the presence of an ON segment of a ring signal on the telephone line.
~DTR	IA	**Data Terminal Ready (EIA CD/CCITT CT108).** The ~DTR input is turned ON (low) by the DTE when the DTE is ready to transmit or receive data. ~DTR ON prepares the modem to be connected to the telephone line, and maintains the connection established by the DTE (manual answering) or internally (automatic answering). ~DTR OFF places the modem in the disconnect state under control of the &Dn and &Qn commands.
~RTS	IA	**Request To Send (EIA CA/CCITT CT105).** ~RTS input ON (low) indicates that the DTE is ready to accept data from the modem. In the command state, the modem ignores ~RTS. In asynchronous operation, the modem ignores ~RTS unless RTS/CTS flow control is selected by the &Kn command. In synchronous on-line operation, the modem can be commanded by the &Rn command to ignore ~RTS or to respond to ~RTS by turning on ~CTS after the delay specified by Register S26.
INDICATOR INTERFACE (E39 MCU WITH SERIAL INTERFACE)		
~AAIND	OA	**Auto Answer Indicator.** ~AAIND output ON (low) corresponds to the indicator on. ~AAIND output is active when the modem is configured to answer the ring automatically (ATS0 command ≠ 0).
~TMIND	OA	**Test Mode Indicator.** ~TMIND output ON (low) corresponds to the indicator on. ~TMIND output pulses (LED flashes) when the modem is in test mode and if an error is detected.
~DTRIND	OA	**DTR Indicator.** ~DTRIND output ON (low) corresponds to the indicator on. The ~DTRIND state reflects the ~DTR output state except when the &D0 command is active, in which case ~DTRIND is low.

Table 10. MCU Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
UNIQUE TO P39 MCU		
SYSTEM OVERHEAD		
XTLI, XTLO	IE, OE	**MCU Crystal/Clock In and Crystal Out.** Connect XTLI and XTLO to an external crystal circuit consisting of a 8.064 MHz crystal and a capacitance network.
RINT_RC	IF/O	**Ring Integrate C Network.** An external C network (0.1 µF in parallel with 0.1 µF to GND) is tied to this pin for use in integrating the ring signal on the RINGIN pin. The input buffer is Schmitt Triggered and the output driver can drive a 0.1 µF capacitive load.
POR_RC	IF/O	**Power On Reset RC Network.** Active low Schmitt Trigger input. An external RC network (R = 180K Ω and C = 0.1 µF) provides a time constant for MCU reset by internally asserting the ~MRES signal low at Power On. The PCMCIA interface is not affected except for SReset bit in the Configuration Option Register which is reset to a 0.
VDD	PWR	**+ 5V Digital Supply.** +5V ± 5%.
GND	GND	**Digital Ground.** Connect to ground.
MODEM DATA PUMP (MDP) INTERFACE		
~MRES	I/O	**Modem Data Pump Reset.** The ~MRES output is asserted low during any of three conditions: 1. At card power on until the RC time constant on the POR_RC pin has timed out; 2. While the RESET pin is asserted; 3. While the SReset bit in the Configuration Option Register is set to a one. When asserted, the MCU core signals are tri-stated but the PCMCIA interface logic remains functional so that the signals which connect between the PCMCIA interface and the MCU core can be driven. The pin is an open drain with an active internal 100K ohm pull-up. Connect this pin to the MDP ~POR1 and ~POR2 pins.
DPIRQ	IA	**MDP Interrupt Request.** This input pin is asserted high when the MDP requests interrupt service from the MCU. Connect this pin to the MDP IRQ pin.
MRDY	IA	**Modem Ready.** A low level on this input pin indicates that the MCU is busy initializing the modem after power up, reset, or release from low power stop mode. The MCU sets READY high upon completion of this initialization.
RINGOUT (PA0)	OA	**Ring Output.** When the PwrDwn bit in the Configuration and Status Register is a 0, this pin directly reflects the signal at the RINGIN input pin. Connect this pin to the MDP RINGD input.
RINGIN	IF	**Ring Frequency.** A high-going edge on the RINGIN input initiates an internal ring frequency measurement. The RINGIN input from an external ring detect circuit is monitored to determine when to wake up from sleep or stop mode. The RINGIN input is typically connected to the output of an optoisolator or equivalent. The idle state (no ringing) output of the ring detect circuit is low. This signal is normally passed through to the RINGOUT output. However, when the PwrDwn bit (CCSR2) in the Card Configuration and Status Register is set to a 1, pass through of this signal is blocked. Additionally, when the RingEn bit (CCSR4) in the CCSR is a 1, ringing on this pin is integrated using the RC network on the RINT_RC pin and the integrated signal is used to assert the ~STSCHG pin. The ring detect circuit output can have a very slow rise time. The input buffer is Schmitt Triggered.
MISCELLANEOUS		
HINT (PB7)	OA	**Host Bus Interrupt.** Active high output asserted in the 16550 host interface (HCR2 = 1 and HCR1 = 1) under various conditions (PBS7 = 0). In Level Interrupt Mode , this signal is inverted and passed through to the ~IREQ pin. When HINT is set high by the controller's 16550 interface to indicate an interrupt request, the ~IREQ pin is asserted low. In Pulse Interrupt Mode, when HINT transitions from low to high, HINT is used internally to the MCU and is not normally used external to the MCU in the PCMCIA application.
DIGITIZED SPEAKER CIRCUIT		
SPKRIN	I	**Digitized Speaker Input.** The input to this pin is a digitized audio signal. This signal is passed through to the SPKROUT pin when the Audio bit in the Configuration and Status Register is a 1. This pin should be tied high if not used.

Table 10. MCU Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
UNIQUE TO P39 MCU (CONTINUED)		
PCMCIA HOST INTERFACE		
The parallel interface emulates a 16550A UART-compatible interface. The parallel interface is compatible with communications software designed to operate with a 16550A interface.		
HA0-HA11	IA	**Host Bus Address Lines 0-11.** During a host read or write operation with ~CE1 low, HA0-HA2 select an internal MCU 16550A-compatible register. HA3 - HA11 are used for Card Configuration Register selection, I/O decoding and CIS Memory selection.
HD0-HD7	IA/OA	**Host Bus Data Lines 0-7.** HD0-HD7 are comprised of eight three-state input/output lines providing bidirectional communication between the host and the MCU. Data, control words, and status information are transferred over HD0-HD7.
~IORD	IA	**I/O Read.** ~IORD is an active low read control input when Host Mode is enabled (HCR2 = 1). The host asserts ~IORD to read data from the 16550 interface registers. The ~REG and ~CE1 signals must also be active for a 16550 interface register read to occur.
~IOWR	IA	**I/O Write.** ~IOWR is an active low write control input when Host Mode is enabled (HCR2 = 1). The host asserts ~IOWR to write data to the 16550 interface registers (the I/O space). The ~REG and ~CE1 signals must also be active for a 16550 interface register write to occur. Data is clocked into the registers on the rising edge of ~IOWR.
~WAIT	OA	**I/O Wait.** Active low output asserted when either a host RX FIFO read or host TX FIFO write occurs. The ~WAIT line is held high (disabled) when the host GP mode is selected (HCR2 = 1) or when the device is in the low power mode. Available only when the host is accessing the 16550 FIFOs.
~CE1	IA	**Card Enable .** Active low input asserted by the host during an access to an even numbered address byte in attribute memory and during I/O accesses.
~REG	IA	**Register Select & I/O Enable signal.** Active low input asserted by the host during an I/O access, CIS Memory access, or an access to the Card Configuration Registers.
~OE	IA	**Output Enable.** Active low input asserted by the host to gate data out during a memory read cycle to CIS Memory or the Card Configuration Registers.
~WE	IA	**Write Enable.** Active low input asserted by the host to strobe write data in during a write cycle to CIS Memory or the Card Configuration Registers.
~INPACK	OA	**Input Acknowledge.** Active low output asserted in response to a valid 16550 interface register read access. For a 16550 read access to be valid, the Card Configuration Option Register must be properly configured and an I/O read to the configured address window must occur.
~STSCHG	OA	**Status Changed.** Active low output asserted to alert the host to changes in the RRdy/-Bsy bit (PRR1) in the Pin Replacement Register (PRR) and to the setting of the ReqAttn bit (ESR4) in the Extended Status Register (ESR). Optionally, if the RingEn bit in the Card Configuration and Status Register (CCSR) is a 1, then this pin is used for ring indication to the host as follows: while the input on the RINGIN pin is low (no ringing) the ~STSCHG pin is held high. While the input on the RINGIN pin is toggling indicating an incoming ring, the ~STSCHG pin is held low.
~IREQ	OA	**Interrupt Request.** In Level Interrupt Mode, an active low output is asserted to indicate an interrupt request by the 16550 interface. In Pulse Interrupt Mode, a low going output pulse is generated to indicate that the HINT signal has been asserted. Additionally, after any of the three possible reset conditions (Power-on reset, soft reset through bit 7 of the Configuration Option Register, or hard reset via the RESET pin) this pin serves as the memory interface RDY/BSYP pin and is held low (busy state indication) until a positive edge occurs on the MRDY pin, indicating the modem is ready, at which time this pin is set high (ready state indication).
RESET	IC	**Card Reset.** Active high Schmitt Trigger input asserted by the host to request a PC Card reset. When this line is asserted, the Card Configuration Registers are reset and the ~MRES signal is forced low to reset MCU core circuits and registers. The MCU remains in the reset state until the RESET pin is deasserted.
SPKROUT	OA	**Digital Audio Output.** When the Audio bit (CCSR3) in the Configuration and Status Register is a 1, this pin reflects the signal at the SPKRIN pin. When the Audio bit is a 0, this pin is held high.

Table 10. MCU Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
COMMON TO E39 AND TO P39 MCU		
EXTERNAL MEMORY BUS INTERFACE		
A0-A16	OA	**Address Lines 0-16.** A0-A16 are the external memory bus address lines.
D0-D7	IA/OA	**Data Line 0-7.** D0-D7 are the external memory bus data lines.
~READ	OA	**Read Enable.** ~READ output low enables data transfer from the selected device to the D0-D7 lines.
~WRITE	OA	**Write Enable.** ~WRITE output low enables data transfer from the D0-D7 lines to the selected device.
~DPSEL	OA	**Modem Data Pump Select.** ~DPSEL output low selects the MDP.
~RAMSEL	OA	**RAM Select.** ~RAMSEL output low selects the external 32k-byte RAM.
~ROMSEL	OA	**ROM Select.** ~ROMSEL output low selects an external 128k-byte ROM or flash ROM.
MISCELLANEOUS		
READY	OA	**Ready.** The MCU resets READY low to indicate that it is busy initializing the modem after power up, reset, or release from low power stop mode. The MCU sets READY high upon completion of this initialization.
NVRAM INTERFACE		
NVMCLK	OA	**NVRAM Clock.** NVMCLK output high enables the NVRAM.
NVMDATA	IA/OA	**NVRAM Data.** The NVMDATA pin supplies a serial data interface to the NVRAM.
TELEPHONE LINE INTERFACE (WIRELINE OPERATION ONLY)		
~RLY1	OA	**Relay 1 Control (~OH).** When cellular interface is not selected (CELL/DAA = high), PE0 is assigned to the ~RLY1 output signal. The active low ~RLY1 output can be used to control the normally open off-hook relay. The ~PULSE function can alternatively be provided on this line in addition to the ~OH function for single ~OH/~PULSE relay application.
~RLY2	OA	**Relay 2 Control (~PULSE).** When cellular interface is not selected (CELL/DAA = high), PE1 is assigned to the ~RLY2 output signal. The active low ~RLY2 output can be used to control the normally open pulse dial relay. The ~PULSE function can alternatively be provided on the ~RLY1 line in addition to the ~OH function for single ~OH/~PULSE relay application.
~RLY3	OA	**Relay 3 Control (~A/A1, ~MUTE).** The active low ~RLY3 output can be used to control the normally open key telephone hold indicator (A/A1) relay. In W-class, ~RLY3 output can be used to control the normally open mute relay.
~RLY4	OA	**Relay 4 Control (~T/DRLY, ~EARTH).** The active low ~RLY4 output can be used to control the normally closed talk/data relay. In W-class, ~RLY4 output can be used to control the normally open earthing relay.
LCS	IA	**Loop Current Sense.** LCS is an active high input that indicates a handset off-hook status.

Table 10. MCU Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
COMMON TO E39 AND TO P39 MCU (CONTINUED)		
DAA/CELLULAR SELECT		
DAA/CELL	IA	**DAA/Cellular Interface Select.** When DAA/CELL input is high, the wireline DAA interface is selected. When DAA/CELL input is low, the cellular interface is selected with the following cellular signals assigned to the corresponding ports instead of the wireline signals.

MCU Port	Cellular Signal (DAA/CELL = Low)	Wireline Signal for E39 MCU DTE Serial Interface (DAA/CELL = High)	Wireline Signal for E39 MCU Host Parallel Interface or P39 MCU PCMCIA Interface (DAA/CELL = High)
PE0	CTRL0	~OH	~OH
PE1	CTRL1	~PULSE	~PULSE
PE2	CELBSY	~MUTE, ~A/A1	~MUTE, ~A/A1
PE5	CELDATA	~CLKSTOP	None
PE7	DAA/CELL	IDID*	IDID*
PA3	~CELBSY	None	None
PA4	CELCLK	None	None

* Used during reset initialization only.

CELLULAR PHONE INTERFACE (CELLULAR OPERATION ONLY)		
CTRL0	OA	**Cellular Control 0.** When cellular interface is selected (CELL/DAA = low), PE0 is assigned to the CTRL0 output signal. CTRL0 is defined by the cellular firmware driver.
CTRL1	OA	**Cellular Control 1.** When cellular interface is selected (CELL/DAA = low), PE1 is assigned to the CTRL1 output signal. CTRL1 is defined by the cellular firmware driver.
CELCLK	IA	**Cellular Clock.** When cellular interface is selected (CELL/DAA = low), PA4 is assigned to the CELCLK input signal. CELCLK is defined by the cellular firmware driver.
CELDATA	IA/OA	**Cellular Data.** When cellular interface is selected (CELL/DAA = low), PE5 is assigned to the bidirectional CELDATA line. CELDATA is defined by the cellular firmware driver.
CELBSY	OA	**Cellular Busy.** When cellular interface is selected (CELL/DAA = low), PE2 is assigned to the CELBSY output signal. CELBSY is defined by the cellular firmware driver.
~CELBSY	IA	**Cellular Not Busy.** When cellular interface is selected (CELL/DAA = low), PA3 is assigned to the ~CELBSY input signal. ~CELBSY is defined by the cellular firmware driver.

Table 11. MDP Signal Definitions

Label	I/O Type	Signal/Definition
		OVERHEAD SIGNALS
XTLI, XTLO	I, O	**Crystal In and Crystal Out.** Connect to an external crystal circuit consisting of a 35.2512 MHz crystal, three capacitors, a resistor, and an inductor; or connect to a square wave generator/sine wave oscillator.
YCLK	O	**Crystal Divide by Four Out.** This output is the MDP Crystal In frequency divided by four. This output is not used and should be left open (no external connection).
XCLK	O	**Crystal Divide by Two Out.** This output is the MDP Crystal In frequency divided by two. This output is not used and should be left open (no external connection).
~POR1, ~POR2	IA	**Power-On Reset.** ~POR1 and ~POR2 low hold the modem in the reset state. ~POR1 and ~POR2 must be low for at least 3 µs. ~POR1 and ~POR2 going high initiates internal hardware normal operation (but not modem processing). For parallel interface, the ~POR inputs are typically connected to the host bus RESET line through an inverter. For PCMCIA interface, connect ~POR1 and ~POR2 to the P39 MCU or PICA ~RES output.
~RESIN	OA	**Reset Input.** Connect ~RESIN to ~RESOUT.
VC	MI	**Centerpoint Voltage.** Connect to analog ground through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel.
VREF	MI	**Voltage Reference.** Connect to VC through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel.
DETOUT	MI	**Detected Level Out.** No external connection.
DETIN	MI	**Detected Level In.** Connect to VCC (+5VDC).
VDDR	MI	**Digital Supply Voltage Regulated.** Connect to VCC (+5VDC).
GND	GND	**Digital Ground.** Connect to ground.
AGND	GND	**Analog Ground.** Connect to analog ground.
VDD1, VDD2	PWR	**DSP Digital Supply Voltage.** Connect to VCC (+5VDC).
DVDD	PWR	**IA Digital Circuits Power.** Connect to VCC (+5VDC).
AVDD1	PWR	**IA Digital Supply Voltage 1.** Connect to VCC (+5VDC).
AVDD2	PWR	**IA Digital Supply Voltage 2.** Connect to VCC (+5VDC) through RC filter.
VAAOUT	MI	**Analog Supply Voltage Output.** Connect to VAA1 and VAA2.
VAA1, VAA2	PWR	**Analog Supply Voltage.** Connect to VAAOUT. Connect to analog ground through 10 µF and 0.1 µF capacitors in parallel.
REGOUT	MI	**Regulator Out.** No external connection.
REGIN	MI	**Regulator In.** Connect to ground.
CAPP	MI	**Capacitor Plus Connection.** No external connection.
CAPN	MI	**Capacitor Negative Connection.** No external connection.
		MCU INTERFACE
D0–D7	IA/OB	**Data Lines.** Connect to the MCU D0-D7, respectively.
RS0–RS4	IA	**Register Select Lines.** Connect to the MCU A0–A4, respectively.
~CS	IA	**Chip Select.** Connect to MCU ~DPSEL output.
~READ	IA	**Read Enable.** Connect to MCU ~READ.
~WRITE	IA	**Write Enable.** Connect to MCU ~WRITE.
IRQ	OA	**Interrupt Request.** Connect to MCU DPIRQ.
~RESOUT	OA	**Reset Output.** ~RESOUT going high indicates internal hardware normal operation has been attained and initiates internal modem processing. The MDP is ready to use 500 ms after the low-to-high transition of ~RESOUT. Connect to the ~RESIN pin. For PCMCIA operation, connect to the E39 MCU ~RES input.

Table 11. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		COMMON TELEPHONE LINE AND CELLULAR PHONE SIGNALS
TXA1, TXA2	O(DF)	**Transmit Analog 1 and 2.** The TXA1 and TXA2 outputs are differential outputs 180 degrees out of phase with each other. Each output can drive a 300 Ω load.
RIN	I(DA)	**Receive Analog.** RIN is a single-ended receive data input from the telephone line interface or an optional external hybrid circuit.
		TELEPHONE LINE INTERFACE ONLY SIGNALS
RINGD	IA	**Ring Detect.** The RINGD input is monitored for pulses in the range of 15 Hz to 68 Hz. The frequency detection range may be changed by the host in DSP RAM. The circuit driving RINGD should be a 4N35 optoisolator or equivalent. The circuit driving RINGD should not respond to momentary bursts of ringing less than 125 ms in duration, or less than 40 VRMS (15 Hz to 68 Hz) across TIP and RING. Detected ring signals are reflected on the ~RI output signal as well as the RI bit.
~RLYA (~OHRC)	OD	**Relay A Control.** For Caller ID application, the MDP ~RLYA output is connected to the normally closed Caller ID relay (DPDT). When Caller ID is enabled, the modem will assert this output to open the Caller ID relay and close the off-hook relay in order to detect Caller ID information between the first and second rings. The ~RLYA output can each directly drive a +5V reed relay coil with a minimum resistance of 360 ohms and having a must-operate voltage of no greater than 4.0 Vdc. A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor, such as an MPSA20, can be used to drive heavier loads (e.g., electro-mechanical relays). ~RLYA is controlled by the MCU setting/resetting of the RA bit.
~RLYB (~TALK)	OD	**Relay B Control.** For voice application, the MDP ~RLYB output is connected to the normally open Voice relay (DPDT). In voice mode, ~VOICE active closes the relay to switch the handset from the telephone line to a current source to power the handset so it can be used as a microphone and speaker interface to the modem. The ~RLYB output can each directly drive a +5V reed relay coil with a minimum resistance of 360 ohms and having a must-operate voltage of no greater than 4.0 Vdc. A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor, such as an MPSA20, can be used to drive heavier loads (e.g., electro-mechanical relays). ~RLYB is controlled by the MCU setting/resetting of the RB bit.
		SPEAKER INTERFACE
SPKR	O(DF)	**Speaker Analog Output.** The SPKR output reflects the received analog input signal. The SPKR is controlled by the ATMn command. The SPKR output can drive an impedance as low as 300 ohms. For PCMCIA interface, the SPKR is typically connected to a analog to digital conversion circuit.
		DIAGNOSTIC SIGNALS Three signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified.
EYEXY	OA	**Serial Eye Pattern X/Y Output.** EYEXY is a serial output containing two 15-bit diagnostic words (EYEX and EYEY) for display on the oscilloscope X axis (EYEX) and Y axis (EYEY). EYEX is the first word clocked out; EYEY follows. Each word has 8-bits of significance. Each 15-bit data word is shifted out most significant bit first with the seven most significant bits set to zero. EYEXY is clocked by the rising edge of ~EYECLK. This serial digital data must be converted to parallel digital form by a serial-to-parallel converter, and then to analog form by two digital-to-analog (D/A) converters.
~EYECLK	OA	**Serial Eye Pattern Clock.** ~EYECLK is a 288 kHz output clock for use by the serial-to-parallel converters. The low-to-high transitions of ~RDCLK coincide with the low-to-high transitions of ~EYECLK. ~EYECLK, therefore, can be used as a receiver multiplexer clock.
EYESYNC	OA	**Serial Eye Pattern Strobe.** EYESYNC is a strobe for loading the D/A converters. Connect EYESYNC to the GP0 pin.

Table 11. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		DTE SERIAL/CONTROL/INDICATOR SIGNALS
TXD	IA	**Transmitted Data.** PIF: Not used; leave open.
RXD	OA	**Received Data.** PIF: Not used; leave open.
TDCLK	OA	**Transmit Data Clock.** PIF: Not used; leave open. SIF: Connect to the DTE IF TDCLK signal.
XTCLK	IA	**External Transmit Clock.** PIF: Not used; leave open. SIF: Connect to the DTE IF XTCLK signal.
~RDCLK	OA	**Receive Data Clock.** PIF: Not used; leave open. SIF: Connect to the DTE IF ~RDCLK signal.
~RLSD	OA	**Received Line Signal Detector.** PIF: Not used, leave open. SIF: Connect to the ~RLSD indicator circuit.
~RTS	IA	**Request to Send.** PIF: Not used; pull up to VCC through 20k Ω.
~DTR	IA	**Data Terminal Ready.** Not used; pull up to VCC through 20k Ω.
~CTS	OA	**Clear to Send.** Not used; leave open.
~DSR	OA	**Data Set Ready.** Not used; leave open.
~RI	OA	**Ring Indicate.** Not used; leave open.
		REFERENCE SIGNALS AND MODEM INTERCONNECT
SR1IO	MI	**SR1IO.** Connect to RMODE and TMODE.
TMODE	MI	**Transmitter Mode.** Connect to SR1IO.
RMODE	MI	**Receiver Mode.** Connect to SR1IO.
SR3IN	MI	**SR3IN.** Connect to RXOUT.
RXOUT	MI	**Receive Data.** Connect to SR3IN.
SR4OUT	MI	**SR4OUT.** Connect to TXDAT.
TXDAT	MI	**Transmit Data.** Connect to SR4OUT.
PB0	MI	**PB0.** Connect to CLKIN.
CLKIN	MI	**Clock.** Connect to PB0.
IA1CLK	MI	**IA1CLK.** Connect to TSTROBE.
TSTROBE	MI	**Transmitter Strobe.** Connect to IA1CLK.
SA1CLK	MI	**SA1CLK.** Connect to TRESET.
TRESET	MI	**Transmitter Reset.** Connect to SA1CLK.
SLEEP	MI	**Sleep.** Connect to PF5.
PF5	MI	**PF5.** Connect to SLEEP.
GP0	MI	**GP0.** Connect to EYESYNC.

Table 12. Digital Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions [1]
Input High Voltage	V_{IH}				VDC	
Type IA		2.0	–	V_{CC}		
Type IC		0.7 V_{CC}	–	V_{CC} + 0.3		
Type ID		0.8 V_{CC}	–	V_{CC} + 0.3		
Type IE		–	4.0	–		Note 2.
Input Low Voltage	V_{IL}				VDC	
Type IA, 1C, and ID		–0.3		0.8		
Type IE		–	1.0	–		Note 2.
Input High Current	I_{IH}			40	µA	V_{IN} = 5.25V, V_{CC} = 5.25V,
Input Low Current	I_{IL}			400	µA	V_{CC} = 5.25V
Input Leakage Current	I_{IN}				µADC	V_{IN} = 0 to 5V, V_{CC} = 5.25V
~RES and PD0-PD7		–	–	±2.5		
XTLI		–	–	±10		
~NMI and ~TST		–	–	±100		
Output High Voltage	V_{OH}				VDC	
Type OA and OB		2.4	–	–		I_{LOAD} = – 100 µA
Type OD		–	–	V_{CC}		I_{LOAD} = 0 mA
Type OE						Note 3.
Output Low Voltage	V_{OL}				VDC	
Type OA		–	–	0.4		I_{LOAD} = 1.6 mA
Type OB		–	–	0.4		I_{LOAD} = 0.8 mA
Type OD		–	–	0.75		I_{LOAD} = 15 mA
Three-State (Off) Current	I_{TSI}			±10	µADC	V_{IN} = 0 V to V_{CC}

Notes:

1. Test Conditions: VCC = 5V ± 5%
   TA = 0°C to 70°C, (unless otherwise stated).
   Output loads: Data bus (D0-D7), address bus (A0-A15), chip selects, ~READ, and ~WRITE loads = 70 pF + one TTL load.
   Other = 50 pF + one TTL load.
2. Type IE inputs are centered approximately 2.5 V and swing 1.5 V_{PEAK} in each direction.
3. Type OE outputs provide oscillator feedback when operating with an external crystal.

Table 13. Analog Electrical Characteristics

Name	Type	Characteristic	Value
RIN	I (DA)	Input Impedance	> 70K Ω
		AC Input Voltage Range	1.1 VP-P**
		Reference Voltage	+2.5 VDC
TXA1, TXA2	O (DD)	Minimum Load	300 Ω
		Maximum Capacitive Load	0 µF
		Output Impedance	10 Ω
		AC Output Voltage Range	2.2 VP-P
		Reference Voltage	+2.5 VDC
		DC Offset Voltage	± 200 mV
SPKR	O (DF)	Minimum Load	300 Ω
		Maximum Capacitive Load	0.01 µF
		Output Impedance	10 Ω
		AC Output Voltage Range	1.1 VP-P
		Reference Voltage	+2.5 VDC
		DC Offset Voltage	± 20 mV

* Reference Voltage provided internal to the MDP.
** Corresponds to 2.2 VP-P at Tip and Ring.

Table 14. Current and Power Requirements

Mode	Current (ID)			Power (PD)			Notes
	Typical Current @ 25°C (mA)	Maximum Current @ 0°C (mA)	Maximum Current @ -40°C (mA)	Typical Power @ 25°C (mW)	Maximum Power @ 0°C (mW)	Maximum Power @ -40°C (mW)	
E39 MCU							
MCU							f_{IN} = 8.064 MHz
Normal mode	24	30.5	34.3	120	160	180	
Sleep mode	2.2	2.7	2.8	11.0	14.2	14.7	
Stop mode	0.15	0.2	0.2	0.8	1.1	1.1	
MDP							f_{IN} = 35.2512MHz
Normal mode	45	54	68	225	285	355	
Sleep mode	2.0	2.4	3.1	10.0	12.6	16.3	
Total							
Normal mode	69	84.5	102.3	345	445	535	
Sleep mode	4.2	5.1	5.9	21.0	26.8	31.0	
Stop mode	2.15	2.6	3.3	10.8	13.7	17.4	
P39 MCU							
MCU							f_{IN} = 8.064 MHz
Normal mode	30	34	35	150	180	185	
Sleep mode	2.2	2.7	2.8	11.0	14.2	14.7	
Stop mode	0.15	0.2	0.2	0.8	1.1	1.1	
MDP							f_{IN} = 35.2512MHz
Normal mode	45	54	68	225	285	355	
Sleep mode	2.0	2.4	3.1	10.0	12.6	16.3	
Total							
Normal mode	75	88	103	375	465	540	
Sleep mode	4.2	5.1	5.9	21.0	26.8	31.0	
Stop mode	2.15	2.6	3.3	10.8	13.7	17.4	

Notes:
1. Maximum power @ -40°C specified only for extended temperature range parts.
2. Test conditions: VCC = 5.0 VDC for typical values; VCC = 5.25 VDC for maximum values.

Table 15. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to (+5VD +0.5)	V
Operating Temperature Range	T_A		°C
Commercial		-0 to +70	
Extended		-40 to +85	
Storage Temperature Range	T_{STG}	-55 to +125	°C
Analog Inputs	V_{IN}	-0.3 to (+5VA + 0.3)	V
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (+5VD + 0.5)	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	V
Latch-up Current (25°C)	I_{TRIG}	±200	mA

Table 16. Parallel Interface Registers

Register No.	Register Name	Bit No. 7	6	5	4	3	2	1	0
7	Scratch Register (SCR)	Scratch Register							
6	Modem Status Register (MSR)	Data Carrier Detect (DCD)	Ring Indicator (RI)	Data Set Ready (DSR)	Clear to Send (CTS)	Delta Data Carrier Detect (DDCD)	Trailing Edge of Ring Indicator (TERI)	Delta Data Set Ready (DDSR)	Delta Clear to Send (DCTS)
5	Line Status Register (LSR)	RX FIFO Error	Transmitter Empty (TEMT)	Transmitter Buffer Register Empty (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	Receiver Data Ready (DR)
4	Modem Control Register (MCR)	0	0	0	Local Loopback	Out 2	Out 1	Request to Send (RTS)	Data Terminal Ready (DTR)
3	Line Control Register (LCR)	Divisor Latch Access Bit (DLAB)	Set Break	Stick Parity	Even Parity Select (EPS)	Parity Enable (PEN)	Number of Stop Bits (STB)	Word Length Select Bit 1 (WLS1)	Word Length Select Bit 0 (WLS0)
2	Interrupt Identify Register (IIR) (Read Only)	FIFOs Enabled	FIFOs Enabled	0	0	Pending Interrupt ID Bit 2	Pending Interrupt ID Bit 1	Pending Interrupt ID Bit 0	"0" if Interrupt Pending
2	FIFO Control Register (FCR) (Write Only)	Receiver Trigger MSB	Receiver Trigger LSB	Reserved	Reserved	DMA Mode Select	TX FIFO Reset	RX FIFO Reset	FIFO Enable
1 (DLAB = 0)	Interrupt Enable Register (IER)	0	0	0	0	Enable Modem Status Interrupt (EDSSI)	Enable Receiver Line Status Interrupt (ELSI)	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Enable Received Data Available Interrupt (ERBFI)
0 (DLAB = 0)	Transmitter Buffer Register (THR)	Transmitter FIFO Buffer Register (Write Only)							
0 (DLAB = 0)	Receiver Buffer Register (RBR)	Receiver FIFO Buffer Register (Read Only)							
1 (DLAB = 1)	Divisor Latch MSB Register (DLM)	Divisor Latch MSB							
0 (DLAB = 1)	Divisor Latch LSB Register (DLL)	Divisor Latch LSB							

PCMCIA INTERFACE

PCMCIA Interface Functions

Figure 10 shows a block diagram of the MCU PCMCIA interface with a partial block diagram of the MCU core logic. The signals on the left hand side of the diagram show interface signals to the PCMCIA socket.

The memory space of a PCMCIA socket consists of Attribute Memory space, Common Memory space and I/O space. When used in a PCMCIA application, the MCU is placed in the 16550 host bus interface mode and the PCMCIA interface logic provides the host address decoding to interface the proper registers to the PCMCIA socket's I/O space. The PCMCIA interface provides a set of four configuration registers which provide control of various PCMCIA functions as well as status information, and are accessible over the host interface bus in Attribute memory space. Additional PCMCIA functions include: pass-through control of a digital audio signal, pass-through control and integration of a modem ring signal, a power on reset RC network pin, software reset, hardware reset, power down request and control logic, 512 bytes of internal dual port RAM for holding the CIS, and modem status indication and control logic.

PCMCIA Interface Decode Logic

A PCMCIA socket interface provides for three different types of memory space: Common Memory, Attribute Memory and I/O Address Space. The CIS and Card Configuration Registers reside in Attribute Memory Space. Only even address accesses are valid in Attribute Memory. The host memory address space decoding is shown in Table 17. The 16550 interface registers reside in I/O address space.

The host must assert both the Card Enable signal (~CE1) and the Register Select and I/O enable signal (~REG) to access either Attribute Memory or I/O Space. When the host accesses the card's I/O Address Space, the PCMCIA interface decodes the address lines based on the Configuration Index which has been written to the Configuration and Option Register and asserts the internal Modem Chip Select (MCSP) which is internally connected to the 16550 interface's Host Chip Select (~HCS) via PD4. The I/O address space decoding is shown in Table 18.

PCMCIA Configuration Registers

The PCMCIA Configuration Registers are shown in Table 19.

SCHEMATICS

Typical interface schematics for the E39 MCU with seria DTE interface are shown in Figure 11.

Typical interface schematics for the E39 MCU with parallel host interface are shown in Figure 12.

Typical interface schematic for the P39 MCU with PCMCIA interface is shown in Figure 13.

Typical interface schematics for the MDP are shown in Figure 14.

A schematic for a typical line interface circuit is shown in Figure 15.

Figure 16 is a schematic of a typical external hybrid circuit.

A schematic for a typical speaker circuit connected to the MDP SPKR output is shown in Figure 17.

Consult applicable AccelerATor Kits or Reference Designs for full schematics of typical applications.

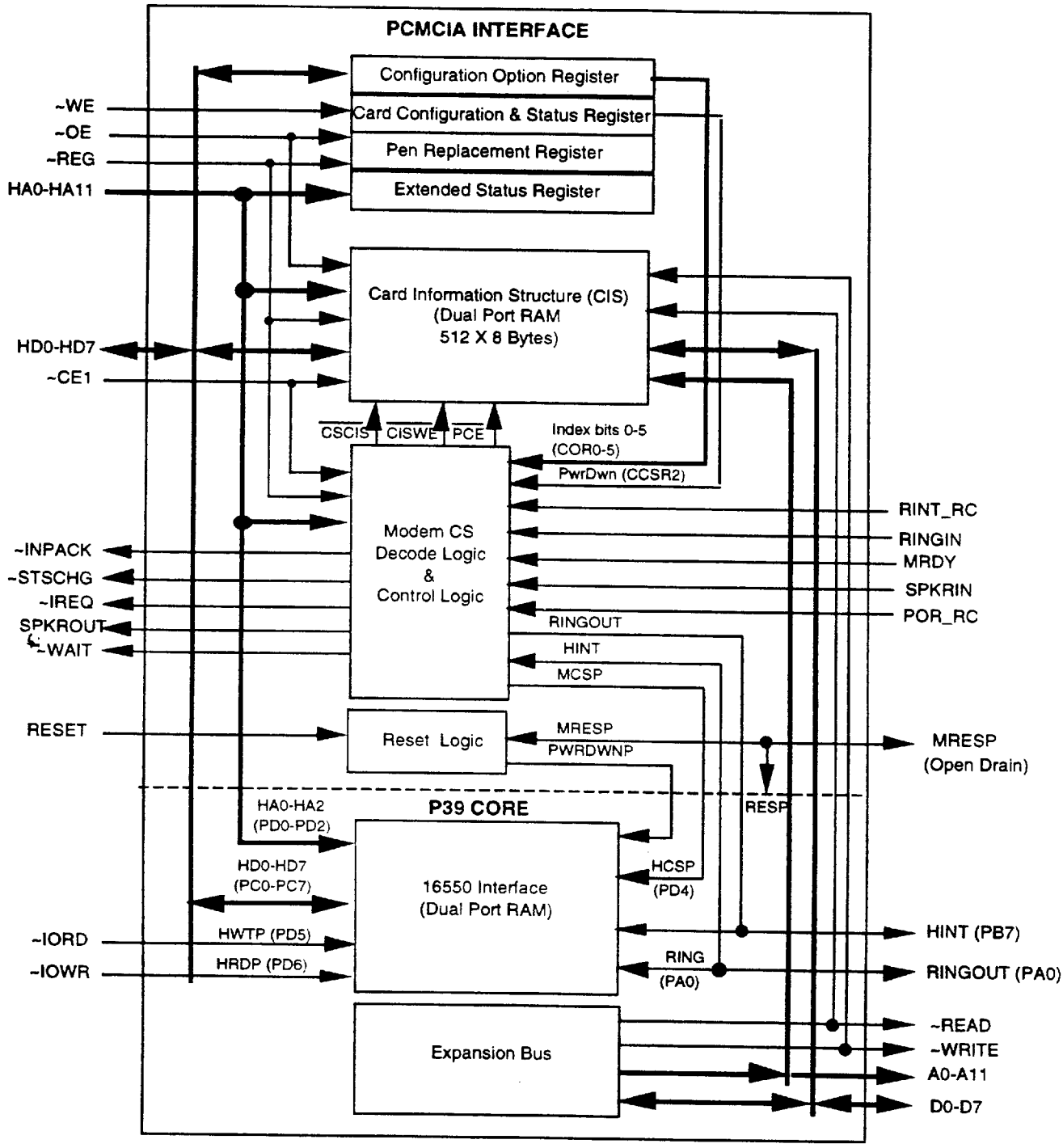


Figure 10. P39 MCU PCMCIA Interface Block Diagram

Table 17. Host Memory Address Space Decoding

Input Line						Selected Register or Space
~CE1	~REG	~OE	~WE	A11 - A0	A0	
H	X	X	X	X	X	Standby.
L	H	X	X	X	X	Common Memory Access. (Not supported).
L	L	X	X	X	H	Invalid Access.
L	L	L	H	000-1FE	L	Host CIS Memory Read (256 bytes).
L	L	H	L	000-1FE	L	Host CIS Memory Write (256 bytes).
L	L	L	H	200		Configuration Option Register (COR) Read.
L	L	H	L	200		Configuration Option Register(COR) Write.
L	L	L	H	202		Card Configuration and Status Register (CCSR) Read.
L	L	H	L	202		Card Configuration and Status Register CCSR) Write.
L	L	L	H	204		Pin Replacement Register (PRR) Read.
L	L	H	L	204		Pin Replacement Register (PRR) Write.
L	L	L	H	208		Extended Status Register (ESR) Read.
L	L	H	L	208		Extended Status Register (ESR) Write.
L	L	L	H	210-40E	L	Host CIS Memory Read (256 bytes).
L	L	H	L	210-40E	L	Host CIS Memory Write (256 bytes).
L	L	L	H	410-FFE	L	Host CIS Memory Read (For future expansion).
L	L	H	L	410-FFE	L	Host CIS Memory Write (For future expansion)

Table 18. I/O Address Space Decoding

~CE1	~REG	~IORD	~IOWR	Selected Register or Space
H	X	X	X	Standby.
L	L	L	H	16550 Interface Register Read.
L	L	H	L	16550 Interface Register Write

Table 19. Configuration Registers Bit Map

Addr. (Hex)	Function	Bit								Default Value
		7	6	5	4	3	2	1	0	
200	Configuration Option Register (COR)	SReset	LevIREQ	Configuration Index						00h
202	Card Configuration and Status Register (CCSR)	Changed	SigChg	0	RingEn	Audio	PwrDwn	Intr	0	00h
204	Pin Replacement Register (PRR)	0	0	CRdy/-Bsy	0	0	0	RRdy/-Bsy	0	00h
206	(Unused)									
208	Extended Status Register (ESR)	0	0	0	ReqAtten	0	0	0	RAENnab	00h

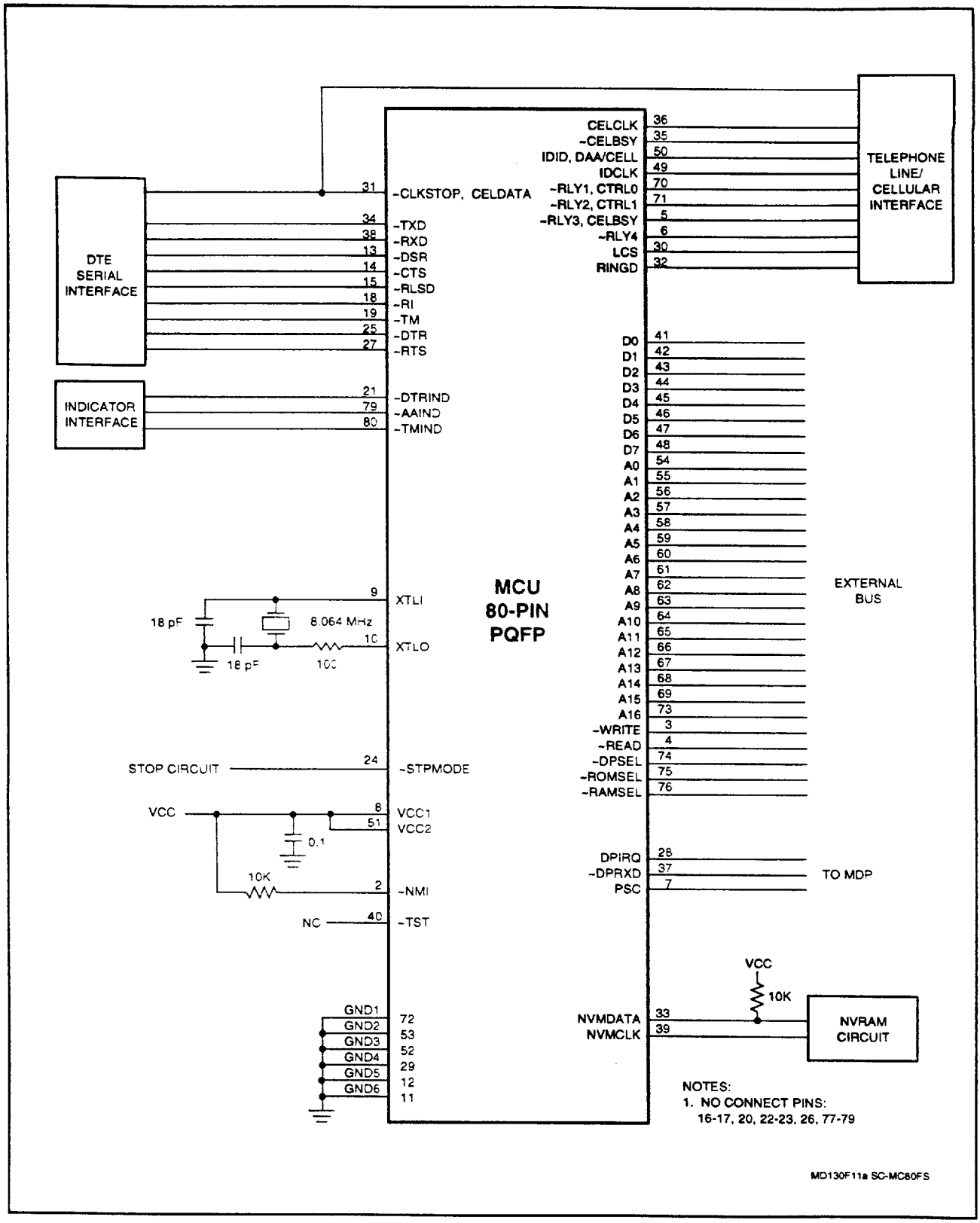


Figure 11a. Interface Schematic - E39 MCU with Serial DTE Interface - 80-Pin PQFP

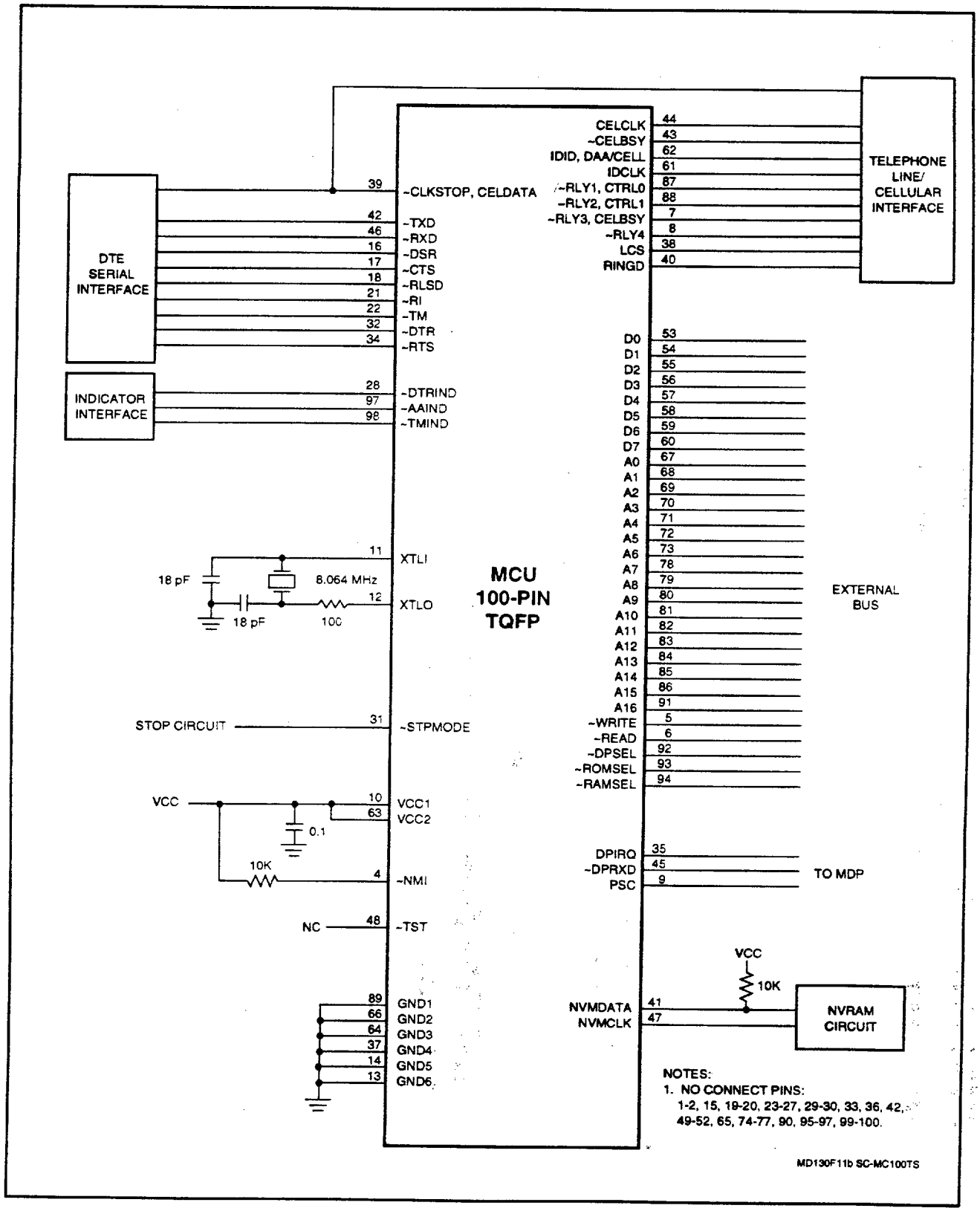


Figure 11b. Interface Schematic - E39 MCU with Serial DTE Interface - 100-Pin TQFP

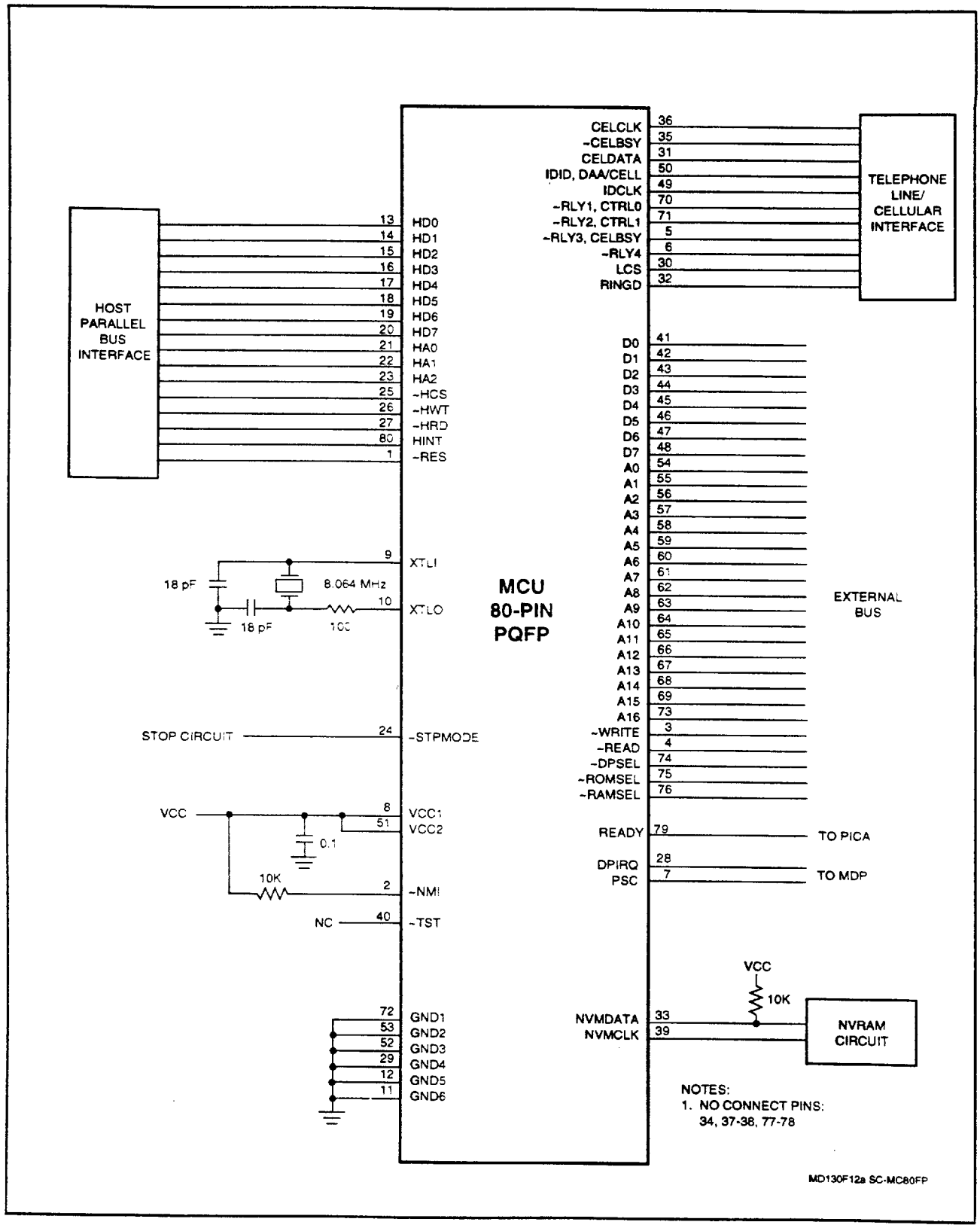


Figure 12a. Interface Schematic - E39 MCU with Parallel Host Interface - 80-Pin PQFP

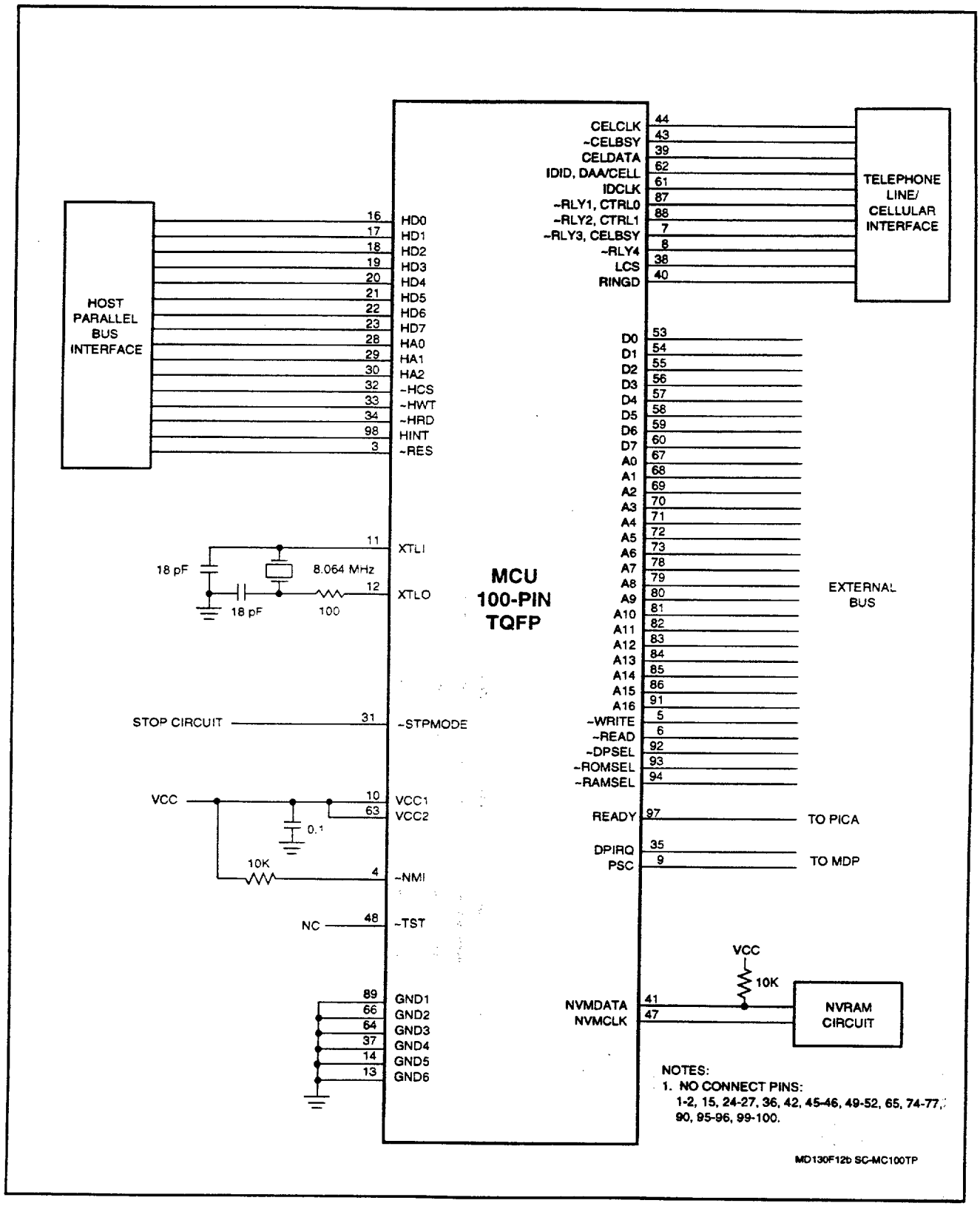


Figure 12b. Interface Schematic - E39 MCU with Parallel Host Interface - 100-Pin TQFP

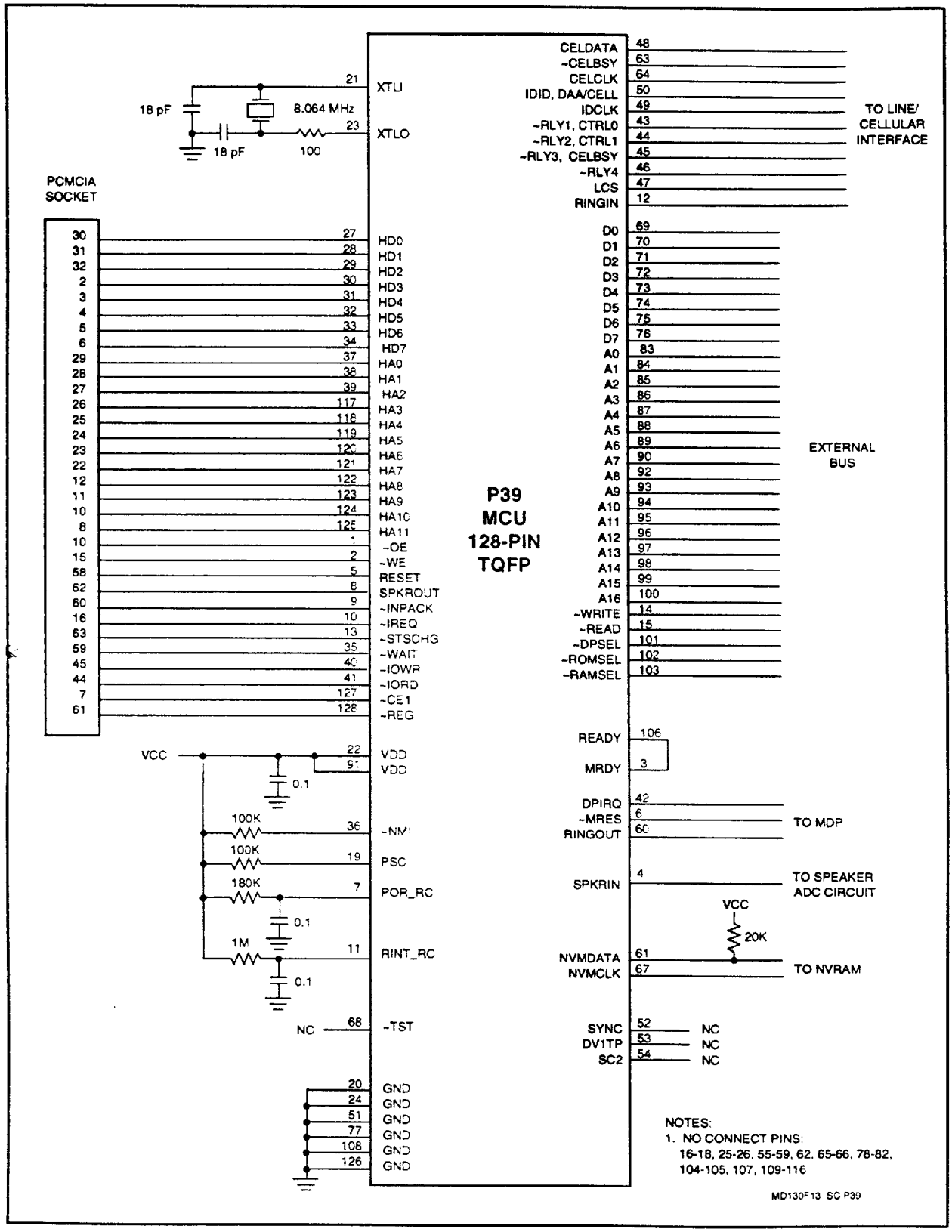


Figure 13. Interface Schematic - P39 MCU with PCMCIA Interface - 128-Pin TQFP

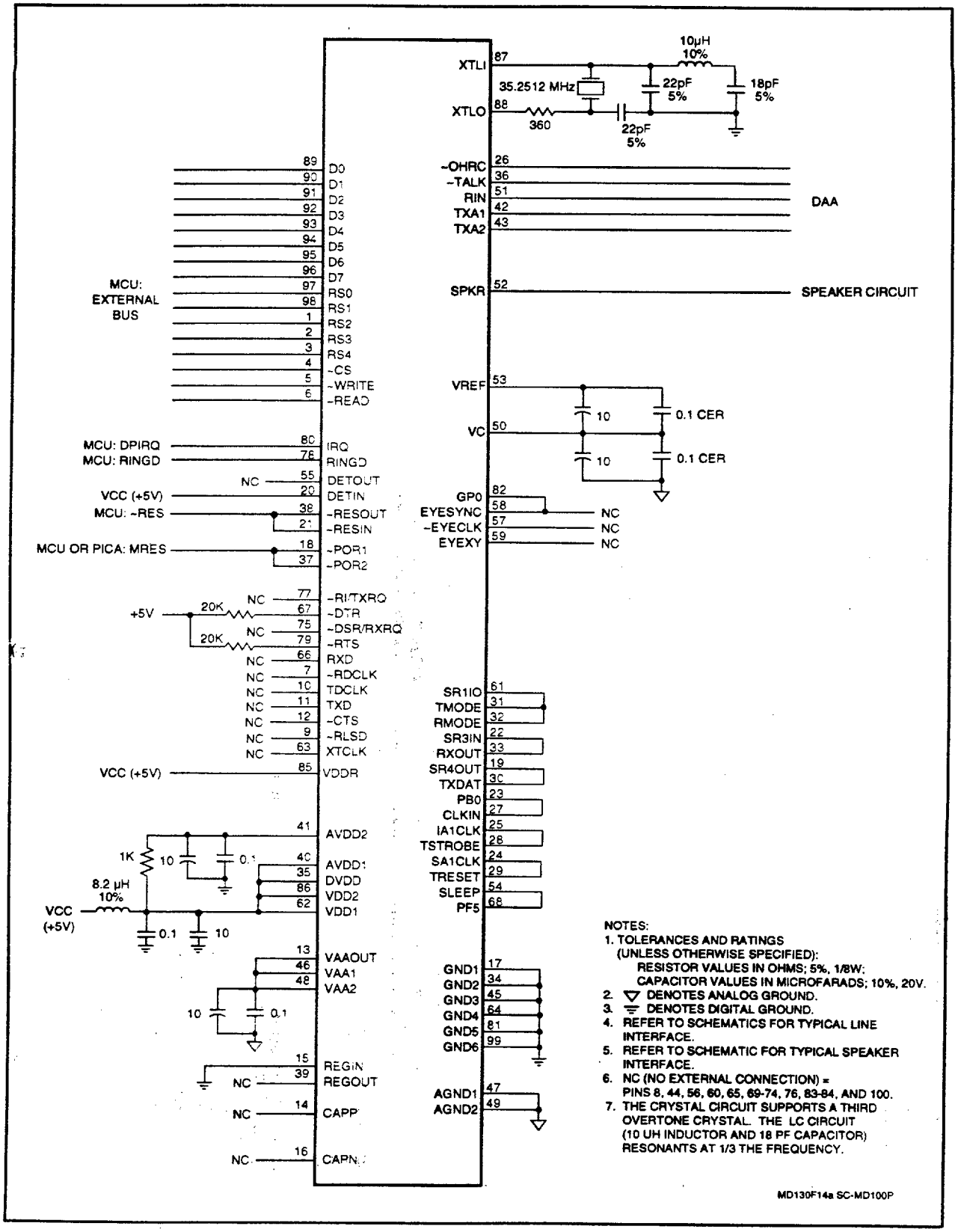


Figure 14a. Interface Schematic - MDP - 100-Pin PQFP (Parallel Host Interface)

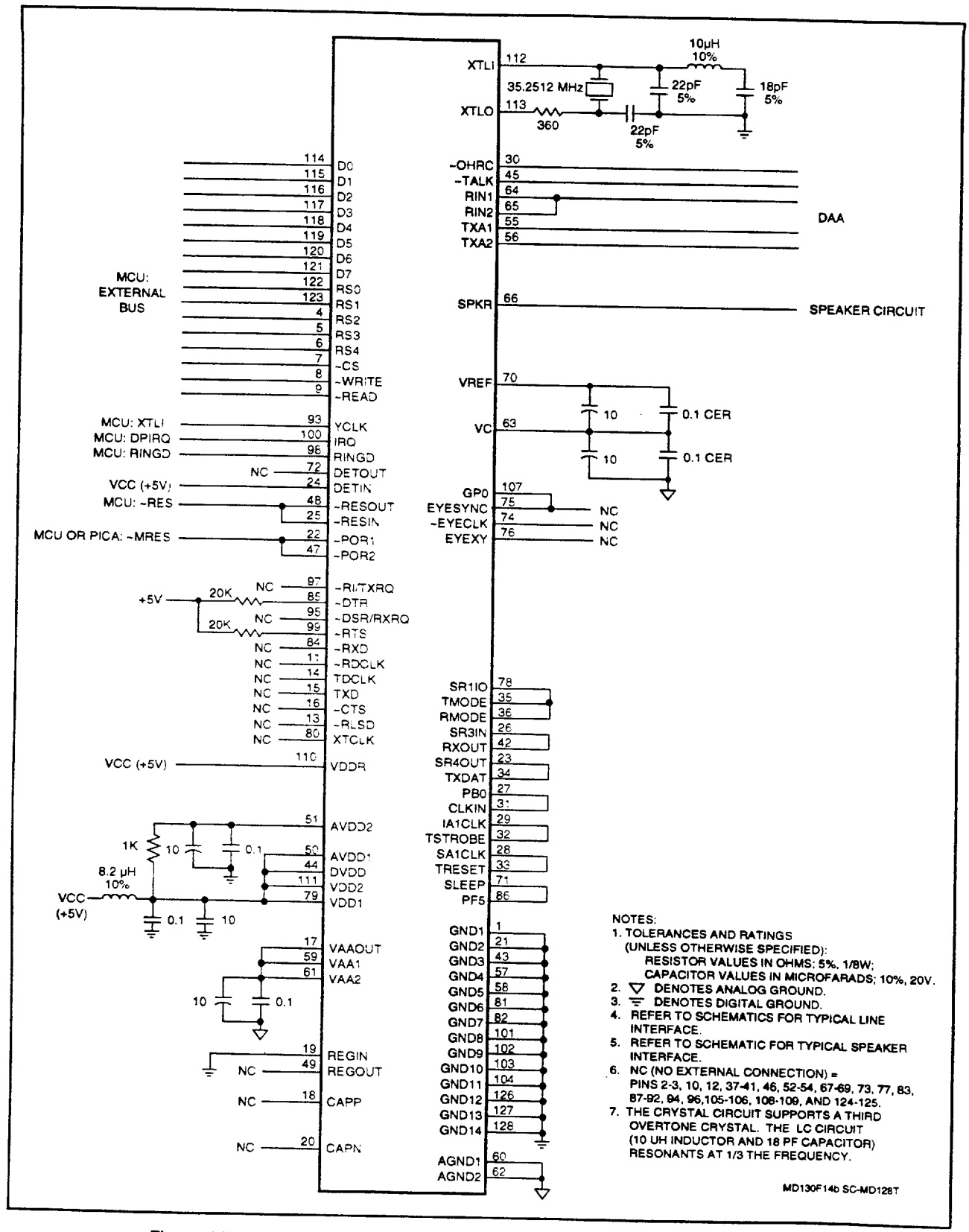


Figure 14b. Interface Schematic - MDP - 128-Pin TQFP (Parallel Host Interface)

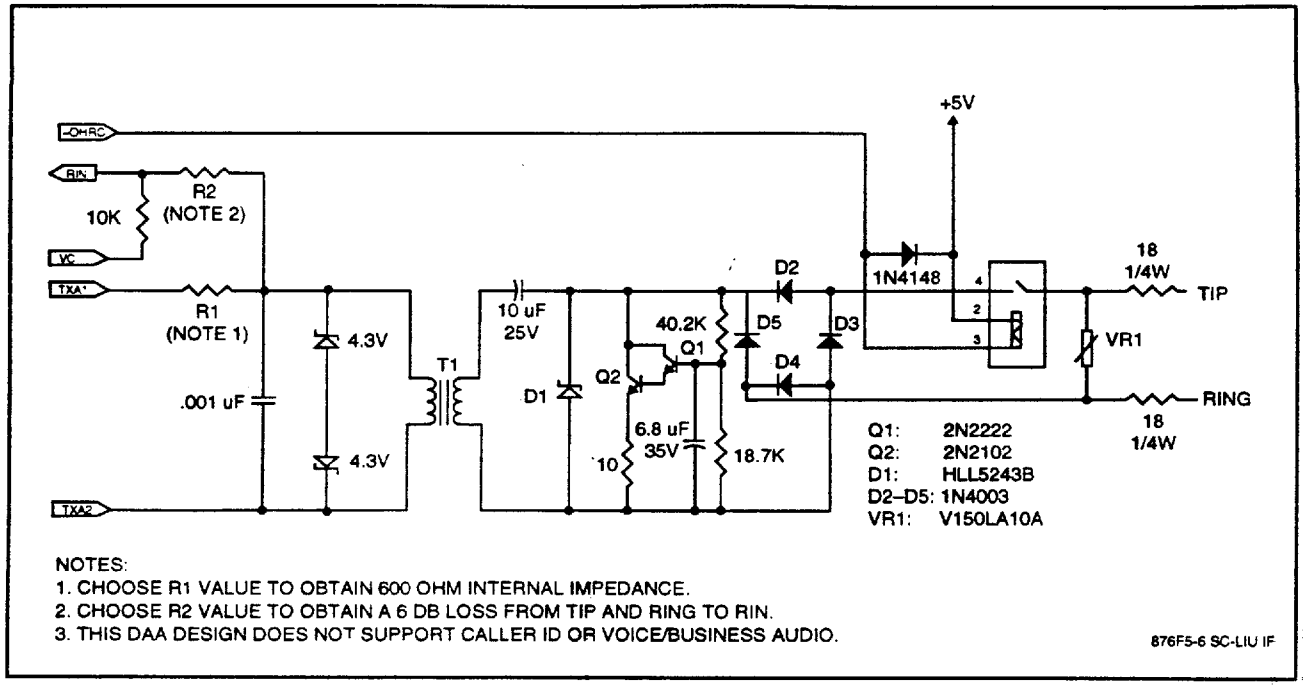


Figure 15. Typical Line Interface

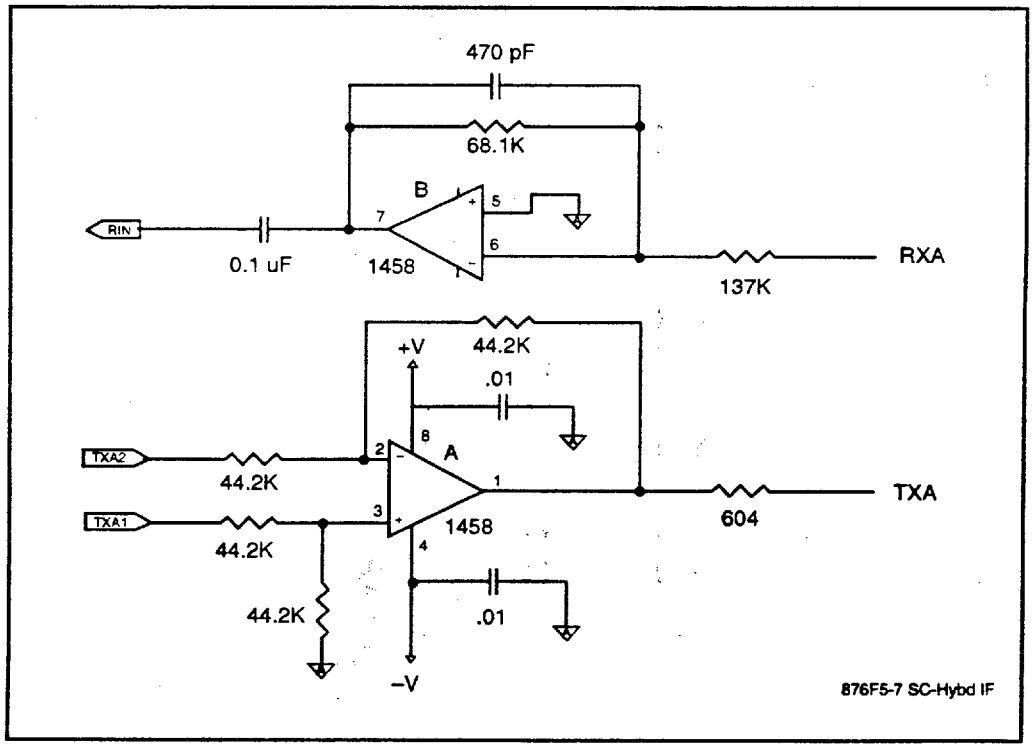


Figure 16. Typical Interface to External Hybrid

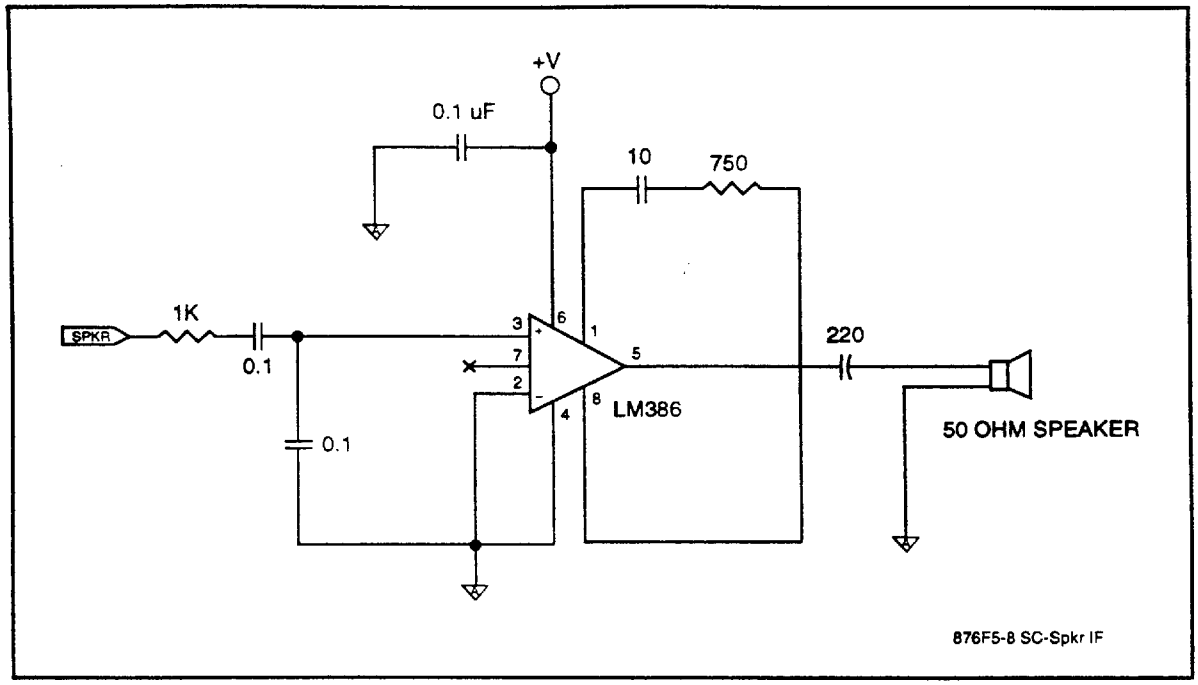
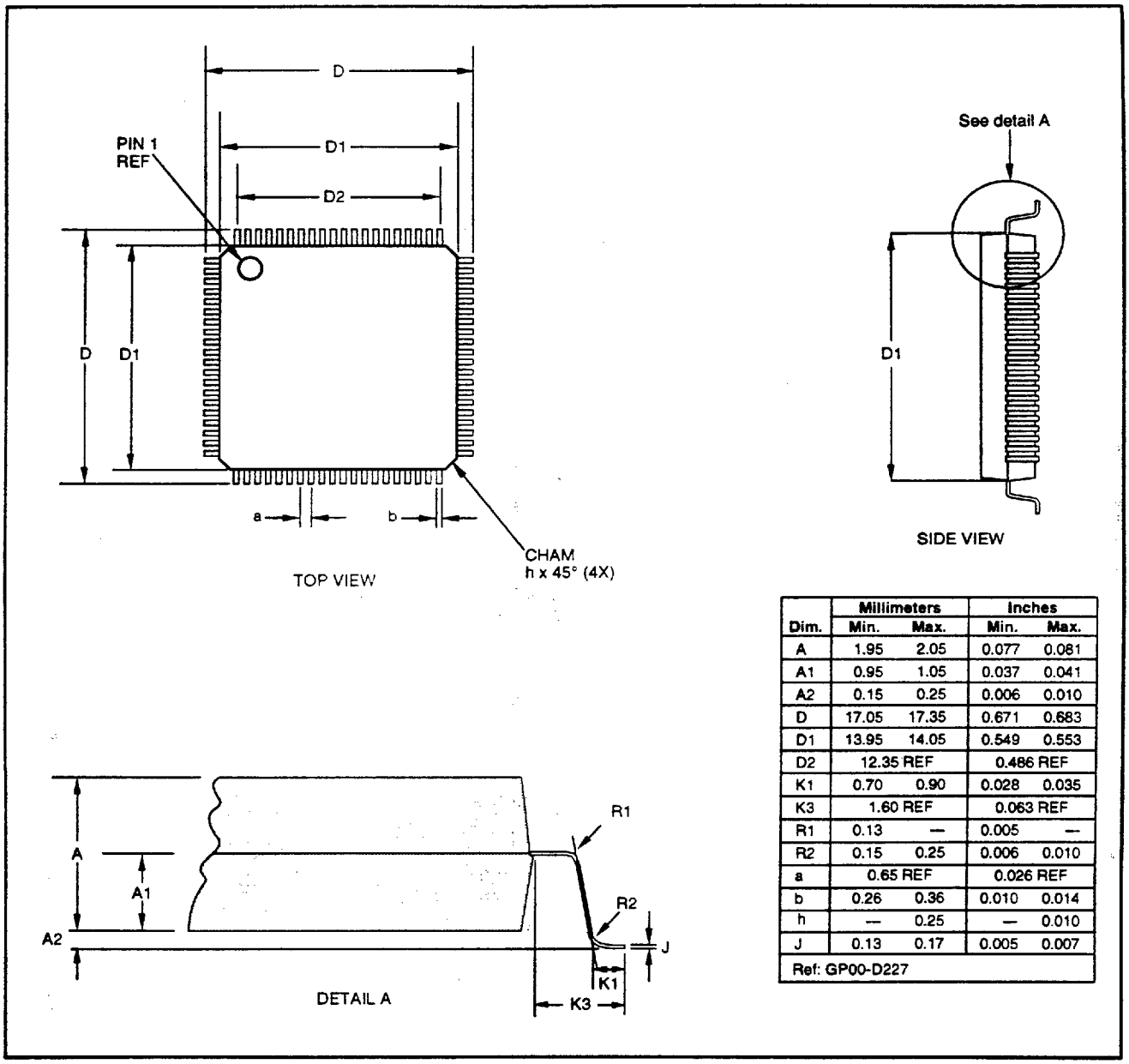


Figure 17. Typical External Speaker Circuit

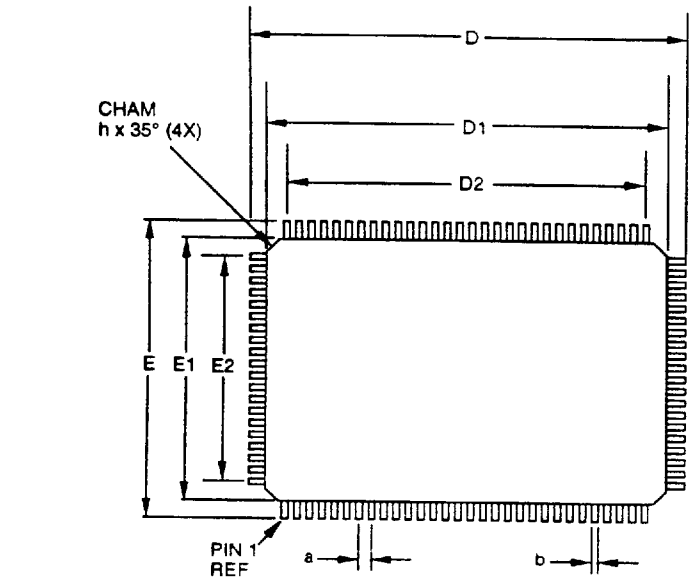
PACKAGE DIMENSIONS

The package dimensions are shown in Figure 18.

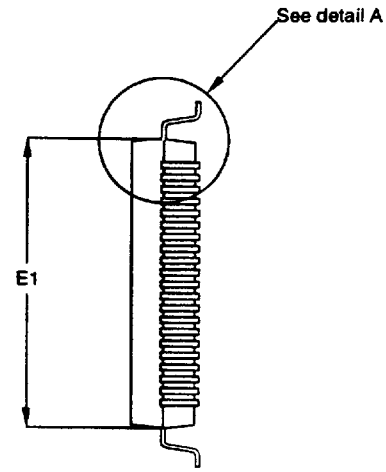


Dim.	Millimeters Min.	Millimeters Max.	Inches Min.	Inches Max.
A	1.95	2.05	0.077	0.081
A1	0.95	1.05	0.037	0.041
A2	0.15	0.25	0.006	0.010
D	17.05	17.35	0.671	0.683
D1	13.95	14.05	0.549	0.553
D2	12.35 REF		0.486 REF	
K1	0.70	0.90	0.028	0.035
K3	1.60 REF		0.063 REF	
R1	0.13	—	0.005	—
R2	0.15	0.25	0.006	0.010
a	0.65 REF		0.026 REF	
b	0.26	0.36	0.010	0.014
h	—	0.25	—	0.010
J	0.13	0.17	0.005	0.007
Ref: GP00-D227				

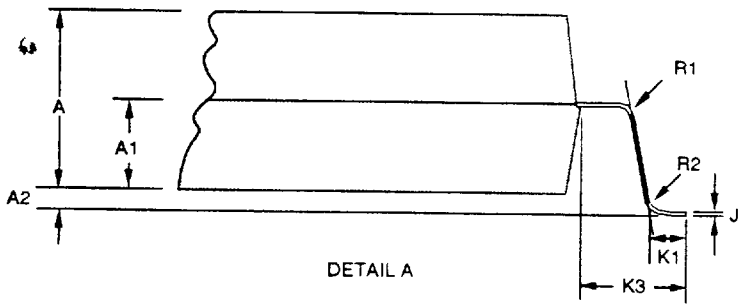
Figure 18a. Package Dimensions - 80-Pin PQFP



TOP VIEW



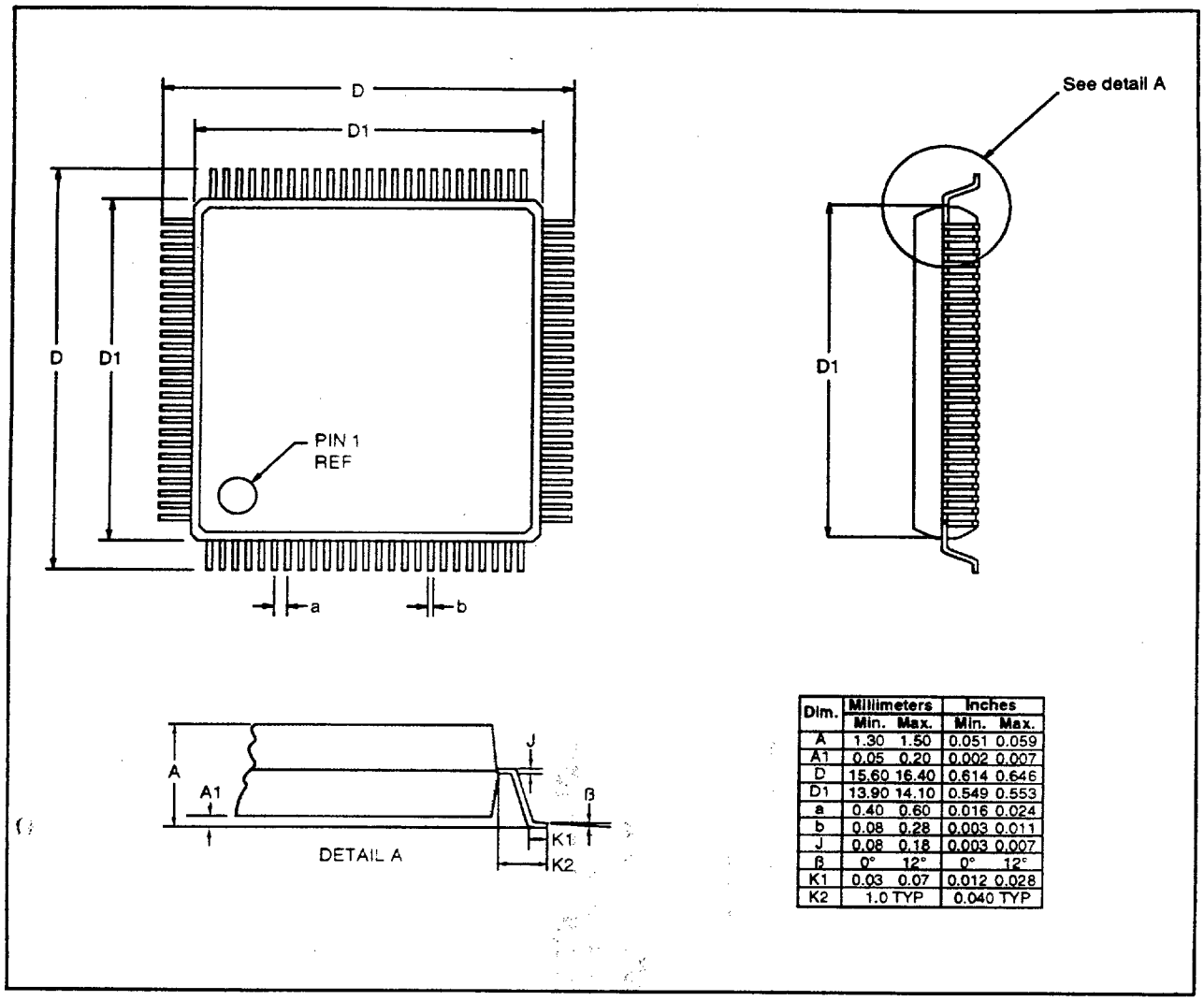
SIDE VIEW



DETAIL A

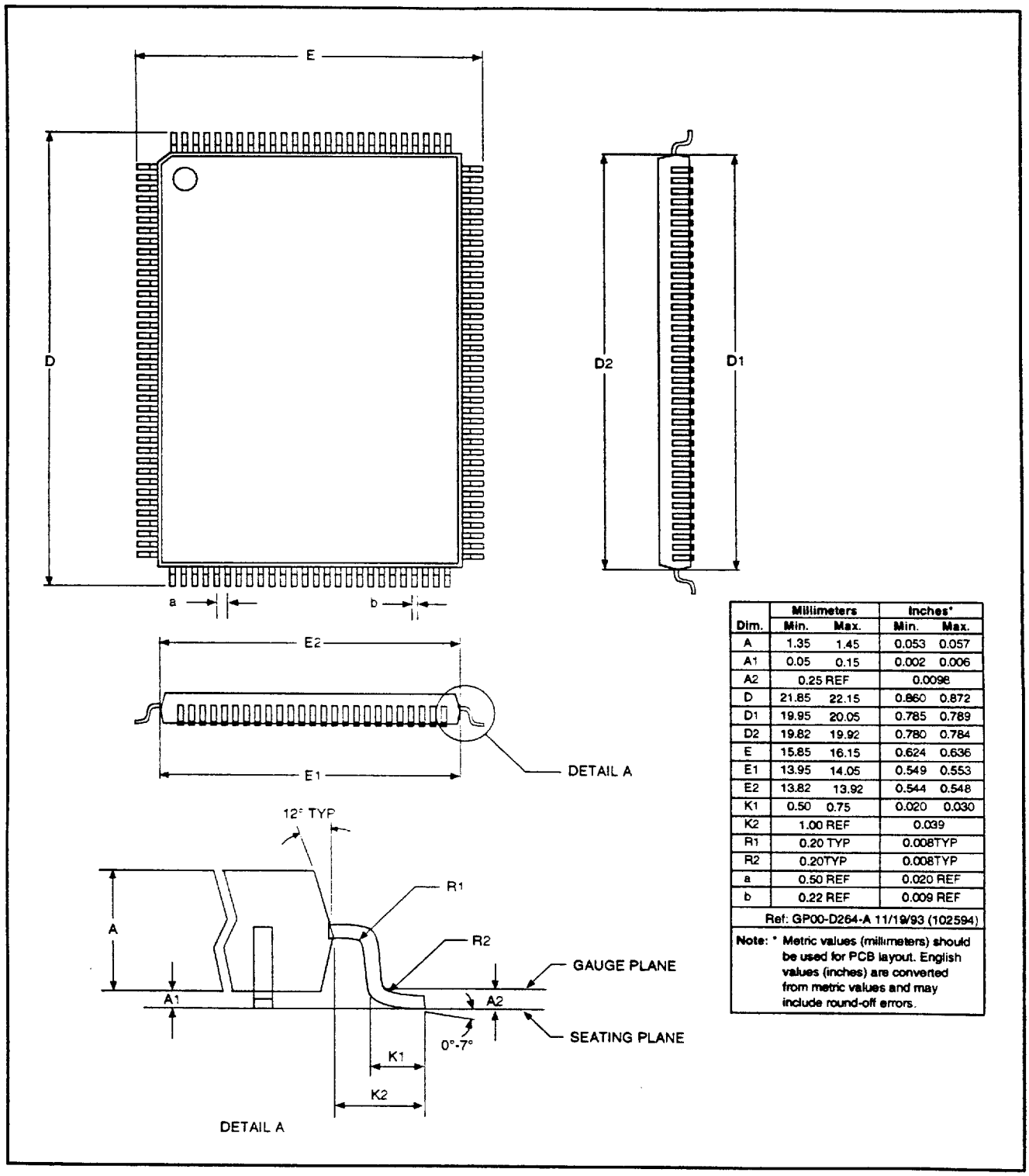
Dim.	Millimeters Min.	Millimeters Max.	Inches Min.	Inches Max.
A	1.95	2.05	0.077	0.081
A1	0.95	1.05	0.037	0.041
A2	0.25 REF		0.010 REF	
D	23.05	23.35	0.907	0.919
D1	19.95	20.05	0.785	0.789
D2	18.85 REF		0.742 REF	
E	17.05	17.35	0.671	0.683
E1	13.95	14.05	0.549	0.553
E2	12.35 REF		0.486 REF	
K1	0.70	0.90	0.028	0.035
K3	1.60 REF		0.063 REF	
R1	0.13	---	0.005	---
R2	0.15	0.25	0.006	0.010
a	0.65 REF		0.026 REF	
b	0.30 REF		0.012 REF	
h	–	0.50	–	0.020
J	0.1524 REF		0.006 REF	
Ref: GP00-D234-5/92				

Figure 18b. Package Dimensions - 100-Pin PQFP



Dim.	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.30	1.50	0.051	0.059
A1	0.05	0.20	0.002	0.007
D	15.60	16.40	0.614	0.646
D1	13.90	14.10	0.549	0.553
a	0.40	0.60	0.016	0.024
b	0.08	0.28	0.003	0.011
J	0.08	0.18	0.003	0.007
β	0°	12°	0°	12°
K1	0.03	0.07	0.012	0.028
K2	1.0 TYP		0.040 TYP	

Figure 18c. Package Dimensions - 100-Pin TQFP



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.35	1.45	0.053	0.057
A1	0.05	0.15	0.002	0.006
A2	0.25 REF		0.0098	
D	21.85	22.15	0.860	0.872
D1	19.95	20.05	0.785	0.789
D2	19.82	19.92	0.780	0.784
E	15.85	16.15	0.624	0.636
E1	13.95	14.05	0.549	0.553
E2	13.82	13.92	0.544	0.548
K1	0.50	0.75	0.020	0.030
K2	1.00 REF		0.039	
R1	0.20 TYP		0.008TYP	
R2	0.20TYP		0.008TYP	
a	0.50 REF		0.020 REF	
b	0.22 REF		0.009 REF	

Ref: GP00-D264-A 11/19/93 (102594)

Note: * Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

Figure 18d. Package Dimensions - 128-Pin TQFP

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