

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

524,288-WORD BY 8-BIT STATIC RAM

DESCRIPTION

The TC554001AFI/AFTI/ATRI is a 4,194,304-bit static random access memory (SRAM) organized as 524,288 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 5V ± 10% power supply. Advanced circuit technology provides both high speed and low power at an operating current of 10 mA/MHz (typ) and a minimum cycle time of 70 ns. It is automatically placed in low-power mode at 2 μA standby current (typ) when chip enable (\overline{CE}) is asserted high. There are two control inputs. \overline{CE} is used to select the device and for data retention control, and output enable (\overline{OE}) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating extreme temperature range of -40° to 85°C, the TC554001AFI/AFTI/ATRI can be used in environments exhibiting extreme temperature conditions. The TC554001AFI/AFTI/ATRI is available in a standard plastic 32-pin small-outline package (SOP) and normal and reverse pinout plastic 32-pin thin-small-outline package (TSOP).

FEATURES

- Low-power dissipation
Operating: 55 mW/MHz (typical)
- Single power supply voltage of 5 V ± 10%
- Power down features using \overline{CE} .
- Data retention supply voltage of 2.0 to 5.5 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of -40° to 85°C
- Standby Current (maximum):

	TC554001AFI/AFTI/ATRI	
	-70,-85,-10	-70L,-85L,-10L
5.5 V	200 μA	100 μA
3.0 V	100 μA	50 μA

- Access Times (maximum):

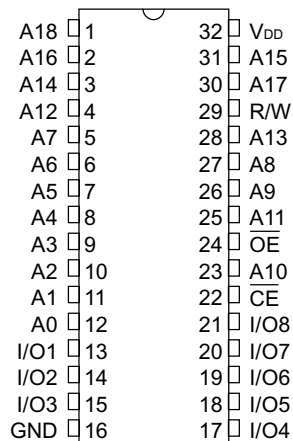
	TC554001AFI/AFTI/ATRI		
	-70,-70L	-85,-85L	-10,-10L
Access Time	70 ns	85 ns	100 ns
\overline{CE} Access Time	70 ns	85 ns	100 ns
\overline{OE} Access Time	35 ns	45 ns	50 ns

- Package:

SOP32-P-525-1.27 (AFI) (Weight: 1.14 g typ)
 TSOP II32-P-400-1.27 (AFTI) (Weight: 0.53 g typ)
 TSOP II32-P-400-1.27A (ATRI) (Weight: 0.53 g typ)

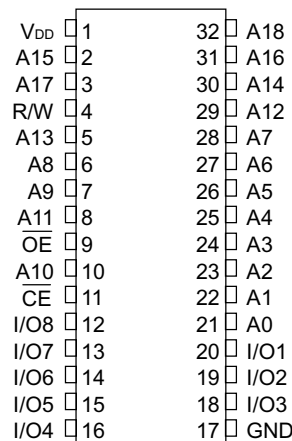
PIN ASSIGNMENT (TOP VIEW)

32 PIN SOP & TSOP



(AFI/AFTI)

32 PIN TSOP

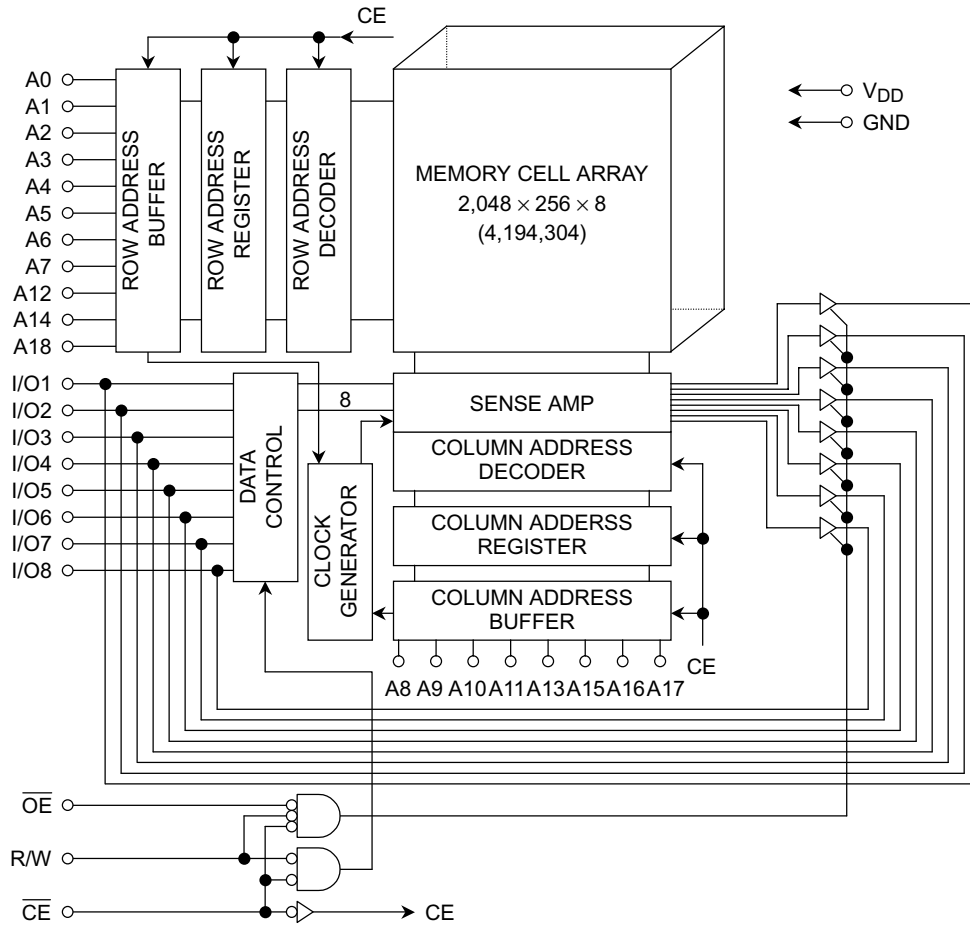


(ATRI)

PIN NAMES

A0~A18	Address Inputs
R/W	Read/Write Control
\overline{OE}	Output Enable
\overline{CE}	Chip Enable
I/O1~I/O8	Data Inputs/Outputs
V _{DD}	Power (+5 V)
GND	Ground

BLOCK DIAGRAM



OPERATING MODE

MODE	\overline{CE}	\overline{OE}	R/W	I/O1~I/O8	POWER
Read	L	L	H	Output	I_{DDO}
Write	L	*	L	Input	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	$I_{D DS}$

* = don't care
H = logic high
L = logic low

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	-0.3~7.0	V
V_{IN}	Input Voltage	-0.3*~7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	0.6	W
T_{solder}	Soldering Temperature (10s)	260	°C
T_{stg}	Storage Temperature	-55~150	°C
T_{opr}	Operating Temperature	-40~85	°C

*: -3.0 V when measured at a pulse width of 50ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = -40° to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.4	—	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage	-0.3*	—	0.6	V
V _{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

*: -3.0 V when measured at a pulse width of 50 ns

DC CHARACTERISTICS (Ta = -40° to 85°C, V_{DD} = 5 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT					
I _{IL}	Input Leakage Current	V _{IN} = 0 V~V _{DD}	—	—	±1.0	μA					
I _{OH}	Output High Current	V _{OH} = 2.4 V	-1.0	—	—	mA					
I _{OL}	Output Low Current	V _{OL} = 0.4 V	2.1	—	—	mA					
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $RW = V_{IL}$ or $\overline{OE} = V_{IH}$, V _{OUT} = 0 V~V _{DD}	—	—	±1.0	μA					
I _{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ and $RW = V_{IH}$, I _{OUT} = 0 mA, Other Input = V _{IH} /V _{IL}	t _{cycle} = MIN	—	—	70	mA				
			t _{cycle} = 1 μs	—	15	—					
I _{DDO2}	Operating Current	$\overline{CE} = 0.2$ V and $RW = V_{DD} - 0.2$ V, I _{OUT} = 0 mA, Other Input = V _{DD} - 0.2 V/0.2 V	t _{cycle} = MIN	—	—	60	mA				
			t _{cycle} = 1 μs	—	10	—					
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$ $\overline{CE} = V_{DD} - 0.2$ V, V _{DD} = 2.0 V~5.5 V				3	μA				
I _{DDS2}						-70,-85,-10		Ta = 25°C	—	2	—
								Ta = -40~85°C	—	—	200
I _{DDS2}						-70L,-85L,-10L		Ta = 25°C	—	2	5
	Ta = -40~85°C	—	—	100							

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = -40° to 85°C, VDD = 5 V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC554001AFI/AFTI/ATRI						UNIT
		-70,-70L		-85,-85L		-10,-10L		
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	70	—	85	—	100	—	ns
t _{ACC}	Address Access Time	—	70	—	85	—	100	
t _{CO}	Chip Enable Access Time	—	70	—	85	—	100	
t _{OE}	Output Enable Access Time	—	35	—	45	—	50	
t _{COE}	Chip Enable Low to Output Active	5	—	5	—	5	—	
t _{OEE}	Output Enable Low to Output Active	0	—	0	—	0	—	
t _{OD}	Chip Enable High to Output High-Z	—	30	—	35	—	40	
t _{ODO}	Output Enable High to Output High-Z	—	30	—	35	—	40	
t _{OH}	Output Data Hold Time	10	—	10	—	10	—	

WRITE CYCLE

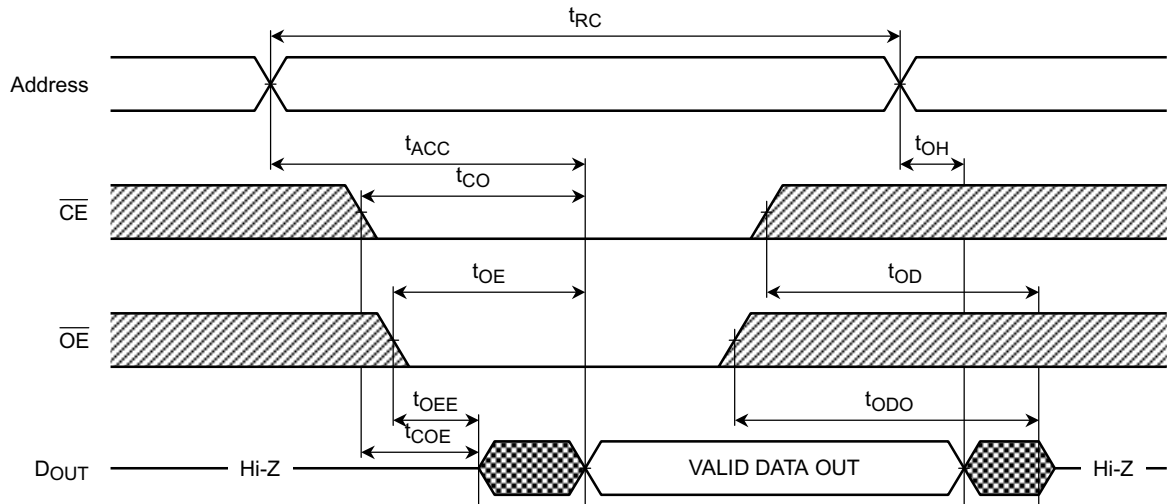
SYMBOL	PARAMETER	TC554001AFI/AFTI/ATRI						UNIT
		-70,-70L		-85,-85L		-10,-10L		
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	70	—	85	—	100	—	ns
t _{WP}	Write Pulse Width	50	—	55	—	60	—	
t _{CW}	Chip Enable to End of Write	60	—	70	—	80	—	
t _{AS}	Address Setup Time	0	—	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	0	—	
t _{ODW}	R/W Low to Output High-Z	—	30	—	35	—	40	
t _{OEW}	R/W High to Output Active	0	—	0	—	0	—	
t _{DS}	Data Setup Time	30	—	35	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	

AC TEST CONDITIONS

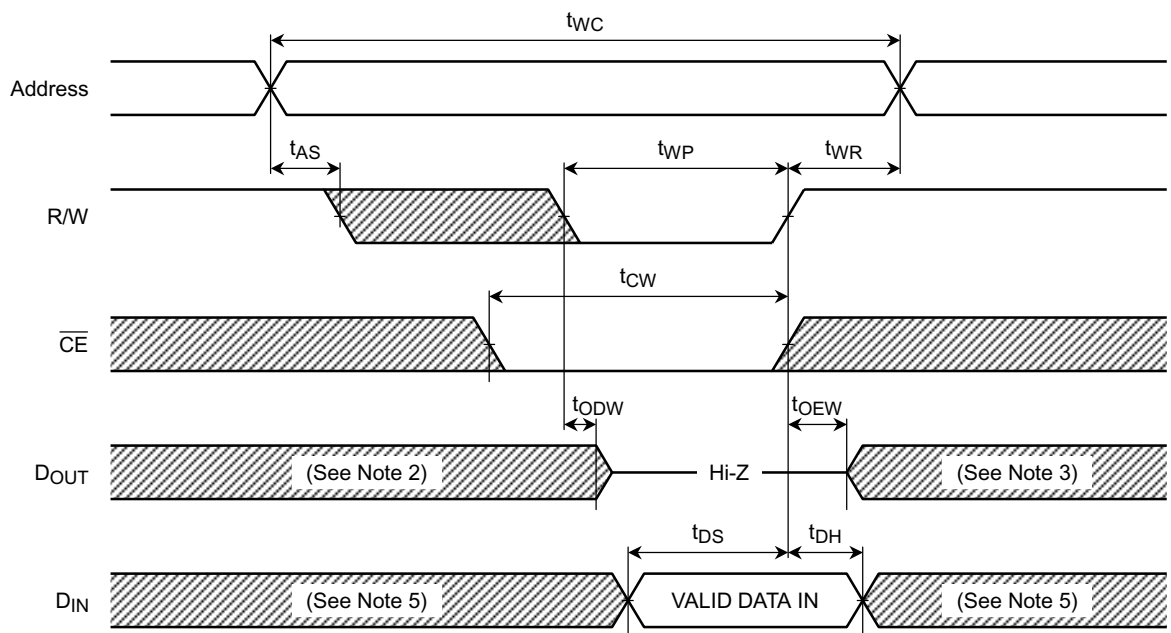
PARAMETER	TEST CONDITION
Output load	100 pF + 1 TTL Gate
Input pulse level	0.4 V, 2.6 V
Timing measurements	1.5 V
Reference level	1.5 V
t _R , t _F	5 ns

TIMING DIAGRAMS

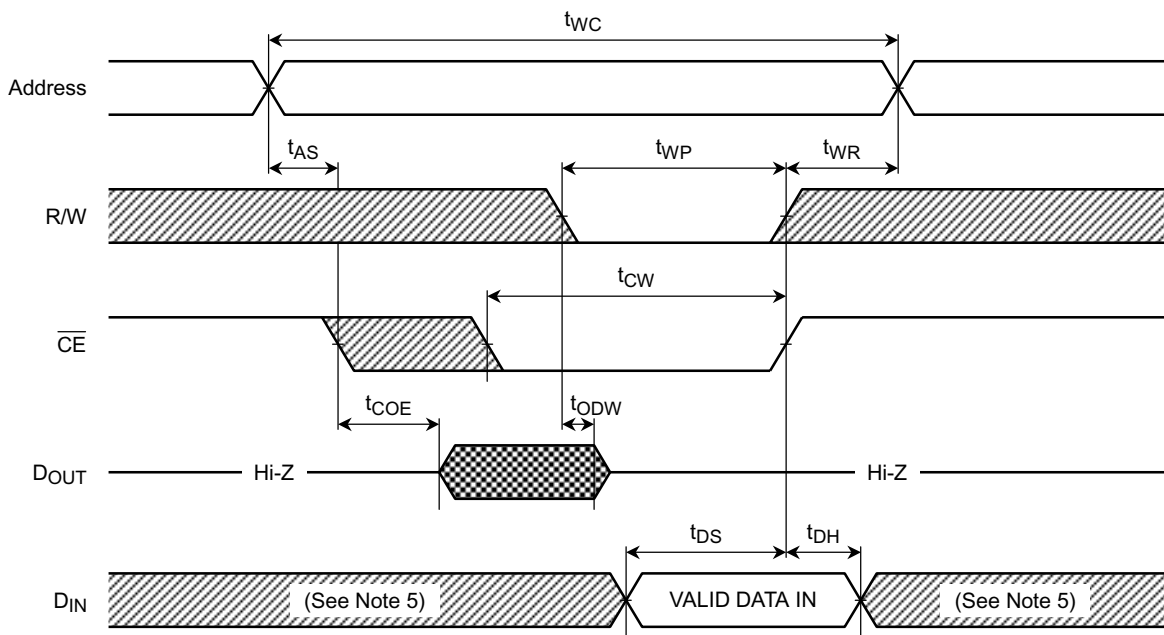
READ CYCLE (See Note 1)



WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 (\overline{CE} CONTROLLED) (See Note 4)



Note:

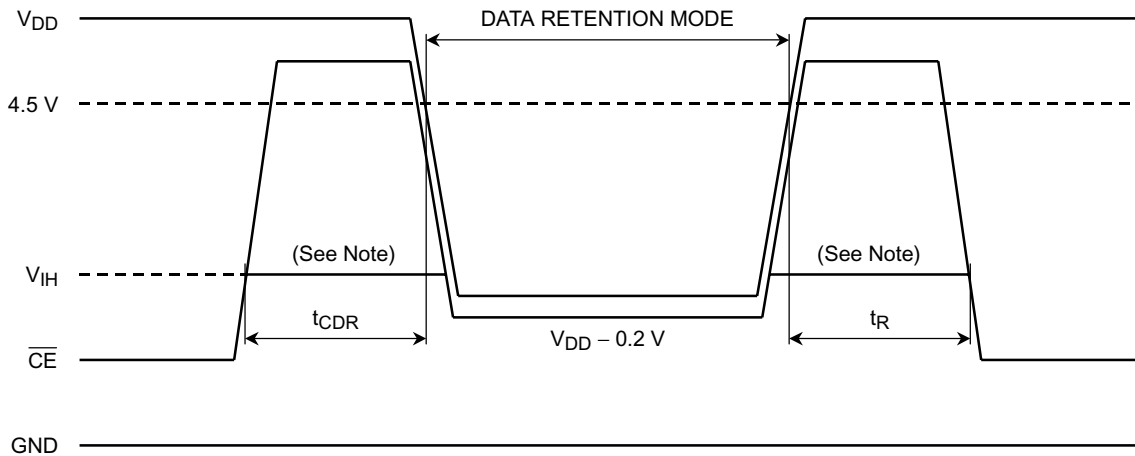
- (1) R/W remains HIGH for the read cycle.
- (2) If \overline{CE} goes LOW coincident with or after R/W goes LOW, the outputs will remain at high impedance.
- (3) If \overline{CE} goes HIGH coincident with or before R/W goes HIGH, the outputs will remain at high impedance.
- (4) If \overline{OE} is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = -40° to 85°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT	
V _{DH}	Data Retention Supply Voltage		2.0	—	5.5	V	
I _{DDS2}	Standby Current	-70,-85,-10	V _{DH} = 3.0 V	—	—	100	μA
			V _{DH} = 5.5 V	—	—	200	
		-70L,-85L,-10L	V _{DH} = 3.0 V	—	—	50*	
			V _{DH} = 5.5 V	—	—	100	
t _{CDR}	Chip Deselect to Data Retention Mode Time		0	—	—	ns	
t _R	Recovery Time		5	—	—	ms	

*: 5 μA (max) at Ta = -40° to 40°C

CE CONTROLLED DATA RETENTION MODE

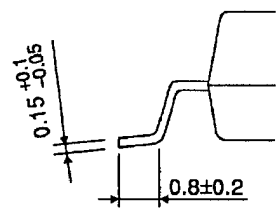
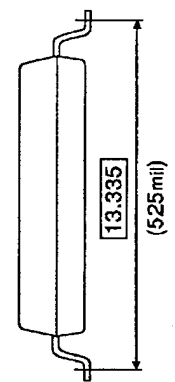
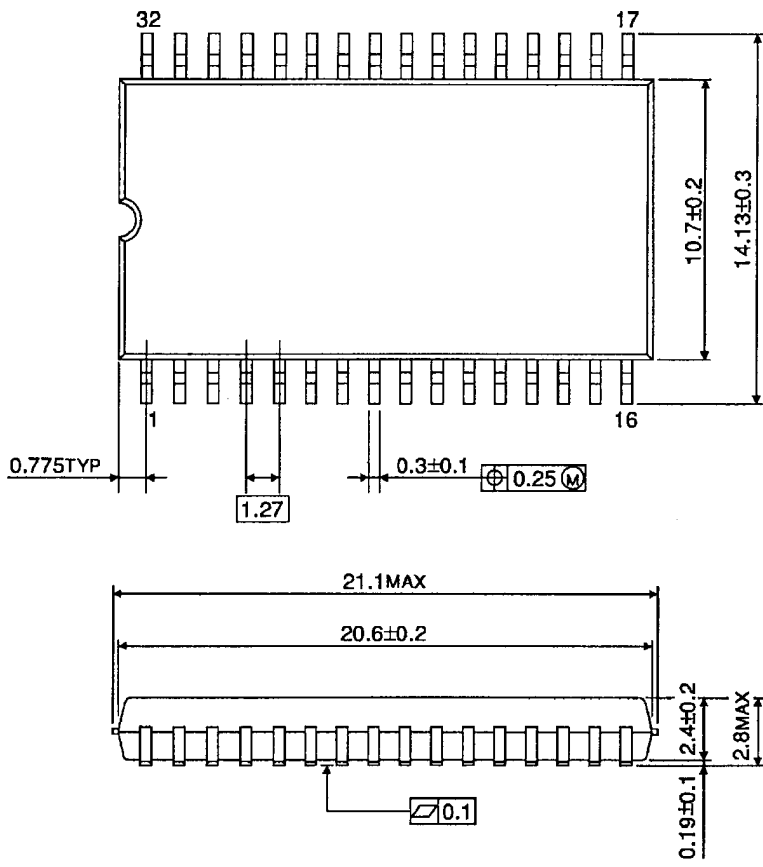


Note: When \overline{CE} is operating at the V_{IH} level (2.4V), the standby current is given by I_{DDS1} during the transition of V_{DD} from 4.5 to 2.6V.

PACKAGE DIMENSIONS

SOP32-P-525-1.27

Unit : mm

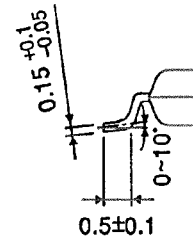
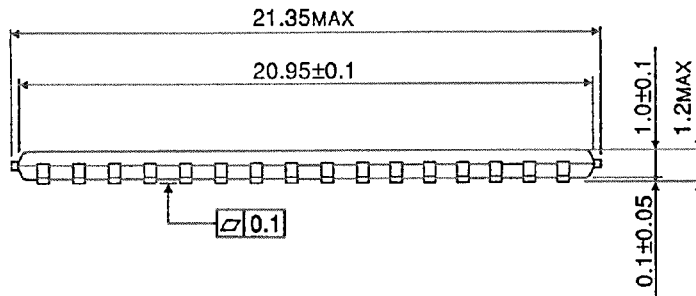
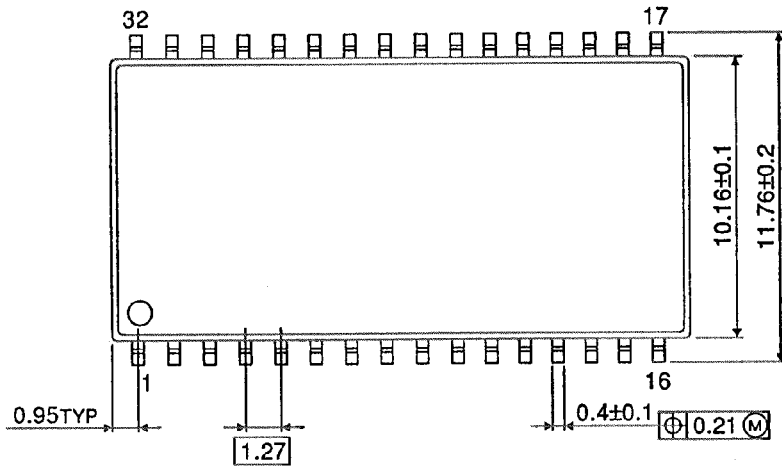


Weight: 1.14 g (typ)

PACKAGE DIMENSIONS

TSOPII32-P-400-1.27

Unit: mm

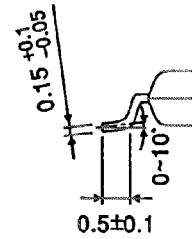
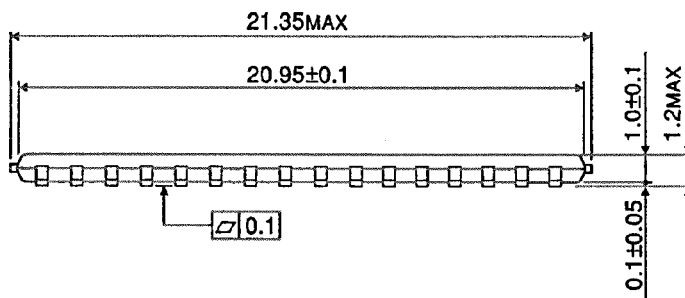
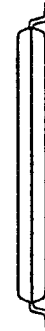
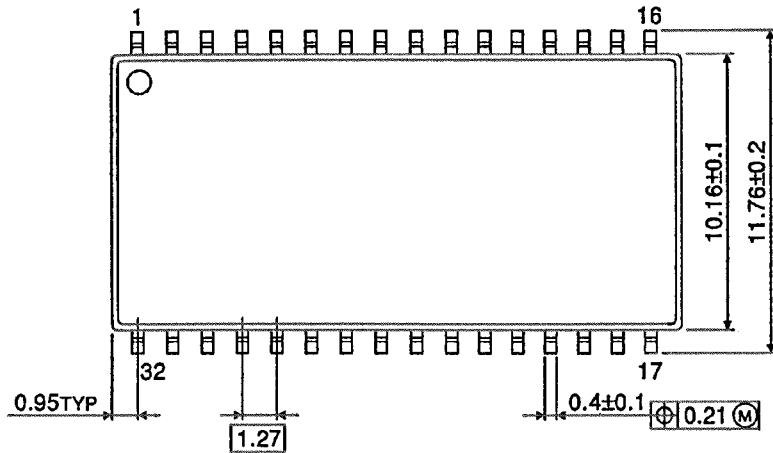


Weight: 0.53 g (typ)

PACKAGE DIMENSIONS

TSOPII32-P-400-1.27A

Unit: mm



Weight: 0.53 g (typ)

RESTRICTIONS ON PRODUCT USE

000707EBA

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer's own risk.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.