

<b>V53C365805A</b>	<b>40</b>	<b>50</b>	<b>60</b>
Max. $\overline{\text{RAS}}$ Access Time, ( $t_{\text{RAC}}$ )	40 ns	50 ns	60 ns
Max. Column Address Access Time, ( $t_{\text{CAA}}$ )	20 ns	25 ns	30 ns
Min. EDO Page Mode Cycle Time, ( $t_{\text{PC}}$ )	16 ns	20 ns	25 ns
Min. Read/Write Cycle Time, ( $t_{\text{RC}}$ )	69 ns	84 ns	104 ns

**Features**

- 8M x 8-bit organization
- EDO Page Mode for a sustained data rate of 63 MHz
- $\overline{\text{RAS}}$  access time: 40, 50, 60 ns
- Low power dissipation
- Read-Modify-Write,  $\overline{\text{RAS}}$ -Only Refresh,  $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  Refresh, Hidden Refresh
- Refresh Interval: 4096 cycles/64 ms
- Available in 32-pin 400 mil SOJ, and 32-pin 400 mil TSOP-II
- Single +3.3 V  $\pm$ 0.3 V Power Supply
- TTL Interface

**Description**

The V53C365805A is a 8,388,608 x 8 bit high-performance CMOS dynamic random access memory. The V53C365805A offers Page mode operation. The V53C365805A has an asymmetric address, 12-bit row and 11-bit column.

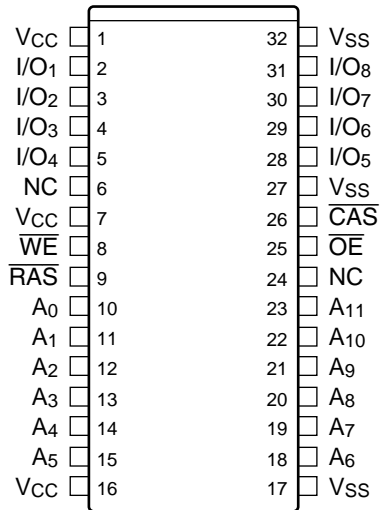
All inputs are TTL compatible. Page Mode operation allows random access up to 2048 x 8 bits, within a page, with cycle times as short as 16 ns.

These features make the V53C365805A ideally suited for a wide variety of high performance computer systems and peripheral applications.

**Device Usage Chart**

Operating Temperature Range	Package Outline		Access Time (ns)			Power	Temperature Mark
	K	T	40	50	60	Std.	
0°C to 70°C	•	•	•	•	•	•	Blank

**32 Pin Plastic SOJ /TSOP-II  
PIN CONFIGURATION  
Top View**



316580500-02

**Pin Names**

A <sub>0</sub> -A <sub>11</sub>	Row, Column Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
I/O <sub>1</sub> -I/O <sub>8</sub>	Data Input, Output
V <sub>CC</sub>	+3.3V Supply
V <sub>SS</sub>	0V Supply
NC	No Connect

**Absolute Maximum Ratings\***

Operating temperature range .....0 to 70 °C  
 Storage temperature range ..... -55 to 150 °C  
 Soldering temperature .....260 °C  
 Soldering time..... 10 s  
 Input/output voltage .... -0.5 to min (V<sub>CC</sub>+0.5, 4.6) V  
 Power supply voltage .....-0.5V to 4.6 V  
 Power dissipation ..... 1.0 W  
 Data out current (short circuit) ..... 50 mA

\*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

**Capacitance\***

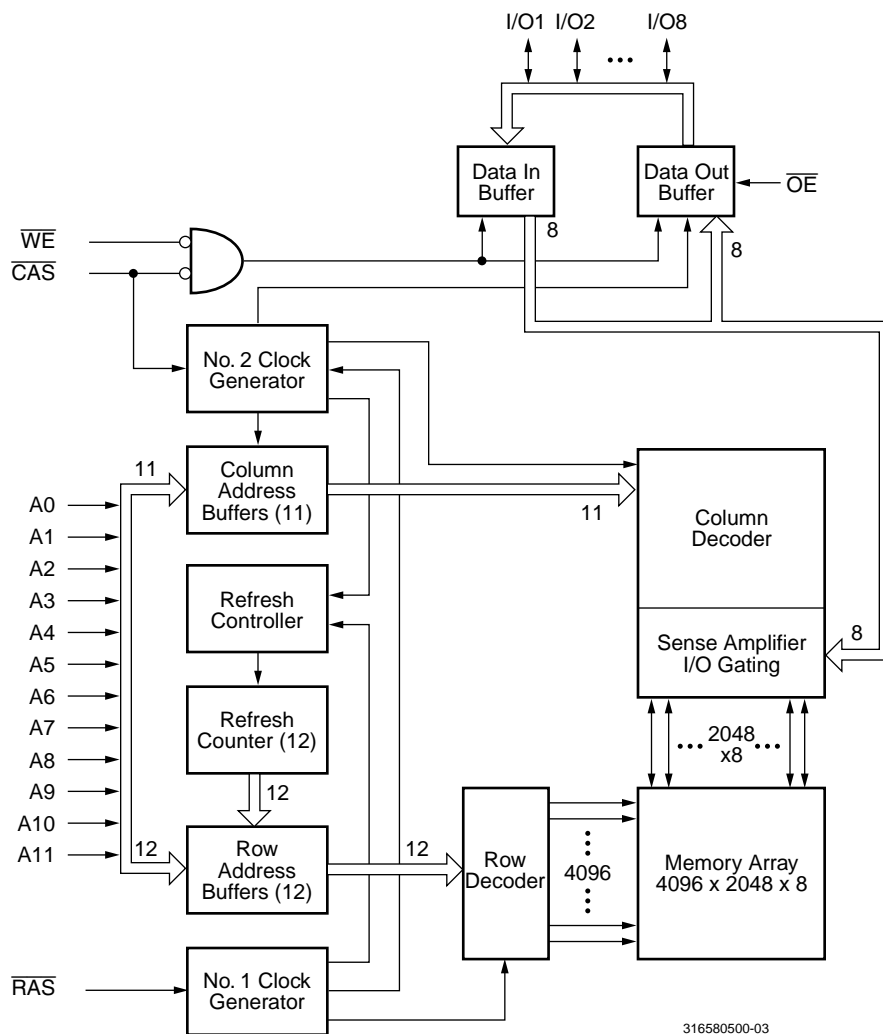
T<sub>A</sub> = 25°C, V<sub>CC</sub> = 3.3 V ± 0.3 V, V<sub>SS</sub> = 0 V, f = 1 Mhz

Symbol	Parameter	Min.	Max.	Unit
C <sub>IN1</sub>	Address Input	—	5	pF
C <sub>IN2</sub>	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$	—	7	pF
C <sub>OUT</sub>	Data Input/Output	—	7	pF

\*Note: Capacitance is sampled and not 100% tested.

**Block Diagram**

8M x 8



**DC and Operating Characteristics (1, 2)**

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , unless otherwise specified.

Symbol	Parameter	Access Time	V53C365805A			Unit	Test Conditions	Notes
			Min.	Typ.	Max.			
$I_{LI}$	Input Leakage Current (any input pin)		-2		2	$\mu\text{A}$	$V_{SS} \leq V_{IN} \leq V_{CC}$	
$I_{LO}$	Output Leakage Current (for High-Z State)		-2		2	$\mu\text{A}$	$V_{SS} \leq V_{OUT} \leq V_{CC}$ RAS, CAS at $V_{IH}$	
$I_{CC1}$	$V_{CC}$ Supply Current, Operating	40			155	mA	$t_{RC} = t_{RC}(\text{min.})$	2, 3, 4
		50			130			
		60			105			
$I_{CC2}$	$V_{CC}$ Supply Current, TTL Standby				2	mA	RAS, CAS at $V_{IH}$ other inputs $\geq V_{SS}$	
$I_{CC3}$	$V_{CC}$ Supply Current, RAS-Only Refresh	40			155	mA	$t_{RC} = t_{RC}(\text{min.})$	2, 4
		50			130			
		60			105			
$I_{CC4}$	$V_{CC}$ Supply Current, EDO Page Mode Operation	40			70	mA	Minimum Cycle	2, 3, 4
		50			60			
		60			50			
$I_{CC5}$	$V_{CC}$ Supply Current, CMOS Standby				500	$\mu\text{A}$	RAS $\geq V_{CC} - 0.2\text{ V}$ , CAS $\geq V_{CC} - 0.2\text{ V}$	
$I_{CC6}$	$V_{CC}$ Supply Current, during CAS-before-RAS Refresh	40			155	mA		2, 4
		50			130			
		60			105			
$V_{IL}$	Input Low Voltage		-0.3		0.8	V		1
$V_{IH}$	Input High Voltage		2.0		$V_{CC} + 0.3$	V		1
$V_{OL}$	Output Low Voltage (LVTTTL)				0.4	V	$I_{OL} = 2\text{ mA}$	1
$V_{OH}$	Output High Voltage (LVTTTL)		2.4			V	$I_{OH} = -2\text{ mA}$	1
$V_{OL}$	Output Low Voltage (LVCMOS)				0.2	V	$I_{OL} = 100\ \mu\text{A}$	1
$V_{OH}$	Output High Voltage (LVCMOS)		$V_{CC} - 0.2$			V	$I_{OH} = -100\ \mu\text{A}$	1

**Truth Table**

<b>FUNCTION</b>		<b><math>\overline{\text{RAS}}</math></b>	<b><math>\overline{\text{CAS}}</math></b>	<b><math>\overline{\text{WE}}</math></b>	<b><math>\overline{\text{OE}}</math></b>	<b>ROW ADDR</b>	<b>COL ADDR</b>	<b>I/O1-I/O4</b>
Standby		H	H → X	X	X	X	X	High Impedance
Read		L	L	H	L	ROW	COL	Data Out
Early-Write		L	L	L	X	ROW	COL	Data In
Delayed-Write		L	L	H → L	H	ROW	COL	Data In
Read-Modify-Write		L	L	H → L	L → H	ROW	COL	Data Out, Data In
EDO Page Mode Read	1st Cycle	L	H → L	H	L	ROW	COL	Data Out
	2nd Cycle	L	H → L	H	L	N/A	COL	Data Out
EDO Page Mode Early Write	1st Cycle	L	H → L	L	X	ROW	COL	Data In
	2nd Cycle	L	H → L	L	X	N/A	COL	Data In
EDO Page Mode RMW	1st Cycle	L	H → L	H → L	L → H	ROW	COL	Data Out, Data In
	2nd Cycle	L	H → L	H → L	L → H	N/A	COL	Data Out, Data In
$\overline{\text{RAS}}$ only refresh		L	H	X	X	ROW	N/A	High Impedance
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh		H → L	L	H	X	X	N/A	High Impedance
Test Mode Entry		H → L	L	L	X	X	N/A	High Impedance
Hidden Refresh	READ	L→H→L	L	H	L	ROW	COL	Data Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data In

**AC Characteristics (6,7,8)** $T_A = 0$  to  $70\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{V}$ 

#	Symbol	Parameter	-40		- 50		- 60		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
<b>Common Parameters</b>										
1	$t_{RC}$	Random read or write cycle time	69	–	84	–	104	–	ns	
2	$t_{RAS}$	$\overline{RAS}$ pulse width	40	100k	50	100k	60	100k	ns	
3	$t_{CAS}$	$\overline{CAS}$ pulse width	6	10k	8	10k	10	10k	ns	
4	$t_{RP}$	$\overline{RAS}$ precharge time	25	–	30	–	40	–	ns	
5	$t_{CP}$	$\overline{CAS}$ precharge time	6	–	8	–	10	–	ns	
6	$t_{ASR}$	Row address setup time	0	–	0	–	0	–	ns	
7	$t_{RAH}$	Row address hold time	5	–	7	–	10	–	ns	
8	$t_{ASC}$	Column address setup time	0	–	0	–	0	–	ns	
9	$t_{CAH}$	Column address hold time	5	–	7	–	10	–	ns	
10	$t_{RCD}$	$\overline{RAS}$ to $\overline{CAS}$ delay time	9	30	11	37	14	45	ns	
11	$t_{RAD}$	$\overline{RAS}$ to column address delay	7	20	9	25	12	30	ns	
12	$t_{RSH}$	$\overline{RAS}$ hold time	6	–	8	–	10	–	ns	
13	$t_{CSH}$	$\overline{CAS}$ hold time	32	–	40	–	48	–	ns	
14	$t_{CRP}$	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	–	5	–	5	–	ns	
15	$t_T$	Transition time (rise and fall)	1	50	1	50	1	50	ns	7
16	$t_{REF}$	Refresh period for 4k-refresh	–	64	–	64	–	64	ms	
<b>Read Cycle</b>										
17	$t_{RAC}$	Access time from $\overline{RAS}$	–	40	–	50	–	60	ns	8, 9
18	$t_{CAC}$	Access time from $\overline{CAS}$	–	10	–	13	–	15	ns	8, 9
19	$t_{CAA}$	Access time from column address	–	20	–	25	–	30	ns	8,10
20	$t_{OEA}$	$\overline{OE}$ access time	–	10	–	13	–	15	ns	8
21	$t_{RAL}$	Column address to $\overline{RAS}$ lead time	20	–	25	–	30	–	ns	
22	$t_{RCS}$	Read command setup time	0	–	0	–	0	–	ns	
23	$t_{RCH}$	Read command hold time	0	–	0	–	0	–	ns	11
24	$t_{RRH}$	Read command hold time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	11
25	$t_{CLZ}$	$\overline{CAS}$ to output in low-Z	0	–	0	–	0	–	ns	8
26	$t_{OFF}$	Output buffer turn-off delay	0	10	0	13	0	15	ns	12
27	$t_{OEZ}$	Output buffer turn-off delay from $\overline{OE}$	0	10	0	13	0	15	ns	12
28	$t_{DZO}$	Data to $\overline{OE}$ low delay	0	–	0	–	0	–	ns	13
29	$t_{CDD}$	$\overline{CAS}$ high to data delay	10	–	13	–	15	–	ns	14
30	$t_{ODD}$	$\overline{OE}$ high to data delay	10	–	13	–	15	–	ns	14

**AC Characteristics (6,7,8) (Continued)** $T_A = 0$  to  $70\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{V}$ 

#	Symbol	Parameter	-40		- 50		- 60		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
<b>Write Cycle</b>										
31	$t_{WCH}$	Write command hold time	5	–	7	–	10	–	ns	
32	$t_{WP}$	Write command pulse width	5	–	7	–	10	–	ns	
33	$t_{WCS}$	Write command setup time	0	–	0	–	0	–	ns	15
34	$t_{RWL}$	Write command to $\overline{RAS}$ lead time	6	–	8	–	10	–	ns	
35	$t_{CWL}$	Write command to $\overline{CAS}$ lead time	6	–	8	–	10	–	ns	
36	$t_{DS}$	Data setup time	0	–	0	–	0	–	ns	16
37	$t_{DH}$	Data hold time	5	–	7	–	10	–	ns	16
<b>Read-modify-Write Cycle</b>										
38	$t_{RWC}$	Read-write cycle time	89	–	109	–	128	–	ns	
39	$t_{RWD}$	$\overline{RAS}$ to $\overline{WE}$ delay time	52	–	65	–	77	–	ns	15
40	$t_{CWD}$	$\overline{CAS}$ to $\overline{WE}$ delay time	22	–	28	–	32	–	ns	15
41	$t_{AWD}$	Column address to $\overline{WE}$ delay time	32	–	40	–	47	–	ns	15
42	$t_{OEHL}$	$\overline{OE}$ command hold time	5	–	7	–	10	–	ns	
<b>EDO Page Mode Cycle</b>										
43	$t_{PC}$	EDO Page Mode cycle time	16	–	20	–	24	–	ns	
44	$t_{CPA}$	Access time from $\overline{CAS}$ precharge	–	22	–	28	–	34	ns	7
45	$t_{RAS}$	$\overline{RAS}$ pulse width in EDO page mode	40	200k	50	200k	60	200k	ns	
46	$t_{RHPC}$	$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	25	–	30	–	35	–	ns	
47	$t_{COH}$	Output Data Hold Time	5	–	5	–	5	–	ns	
48	$t_{OEP}$	$\overline{OE}$ Pulse Width	5	–	5	–	5	–	ns	
49	$t_{OEHC}$	$\overline{OE}$ Hold Time from $\overline{CAS}$ High	5	–	5	–	5	–	ns	
50	$t_{WEZ}$	Output Buffer Turn-off Delay from $\overline{WE}$	0	10	0	13	0	15	ns	
<b>EDO Page Mode Read-Modify-Write Cycle</b>										
51	$t_{PRWC}$	EDO page mode read-write cycle time	42	–	53	–	63	–	ns	
52	$t_{CPWD}$	$\overline{CAS}$ precharge to $\overline{WE}$	32	–	41	–	49	–	ns	
<b><math>\overline{CAS}</math> before <math>\overline{RAS}</math> Refresh Cycle</b>										
53	$t_{CSR}$	$\overline{CAS}$ setup time	5	–	5	–	5	–	ns	
54	$t_{CHR}$	$\overline{CAS}$ hold time	5	–	5	–	10	–	ns	
55	$t_{RPC}$	$\overline{RAS}$ to $\overline{CAS}$ precharge time	0	–	0	–	0	–	ns	
56	$t_{WRP}$	Write to $\overline{RAS}$ precharge time	5	–	5	–	10	–	ns	
57	$t_{WRH}$	Write hold time referenced to $\overline{RAS}$	5	–	5	–	10	–	ns	

**AC Characteristics** <sup>(6,7,8)</sup> **(Continued)** $T_A = 0$  to  $70\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{V}$ 

#	Symbol	Parameter	-40		- 50		- 60		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
<b>Test Mode Cycle</b>										
58	$t_{WTS}$	Write command setup time	5	–	5	–	5	–	ns	18
59	$t_{WTH}$	Write command hold time	5	–	5	–	5	–	ns	18

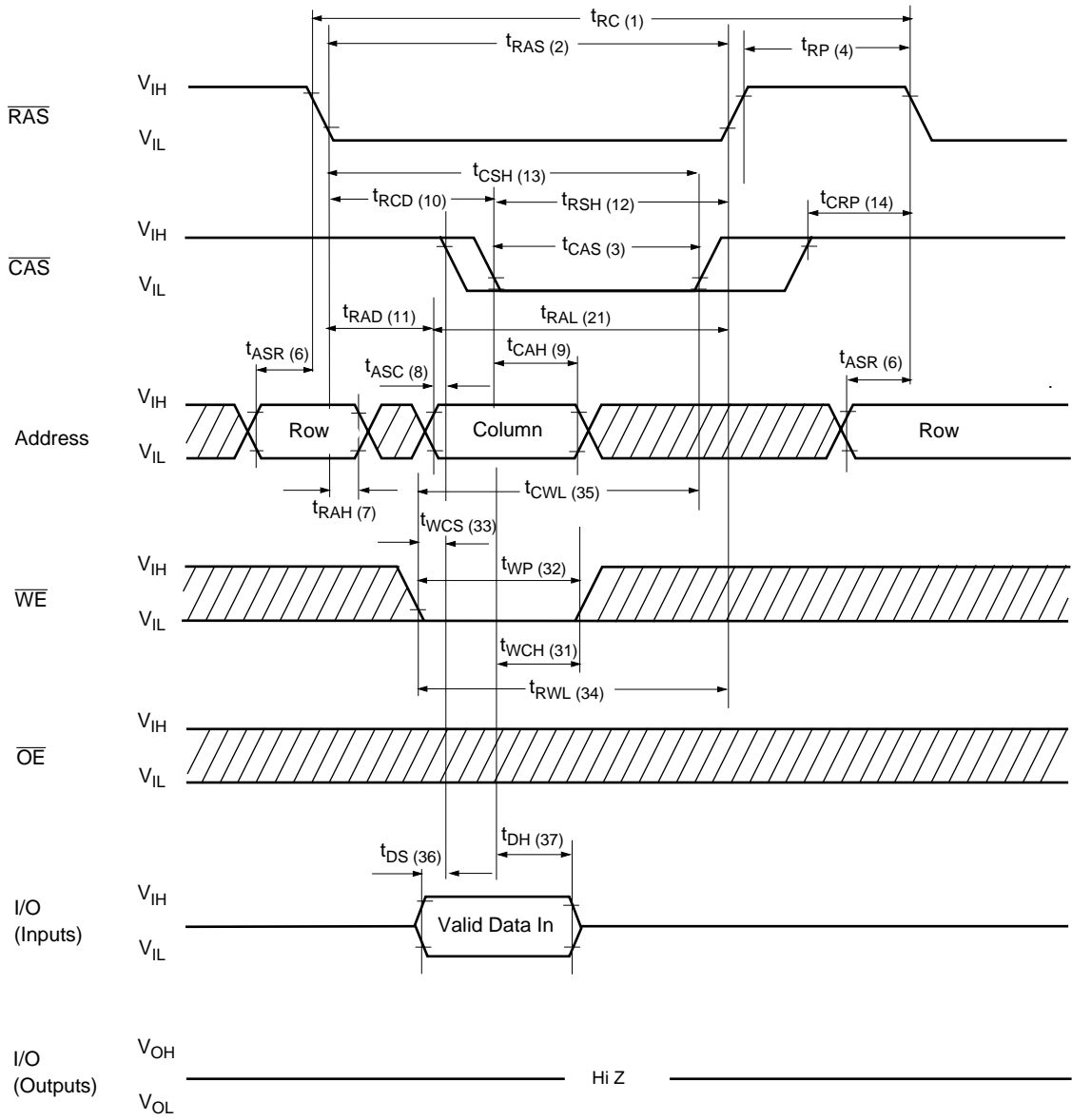


**Notes:**

- 1) All voltages are referenced to VSS.  
 $V_{IH}$  may overshoot to  $V_{CC} + 0.2V$  for pulse widths of  $< 4ns$  with 3.3V.  $V_{IL}$  may undershoot to  $-2.0V$  for pulse width  $< 4.0 ns$  with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.
- 2)  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC6}$  and  $I_{CC7}$  depend on cycle rate.
- 3)  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are measured with the output open.
- 4) Address can be changed once or less while  $\overline{RAS} = V_{IL}$ . In the case of  $I_{CC4}$  it can be changed once or less during a edo page mode cycle ( $t_{PC}$ ).
- 5) An initial pause of 100  $\mu s$  is required after power-up followed by 8  $\overline{RAS}$ -only-refresh cycles, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
- 6) AC measurements assume  $t_T = 5 ns$ .
- 7)  $V_{IH (min.)}$  and  $V_{IL (max.)}$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- 8) Measured with the specified current load and 100 pF at  $V_{OH} = 2.0 V$  and  $V_{OL} = 0.8 V$ .
- 9) Operation within the  $t_{RCD (max.)}$  limit ensures that  $t_{RAC (max.)}$  can be met.  $t_{RCD (max.)}$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD (max.)}$  limit, then access time is controlled by  $t_{CAC}$ .
- 10) Operation within the  $t_{RAD (max.)}$  limit ensures that  $t_{RAC (max.)}$  can be met.  $t_{RAD (max.)}$  is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD (max.)}$  limit, then access time is controlled by  $t_{CAA}$ .
- 11) Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
- 12)  $t_{OFF (max.)}$  and  $t_{OEZ (max.)}$  define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
- 13) Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.
- 14) Either  $t_{CDD}$  or  $t_{ODD}$  must be satisfied.
- 15)  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} > t_{WCS (min.)}$ , the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if  $t_{RWD} > t_{RWD (min.)}$ ,  $t_{CWD} > t_{CWD (min.)}$ ,  $t_{AWD} > t_{AWD (min.)}$  and  $t_{CPWD} > t_{CPWD (min.)}$ , the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
- 16) These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WRITE}$  leading edge in Read-Modify-Write cycles.
- 17) In a Test Mode Read Cycle, the value of  $t_{RAC}$ ,  $t_{CAA}$ ,  $t_{CAC}$  and  $t_{CPA}$  are delayed by 5 ns from the specified value. These parameters must be adjusted in Test Mode cycles by adding 5ns to the specified value. Associated timings must be adjusted by 5 ns.



**Waveforms of Write Cycle (Early Write)**

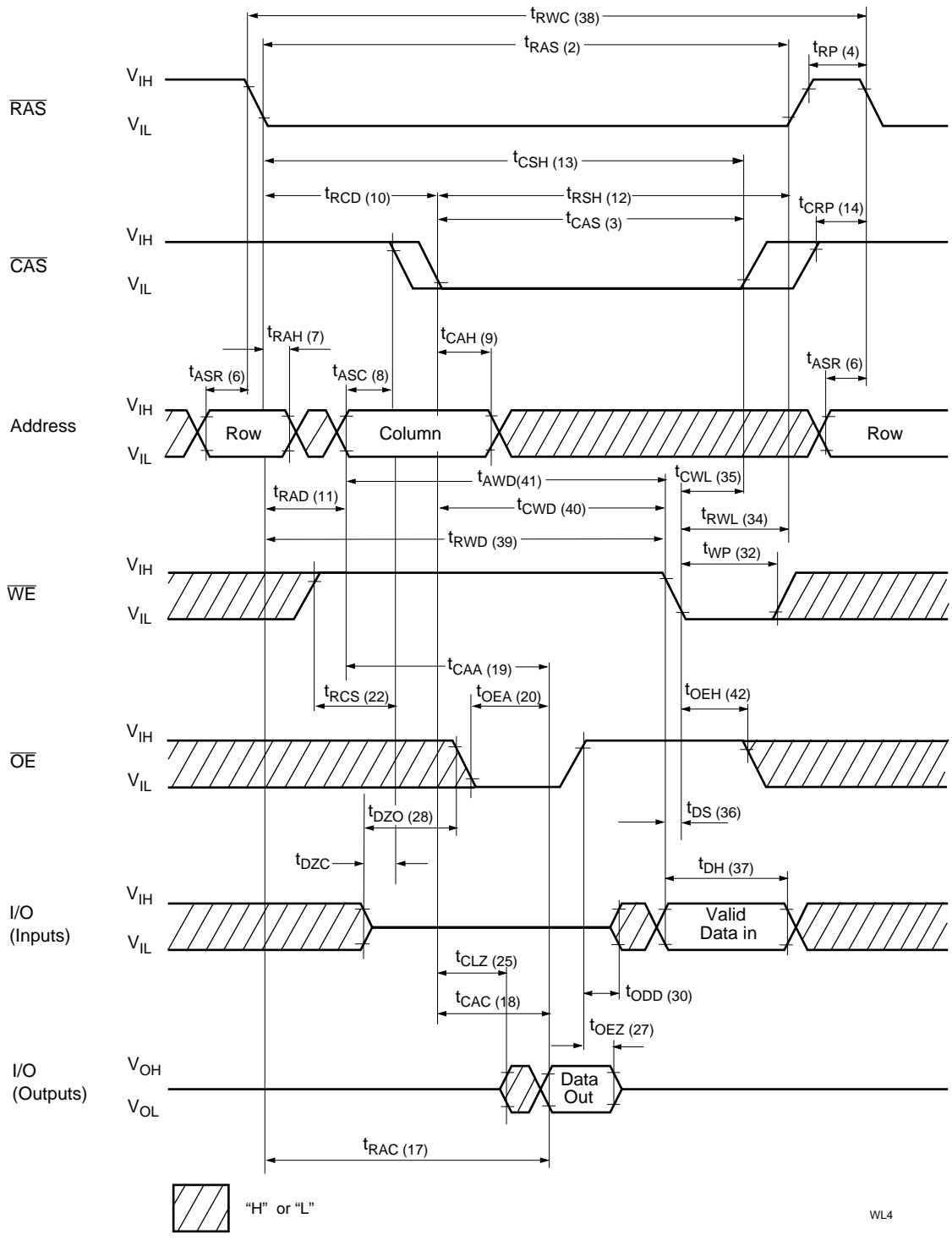


 "H" or "L"

WL2



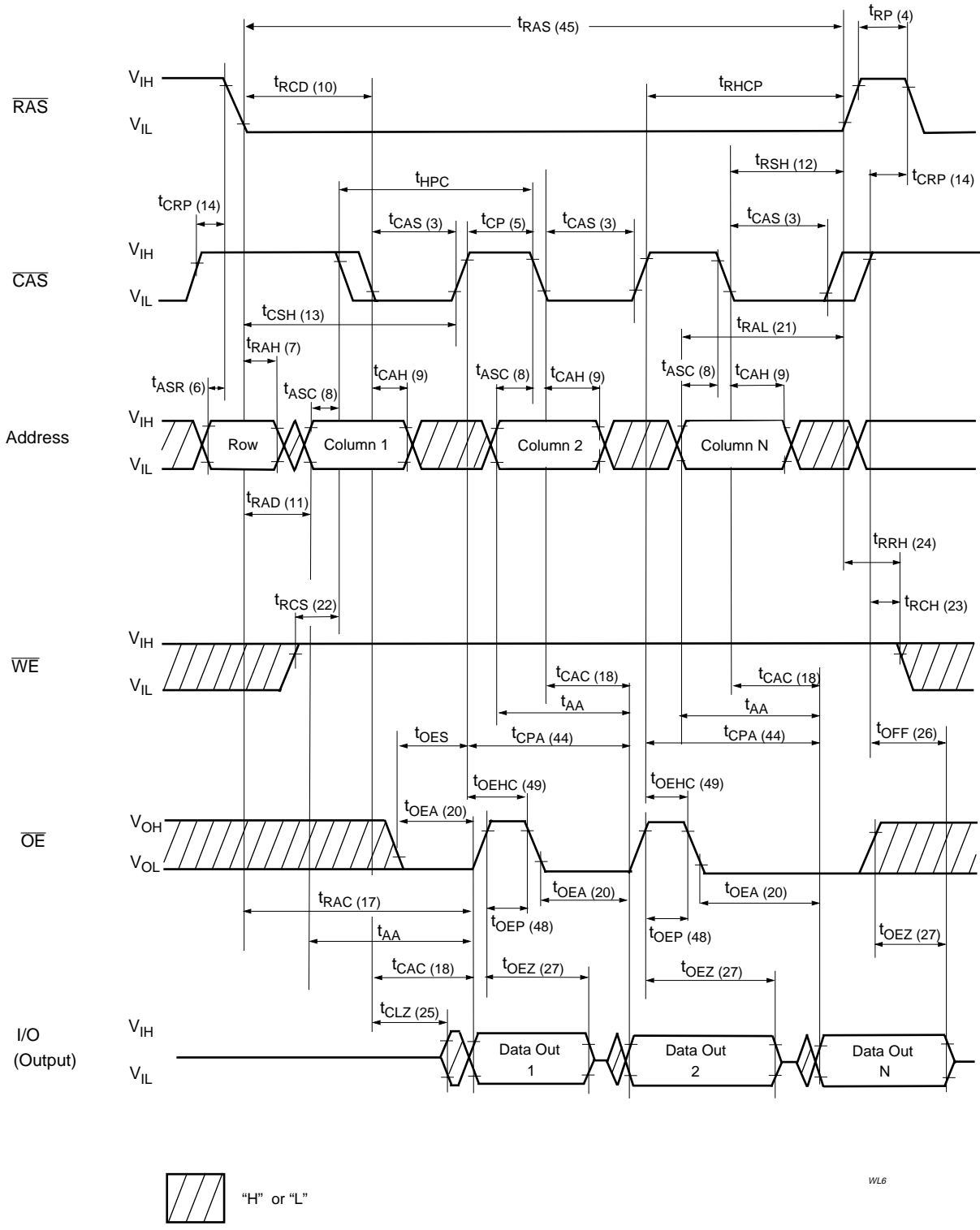
Waveforms of Read-Write (Read-Modify-Write) Cycle



WL4



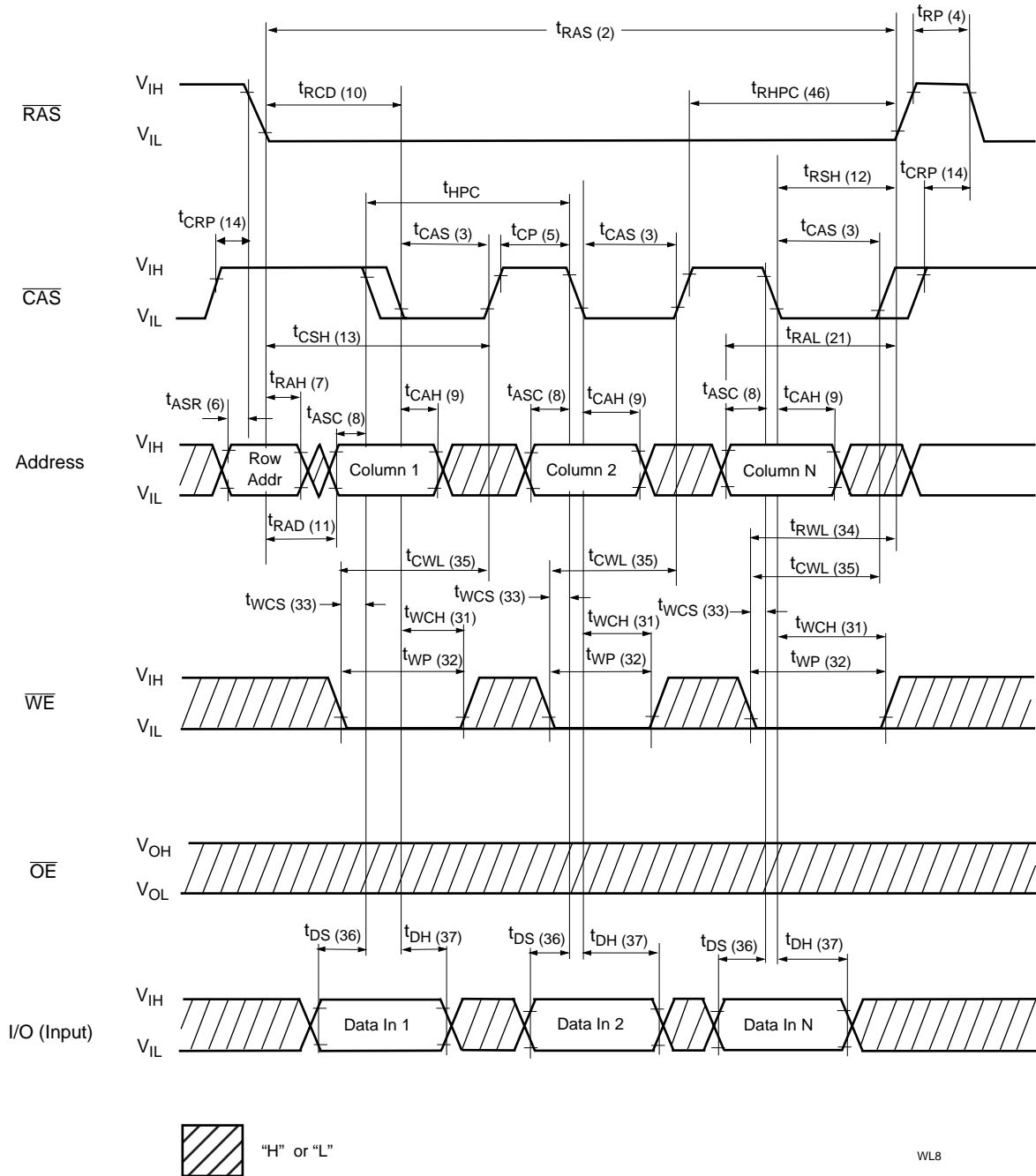
Waveforms of EDO Page Mode Read Cycle ( $\overline{OE}$  Control)



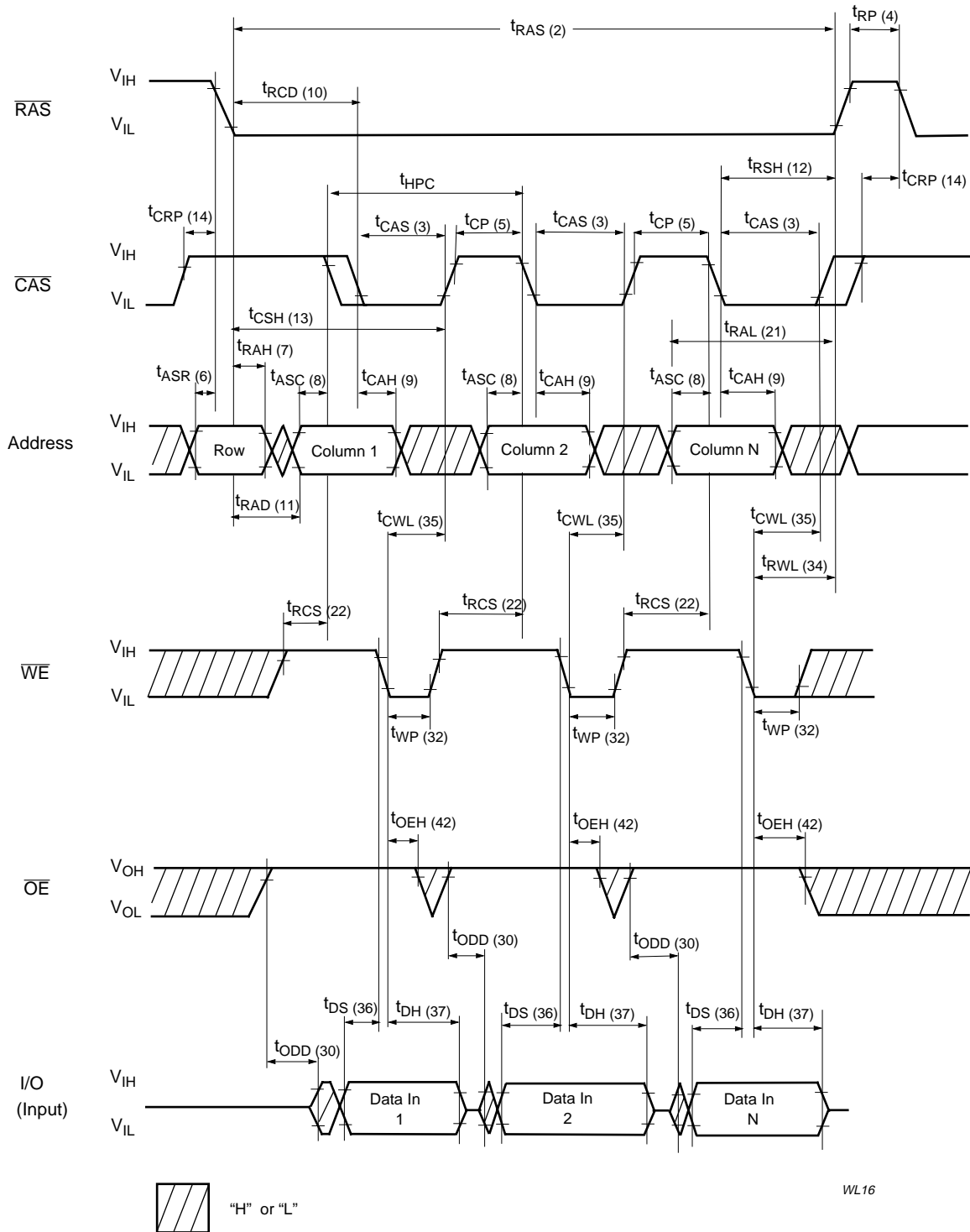




Waveforms of EDO Page Mode Early Write Cycle



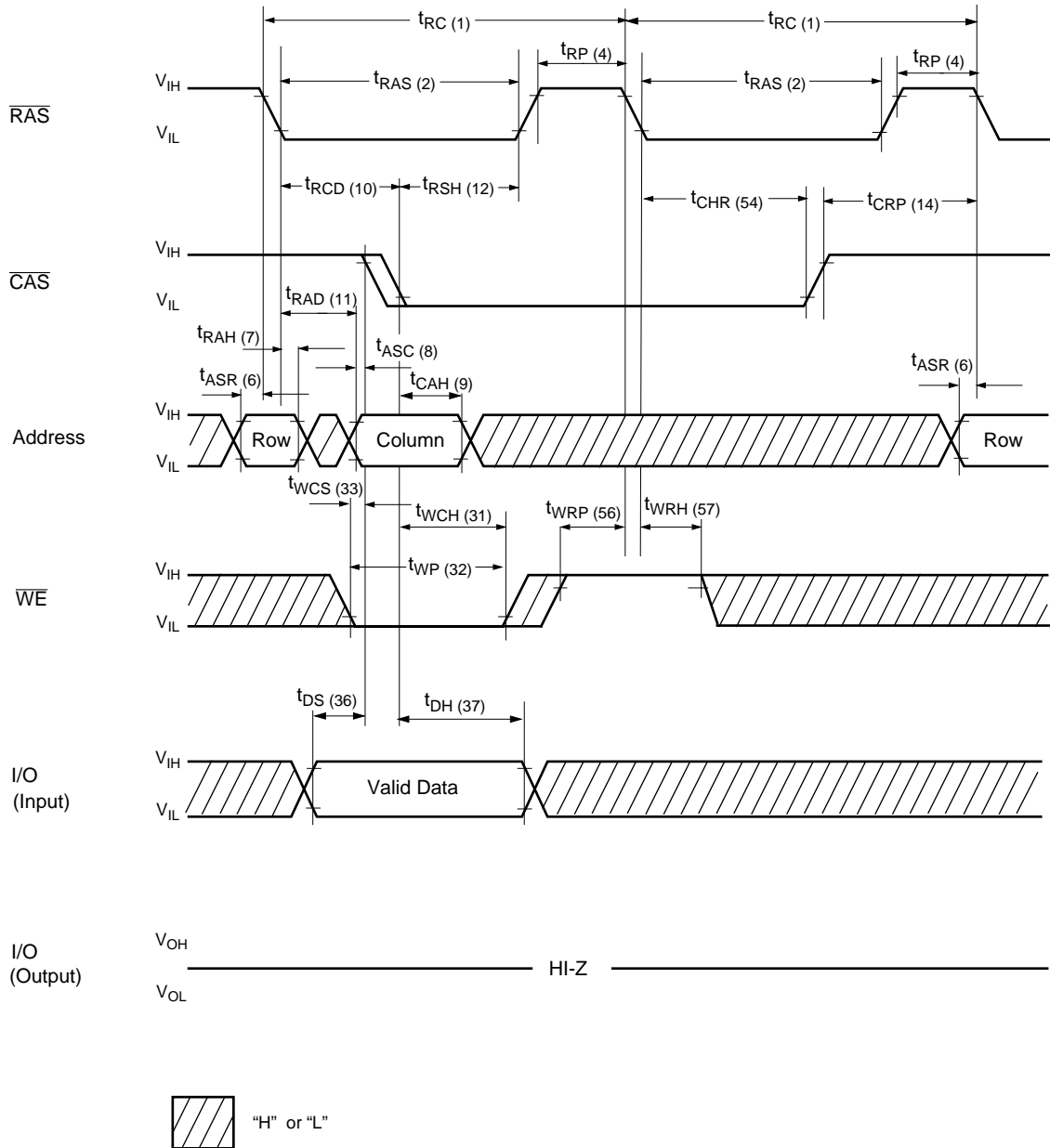
Waveforms of EDO Page Mode Late Write Cycle



WL16

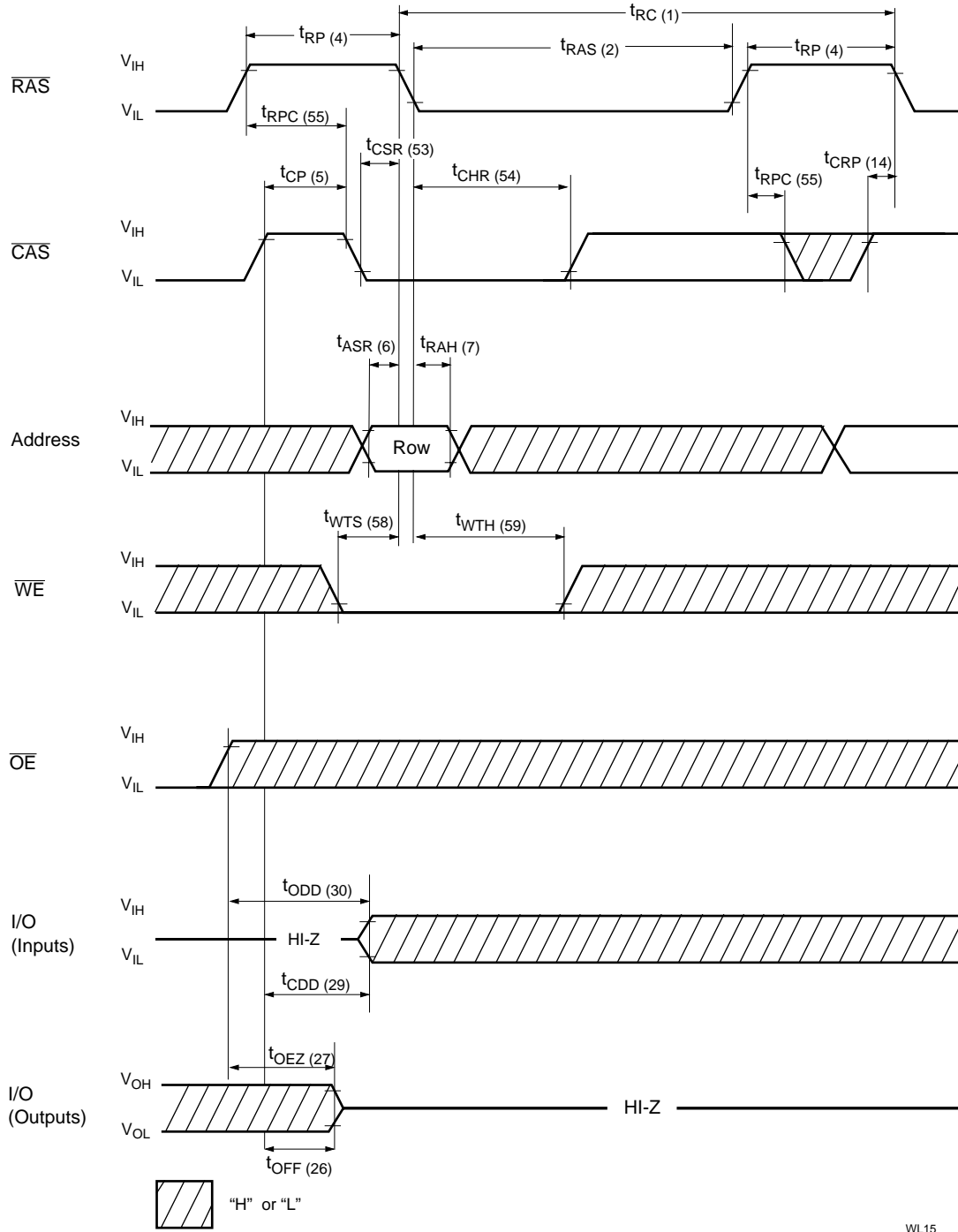


**Waveforms of Hidden Refresh Cycle (Early Write)**



WL12

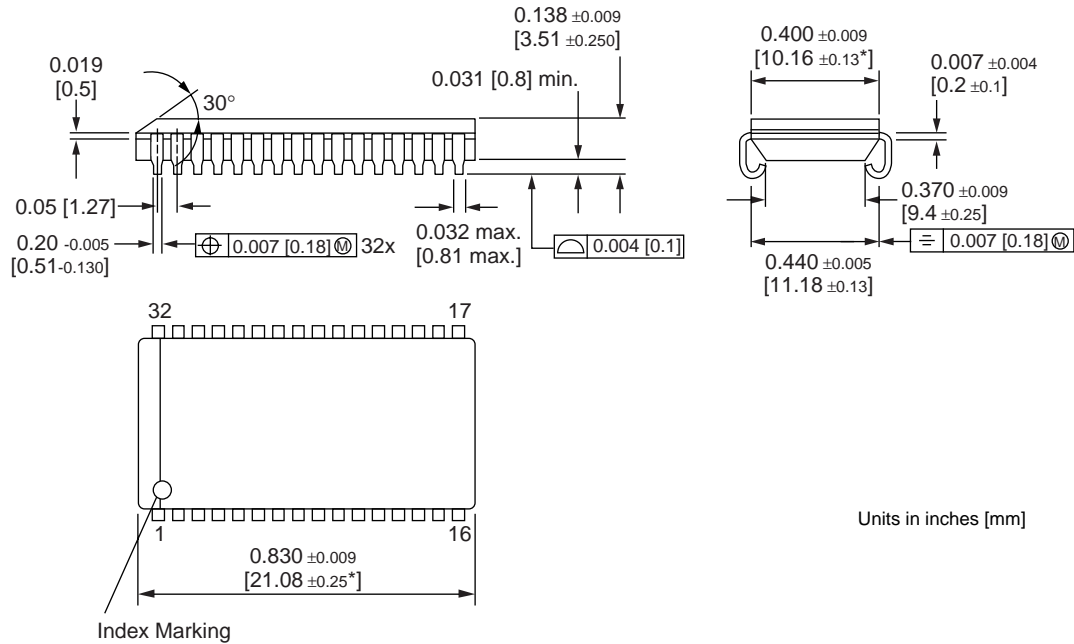
**Waveforms of Test Mode Entry Cycle**



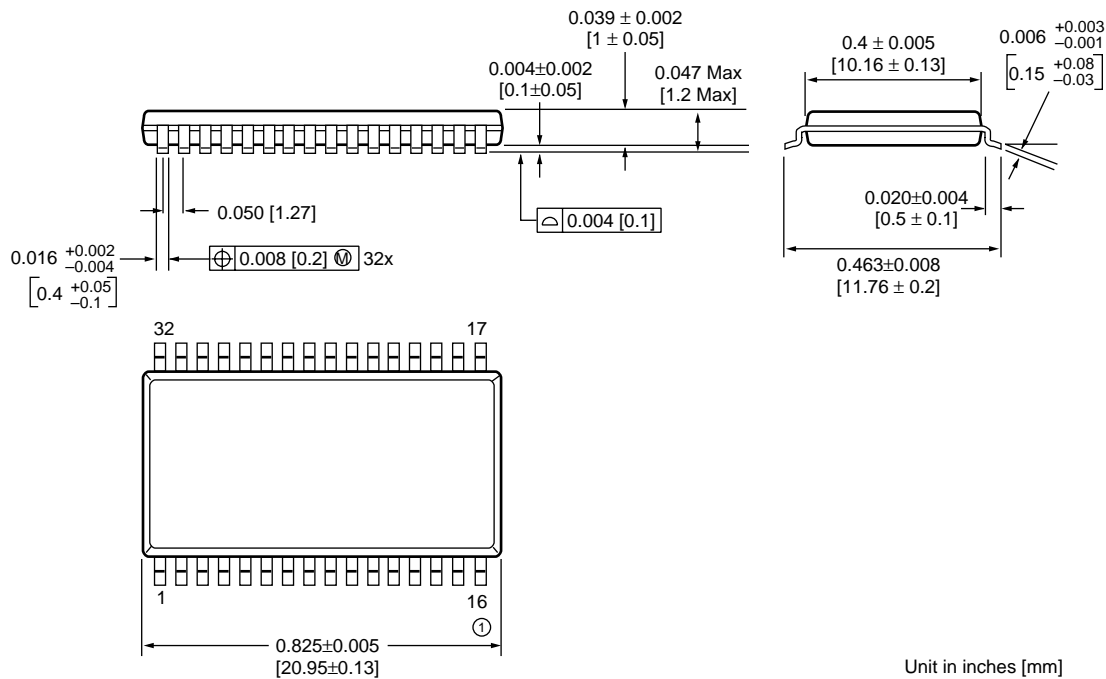
WL15

**Package Diagrams**

**32-pin 400 mil SOJ**



**32-pin 400 mil TSOP-II**



**Notes:**

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