YAMAHA LSI

YTD423

IHDLC2

ISDN BRI controller with B-ch HDLC controllers

1 INTRODUCTION

YTD423 is a high-performance communication LSI for the ISDN BRI user-network interface function (digital four-wire time-division full-duplex operation), supporting D-channel layer 1, layer 2 and HDLC controller for B-channels, all in one 100-pin SQFP chip. YTD423 supports layer 1 (physical layer) control function conforming to ITU-T Recommendation I.430 and fully supports layer 2 (LAP-D protocol) function conforming to ITU-T Recommendations Q.920 and Q.921. ETSI (European Telecommunications Standards Institute) and several North American standard operating modes are also supported. In addition, YTD423 includes layer 3 processor interface function and 2-channel HDLC controller for B-channels, which operate in DMA transfer mode or I/O transfer mode. This gives a great advantage to mounting and functional designing of both "active" (with CPU on board) terminal equipment and "passive" (no CPU on board) PC cards. In order to support the U interface, YTD423 has a TTL interface (no built-in analog driver/receiver) suitable for connecting to an NT1 chip or a DSU module. S/T reference point can also be supported by connecting it to YTD421 (analog driver/receiver LSI).

1.1 Features

1. Layer 1 function

   - Supports layer 1 control function conforming to ITU-T Recommendation I.430 [1992 edition] and TTC Standard JT-I430 [1993 edition] (default)
     - TTL interface
     - 192 kbps transmission rate
     - Interface structure : 2B + D (B = 64 kbps, D = 16 kbps)
     - Frame assembling and disassembling function
     - Collision control (built-in random number (Ri) reset), priority control (built-in retransmission control), and state transition control
     - Programmable T3 and T4 timers

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YTD423D CATALOG
CATALOG No.:4TD423D2
1999.2

- Supports ETSI ETS 300 012 [April 1992] and ANSI T1.605 operating modes
- Leased line capability (JT-I430-a)
- B channel I/O clock selection function
  - Internal clock mode: Inputs/outputs the B-channel data with 64 k, 56 k or 32 kHz internal clock
  - External clock mode (PCM Highway mode): Inputs/outputs the B channel data with a 128 kHz to 2048 kHz external clock
- B channel selection function
  - Internal clock mode: Selects/switches B channel I/O pins
  - External clock mode (PCM Highway mode): Selects/switches B channel time slots
- Multiframing capability
- Abundant Test functions (for testing and maintenance)
  - Three kinds of loop-back modes (Loop-back 1 to 3)
  - INFO signals output for testing
  - Test pulse output for pulse shape evaluation
- INFO1 transmission and INFO4 reception monitor pins
- SLEEP monitor pin
- I.430 transmission frame phase adjustment function

2. Layer 2 function

- Conforms to ITU-T Recommendation Q.920 and Q.921 [1992 edition] and TTC Standard JT-Q920 and JT-Q921 [1993 edition] (default)
  - HDLC frame control (Flag control, FCS generation/checking, automatic zero insertion/deletion, abort pattern transmission/detection, etc.)
  - LAP-D status control (sequence control, flow control, SAPI control)
  - Built-in timer for time-out check
- Supports ETSI ETS 300 125 [September 1991], National ISDN-1/2, AT&T 5ESS 5E9 and Nortel DMS-100 S208-6 operating modes
- Multi-link capability (circuit switching, packet switching)
- Automatic assigned TEI/non-automatic assigned TEI (VC/PVC)
- Leased line mode (disable layer 2 function)

3. Layer 3 interface function

- Connects to 8-bit or 16-bit microprocessor (8086 family, Z80 family, 6800 family and 68000 family)
- Operates in one of two data transfer modes
  - DMA transfer mode (with the built-in 24-bit address DMA controller)
  - I/O transfer mode (with the built-in FIFO)
- Primitive logical interface

4. HDLC controller for B-channels
   - HDLC frame control (Flag control, optional marks or flags in idle state, optional FCS generation/checking, automatic zero insertion/deletion, abort pattern transmission/detection, optional address field generation/checking etc.)
   - Full-duplex communication × 2 channels
   - Data rates Network synchronization clock mode : 56 k or 64 kbps
     Network independent clock mode : Up to 128 kbps
   - Optional 16-bit/32-bit CRC
   - Programmable data transfer modes
     - DMA transfer mode (with the built-in DMA controller)
       * optional 8-bit/16-bit access
       * 24-bit address
       * 4 channels
     - I/O transfer mode (with the built-in FIFO)
       * Tx FIFO : 32 bytes × 2
       * Rx FIFO : 64 bytes × 2
       * Variable interrupt levels
       * Byte/Word access selection
   - Optional transparent mode (disable HDLC controller function)
5. Low-power operation (the host processor clock control function, LSI internal clock freezing function)
6. CMOS technology
7. 100-pin SQFP
8. Single +5V volt supply

1.2 Applications

- Terminal Adapter (TA)
- Router
- ISDN PC Card
- PBX
- ISDN Telephone

2 BLOCK DIAGRAM

2.1 User Network Interface Block Diagram

YTD423 is the most-suited LSI for terminal equipment such as terminal adapters and ISDN telephones and for PHS base stations. YTD423 contains layer 1 and layer 2 functions as well as the HDLC controller and DMA controller for the B channel. Because of this, terminal equipment can be optimally configured by adding few circuits such as the layer 3 control processor and analog driver/receiver.
The block diagram of the user network interface with YTD423 is shown in Figure 1.

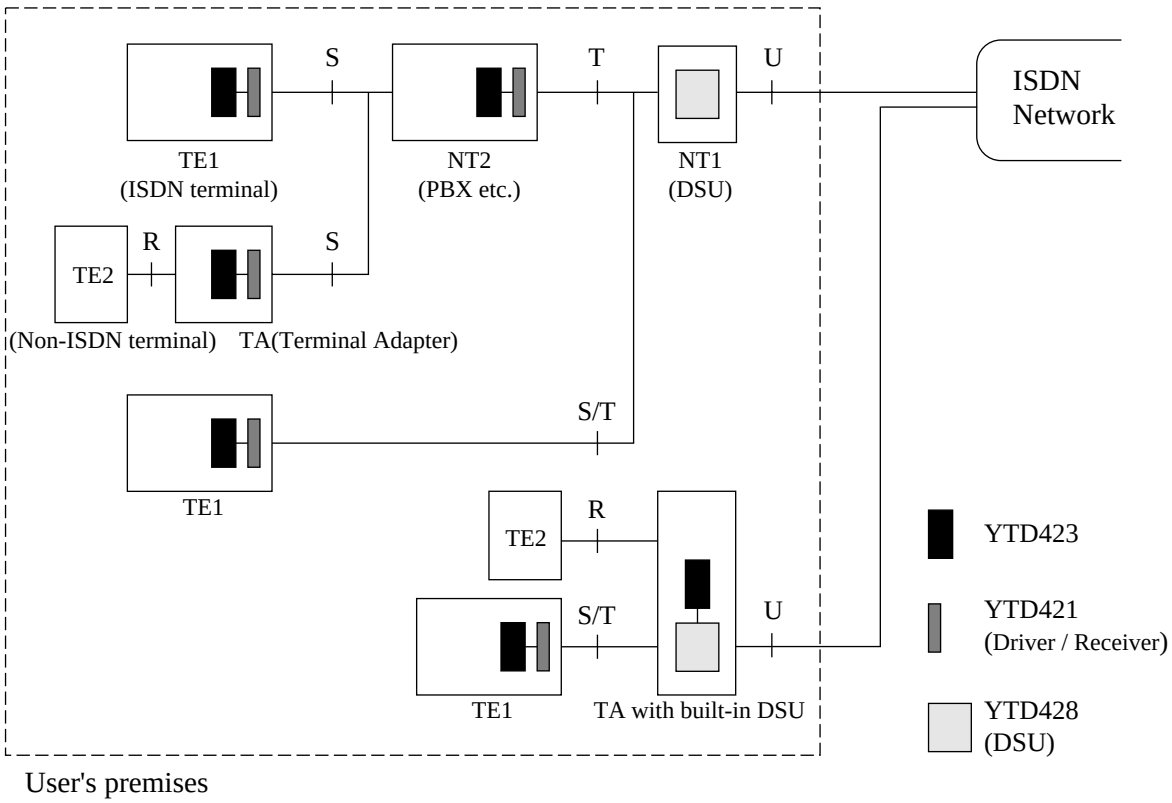


Figure 1: User Network Interface Block Diagram

2.2 YTD423 Peripheral LSI Interface Block Diagram

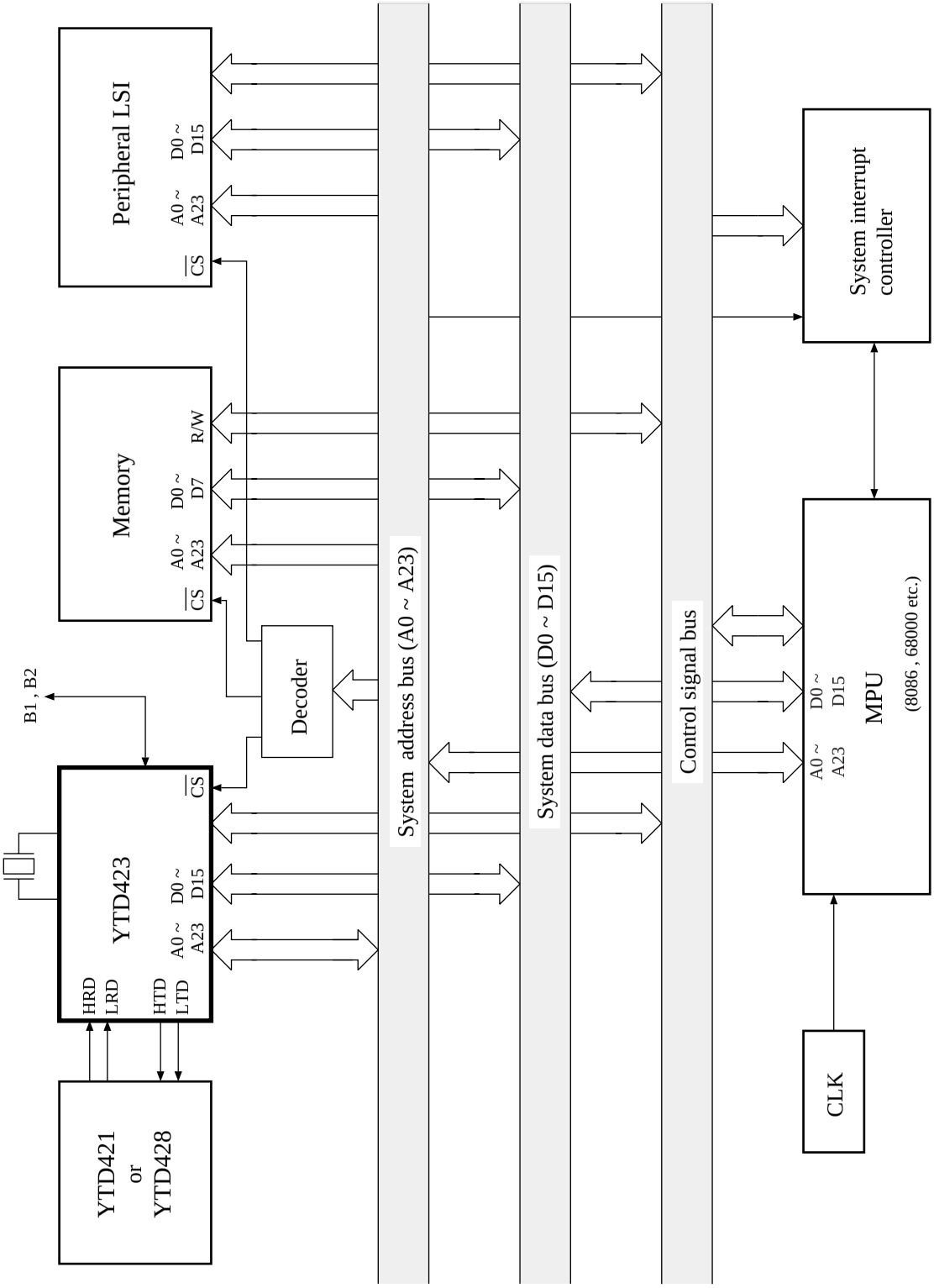


Figure 2: Peripheral LSI Interface Block Diagram

2.3 YTD423 Internal Block Diagram

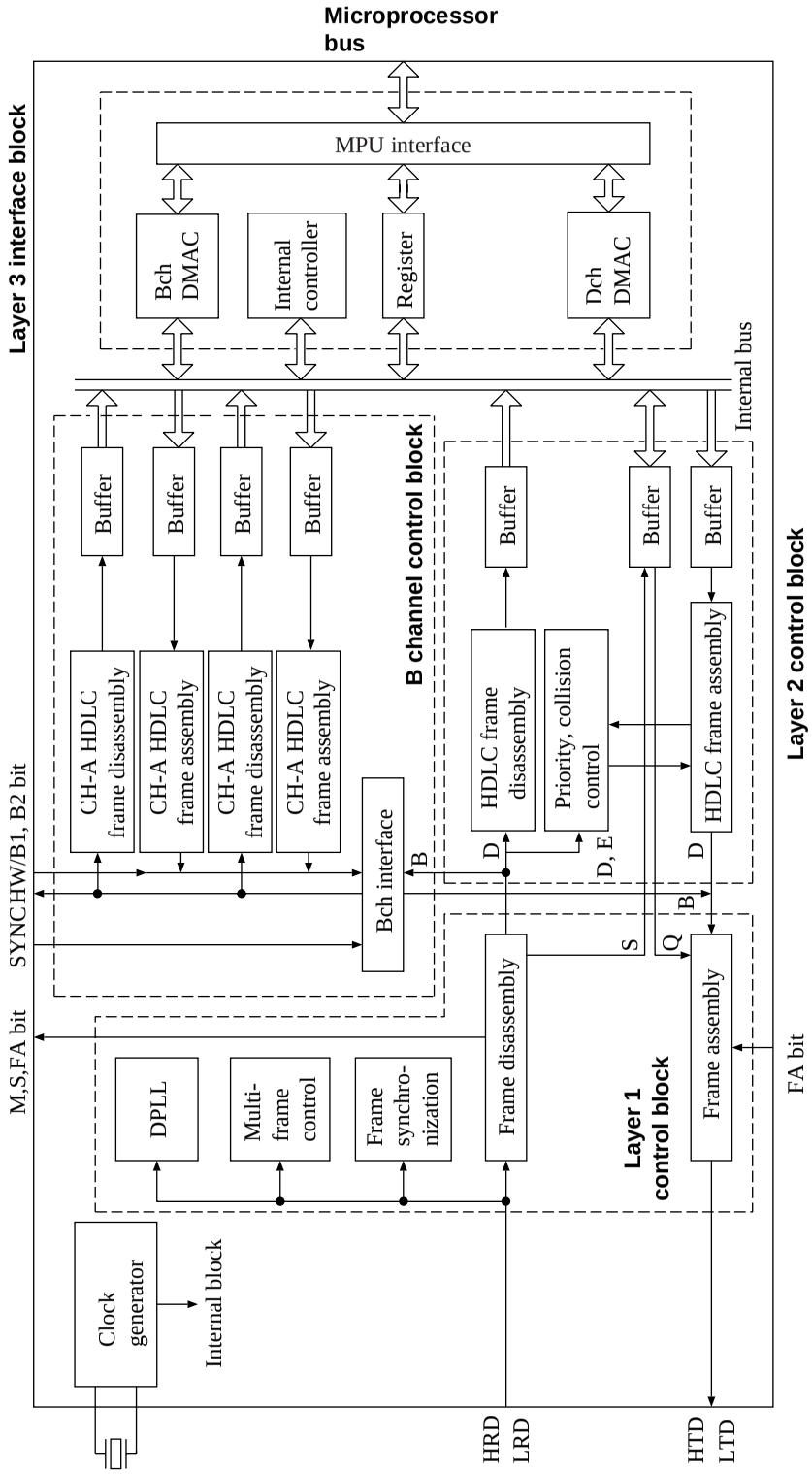


Figure 3: Internal Block Diagram

3 Pin Assignments

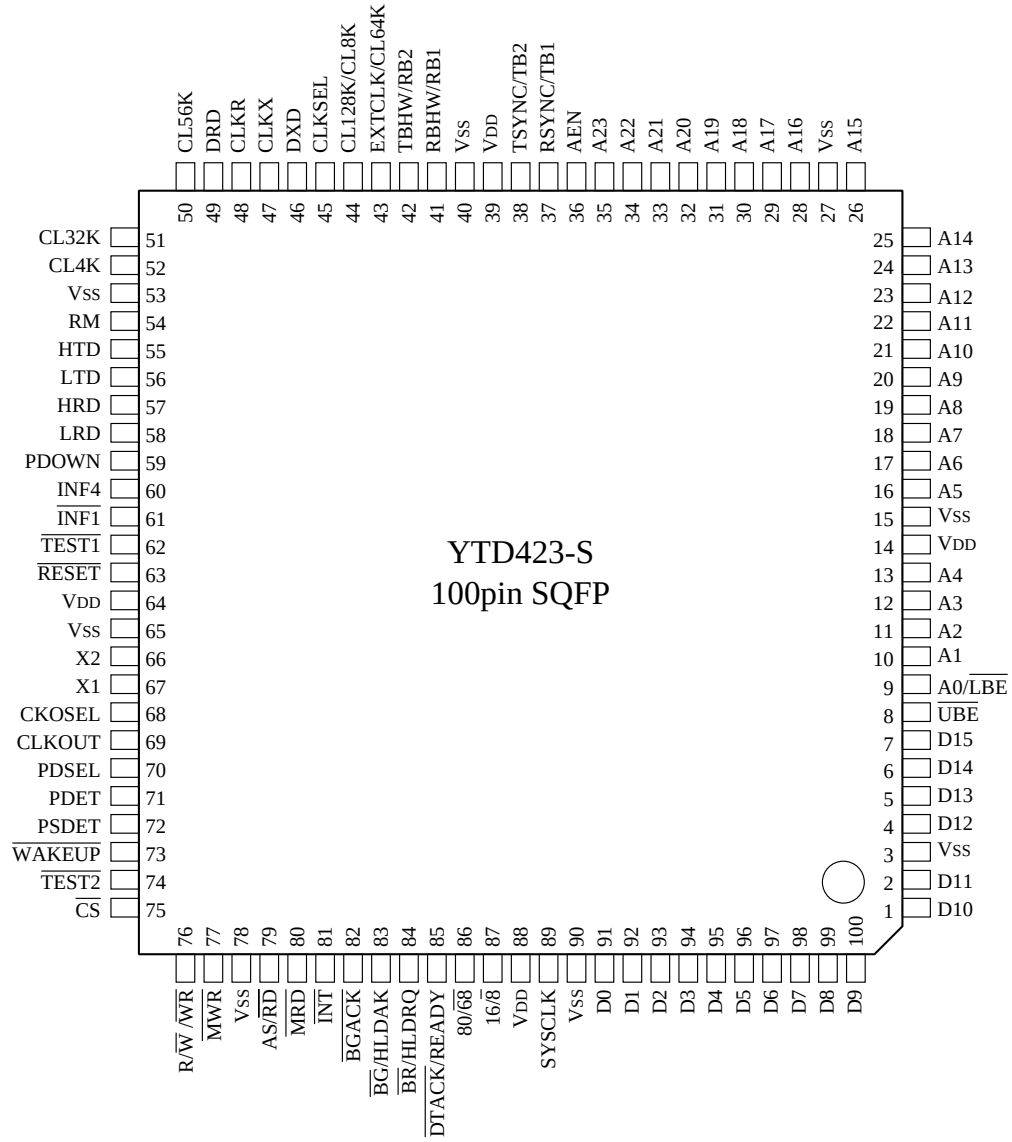


Figure 4: YTD423-S (100-pin SQFP) Pin Assignments

4 ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{DD}	-0.3	$+7.0$	V
Input Voltage	V_{IN}	-0.3	$V_{DD}+0.3$	V
Operating Temperature	T_{op}	-20	$+70$	°C
Storage Temperature	T_{stg}	-50	$+125$	°C

(Based on V_{SS} = 0.0 V)

4.2 Recommended Operating Conditions

Supply Voltage	5 V ± 5 % (Based on V_{SS} = 0.0V)
Operating Temperature	-20 - 70 °C

4.3 DC Characteristics

(V_{DD} = 5 V ± 5%, T_{op} = −20 - 70 °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
High-Level Input Voltage (CMOS)	V_{IH}	**(Note 1)**	0.8V_{DD}			V
Low-Level Input Voltage (CMOS)	V_{IL}	**(Note 1)**			0.2V_{DD}	V
High-Level Input Voltage (TTL)	V_{IH}	**(Note 2)**	2.2			V
Low-Level Input Voltage (TTL)	V_{IL}	**(Note 2)**			0.8	V
High-Level Output Voltage (CMOS)	V_{OH}	$\|I_{OH}\| < 10\mu A$	$V_{DD}-0.4$			V
Low-Level Output Voltage (CMOS)	V_{OL}	$\|I_{OL}\| < 10\mu A$			$V_{SS}+0.4$	V
High-Level Output Voltage (TTL)	V_{OH}	**(Note 3)**	2.7			V
Low-Level Output Voltage (TTL)	V_{OL}	**(Note 3)**			0.4	V
Low-Level Output Voltage (Open-D)	V_{OL}	**(Note 4)**			0.4	V
Leakage Current	I_L		−10		10	μA
Off-State Leakage Current	I_{LZ}	**(Note 5)**	−10		10	μA
Power Supply Current	I_{DD}	**(Note 6)**		17		mA
		(Note 7)		0.2		mA

Note 1: With respect to X1,$\overline{\text{RESET}}$, $\overline{\text{TEST1}}$, $\overline{\text{TEST2}}$, $\overline{\text{WAKEUP}}$, PDET, CLKSEL, PSDET pins.

Note 2: With respect to other pins.

Note 3: CLKOUT pin Test condition: I_{OH} = -1.0 mA, I_{OL} = 2.0 mA
other output pins Test condition: I_{OH} = -0.4 mA, I_{OL} = 1.2 mA

Note 4: HTD, LTD, $\overline{\text{INT}}$ pin Test condition : I_{OL} = 1.2 mA
$\overline{\text{INF1}}$ pin Test condition : I_{OL} = 3 mA
RBHW pin Test condition : I_{OL} = 0.8 mA, R_L = 500 Ω

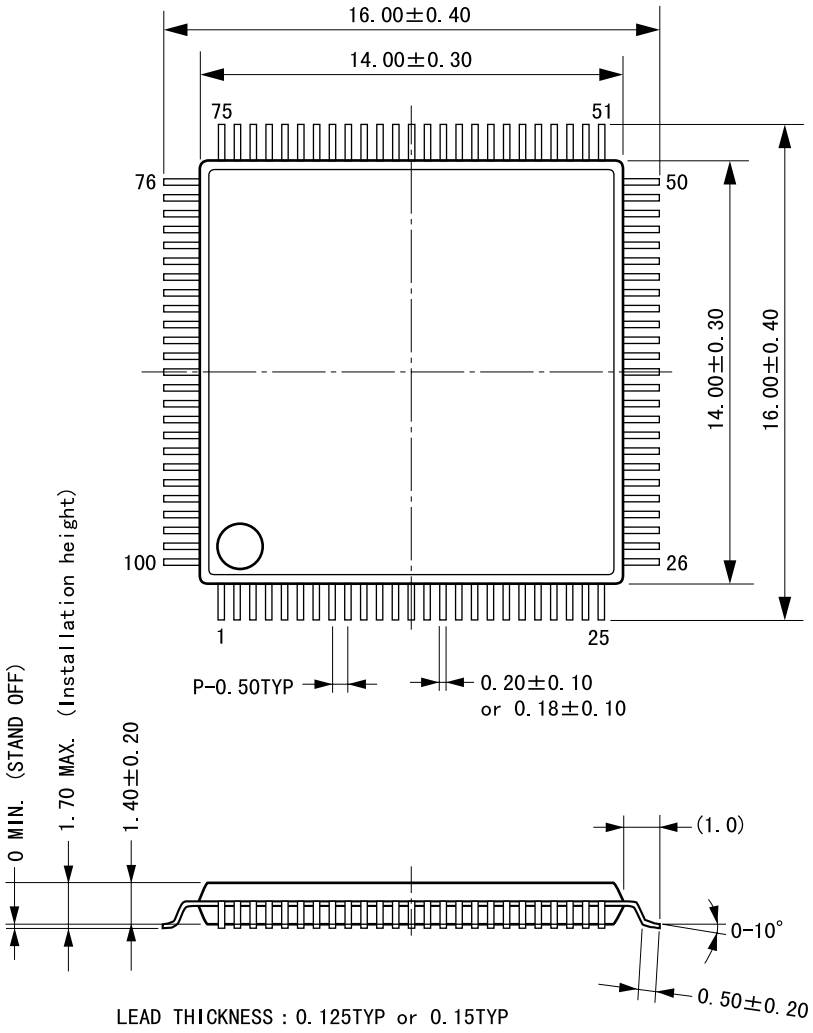
Note 5: With respect to cases in which D0-D15, A0-A23, and $\overline{\text{UBE}}$ pins are in the input state and $\overline{\text{MWR}}$ and $\overline{\text{MRD}}$ pins are in Hi-Z state.

Note 6: RUN state (SYSCLK = 8 MHz)

Note 7: SLEEP state

5 PACKAGE OUTLINE

C-PK100SP-1



(UNIT) : mm (millimeters)

The shape of the molded corner may slightly different from the shape in this diagram.

The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

(Note)	The LSIs for surface mount need special consideration on storage and soldering conditions. For detailed information, please contact your nearest Yamaha agent.

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