TDK SEMICONDUCTOR CORP.

5503 DCR
Direct Conversion Receiver

Advanced Information

February 2001

DESCRIPTION

The 5503 is a low cost, high performance direct conversion receiver (DCR) specifically designed for digital wireless applications. The DCR architecture provides a receiver design with fewer external components than the conventional dual conversion approach. The 5503 is designed to operate over an input frequency range of 950 to 1450 MHz. The device accepts an input signal in this frequency range and down converts directly to baseband. The local oscillator signal is generated by a completely integrated phase lock loop that is fully programmable through a standard serial port interface.

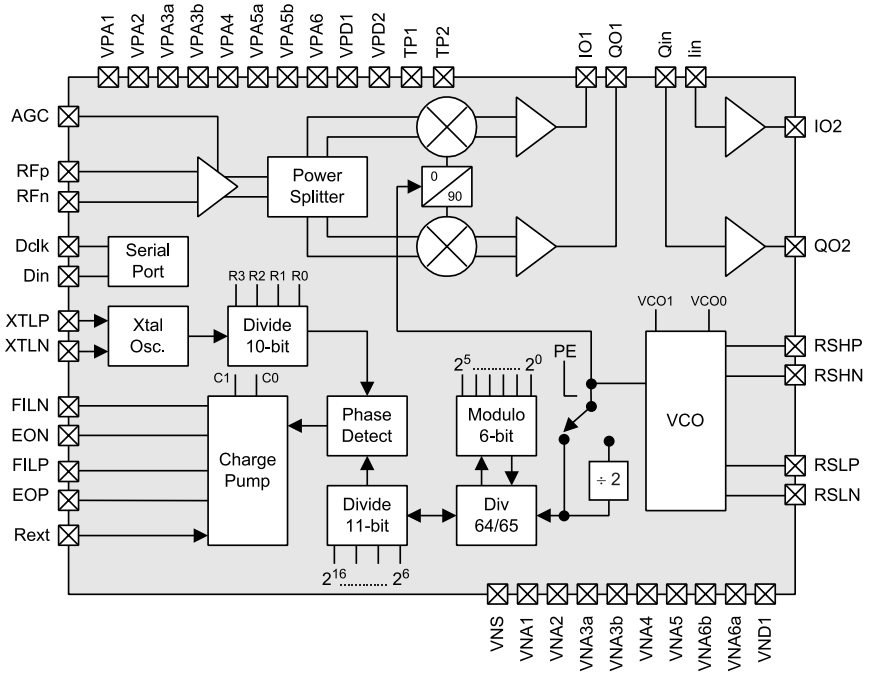
FEATURES

- **Wideband I/Q demodulator**
  - **– RF input 950 to 1450 MHz**
  - **– External lowpass filter**
  - **- Integrated post-filter baseband drivers**
- **Integrated VCO and frequency synthesizer**
- **AGC Amplifier**

APPLICATIONS

- **Digital Satellite**
- **VSAT Receivers**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

AGC Amplifier

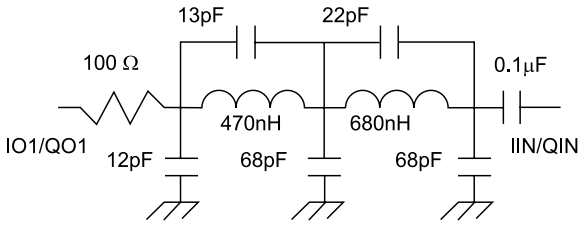
The 5503 RF input can be driven differentially or single ended. The *RFp* and *RFn* inputs are self-biasing and are designed to be driven from a 50 Ohm source. For single-ended operation, the *RFn* pin should be AC coupled to analog ground. A gain control input, AGC, provides a 22 dB gain variation with 0V providing minimum gain and 4V providing maximum gain.

I/Q Mixer

The AGC amplifier drives the RF port of two identical double balanced mixers. The LO ports of these mixers are driven from an on-chip quadrature network.

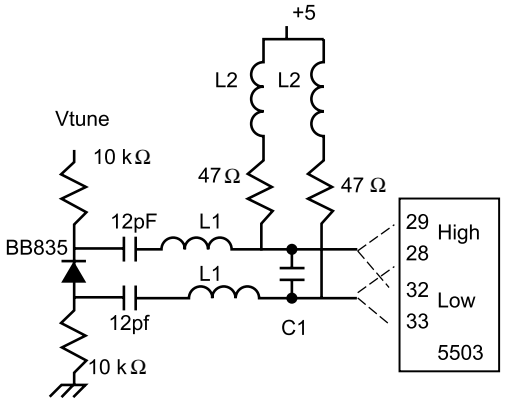
Low Pass Filtering and Buffering

Following each mixer is a buffer amplifier for driving an external passive low-pass filter. An external series resistor connected to the *IO1* or *QO1* output is used to provide the source match for the filter. A second high impedance buffer amplifier is provided (*IIN* or *QIN*) for additional gain and isolation after the filter. The figure below shows a typical filter designed for 20 Megasymbol per second operation:



Dual VCO

The 5503 uses two VCOs to cover the entire specified tuning range. Both VCOs use nearly identical architecture with the only difference being slight design modifications to optimize the range of operation. The lower range VCO requires an external resonator that supports a tuning range of 950 to 1150 MHz. The higher range VCO requires a similar resonator with inductor values designed to support the range of 1100 to 1475 MHz. A typical lumped-element resonator circuit incorporating varactor tuning is shown in the following figure:



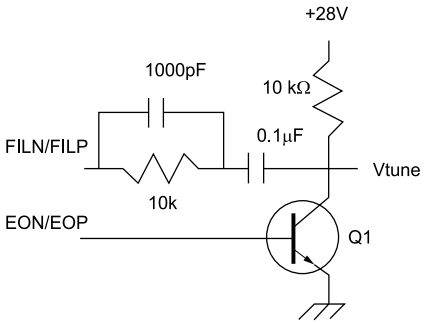
Note: A separate resonator circuit is required for each oscillator

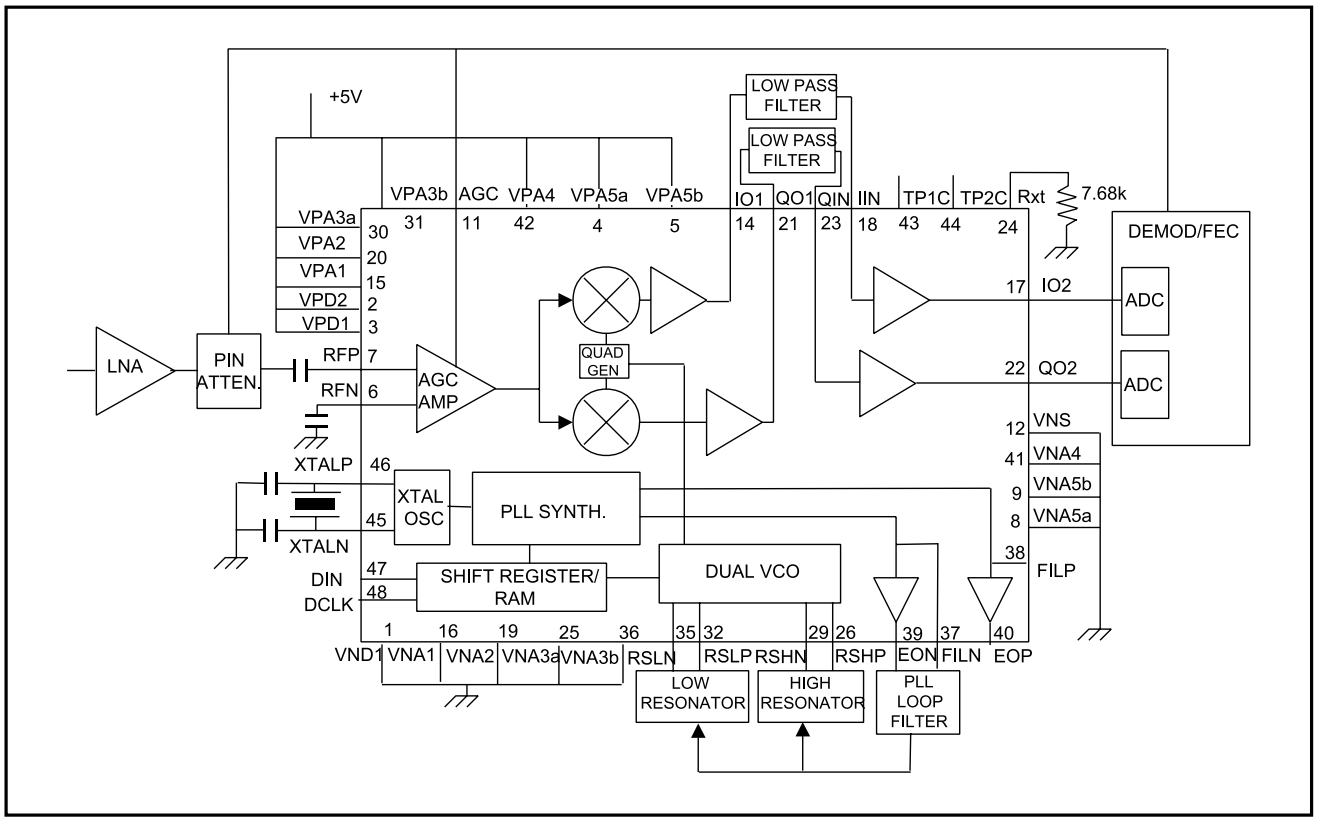
PLL Synthesizer

The synthesizer derives its reference from a source which can be either an externally derived clock or an external crystal coupled to the internal oscillator. This source drives a programmable reference divider with 15 preset divide ratios from 2 to 320. This output provides the PLL reference by driving one input of a phase/frequency detector. The VCO output drives a divider chain incorporating a selectable divide by two prescaler followed by a variable modulus prescaler and divider. The divider is programmed by a 17-bit control word. This divider chain output drives the other input of the phase/frequency detector.

Loop Filter

The phase/frequency detector provides two output pairs, *FILN*/*EON* and *FILP*/*EOP*. The *FILN*/*EON* outputs are used when the VCO has a positive gain characteristic (increasing voltage yields increasing frequency). The *FILP*/*EOP* outputs are used for a negative VCO gain characteristic. Below is shown a typical loop filter:





DCR Application Drawing

PIN DESCRIPTIONS

ANALOG PINS

NAME	TYPE	DESCRIPTION
RFP, RFN	I	RF inputs: balanced differential inputs to the receiver. The input signals placed on this line are amplified with a variable gain amplifier before being passed to the I/Q demodulator.
AGC	I	Automatic gain control input. A voltage from 0 to 4 volts on this pin varies the input amplifier gain from minimum to maximum. The gain increase is 22 dB typical
Eop, Filp	I/O	External loop filter interface. *Eop* drives the base of an external common emitter transistor. *Filp* is the feedback input from the loop filter capacitor. This output is used for a negative VCO gain characteristic.
Eon, Filn	I/O	External loop filter interface. *Eon* drives the base of an external common emitter transistor. *Filn* is the feedback input from the loop filter capacitor. This output is used for a positive VCO gain characteristic.
XTLP, XTLN	I	Reference crystal input. An external crystal connected between these pins establishes the reference frequency for the PLL synthesizer. The crystal frequency must be 8 MHz and have an ESR of less than 100 Ohms. Following this oscillator is a programmable divider which establishes the synthesizer step size.
IO2, QO2	O	Baseband outputs. These typically drive an A/D converter prior to digital demodulation and processing.
IO1, QO1	O	I and Q channel outputs to external low pass filter. An external series resistor is connected between this output and the filter to provide the source match.
IIN, QIN	I	I and Q channel inputs from external low pass filter. These are high impedance inputs (>1000Ω). The low pass filter must be designed for a low input and high output impedance.
Rxt	I	External reference resistor. This resistor is connected to ground and must be 7.68k ±1% . It is used as a reference for internal bias currents.
RSHP, RSHN	I	High range VCO resonator inputs
RSLP, RSLN	I	Low range VCO resonator inputs

DIGITAL PINS

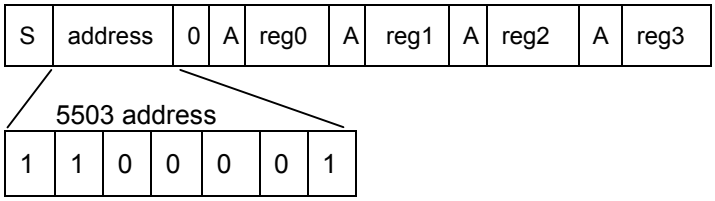
Din	I/O	I2C data. This signal is connected to the I2C internal block. An external resistor (typically 2.2 kΩ) is connected between Din and Vcc for proper operation
Dclk	I	I2C clock Input: *Dclk* should nominally be a square wave with a maximum frequency of 400kHz. SCL is generated by the system I2C master

POWER PINS

VPA1, VPA2, VPA3a, VPA3b, VPA4, VPA5a, VPA5b, VPA6	I	Analog Vcc pins
VPD1, VPD2	I	Digital Vcc pin.
VNA1, VNA2, VNA3a, VNA3b, VNA4, VNA6, VNA7	I	Analog ground pins.
VND1	I	Digital ground pin.
VNS	I	Substrate ground pin.

MICROCONTROLLER SERIAL INTERFACE

I²C REGISTERS: WRITE MODE



S : start bit

A : acknowledge bit

P : stop bit

TABLE 1: MICROCONTROLLER INTERFACE REGISTER

REGISTER	7(MSB)	6	5	4	3	2	1	0 (LSB)
0	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
1	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
2	1	2^{16}	2^{15}	PE	R3	R2	R1	R0
3	C1	C0	test1	test0	test2	vco1	vco0	x

DESCRIPTION OF INTERNAL REGISTERS

Register 0 VCO divide ratio, bits 14 thru 8, msb always set to 0

Register 1 VCO divide ratio, bits 7 thru 0

Register 2 msb Not Used. Always set to 1
VCO divide ratio, bits 16 and 15
PE, Prescaler enable. PE=1 enables divide by two prescaler
R3,R2,R1,R0 Reference division ratio, as shown in following table:

R3 R2 R1 R0	Reference division ratio
0 0 0 0	2
0 0 0 1	4
0 0 1 0	8
0 0 1 1	16
0 1 0 0	32
0 1 0 1	64
0 1 1 0	128
0 1 1 1	256
1 0 0 0	Undefined
1 0 0 1	5
1 0 1 0	10
1 0 1 1	20
1 1 0 0	40
1 1 0 1	80
1 1 1 0	160
1 1 1 1	320

Register 3 C1, C0 Phase detector current control, as shown in following table:

ipump word C1 C0	Phase Detector charge current μA
0 0	100
0 1	200
1 0	300
1 1	400

test0, test1 Test point select as shown in following table:

test1	test0	tp1	tp2
0	0	disabled	disabled
0	1	pump up	pump down
1	0	M cnt	N cnt
1	1	prescaler	modulus

test2 Phase detector disable (1 = disable, 0 = enable)

(vco0, vco1) Vco select word as shown in following table:

vco1	vco0	Low band VCO	High band VCO
0	0	disabled	disabled
0	1	enabled	disabled
1	0	disabled	enabled
1	1	undefined	undefined

ABSOLUTE MAXIMUM RATINGS

Operation beyond maximum rating may permanently damage the device.

PARAMETER	RATING
Storage temperature	-55 to 150 °C
Junction operating temperature	+110 °C
Positive supply voltage (Vp)	-0.3 to 6V
Voltage applied to any pin	-0.3V to VCCn+0.3V

TARGET SPECIFICATIONS

Unless otherwise specified: 0° < Ta < 70 °C; positive power supply (VCCn) = +5.0 V ±5%.

OPERATING CHARACTERISTICS

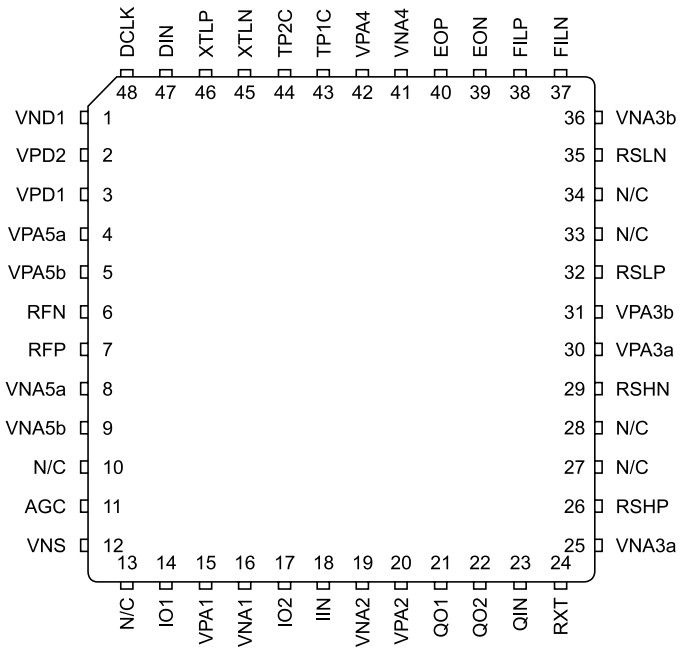
PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Supply current	All outputs loaded		120	150	mA
Digital I/O Characteristics (Din, Dclk)					
High level input voltage		2		Vcc+0.3	V
Low level input voltage		Gnd - 0.3		0.8	V
High level input current	Vin = Vcc - 1.0V			100	uA
Low level input current	Vin = 1.0V			- 400	uA
Receiver Characteristics Unless otherwise noted, input source impedance is 75 Ω					
Input impedance, RFp	RFn bypassed to ground with 100 pf		50		Ω
Input signal range		-58		-38	dBm
Input frequency range		950		1450	MHz
AGC Range	0V < V_{AGC} < 4V	20	22		dB
DCR Gain, Lower Band Range	Fin = 950 MHz	42		62	dB
DCR Gain, Upper Band Range	Fin = 1450 MHz	42		62	dB
Noise figure	Measured at maximum gain		15		dB
2^{nd} order IIP	Vrf_in = -38 dBm/tone		0		dBm
3^{rd} order IIP	Vrf_in = -38 dBm/tone	-12	-10		dBm
Lo Leakage	Measured at RFp		-60		dBm
VCO Characteristics					
Tuning range, Low OSC	L_1 = 8.2nH L_2 = 27nH C_1 = 1pF	950		1150	MHz
Tuning range, High OSC	L_1 = 3.9nH L_2 = 22nH C_1 = .6pF	1100		1475	MHz
Phase Noise	10kHz offset		-78		dBc/Hz

OPERATING CHARACTERISTICS (continued)

Low Pass Filter Interface					
IOLPF, QOLPF output imped.				10	Ω
Filter Loss				6db	
Filter Input Impedance	source match is by external R	50			Ω
I and Q Buffer Amplifier (each output loaded with 4pF in parallel with 20kΩ)					
Input impedance		1000			Ω
Voltage Gain	Freq = 30 MHz		23		dB
Output impedance				10	Ω
I/Q output amplitude			1.0	1.2	Vpp
-3dB frequency, Frf-Flo			75		MHz
Buffer THD			1%	2%	
Amplitude and Phase Characteristics					
I/Q quadrature accuracy		-3		+3	degree
I/Q amplitude matching		-1		+1	dB

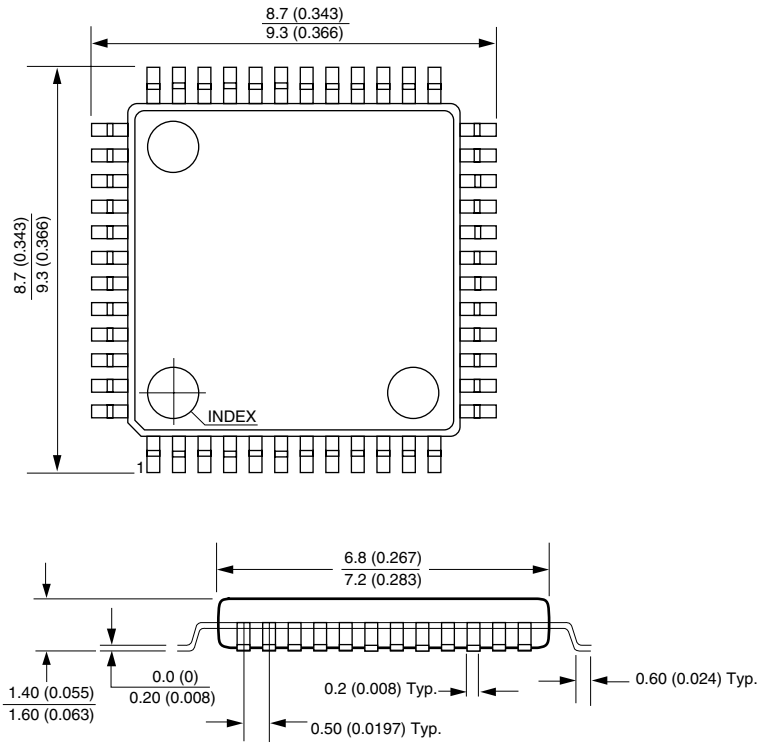
PACKAGE PIN DESIGNATIONS

(Top View)



48-TQFP
5503-CGT

MECHANICAL DRAWING



48-Lead Thin Quad Flatpack

Note: Controlling dimensions are in mm

PART DESCRIPTION	ORDER NO.	PACKAGE MARK
5503 DCR Direct Conversion Receiver	5503-CGT	5503-CGT

Advanced Information: The Advanced Information data sheet is to be approved for Beta Site and advanced customer information purposes only. It is not intended to replace the electrical specification for the specific device it represents. This document will be updated and converted into a Final (Preliminary Data Sheet) upon completion of Design Engineering Validation. Design Engineering should review this documentation for its accuracy to the definition and the design goals for the product it represents.

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