Low Voltage Controller for Touch Screens

AD7879

FEATURES

4-wire touch screen interface
1.6 V to 3.6 V operation
Median and averaging filter to reduce noise
Automatic conversion sequencer and timer
User-programmable conversion parameters
Auxiliary analog input/battery monitor (0.5 V to 5 V)
1 optional GPIO
Interrupt outputs ($\overline{\text{INT}}$, $\overline{\text{PENIRQ}}$)
Touch-pressure measurement
Wake-up on touch function
Shutdown mode: 6 µA maximum
12-ball, 1.6 mm × 2 mm WLCSP
16-lead, 4 mm × 4 mm LFCSP

APPLICATIONS

Personal digital assistants
Smart hand-held devices
Touch screen monitors
Point-of-sale terminals
Medical devices
Cell phones

FUNCTIONAL BLOCK DIAGRAM

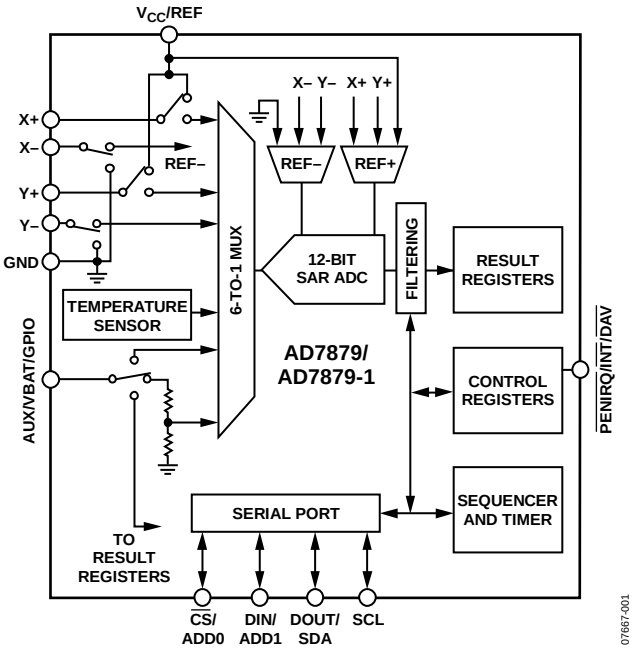

Figure 1.

GENERAL DESCRIPTION

The AD7879 is a 12-bit successive approximation analog-to-digital converter (ADC) with a synchronous serial interface and low on-resistance switches for driving 4-wire resistive touch screens. The AD7879 works with a very low power supply (a single 1.6 V to 3.6 V) and features throughput rates of 105 kSPS.

The device includes a shutdown mode that reduces its current consumption to less than 6 µA.

To reduce the effects of noise from LCDs and other sources, the AD7879 contains a preprocessing block. The preprocessing function consists of a median and an averaging filter. The combination of these two techniques provides a more robust solution, discarding the spurious noise in the signal and keeping only the data of interest. The size of both filters is programmable. Other user-programmable conversion controls include variable acquisition time and first conversion delay; up to 16 averages can be taken per conversion. The AD7879 can run in either slave or standalone mode, using an automatic conversion sequencer and timer.

The AD7879 has a programmable pin that can operate as an auxiliary input to the ADC, as a battery monitor, or as a GPIO. There is also a programmable interrupt output that can operate in three modes: as a general-purpose interrupt to signal when new data is available $\overline{\text{INT}}$, as an interrupt to indicate when limits are exceeded, or as a pen-down interrupt when the screen is touched ($\overline{\text{PENIRQ}}$). The AD7879 offers temperature measurement and touch-pressure measurement.

The AD7879 is available in a 12-ball, 1.6 mm × 2 mm WLCSP and in a 16-lead, 4 mm × 4 mm LFCSP. The part also has either an SPI (AD7879) or I²C (AD7879-1) interface.

Rev. 0

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REVISION HISTORY

10/08—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 1.6 V to 3.6 V, T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC ACCURACY					
Resolution	12			Bits	
No Missing Codes	11	12		Bits	
Integral Nonlinearity (INL)[1]			±3	LSB	LSB size = 390 µV
Differential Nonlinearity (DNL)[1]					LSB size = 390 µV
Negative DNL			−0.99	LSB	
Positive DNL			+2	LSB	
Offset Error[2]		±2	±6	LSB	
Gain Error[2]			±4	LSB	
Noise[3]		70		µV rms	
Power Supply Rejection[3]		60		dB	
Internal Clock Frequency		2		MHz	
SWITCH DRIVERS					
On Resistance[1]					
Y+, X+		6		Ω	
Y−, X−		5		Ω	
ANALOG INPUTS					
Input Voltage Ranges	0		V_{CC}	V	
DC Leakage Current		±0.1		µA	
Input Capacitance		30		pF	
Accuracy		0.3		%	
TEMPERATURE MEASUREMENT					
Temperature Range	−40		+85	°C	
Resolution		0.3		°C	
Accuracy[2]		±2		°C	Calibrated at 25°C
BATTERY MONITOR					
Input Voltage Range	0		5	V	
Input Impedance[3]		16		kΩ	
Accuracy		2	5	%	Uncalibrated accuracy
LOGIC INPUTS (DIN, SCL, $\overline{CS}$, SDA, GPIO)					
Input High Voltage, V_{INH}	0.7 V_{CC}			V	
Input Low Voltage, V_{INL}			0.3 V_{CC}	V	
Input Current, I_{IN}		0.01		µA	V_{IN} = 0 V or V_{CC}
Input Capacitance, C_{IN}[3]		10		pF	
LOGIC OUTPUTS (DOUT, GPIO, SCL, SDA, $\overline{INT}$)					
Output High Voltage, V_{OH}	V_{CC} − 0.2			V	
Output Low Voltage, V_{OL}			0.4	V	
Floating-State Leakage Current		±0.1		µA	
Floating-State Output Capacitance[2]		5		pF	
CONVERSION RATE[3]					
Conversion Time		9.5		µs	Including 2 µs of acquisition time
Throughput Rate		105		kSPS	
POWER REQUIREMENTS					
V_{CC} (Specified Performance)	1.6	2.6	3.6	V	
I_{CC}					Digital inputs = 0 V or V_{CC}
Converting Mode		480	650	µA	ADC on, PM = 10
Static		406		µA	ADC and temperature sensor are off; the reference and oscillator are on; PM = 01, 11
Shutdown Mode		0.5	6	µA	PM = 00

[1] See the Terminology section.
[2] Guaranteed by characterization, not production tested.
[3] Sample tested at 25°C to ensure compliance.

SPI TIMING SPECIFICATIONS (AD7879)

T_A = −40°C to +85°C; V_{CC} = 1.6 V to 3.6 V, unless otherwise noted. Sample tested at 25°C to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.4 V.

Table 2.

Parameter[1]	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCLK}	5	MHz max	
t_1	5	ns min	$\overline{CS}$ falling edge to first SCL falling edge
t_2	20	ns min	SCL high pulse width
t_3	20	ns min	SCL low pulse width
t_4	15	ns min	DIN setup time
t_5	15	ns min	DIN hold time
t_6	20	ns max	DOUT access time after SCL falling edge
t_7	16	ns max	$\overline{CS}$ rising edge to DOUT high impedance
t_8	15	ns min	SCL rising edge to $\overline{CS}$ high

[1] Guaranteed by design, not production tested.

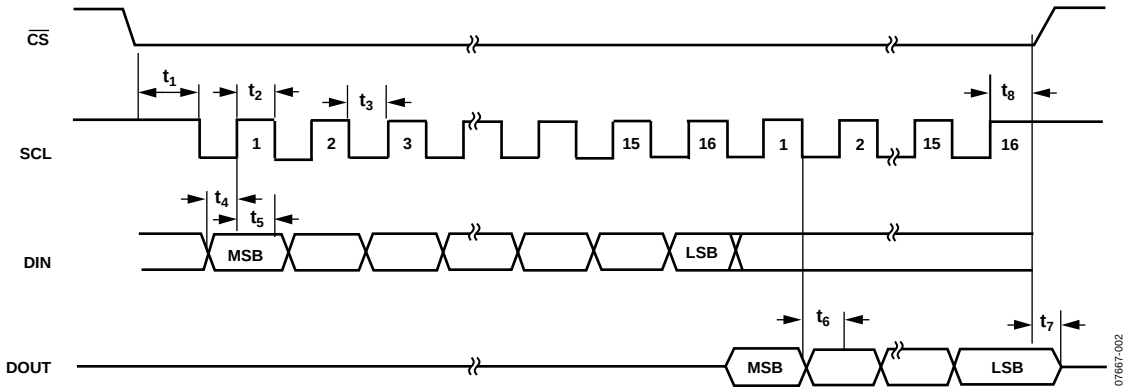


Figure 2. Detailed SPI Timing Diagram

I²C TIMING SPECIFICATIONS (AD7879-1)

T_A = −40°C to +85°C; V_{CC} = 1.6 V to 3.6 V, unless otherwise noted. Sample tested at 25°C to ensure compliance. All input signals are timed from a voltage level of 1.4 V.

Table 3.

Parameter[1]	Limit	Unit	Description
f_{SCLK}	400	kHz max	
t_1	0.6	µs min	Start condition hold time, $t_{HD; STA}$
t_2	1.3	µs min	Clock low period, t_{LOW}
t_3	0.6	µs min	Clock high period, t_{HIGH}
t_4	100	ns min	Data setup time, $t_{SU; DAT}$
t_5	300	ns min	Data hold time, $t_{HD; DAT}$
t_6	0.6	µs min	Stop condition setup time, $t_{SU; STO}$
t_7	0.6	µs min	Start condition setup time, $t_{SU; STA}$
t_8	1.3	µs min	Bus free time between stop and start conditions, t_{BUF}
t_R	300	ns max	Clock/data rise time
t_F	300	ns max	Clock/data fall time

[1] Guaranteed by design, not production tested.

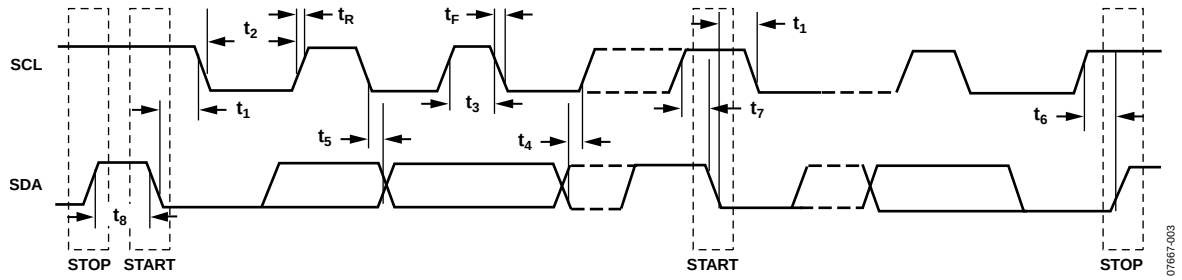


Figure 3. Detailed I²C Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 4.

Parameter	Rating
V_{CC} to GND	−0.3 V to +3.6 V
Analog Input Voltage to GND	−0.3 V to V_{CC} + 0.3 V
AUX/VBAT to GND	−0.3 V to V_{CC} + 5 V
Digital Input Voltage to GND	−0.3 V to V_{CC} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[1]	10 mA
ESD Rating (X+, Y+, X−, Y−)	
Air Discharge Human Body Model	15 kV
Contact Human Body Model	10 kV
ESD Rating (All Other Pins)	
Human Body Discharge	4 kV
Field Induced Charge Device Model	1 kV
Machine Model	0.2 kV
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
WLCSP (4-Layer Board)	
Power Dissipation	866 mW
θ_{JA} Thermal Impedance	75°C/W
LFCSP (4-Layer Board)	
Power Dissipation	2.138 W
θ_{JA} Thermal Impedance	30.4°C/W
IR Reflow Peak Temperature	260°C (±0.5°C)
Lead Temperature (Soldering 10 sec)	300°C

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

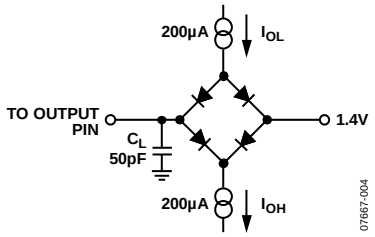


Figure 4. Circuit Used for Digital Timing

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

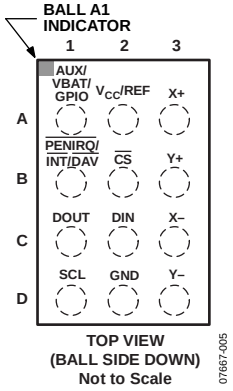


Figure 5. AD7879 WLCSP Pin Configuration

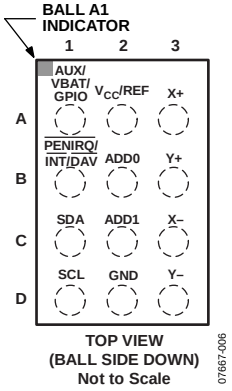


Figure 7. AD7879-1 WLCSP Pin Configuration

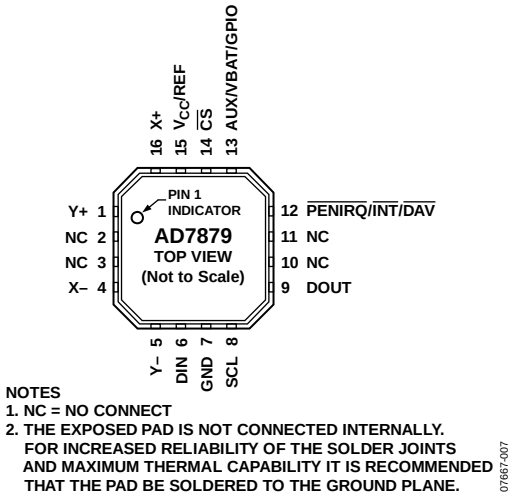


Figure 6. AD7879 LFCSP Pin Configuration

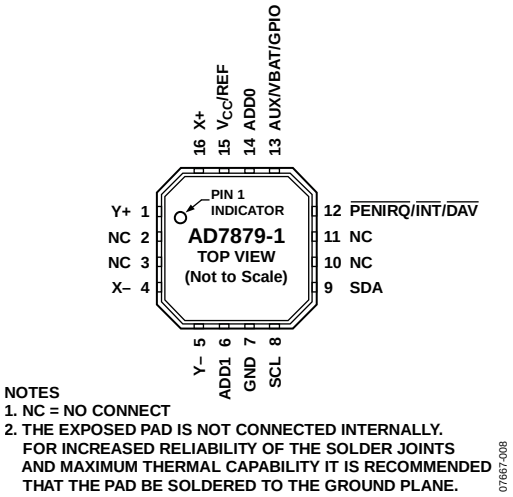


Figure 8. AD7879-1 LFCSP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.			
WLCSP	**LFCSP**	**Mnemonic**	**Description**
1A	13	AUX/VBAT/GPIO	Pin functionality is programmable to be either an auxiliary input to the ADC, as a battery measurement input to the ADC, or as a general-purpose digital input/output.
1B	12	$\overline{\text{PENIRQ}}/\overline{\text{INT}}/\overline{\text{DAV}}$	Interrupt Output. This pin asserts either when the screen is touched, when new data is available in the registers, or when a measurement exceeds the preprogrammed limits. Active low, internal pull-up resistor of 50 kΩ.
1C	9	DOUT SDA	SPI Serial Data Output on the AD7879. Serial Data Input and Output on the AD7879-1.
1D	8	SCL	Serial Interface Clock Input.
2A	15	V_{CC}/REF	Power Supply Input. It is also the ADC reference.
2B	14	$\overline{\text{CS}}$ ADD0	Chip Select for the Serial Interface on the AD7879. Active low. Address Bit 0 for the AD7879-1. This pin can be tied high or low to determine an address for the AD7879-1.
2C	6	DIN ADD1	SPI Serial Data Input to the AD7879. Address Bit 1 for the AD7879-1. This pin can be tied high or low to determine an address for the AD7879-1.
2D	7	GND	Ground. Ground reference point for all circuitry on the AD7879. All analog input signals and any external reference signal should be referred to this voltage.
3A	16	X+	Touch Screen Input Channel.
3B	1	Y+	Touch Screen Input Channel.
3C	4	X–	Touch Screen Input Channel.
3D	5	Y–	Touch Screen Input Channel.
N/A	2, 3, 10, 11	NC	No Connect.
N/A	17	EP	Exposed Pad.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 2.6 V, f_{SAMPLE} = 125 kHz, f_{DCLK} = 16 × f_{SAMPLE} = 2 MHz, unless otherwise noted.

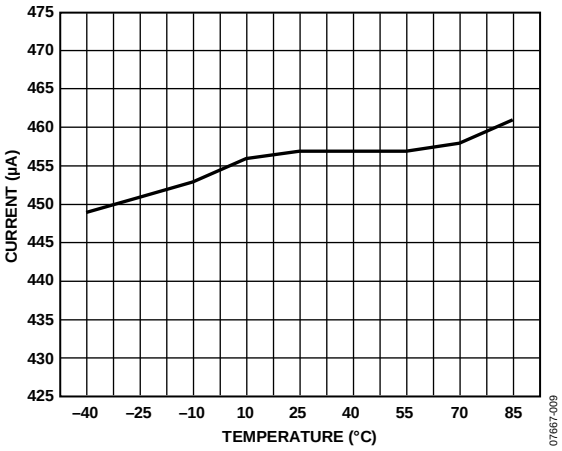


Figure 9. Supply Current vs. Temperature

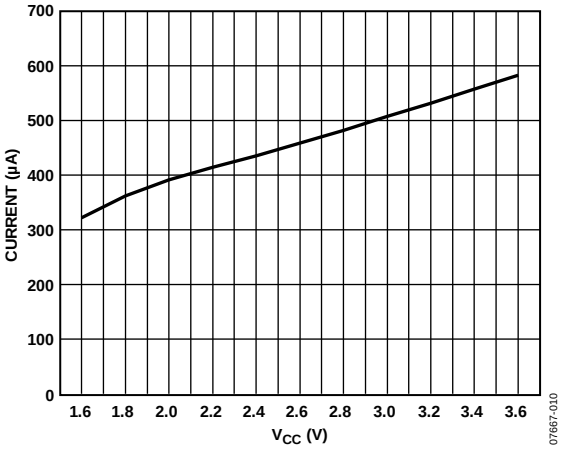


Figure 10. Supply Current vs. V_{CC}

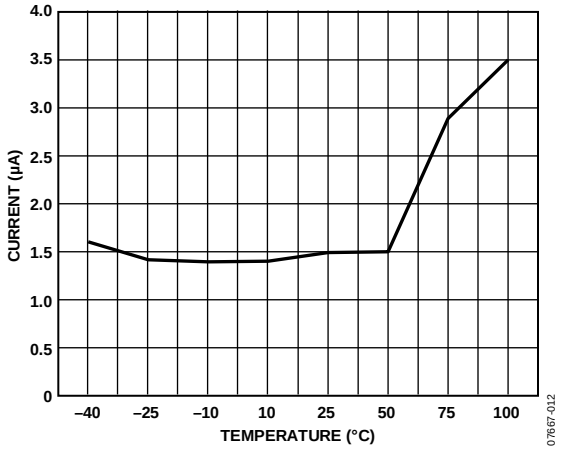


Figure 11. Full Power-Down I_{DD} vs. Temperature

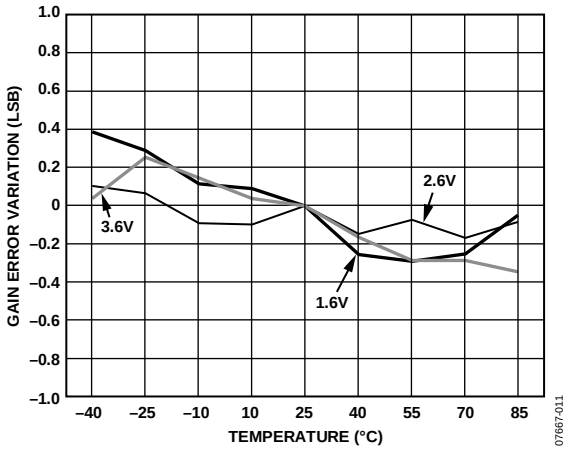


Figure 12. Change in ADC Gain vs. Temperature

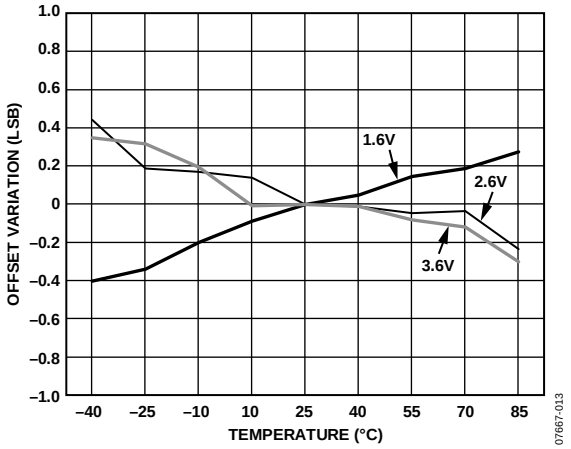


Figure 13. Change in ADC Offset vs. Temperature

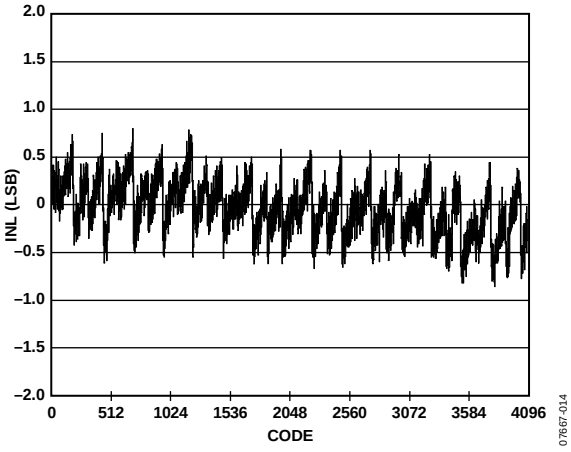


Figure 14. ADC INL Plot

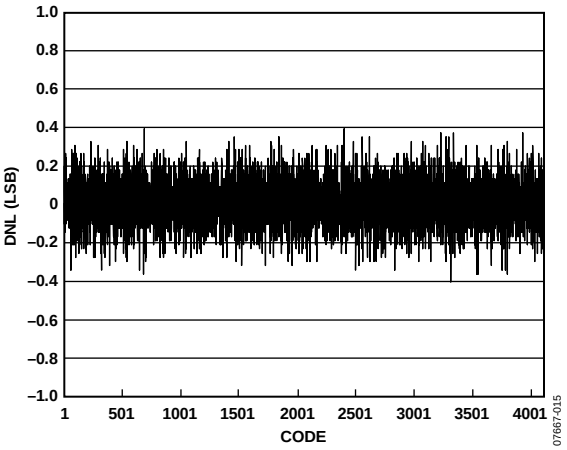


Figure 15. ADC DNL Plot

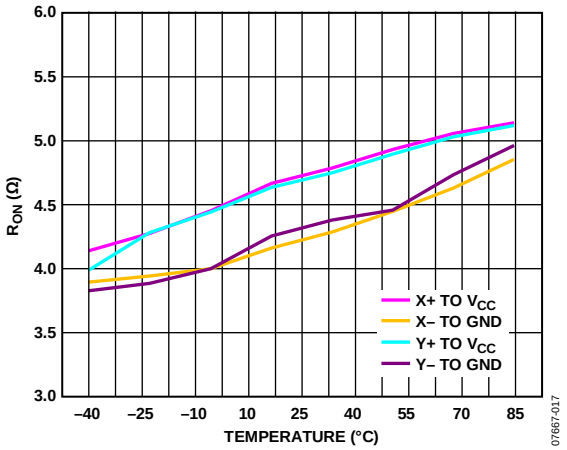


Figure 17 Switch On Resistance vs. Temperature (X+, Y+: V_{CC} to Pin; X–, Y–: Pin to GND)

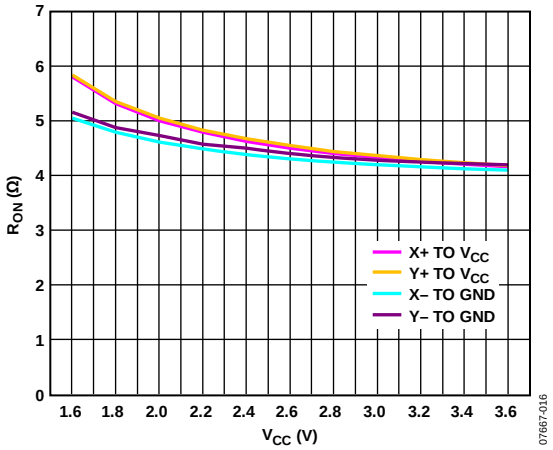


Figure 16. Switch On Resistance vs. V_{CC} (X+, Y+: V_{CC} to Pin; X–, Y–: Pin to GND)

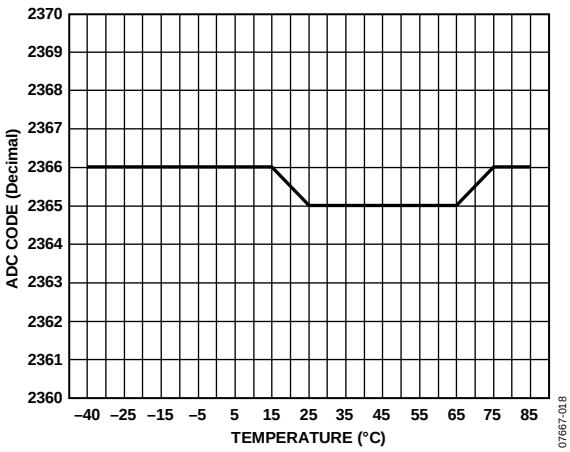


Figure 18. ADC Code vs. Temperature (Fixed Analog Input)

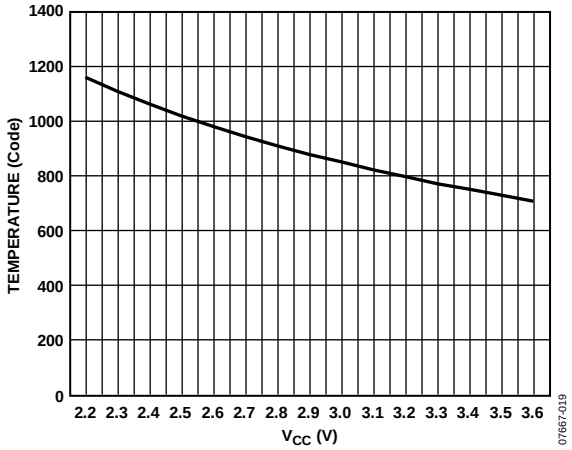


Figure 19. Temperature Code vs. V_{CC} for 25°C

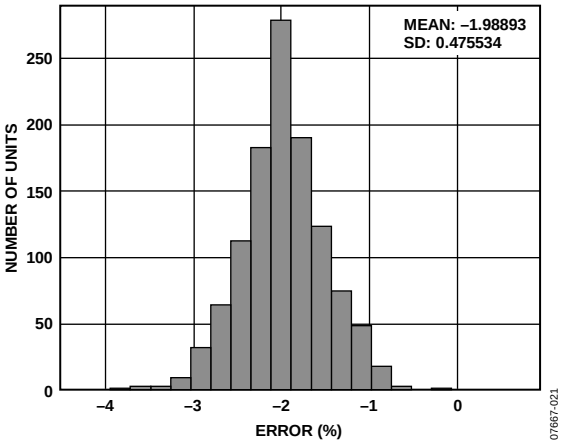


Figure 21. Typical Uncalibrated Accuracy for Battery Channel (25°C)

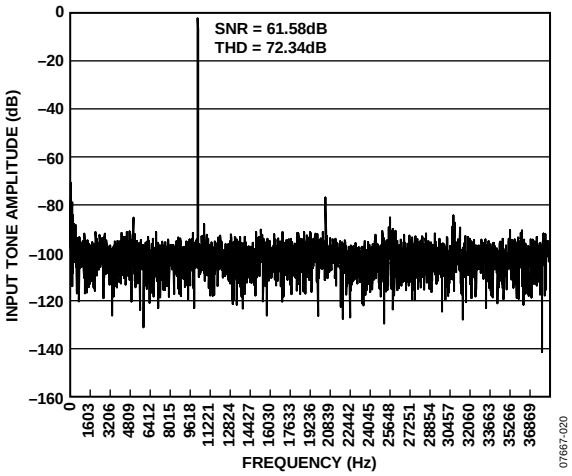


Figure 20. Typical FFT Plot for the Auxiliary Channels at 25 kHz Sampling Rate and 1 kHz Input Frequency

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale at 1 LSB below the first code transition and full scale at 1 LSB above the last code transition.

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
Offset error is the deviation of the first code transition (00 … 000) to (00 … 001) from the ideal (AGND + 1 LSB).

Gain Error
Gain error is the deviation of the last code transition (111 … 110) to (111 … 111) from the ideal (V_{REF} − 1 LSB) after the offset error has been adjusted out.

On Resistance
On resistance is a measure of the ohmic resistance between the drain and the source of the switch drivers.

THEORY OF OPERATION

The AD7879 is a complete, 12-bit data acquisition system for digitizing positional inputs from a 4-wire resistive touch screen. To support this function, data acquisition on the AD7879 is highly programmable so as to ensure accurate and noise free results from the touch screen.

The core of the AD7879 is a high speed, low power, 12-bit analog-to-digital converter (ADC) with input multiplexer, on-chip track-and-hold, and on-chip clock. Conversion results are stored in on-chip results registers. The results from the auxiliary input or the battery input can be compared with high and low limits stored in limit registers to generate an out-of-limit $\overline{\text{INT}}$.

The AD7879 also contains low resistance analog switches to switch the X and Y excitation voltages to the touch screen and the on-chip temperature sensor. The high speed SPI serial bus provides control of the devices, as well as communication with the device. The AD7879-1 is available with an I^2C interface.

Operating from a single supply from 1.6 V to 3.6 V, the AD7879 offers a throughput rate of 105 kHz. The device is available in a 1.6 mm × 2 mm 12-ball wafer level chip scale package (WLCSP) and in a 4 mm × 4 mm 16-lead lead frame chip scale package.

The AD7879 has an on-chip sequencer that schedules a sequence of preprogrammed conversions. The conversion sequence starts automatically when the screen is touched, or at preset intervals, using the on-board timer.

To ensure that the AD7879 works well with different touch screens, the user can select the acquisition time. There is also a programmable delay to ensure that the voltage on the touch screen settles before a measurement is taken.

To help reduce noise in the system, the ADC takes up to 16 conversion results from each channel, and writes the average of the results to the register. To further improve the performance of the AD7879, the median filter can also be used if there is noise present in the system.

TOUCH SCREEN PRINCIPLES

A 4-wire touch screen consists of two flexible, transparent, resistive-coated layers that are normally separated by a small air gap. The X layer has conductive electrodes running down the left and right edges, allowing the application of an excitation voltage across the X layer from left to right.

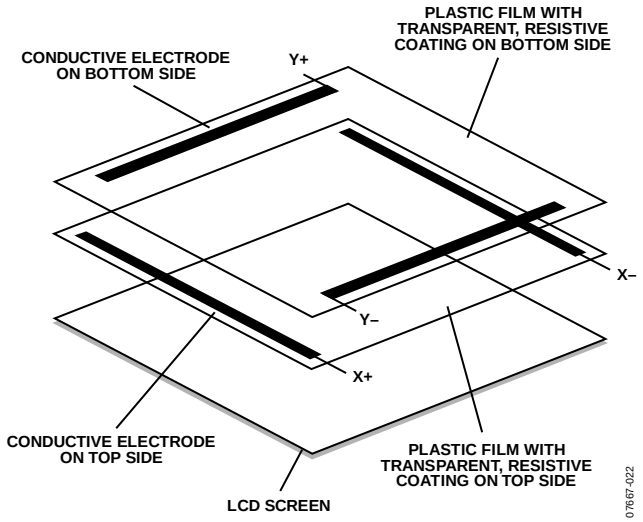


Figure 22. Basic Construction of a Touch Screen

The Y layer has conductive electrodes running along the top and bottom edges, allowing the application of an excitation voltage down the Y layer from top to bottom.

Provided that the layers are of uniform resistivity, the voltage at any point between the two electrodes is proportional to the horizontal position for the X layer and the vertical position for the Y layer.

When the screen is touched, the two layers make contact. If only the X layer is excited, the voltage at the point of contact, and therefore the horizontal position, can be sensed at one of the Y layer electrodes. Similarly, if only the Y layer is excited, the voltage, and therefore the vertical position, can be sensed at one of the X layer electrodes. By switching alternately between X and Y excitation and measuring the voltages, the X and Y coordinates of the contact point can be found.

In addition to measuring the X and Y coordinates, it is also possible to estimate the touch pressure by measuring the contact resistance between the X and Y layers. The AD7879 is designed to facilitate this measurement.

Figure 23 shows an equivalent circuit of the analog input structure of the AD7879, showing the touch screen switches, the main analog multiplexer, the ADC, and the dual 3-to-1 multiplexer that selects the reference source for the ADC.

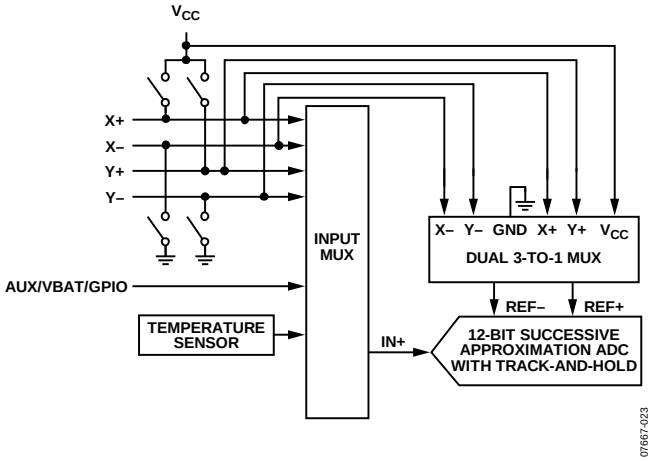


Figure 23. Analog Input Structure

The AD7879 can be set up to automatically convert either specific input channels or a sequence of channels. The results of the ADC conversions are stored in the results registers.

When measuring the ancillary analog inputs (AUX, TEMP, or VBAT), the ADC uses a V_{CC} reference and the measurement is referred to GND.

MEASURING TOUCH SCREEN INPUTS

When measuring the touch screen inputs, it is possible to measure using V_{CC} as a reference, or to use the touch screen excitation voltage as the reference and to perform a ratiometric, differential measurement. The differential method is the default method and is selected by clearing the SER/$\overline{\text{DFR}}$ bit (Bit 9 in Control Register 2) to 0. The single-ended method is selected by setting this bit to 1.

Single-Ended Method

Figure 24 illustrates the single-ended method for the Y position. For the X position, the excitation voltage is applied to X+ and X– and the voltage is measured at Y+.

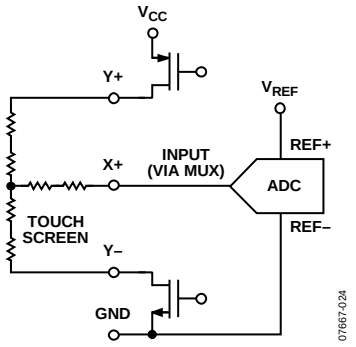


Figure 24. Single-Ended Conversion of Touch Screen Inputs

The voltage seen at the input to the ADC in Figure 24 is

$$V_{IN} = V_{CC} \times \frac{R_{Y-}}{R_{YTOTAL}} \quad (1)$$

The advantage of the single-ended method is that the touch screen excitation voltage is switched off once the signal is acquired. Because a screen can draw over 1 mA, this is a significant consideration for a battery-powered system.

The disadvantage of the single-ended method is that voltage drops across the switches can introduce errors. Touch screens can have a total end-to-end resistance ranging from 200 Ω to 900 Ω. By taking the lowest screen resistance of 200 Ω and a typical switch resistance of 14 Ω, the user can reduce the apparent excitation voltage to 200/228 × 100 = 87% of its actual value. In addition, the voltage drop across the low-side switch adds to the ADC input voltage. This introduces an offset into the input voltage; thus, it can never reach zero.

Ratiometric Method

The ratiometric method illustrated in Figure 25 shows the negative input of the ADC reference tied to Y– and the positive input connected to Y+. Thus, the screen excitation voltage provides the reference for the ADC. The input of the ADC is connected to X+ to determine the Y position.

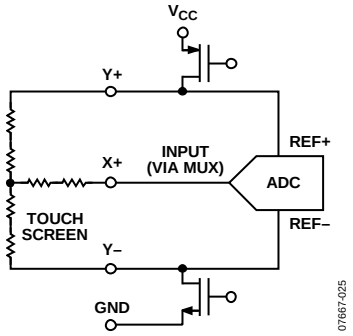


Figure 25. Ratiometric Conversion of Touch Screen Inputs

For greater accuracy, the ratiometric method has two significant advantages. One is that the reference to the ADC is provided from the actual voltage across the screen; therefore, any voltage dropped across the switches has no effect. The other advantage is that because the measurement is ratiometric, it does not matter if the voltage across the screen varies in the long term. However, it must not change after the signal has been acquired.

The disadvantage of the ratiometric method is that the screen must be powered up at all times because it provides the reference voltage for the ADC.

TOUCH-PRESSURE MEASUREMENT

The pressure applied to the touch screen by a pen or finger can also be measured with the AD7879, using some simple calculations. The contact resistance between the X and Y plates is measured providing a good indication of the size of the depressed area and, therefore, the applied pressure. The area of the spot that is touched is proportional to the size of the object touching it. The size of this resistance (R_{TOUCH}) can be calculated using two different methods.

First Method

The first method requires the user to know the total resistance of the X-plate tablet (R_X). Three touch screen conversions are required: measurement of the X position, $X_{POSITION}$ (Y+ input); measurement of the Y– input with the excitation voltage applied to Y+ and X– (Z1 measurement); and measurement of the X+ input with the excitation voltage applied to Y+ and X– (Z2 measurement).

These three measurements are illustrated in Figure 26.

The AD7879 has two special ADC channel settings that configure the X and Y switches for Z1 and Z2 measurement and store the results in the Z1 and Z2 results registers. The Z1 measurement is ADC Channel 101b, and the result is stored in register with Read Address 0x0A. The Z2 measurement is ADC Channel 100b, and the result is stored in register with Read Address 0x0B.

The touch resistance can then be calculated using the following equation:

$$R_{TOUCH} = (R_{XPLATE}) \times (X_{POSITION}/4096) \times [(Z2/Z1) - 1] \quad (2)$$

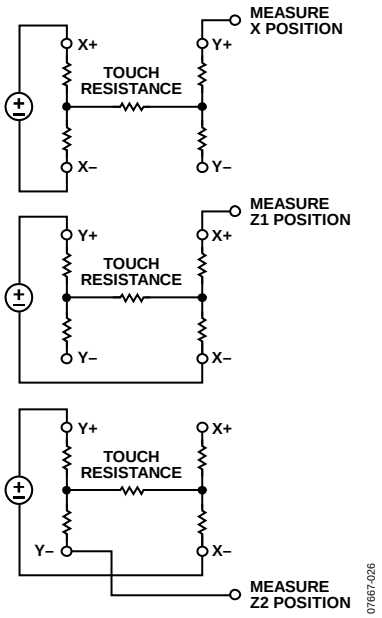


Figure 26. Three Measurements Required for Touch Pressure

Second Method

The second method requires the user to know the resistance of the X-plate and Y-plate tablets. Three touch screen conversions are required: a measurement of the X position ($X_{POSITION}$), the Y position ($Y_{POSITION}$), and the Z1 position.

The following equation also calculates the R_{TOUCH}:

$$R_{TOUCH} = R_{XPLATE} \times (X_{POSITION}/4096) \times [(4096/Z1) - 1] - R_{YPLATE} \times [1 - (Y_{POSITION}/4096)] \quad (3)$$

TEMPERATURE MEASUREMENT

A temperature measurement option called the single conversion method is available on the AD7879. The conversion method requires only a single measurement on ADC Channel 001b. The results are stored in the results registers with Address 0x0D (TEMP). The AD7879 does not provide an explicit output of the temperature reading; the system must perform some external calculations. This method is based on an on-chip diode measurement.

The acquisition time is fixed at 16 ms for temperature measurement.

Conversion Method

The conversion method makes use of the fact that the temperature coefficient of a silicon diode is approximately –2.1 mV/°C. However, this small change is superimposed on the diode forward voltage, which can have a wide tolerance. Therefore, it is necessary to calibrate by measuring the diode voltage at a known temperature to provide a baseline from which the change in forward voltage with temperature can be measured. This method provides a resolution of approximately 0.3°C and a predicted accuracy of ±2°C.

The temperature limit comparison is performed on the result in the TEMP results register, which is the measurement of the diode forward voltage. The values programmed into the high and low limits should be referenced to the calibrated diode forward voltage to make accurate limit comparisons.

Temperature Calculations

If an explicit temperature reading in degrees Celsius is required, calculate for the single measurement method by

1. Calculate the scale factor of the ADC in degrees per LSB

   Degrees per LSB = ADC LSB size/−2.1 mV = (V_{CC}/4096)/−2.1 mV
2. Save the ADC output (D_{CAL}) at the calibration temperature, T_{CAL}.
3. Take the ADC reading, D_{AMB}, at the temperature to be measured, T_{AMB}.
4. Calculate the difference in degrees between T_{CAL} and T_{AMB} by

   $\Delta T = (D_{AMB} - D_{CAL}) \times$ *degrees per LSB*
5. Add ΔT to T_{CAL}.

Example

Using V_{CC} = 2.5 V as reference,

Degrees per LSB = (2.5/4096)/−2.1 × 10^{-3} = −0.291

The ADC output is 983 decimal at 25°C, equivalent to a diode forward voltage of 0.6 V.

The ADC output at T_{AMB} is 880.

ΔT = (880 − 983) × −0.291 = 30°C

T_{AMB} = 25 + 30 = 55°C

MEDIAN AND AVERAGING FILTERS

As explained in the Touch Screen Principles section, touch screens are composed of two resistive layers, normally placed over an LCD screen. Because these layers are in close proximity to the LCD screen, noise can be coupled from the screen onto these resistive layers, causing errors in the touch screen positional measurements.

The AD7879 contains a filtering block to process the data and discard the spurious noise before sending the information to the host. The goal of this block is not just the suppression of noise; the on-chip filtering also remarkably reduces the host processing loading.

The processing function consists of two filters that are applied to the converted results: the median filter and the averaging filter.

The median filter suppresses the isolated out-of-range noise and sets the number of measurements to be taken. These measurements are arranged in a temporary array, where the first value is the smallest measurement and the last value is the largest measurement. Bit 6 and Bit 5 in Control Register 2 (M1, M0) set the window of the median filter, and therefore, the number of measurements taken.

Table 6. Median Filter Size

M1	M0	Function
0	0	Median filter does not operate
0	1	4 measurements
1	0	8 measurements
1	1	16 measurements

The averaging filter size determines the number of values to average. Bit 8 and Bit 7 in Control Register 2 (A1, A0) allow the average of 2, 4, 8, or 16 samples. Only the final averaged result is written into the results register.

Table 7. Averaging filter Size

A1	A0	Function
0	0	Average of 2 middle samples
0	1	Average of 4 middle samples
1	0	Average of 8 middle samples
1	1	Average of 16 samples

When both filter values are 00, only one measurement is transferred to the register map.

The number chosen with the M1 and M0 settings must be equal to or larger than the number chosen with the A1 and A0 settings. If both settings select the same number, the median filter is switched off.

Table 8. Median Averaging Filters (MAVF) Settings

	Function
M = A	Median filter does not operate; output is the average of A converted results
M < A	Not possible because the median filter size is always bigger than the averaging window size
M > A	Output is the average of the middle A values from the array of M measurements

Example

M1, M0 = 11, A1, A0 = 10; in this example the median filter has a window size of 16. This means that 16 measurements are taken and arranged in descending order in a temporary array.

The averaging window size in this case is 8. The output is an average of the middle 8 values of the 16 measurements taken with the median filter.

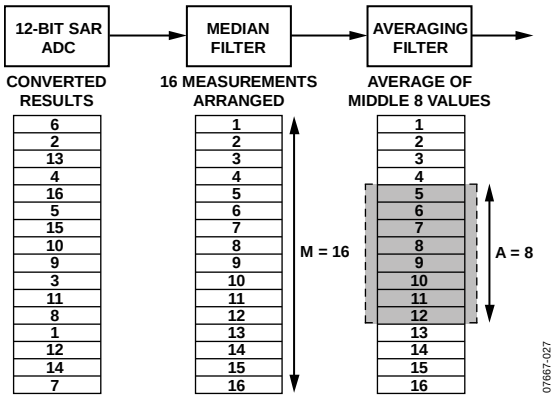


Figure 27. Median and Averaging Filter Example

AUX/VBAT/GPIO PIN

Pin 1A (AUX/VBAT/GPIO) on the AD7879 can be programmed as either an auxiliary input to the ADC, as a battery monitoring input, or as a general-purpose digital input/output. To select the auxiliary measurement, set the ADC channel address to 011. To select a battery measurement, set the ADC channel address to 010. To select the GPIO, set Bit 13 in Control Register 2 (Address 0x02) to 1.

AUXILIARY INPUT

The AD7879 has an auxiliary analog input, AUX. When selected, the signal on the AUX pin (AUX/VBAT/GPIO) is connected directly to the ADC input. This channel has a full-scale input range from 0 V to V_{CC}. The ADC channel addresses for AUX is 011, and the result is stored in Register 0x0C.

BATTERY INPUT

The AD7879 can monitor battery voltages from 0.5 V to 5 V when the BAT measurement is selected. Figure 28 shows a block diagram of a battery voltage monitored through the VBAT pin. The voltage to the V_{CC} pin (V_{CC}/REF) of the AD7879 is maintained at the desired supply voltage via the dc-to-dc regulator while the input to the regulator is monitored. This voltage on VBAT is divided down by 4 internally, so that a 5 V battery voltage is presented to the ADC as 1.25 V. To conserve power, the divider circuit is on only during the sampling of a voltage on VBAT. Note that the possible maximum input is 5 V.

The VBAT input is ADC Channel 010, and the result is stored in Register 0x0C.

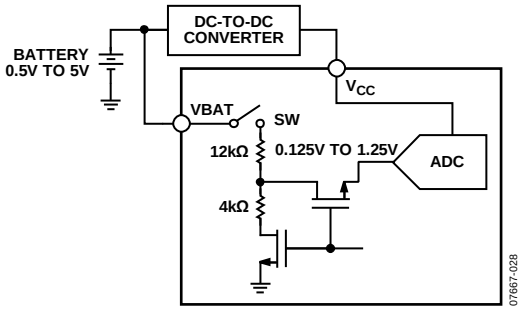


Figure 28. Block Diagram of Battery Measurement Circuit

The maximum battery voltage that the AD7879 can measure changes when a different reference voltage is used. The maximum voltage that is measurable is $V_{CC} \times 4$ because this voltage gives a full-scale output from the ADC. The battery voltage can be calculated using the following formula:

$$V_{BAT}\,(\text{V}) = [(\textit{Register Value}) \times V_{CC} \times 4]/4095$$

LIMIT COMPARISON

The AUX measurement and the battery measurement can be compared with high and low limits stored on-chip. An out-of-limit result generates an alarm output at the $\overline{\text{INT}}$ pin ($\overline{\text{PENIRQ}}/\overline{\text{INT}}/\overline{\text{DAV}}$) provided the $\overline{\text{INT}}$ function is enabled. The high limit for both channels is stored in Register 0x04, while the low limit is stored in Register 0x05.

After a measurement from either AUX or VBAT is taken, it is compared with the high and low limits. The out-of-limit comparison sets a status bit in Control Register 3. There are separate status bits for both the high and low limits to indicate which limit was exceeded. The interrupt sources can be masked by clearing the corresponding enable bit in this register.

GPIO

The AD7879 has one general-purpose logic input/output pin, GPIO (AUX/VBAT/GPIO). To enable the GPIO, set Bit 13 in Control Register 2 to 1. If this bit it 0, then the AUX/VBAT function is active on the pin. The other GPIO configuration bits have no effect, if the GPIO is not enabled.

The GPIO data bit is located in Bit 12 of the Control Register 2.

Direction (Bit 11, Control Register2, Address 0x02)

Bit 11 sets the direction of the GPIO pin (AUX/VBAT/GPIO). When GPIO DIR = 0, the pin is an output. Setting or clearing bits in the GPIO data bit (Register 0x02[12]) outputs a value on the GPIO pin.

When GPIO DIR = 1, the pin is an input. An input value on the GPIO pin sets or clears the GPIO data bit (Register 0x02[12]). GPIO data register bits are read-only when GPIO DIR = 1.

Polarity (Bit 10, Control Register 2, Address 0x02)

When GPIO POL = 0, the GPIO pin is active low. When GPIO POL = 1, the GPIO pin is active high. How this bit affects the GPIO operation also depends on the GPIO DIR bit.

If GPIO POL = 1 and GPIO DIR = 1, a 1 at the input pin sets the corresponding GPIO data register bit to 1. A 0 at the input pin clears the corresponding GPIO data bit to 0.

If GPIO POL = 1 and GPIO DIR = 0, a 1 in the GPIO data register bit puts a 1 on the corresponding GPIO output pin. A 0 in the GPIO data register bit puts a 0 on the GPIO output pin.

If GPIO POL = 0 and GPIO DIR = 1, a 1 at the input pin sets the corresponding GPIO data bit to 0. A 0 at the input pin clears the corresponding GPIO data bit to 1.

If GPIO POL = 0 and GPIO DIR = 0, a 1 in the GPIO data register bit puts a 0 on the corresponding GPIO output pin. A 0 in the GPIO data register bit puts a 1 on the GPIO output pin.

GPIO Interrupt Enable (Bit 12, Control Register 3, Address 0x03)

The GPIO pin can operate as an interrupt source to trigger the $\overline{\text{INT}}$ output. This is controlled by Bit 12 in Control Register 3.

If the GPIO ALERT interrupt enable = 1, the GPIO can trigger $\overline{\text{INT}}$. If this bit = 0, the GPIO cannot trigger $\overline{\text{INT}}$.

$\overline{\text{INT}}$ is asserted if the GPIO data register bit is set when the GPIO is configured as an input, provided that $\overline{\text{INT}}$ is enabled. $\overline{\text{INT}}$ is triggered only when the GPIO is configured as an input, that is, when GPIO DIR = 1.

$\overline{\text{INT}}$ is clear only when the GPIO signal or the GPIO enable changes.

REGISTER MAP

Table 9. Register Table

Address[1]	Name	Description	Default Value	Type
0x00	Unused	Unused	0x0000	R/$\overline{W}$
0x01	Control Register 1	$\overline{PENIRQ}$ enable, channel selection for manual selection, ADC mode, acquisition time, and conversion timer	0x0000	R/$\overline{W}$
0x02	Control Register 2	ADC power management, GPIO control, pen interrupt, averaging, median filter, software reset, and FCD	0x4040	R/$\overline{W}$
0x03	Control Register 3	Status of high/low limit comparisons for TEMP, AUX/VBAT and enable bits to allow them to become interrupts; channel selection for slave/master mode	0x0000	R/$\overline{W}$
0x04	AUX/VBAT high limit	AUX/VBAT high limit for comparison	0x0000	R/$\overline{W}$
0x05	AUX/VBAT low limit	AUX/VBAT low limit for comparison	0x0000	R/$\overline{W}$
0x06	TEMP high limit	TEMP high limit for comparison	0x0000	R/$\overline{W}$
0x07	TEMP low limit	TEMP low limit for comparison	0x0000	R/$\overline{W}$
0x08	X+	X+ measurement for Y position	0x0000	R
0x09	Y+	Y+ measurement for X position	0x0000	R
0x0A	X+ (Z1)	X+ measurement for touch pressure calculation (Z1)	0x0000	R
0x0B	Y− (Z2)	Y− measurement for touch pressure calculation (Z2)	0x0000	R
0x0C	AUX/VBAT	AUX/VBAT measurement	0x0000	R
0x0D	TEMP	Temperature conversion Measurement	0x0000	R
0x0E	Revision and device ID	Revision and device ID	0x0379 (AD7879-1) 0x037A (AD7879)	R

[1] Do not write to addresses outside the register map.

DETAILED REGISTER DESCRIPTIONS

All addresses and default values are expressed in hexadecimal.

Table 10. Control Register 1

Address	Name	Data Bit	Description	Default Value
0x01	Disable $\overline{\text{PENIRQ}}$	15	Pen interrupt enable. 0 = $\overline{\text{PENIRQ}}$ pin is enabled. 1 = $\overline{\text{PENIRQ}}$ is disabled and $\overline{\text{INT}}$ enabled.	0x0000
	CHNL ADD[2:0]	14:12	ADC Channel address for manual conversion (mode 01). 111 = X+ input (Y position). 110 = Y+ input (X position). 101 = X+ (Z1) input for touch-pressure calculation. 100 = Y− (Z2) input (used for touch-pressure measurement). 011 = AUX input[1]. 010 = VBAT input[1]. 001 = temperature measurement. 000 = not applicable.	
	ADC MODE[1:0]	11:10	ADC mode. 00 = no conversion. 01 = single conversion[2]. 10 = conversion sequence (slave mode)[2]. 11 = conversion sequence (master mode).	
	ACQ[1:0]	9:8	ADC acquisition time. 00 = 4 clock periods (2 µs). 01 = 8 clock periods (4 µs). 10 = 16 clock periods (8 µs). 11 = 32 clock periods (16 µs). Note that the acquisition time does not apply to the temperature sensor channels; the temperature channel has a constant settling time of 16 µs.	
	TMR[7:0]	7:0	Conversion interval timer. Starts at 550 µs and continues to 9.440 ms in steps of 35 µs. Note that in slave mode, the conversion interval timer starts to count as soon as the conversion sequence is finished; in master mode, it starts to count again only if the screen remains touched. If the screen is released, the timer stops counting and, on the next screen touch, a conversion starts immediately.	

[1] If GPIO is enabled, AUX and VBAT are both ignored. If AUX and VBAT are both selected, and GPIO is disabled, AUX is ignored, and VBAT is measured.
[2] Note that these settings clear to 00 at the end of the conversion sequence if the conversion interval timer bits in Control Register 1 (0x01) Bits 7:0 = 0x00h at the end of the conversion sequence.

Table 11. Control Register 2

Address	Name	Data Bit	Description	Default Value
0x02	PM[1:0]	15:14	ADC power management. 00 = full shutdown, the ADC, oscillator, BIAS, and temperature sensor are all powered down. 01 = analog blocks to be powered down depend on the ADC mode. If ADC mode is master mode; the ADC, oscillator, BIAS, and temperature sensor are powered down and must wake up when the user touches the screen. If ADC mode is slave mode, the ADC and temperature sensor are powered down while not being used. They wake up automatically when required. The oscillator and BIAS are powered up because they are needed to measure time. This also applies to the single conversion mode. 10 = ADC, BIAS, the oscillator is powered up continuously, irrespective of ADC mode. 11 = as 01.	0x4040
	GPIO EN	13	GPIO enable. 0 = AUX/VBAT channel active. 1 = GPIO enabled on AUX/VBAT/GPIO.	
	GPIO DAT	12	GPIO data bit.	
	GPIO DIR	11	GPIO direction. 0 = output. 1 = input.	
	GPIO POL	10	GPIO polarity. 0 = the GPIO pin is active low. 1 = the GPIO pin is active high.	
	SER/$\overline{\text{DFR}}$	9	SER/$\overline{\text{DFR}}$. Selects normal (single-ended) or conversion. 0 = ratiometric (differential). 1 = normal (single-ended).	
	A[1:0]	8:7	ADC averaging. 00 = 2 middle values averaged (1 measurement when median filter does not operate). 01 = 4 middle values averaged. 10 = 8 middle values averaged. 11 = 16 values averaged.	
	M[1:0]	6:5	Median filter size. 00 = median filter does not operate. 01 = 4 measurements. 10 = 8 measurements. 11 = 16 measurements.	
	SW/RST	4	Software reset; digital part is reset when this bit is set.	
	FCD[3:0]	3:0	ADC first conversion delay[1]. Starts at 128 µs and goes all the way to 4.096 ms in steps of 128 µs.	

[1] This delay occurs before conversion of the X and Y coordinate channels (including Z1 and Z2) to allow for screen settling and before the first conversion to allow the ADC to power up.

Table 12. Control Register 3

Address	Name	Data Bit	Description	Default Value
0x03	TEMP MASK	15	TEMP mask bit 0 = temperature measurement is allowed to cause interrupt 1 = temperature measurement is not allowed to cause interrupt	0x0000
	AUX/VBAT MASK	14	AUX/VBAT mask bit 0 = AUX/VBAT measurement is allowed to cause interrupt 1 = AUX/VBAT measurement is not allowed to cause interrupt	
	INT MODE	13	$\overline{DAV}/\overline{INT}$ mode select 0 = enable $\overline{DAV}$ mode 1 = enable $\overline{INT}$ mode Note that this bit overrides any mask bits associated with individual channels	
	GPIO ALERT	12	GPIO interrupt enable 0 = GPIO can cause an alert on the $\overline{INT}$ output 1 = mask GPIO from causing an alert on the $\overline{INT}$ output	
	AUX/VBAT LOW	11	1 = AUX/VBAT below low limit	
	AUX/VBAT HIGH	10	1 = AUX/VBAT above high limit	
	TEMP LOW	9	1 = TEMP below low limit	
	TEMP HIGH	8	1 = TEMP above high limit	
	X+	7	1 = include measurement of Y position (X+ input)	
	Y+	6	1 = include measurement of X position (Y+ input)	
	Z1	5	1 = include Z1 touch pressure measurement (X+ input)	
	Z2	4	1 = include measurement of Z2 touch pressure measurement (Y– input)	
	AUX	3	1 = include measurement of AUX channel[1]	
	VBAT	2	1 = include measurement of battery monitor (VBAT)[1]	
	TEMP	1	1 = include temperature measurement	
	Not used	0	Unused	

[1] If GPIO is enabled, AUX and VBAT are both ignored. If AUX and VBAT are both selected, and GPIO is disabled, AUX is ignored, and VBAT is measured.

Table 13. Limit Registers

Address	Data Bit	Description	Default Value
0x04	15:0	User-programmable AUX/VBAT high limit register	0x0000
0x05	15:0	User-programmable AUX/VBAT low limit register	0x0000
0x06	15:0	User-programmable TEMP high limit register	0x0000
0x07	15:0	User-programmable TEMP low limit register	0x0000

Table 14. Measurement Result Registers

Address	Data Bit	Description	Default Value
0x08	15:0	Measured X+ input with Y excitation (Y position)	0x0000
0x09	15:0	Measured Y+ input with X excitation (X position)	0x0000
0x0A	15:0	Measured X+ input with X− and Y+ excitation (touch-pressure calculation Z1)	0x0000
0x0B	15:0	Measured Y− input with X− and Y+ excitation (touch-pressure calculation Z2)	0x0000
0x0C	15:0	AUX/VBAT voltage measurement	0x0000
0x0D	15:0	Temperature conversion measurement	0x0000

Table 15. Revision/Device ID Register

Address	Data Bit	Description	Default Value
0x0E	15:12	Unused	0x0379 (AD7879-1) 0x037A (AD7879)
	11:8	Revision and device ID bits	
	7:0	Device ID	

CONTROL REGISTERS

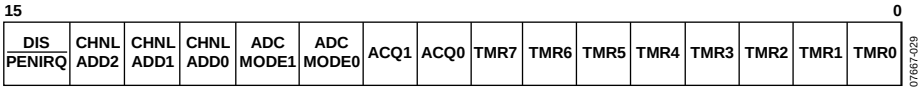


Figure 29. Control Register 1

CONTROL REGISTER 1

Control Register 1 (Address 0x01) contains the ADC channel address and the ADC mode bits. It sets the acquisition time and the timer. It also contains a bit to disable the pen interrupt. Control Register 1 should always be the last register programmed prior to starting conversions. Its power-on default value is 0x0000. To change any parameter after conversion has begun, the part should first be put into Mode 00. Make the changes; then reprogram Control Register 1, ensuring that it is always the last register programmed before conversions begin.

Timer (Control Register 1, Bits[7:0])

The TMR bits in Control Register 1 enable the ADC to repeatedly perform a conversion or to perform a conversion sequence only once or at intervals of 35 µs from 550 µs up to 9.440 ms. In slave mode, the timer starts as soon as the conversion sequence is finished. In master mode, the timer starts at the end of a conversion sequence only if the screen remains touched. If the touch is released at any stage, then the timer stops. The next time the screen is touched, a conversion sequence immediately begins.

Table 16. Control Register 1 Timer Selection

TMR	Function
00000000	Convert one time only (default)
00000001	Every 550 µs
00000010	Every 585 µs
00000011	Every 620 µs
…	…
11111101	Every 9.370 ms
11111110	Every 9.405 ms
11111111	Every 9.440 ms

Acquisition Time (Control Register 1, Bits[9:8])

The ACQ bits in Control Register 1 allow the selection of acquisition times for the ADC of 2 µs (default), 4 µs, 8 µs, or 16 µs. The user can program the ADC with an acquisition time suitable for the type of signal being sampled. For example, signals with large RC time constants can require longer acquisition times.

Table 17. Acquisition Time Selection

ACQ1	ACQ0	Function
0	0	4 clock periods (2 µs)
0	1	8 clock periods (4 µs)
1	0	16 clock periods (8 µs)
1	1	32 clock periods (16 µs)

ADC Mode (Control Register 1, Bits[11:10])

The mode bits select the operating mode of the ADC. The AD7879 has three operating modes. These are selected by writing to the mode bits in Control Register 1. If the mode bits are 00, no conversion is performed.

Table 18. Control Register 1 Mode Selection

ADC MODE1	ADC MODE0	Function
0	0	Do not convert (default)
0	1	Single-channel conversion; the AD7879 is in slave mode
1	0	Sequence 0; the AD7879 is in slave mode
1	1	Sequence 1; the AD7879 is in master mode

If the mode bits are 01, a single conversion is performed on the channel selected by writing to the channel bits of Control Register 1 (Bit 12 to Bit 14). At the end of the conversion, if the TMR bits in Control Register 1 are set to 00000000, the mode bits revert to 00 and the ADC returns to no convert mode until a new conversion is initiated by the host. Setting the TMR bits to a value other than 00000000 causes the conversion to be repeated.

The AD7879 can also be programmed to automatically convert a sequence of selected channels. The two modes for this type of conversion are slave mode and master mode.

For slave mode operation, the channels to be digitized are selected by setting the corresponding bits in Control Register 3. Conversion is initiated by writing 10b to the mode bits of Control Register 1. The ADC then digitizes the selected channels and stores the results in the corresponding results registers. At the end of the conversion, if the TMR bits in Control Register 1 are set to 00000000, the mode bits revert to 00 and the ADC returns to no convert mode until a new conversion is initiated by the host. Setting the TMR bits to a code other than 00000000 causes the conversion sequence to be repeated.

For master mode operation, the channels to be digitized are written to the Control Register 3. Master mode is then selected by writing 11 to the mode bits in Control Register 1. In this mode, the wake-up on touch feature is active; therefore, conversion does not immediately begin. The AD7879 waits until the screen is touched before beginning the sequence of conversions. The ADC then digitizes the selected channels; and the results are written to the result registers. The AD7879 waits for the screen to be touched again, or for a timer event if the screen remains touched, before beginning another sequence of conversions.

ADC Channel (Control Register 1 Bits[14:12])

The ADC channel is selected by Bits[14:12] of Control Register 1 (CHNL ADD2 to CHNL ADD0). A complete list of channel addresses is given in Table 19.

For Mode 0 (single-channel) conversion, the channel is selected by writing the appropriate CHNL ADD2 to CHNL ADD0 code to Control Register 1.

For sequential channel conversion, channels to be converted are selected by setting bits corresponding to the channel number in the Control Register 3 for slave and master mode sequencing.

For both single-channel and sequential conversion, a normal conversion (single-ended) is selected by clearing the SER/$\overline{\text{DFR}}$ bit in Control Register 2 (Bit 9). Ratiometric (differential) conversion is selected by setting the SER/$\overline{\text{DFR}}$ bit.

$\overline{\text{PENIRQ}}$ Enable (Control Register 1, Bit 15)

The AD7879 has a dual function output that performs as $\overline{\text{PENIRQ}}$ or $\overline{\text{INT}}$ depending on the pen interrupt enable bit (Bit 15 of Control Register 1). When this bit is set to 0, the pin is working as a pen interrupt and it goes low whenever the screen is touched. When the pen interrupt enable bit is set to 1, the pin interrupt request is disabled and the pin functions as $\overline{\text{INT}}$.

Table 19. Codes for Selecting Input Channel and Normal or Ratiometric Conversion

Channel	SER/$\overline{\text{DFR}}$	CHNL ADD[2:0]	Analog Input	X Switches	Y Switches	+REF	−REF
0	0	1 1 1	X+ (Y position)	Off	On	Y+	Y−
1	0	1 1 0	Y+ (X position)	On	Off	X+	X−
2	0	1 0 1	X+ (Z1 touch pressure)	X+ off, X− on	Y+ on, Y− off	Y+	X−
3	0	1 0 0	Y− (Z2 touch pressure)	X+ off, X− on	Y+ on, Y− off	Y+	X−
4	0	0 1 1	AUX	Off	Off	V_{CC}	GND
5	0	0 1 0	VBAT	Off	Off	V_{CC}	GND
6	0	0 0 1	TEMP	Off	Off	V_{CC}	GND
	0	0 0 0	Invalid address				
7	1	1 1 1	X+ (Y position)	Off	On	V_{CC}	GND
8	1	1 1 0	Y+ (X position)	On	Off	V_{CC}	GND
9	1	1 0 1	X+ (Z1 touch pressure)	Off	Off	V_{CC}	GND
12	1	1 0 0	Y− (Z2 touch pressure)	Off	Off	V_{CC}	GND
13	1	0 1 1	AUX	Off	Off	V_{CC}	GND
14	1	0 1 0	VBAT	Off	Off	V_{CC}	GND
15	1	0 0 1	TEMP	Off	Off	V_{CC}	GND
	1	0 0 0	Invalid address				

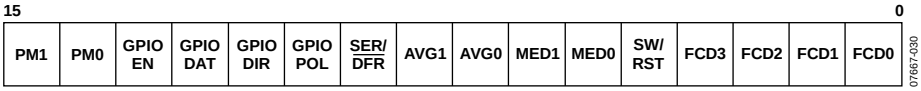


Figure 30. Control Register 2

CONTROL REGISTER 2

Control Register 2 (Address 0x02) contains the power management bits, the GPIO settings, the SER/$\overline{\text{DFR}}$ bit (to choose single or differential methods of touch screen measurement), the averaging and median filter settings, a bit that allows resetting the part, and the first conversion delay bits. Its power-on default value is 0x4040. See the Detailed Register Descriptions section for more information on the control registers.

First Conversion Delay (Control Register 2, Bits[3:0])

The first conversion delay (FCD) bits in Control Register 2 program a delay from 128 µs (default) up to 4.096 ms before the first conversion to allow the ADC time to power up. This delay also occurs before conversion of the X and Y coordinate channels to allow extra time for screen settling, and after the last conversion in a sequence to precharge $\overline{\text{PENIRQ}}$.

Table 20. First Conversion Delay Selection

FCD	Function
0000	128 µs
0001	256 µs
0010	384 µs
0011	512 µs
0100	640 µs
0101	768 µs
0110	896 µs
0111	1.024 ms
1000	1.152 ms
1001	1.280 ms
1010	1.536 ms
1011	1.792 ms
1100	2.048 ms
1101	2.560 ms
1110	3.584 ms
1111	4.096 ms

Power Management (Control Register 2, Bits[15:14])

The power management (PM) bits in Control Register 2 allow the power management features of the ADC to be programmed. If the PM bits are 00, the ADC is permanently powered down. This overrides any setting of the mode bits in Control Register 1. If the PM bits are 01, both the ADC and the reference power down when the ADC is not converting. If the PM bits are 10 or 11, the analog blocks to be powered down depend on the ADC mode settings. Power management overrides the ADC modes.

Table 21. Power Management Selection

PM1	PM0	Function
0	0	Full shutdown; ADC, oscillator, BIAS, and temperature sensor are all turned off. The only way of coming out of this mode is to write to the part over the serial interface and change the PM bits. This setting overrides any other setting on the part, including the ADC mode bits.
0	1	The analog blocks to be powered down depend on the ADC mode settings. If the ADC mode is set to master mode, the ADC, BIAS, temperature sensor, and oscillator are powered down and must wake up when the user touches the screen. If the ADC mode is set to slave mode, the ADC and the TEMP sensor are powered down while not being used. They wake up automatically when required. The oscillator and BIAS are powered up because they are needed to measure time. This also applies to the single-conversion mode.
1	0	ADC, BIAS, and the oscillator are powered up continuously irrespective of ADC mode.
1	1	As 01.

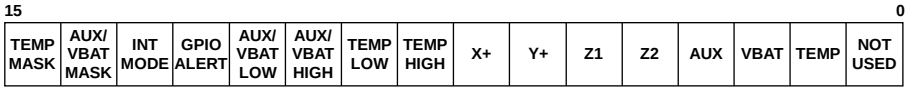


Figure 31. Control Register 3

CONTROL REGISTER 3

Control Register 3 (Address 0x03) includes the interrupt register (Bits[15:8]) and Control Register 3 (Bits[7:0]).

Sequencer

The sequencer bits control which channels are converted during a conversion sequence in both slave and master mode.

To include a measurement in a sequence, the relevant bit must be set in the sequence. Setting Bit 7 includes a measurement on the X+ channel (Y position). Setting Bit 6 includes a measurement on the Y+ channel (X position), and so on.

Figure 32 illustrates the correspondence between the bits in Control Register 3 and the various measurements. Bit 0 is not used.

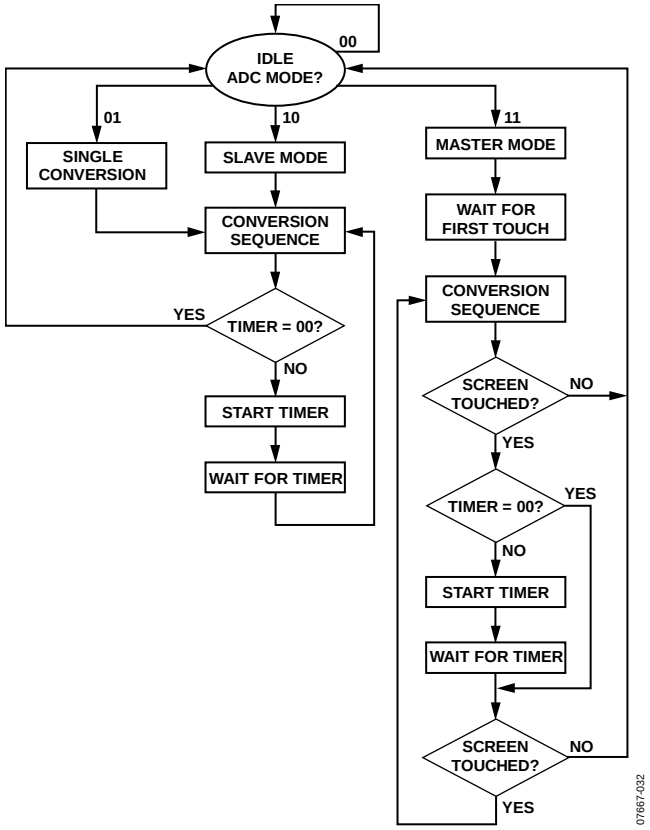


Figure 32. Conversion Modes

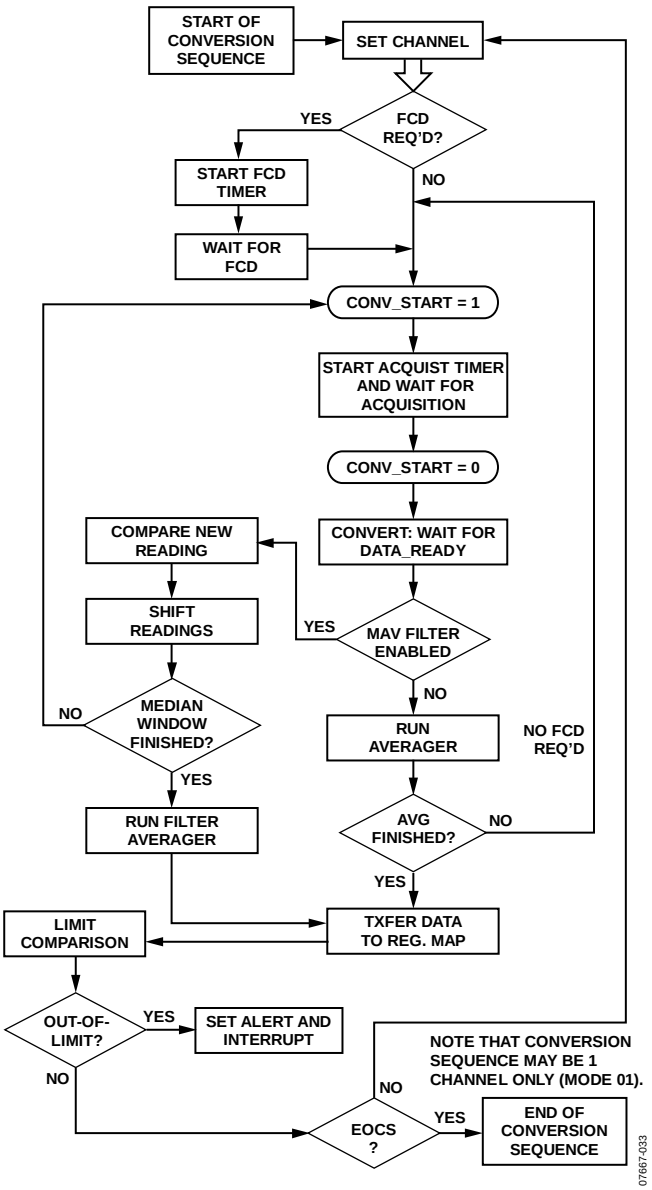


Figure 33. Conversion Sequence

INTERRUPTS

The AD7879 has a dual function interrupt output, $\overline{\text{INT}}$, as well as a pen down interrupt, $\overline{\text{PENIRQ}}$. The $\overline{\text{INT}}$ output can be configured as a data available interrupt, as an out of limit interrupt, or as a GPIO interrupt.

$\overline{\text{INT}}$—Data Available

The behavior of the interrupt output is controlled by Bit 13 in Control Register 3. In default mode, $\overline{\text{INT}}$ operates as a data available interrupt (Bit 13 = 0). When the AD7879 has finished a conversion or a conversion sequence, the interrupt asserts to let the host know that new ADC data is available in the result registers.

While the ADC is idle or is converting, $\overline{\text{INT}}$ is high. When the ADC has finished converting and new data has been written to the results registers, $\overline{\text{INT}}$ goes low. Reading the result registers resets $\overline{\text{INT}}$ to a high condition. $\overline{\text{INT}}$ is also reset if a new conversion is started by the AD7879 because the timer expired. The host should read the results registers only when $\overline{\text{INT}}$ is low. To ensure correct operation of the $\overline{\text{DAV}}$ mode when using the SPI interface it is necessary to write 0x0000 to Register 0x81 after a set of register reads. This clears the internal data read signal.

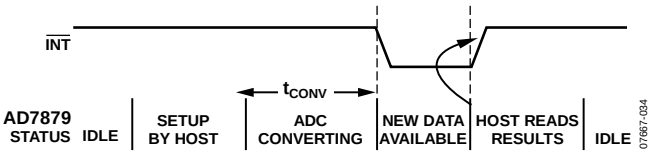


Figure 34. Operation of $\overline{\text{INT}}$ Output

When the on-board timer is programmed to perform automatic conversions, limited time is available to the host to read the results registers before another sequence of conversions begins. The $\overline{\text{INT}}$ signal is reset high when the timer expires, and the host should not access the results registers while $\overline{\text{INT}}$ is high.

$\overline{\text{INT}}$—Out of Limits

The $\overline{\text{INT}}$ pin operates as an alarm or interrupt output when Bit 13 in Register 0x03 is set to 1. The output goes low if any one of the interrupt sources is asserted. The results of high and low limit comparisons on the AUX, VBAT, and TEMP channels are interrupt sources. An out-of-limit comparison sets a status bit in the interrupt register. There are separate status bits for both the high and low limits on each channel to indicate which limit was exceeded. The interrupt sources can be masked by clearing the corresponding enable bit in this register. There is one enable bit per channel.

$\overline{\text{PENIRQ}}$— Pen Interrupt

The pen interrupt request output ($\overline{\text{PENIRQ}}$) goes low whenever the screen is touched and the $\overline{\text{PENIRQ}}$ enable bit is set to 0 (Control Register 1, Bit 15). When $\overline{\text{PENIRQ}}$ enable is set to 1, the pen interrupt request output is disabled.

The pen interrupt equivalent output circuitry is outlined in Figure 35. This is a digital logic output with an internal 50 kΩ pull-up resistor, which means it does not need an external pull-up. The $\overline{\text{PENIRQ}}$ output idles high, and the $\overline{\text{PENIRQ}}$ circuitry is always enabled in master mode (ADC mode = 11), except during conversions.

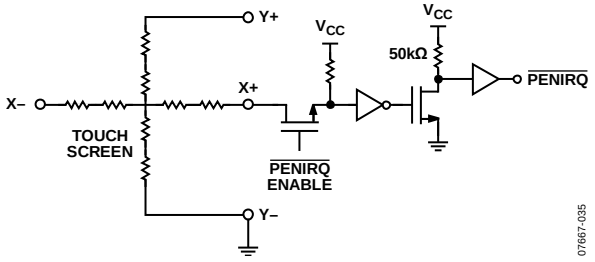


Figure 35. $\overline{\text{PENIRQ}}$ Output Equivalent Circuit

When the screen is touched, $\overline{\text{PENIRQ}}$ goes low. This generates an interrupt request to the host. When the screen touch ends, and if the ADC is idle, $\overline{\text{PENIRQ}}$ immediately goes high. If the ADC is converting, $\overline{\text{PENIRQ}}$ goes high when the ADC becomes idle. The $\overline{\text{PENIRQ}}$ operation for these two conditions is shown in Figure 36.

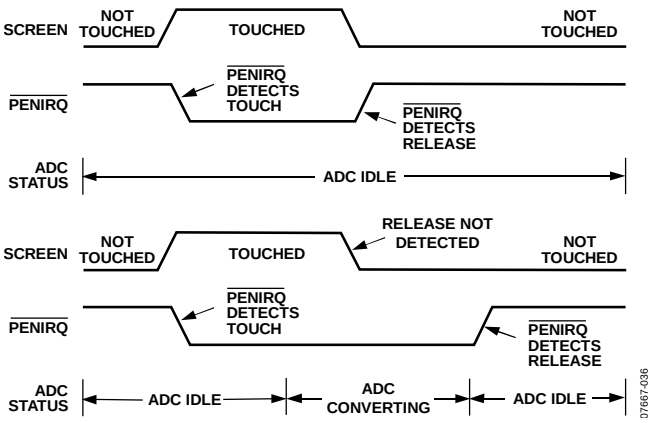


Figure 36. $\overline{\text{PENIRQ}}$ Operation for ADC Idle and ADC Converting

SYNCHRONIZING THE AD7879 TO THE HOST CPU

The two recommended methods for synchronizing the AD7879 to its host CPU are slave mode (in which the mode bits can be either 01b or 10b) and master mode (in which the mode bits are 11b).

In master mode (ADC mode bits = 11b), $\overline{\text{PENIRQ}}$ mode can be used as an interrupt to the host. When $\overline{\text{PENIRQ}}$ goes low to indicate that the screen has been touched, the host is awakened. The host can then program the AD7879 to convert in any mode and read the results after the conversions are completed.

In master mode, $\overline{\text{INT}}$ or $\overline{\text{DAV}}$ can also be used as an interrupt to the host. The host should first define a conversion sequence in Control Register 3, initialize the AD7879 in Mode 11b and enable $\overline{\text{INT}}$ or $\overline{\text{DAV}}$ using Bit 15 in Control Register 1 and Bit 13 in Control Register 3. The host can then enter sleep mode to conserve power. The wake-up on-touch feature of the AD7879 is active in this mode; therefore, when the screen is touched, the programmed sequence of conversions automatically begins. When the $\overline{\text{INT}}$ or $\overline{\text{DAV}}$signal asserts, the host reads the new data available in the AD7879 results registers and returns to sleep mode. This method can significantly reduce the load on the host.

Figure 37 shows how the $\overline{\text{PENIRQ}}$ circuit is enabled. The wake-up on-touch circuit and the $\overline{\text{PENIRQ}}$ circuit are enabled only in master mode (ADC mode = 11). In slave mode, the $\overline{\text{PENIRQ}}$/$\overline{\text{DAV}}$/$\overline{\text{INT}}$ pin can output only $\overline{\text{DAV}}$ or $\overline{\text{INT}}$ signals.

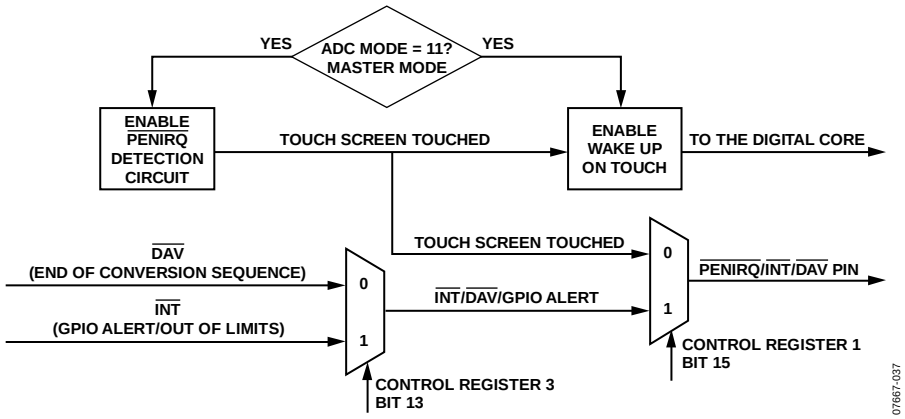


Figure 37. Master Mode Operation

SERIAL INTERFACE

The AD7879 is available with an serial peripheral interface (SPI). The AD7879-1 is available with an I²C®-compatible interface. Both parts are the same, with the exception of the serial interface. It is recommended not to write to addresses outside the register map.

SPI INTERFACE

The AD7879 has a 4-wire SPI. The SPI has a data input pin (DIN) for inputting data to the device, a data output pin (DOUT) for reading data back from the device, and a data clock pin (SCL) for clocking data into and out of the device. A chip select pin ($\overline{CS}$) enables or disables the serial interface. $\overline{CS}$ is required for correct operation of the SPI interface. Data is clocked out of the AD7879 on the negative edge of SCL and data is clocked into the device on the positive edge of SCL.

SPI Command Word

All data transactions on the SPI bus begin with the master taking $\overline{CS}$ from high to low and sending out the command word. This indicates to the AD7879 whether the transaction is a read or a write, and gives the address of the register from which to begin the data transfer. The bit map in Table 22 shows the SPI command word.

Table 22.

MSB						LSB
15	**14**	**13**	**12**	**11**	**10**	**9:0**
1	1	1	0	0	R/$\overline{W}$	Register address

Bits[15:11] of the command word must be set to 11100 to successfully begin a bus transaction.

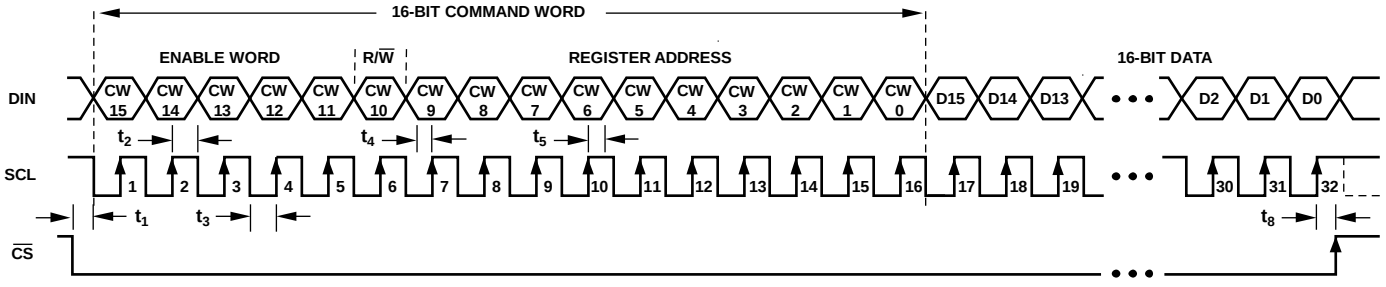
Bit 10 is the read/write bit; 1 indicates a read, and 0 indicates a write.

Bits[9:0] contain the target register address. When reading or writing to more than one register, this address indicates the address of the first register to be written to or read from.

Writing Data

Data is written to the AD7879 in 16-bit words. The first word written to the device is the command word, with the read/write bit set to 0. The master then supplies the 16-bit input data-word on the DIN line. The AD7879 clocks the data into the register addressed in the command word. If there is more than one word of data to be clocked in, the AD7879 automatically increments the address pointer and clocks the next data-word into the following register.

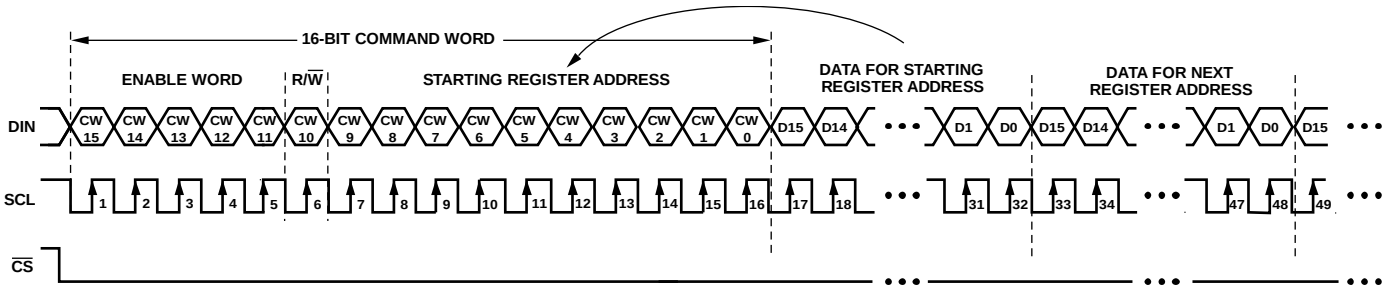
The AD7879 continues to clock in data on the SDA line until either the master finishes the write transition by pulling $\overline{CS}$ high, or until the address pointer reaches its maximum value. The AD7879 address pointer does not wrap around. When it reaches its maximum value, any data provided by the master on the DIN line is ignored by the AD7879.



NOTES
1. DATA BITS ARE LATCHED ON SCL RISING EDGES. SCL CAN IDLE HIGH OR LOW BETWEEN WRITE OPERATIONS.
2. ALL 32 BITS MUST BE WRITTEN: 16 BITS FOR CONTROL WORD AND 16 BITS FOR DATA.
3. 16-BIT COMMAND WORD SETTINGS FOR SERIAL WRITE OPERATION:
   CW[15:11] = 11100 (ENABLE WORD)
   CW[10] = 0 (R/$\overline{W}$)
   CW[9:0] = [AD9, AD8, AD7, AD6, AD5, AD4, AD3, AD2, AD1, AD0] (10-BIT MSB JUSTIFIED REGISTER ADDRESS)

07667-038

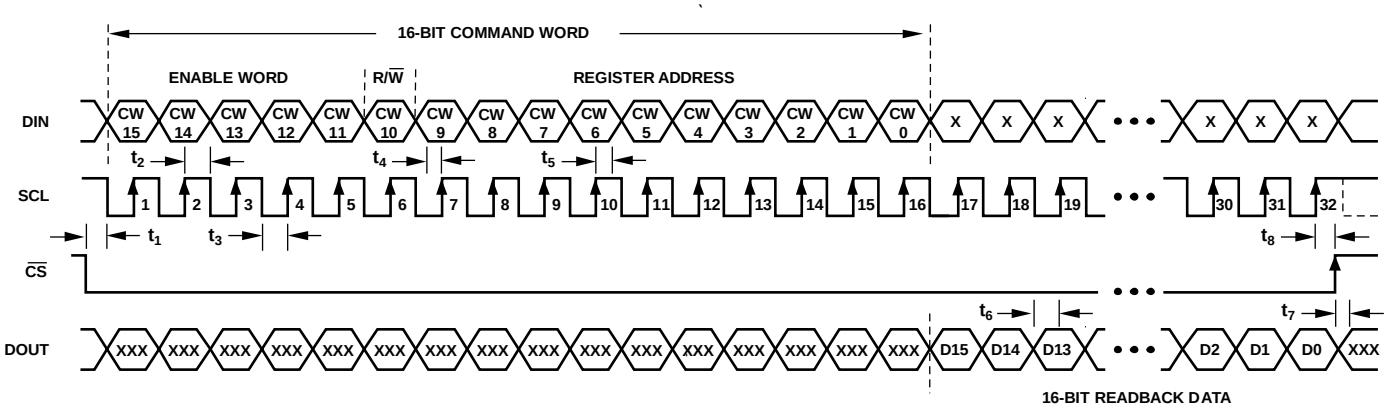
Figure 38. Single Register Write, SPI Timing



NOTES
1. MULTIPLE SEQUENTIAL REGISTERS CAN BE LOADED CONTINUOUSLY.
2. THE FIRST (LOWEST ADDRESS) REGISTER ADDRESS IS WRITTEN, FOLLOWED BY MULTIPLE 16-BIT DATA-WORDS.
3. THE ADDRESS AUTOMATICALLY INCREMENTS WITH EACH 16-BIT DATA-WORD (ALL 16 BITS MUST BE WRITTEN).
4. $\overline{CS}$ IS HELD LOW UNTIL THE LAST DESIRED REGISTER HAS BEEN LOADED.
5. 16-BIT COMMAND WORD SETTINGS FOR SEQUENTIAL WRITE OPERATION:
   CW[15:11] = 11100 (ENABLE WORD)
   CW[10] = 0 (R/$\overline{W}$)
   CW[9:0] = [AD9, AD8, AD7, AD6, AD5, AD4, AD3, AD2, AD1, AD0] (STARTING MSB JUSTIFIED REGISTER ADDRESS)

07667-039

Figure 39. Sequential Register Write SPI Timing



NOTES
1. DATA BITS ARE LATCHED ON SCL RISING EDGES. SCL CAN IDLE HIGH OR LOW BETWEEN WRITE OPERATIONS.
2. THE 16-BIT CONTROL WORD MUST BE WRITTEN ON SDI: 5 BITS FOR ENABLE WORD, 1 BIT FOR R/$\overline{W}$, AND 10 BITS FOR REGISTER ADDRESS.
3. THE REGISTER DATA IS READ BACK ON THE DOUT PIN.
4. X DENOTES DON'T CARE.
5. XXX DENOTES HIGH IMPEDANCE THREE-STATE OUTPUT.
6. $\overline{CS}$ IS HELD LOW UNTIL ALL REGISTER BITS HAVE BEEN READ BACK.
7. 16-BIT COMMAND WORD SETTINGS FOR SINGLE READBACK OPERATION:
   CW[15:11] = 11100 (ENABLE WORD)
   CW[10] = 1 (R/$\overline{W}$)
   CW[9:0] = [AD9, AD8, AD7, AD6, AD5, AD4, AD3, AD2, AD1, AD0] (10-BIT MSB JUSTIFIED REGISTER ADDRESS)

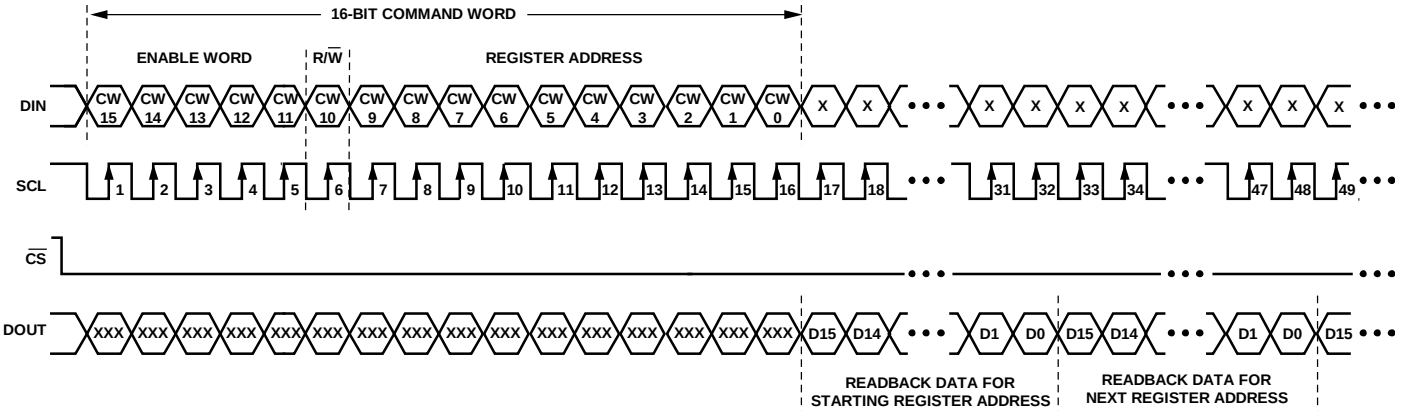
07667-040

Figure 40. Single Register Read Back SPI Timing

Reading Data

A read transaction begins when the master writes the command word to the AD7879 with the read/write bit set to 1. The master then supplies 16 clock pulses per data-word to be read, and the AD7879 clocks out data from the addressed register on the SDA line. The first data-word is clocked out on the first falling edge of SCL following the command word, as shown in Figure 40.

The AD7879 continues to clock out data on the DOUT line provided the master continues to supply the clock signal on SCL. The read transaction finishes when the master takes $\overline{CS}$ high. If the AD7879 address pointer reaches its maximum value, the AD7879 repeatedly clocks out data from the addressed register. The address pointer does not wrap around.



NOTES
1. MULTIPLE REGISTERS CAN BE READ BACK CONTINUOUSLY.
2. THE 16-BIT CONTROL WORD MUST BE WRITTEN ON SDA: 5 BITS FOR ENABLE WORD, 1 BIT FOR R/W, AND 10 BITS FOR REGISTER ADDRESS.
3. THE ADDRESS AUTOMATICALLY INCREMENTS WITH EACH 16-BIT DATA-WORD BEING READ BACK ON THE SDA PIN.
4. CS IS HELD LOW UNTIL ALL REGISTER BITS HAVE BEEN READ BACK.
5. X DENOTES DON'T CARE.
6. XXX DENOTES HIGH IMPEDANCE THREE-STATE OUTPUT.
7. 16-BIT COMMAND WORD SETTINGS FOR SEQUENTIAL READBACK OPERATION:
   CW[15:11] = 11100 (ENABLE WORD)
   CW[10] = 1 (R/W)
   CW[9:0] = [AD9, AD8, AD7, AD6, AD5, AD4, AD3, AD2, AD1, AD0] (STARTING MSB JUSTIFIED REGISTER ADDRESS)

07667-041

Figure 41. Sequential Register Read Back SPI Timing

I²C-COMPATIBLE INTERFACE

The AD7879-1 supports the industry standard 2-wire I²C serial interface protocol. The two wires associated with the I²C timing are the SCL and SDA inputs. The SDA is an I/O pin that allows both register write and register read back operations. The AD7879-1 is always a slave device on the I²C serial interface bus.

It has a 7-bit device address, Address 0101 1XX. The lower two bits are set by tying the ADD0 and ADD1 pins high or low. The AD7879-1 responds when the master device sends its device address over the bus. The AD7879-1 cannot initiate data transfers on the bus.

Table 23. AD7879-1 I²C Device Address

ADD1	ADD0	I²C Address
0	0	0101 100
0	1	0101 101
1	0	0101 110
1	1	0101 111

Data Transfer

Data is transferred over the I²C serial interface in 8-bit bytes. The master initiates a data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line, SDA, while the serial clock line, SCL, remains high. This indicates that an address/data stream follows.

All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/$\overline{W}$ bit that determines the direction of the data transfer. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as the acknowledge bit. All other devices on the bus then remain idle while the selected device waits for data to be read from, or written to it. If the R/$\overline{W}$ bit is a 0, the master writes to the slave device. If the R/$\overline{W}$ bit is a 1, the master reads from the slave device.

Data is sent over the serial bus in a sequence of nine clock pulses (eight bits of data followed by an acknowledge bit from the slave device). Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high can be interpreted as a stop signal. The number of data bytes transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

When all data bytes are read or written, a stop condition is established. A stop condition is defined by a low-to-high transition on SDA while SCL remains high. If the AD7879 encounters a stop condition, it returns to its idle condition.

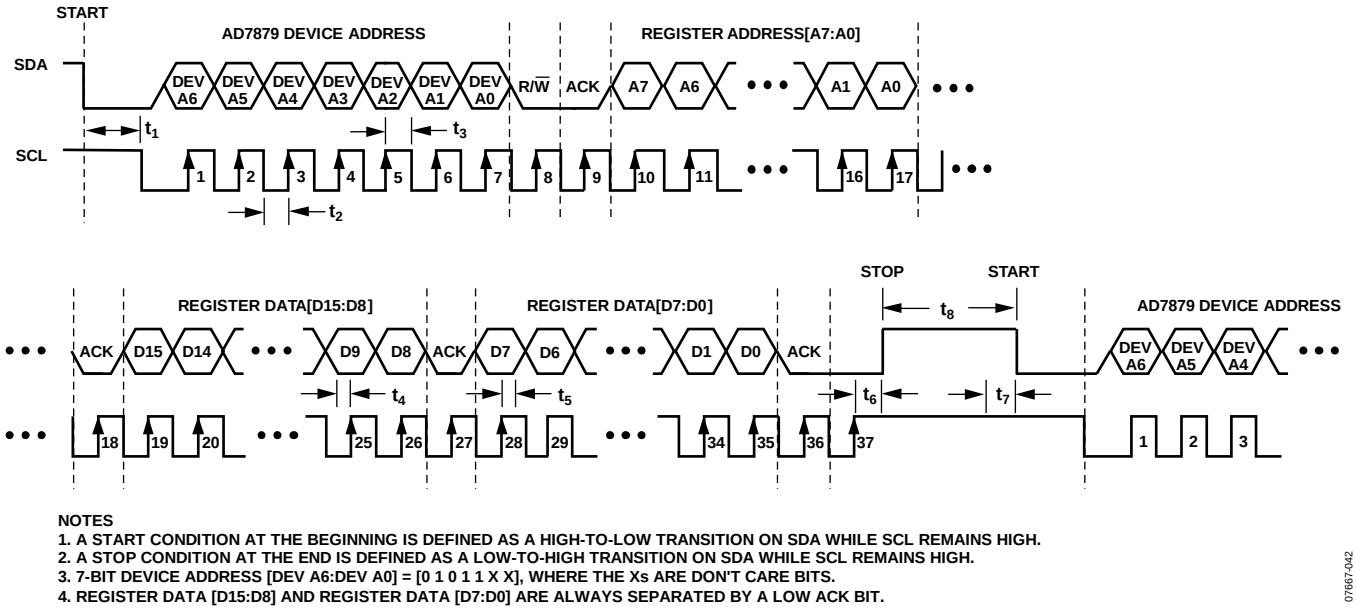


Figure 42. Example of I²C Timing for Single Register Write Operation

Writing Data over the I²C Bus

The process of writing to the AD7879-1 over the I²C bus is shown in Figure 42 and Figure 44. The device address is sent over the bus followed by the R/$\overline{W}$ bit set to 0. This is followed by two bytes of data that contain the 10-bit address of the internal data register to be written. The address is contained in the 8 LSBs of the register address byte. The bit map in Table 24 shows the register address byte.

Table 24.

MSB							LSB
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Register Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

The third data byte contains the 8 MSBs of the data to be written to the internal register. The fourth data byte contains the 8 LSBs of data to be written to the internal register.

The AD7879-1 address pointer register automatically increments after each write. This allows the master to sequentially write to all registers on the AD7879-1 in the same write transaction. However, the address pointer register does not wrap around after the last address.

Any data written to the AD7879-1 after the address pointer has reached its maximum value is discarded.

All registers on the AD7879-1 have 16 bits. Two consecutive 8-bit data bytes are combined and written to the 16-bit registers. To avoid errors, all writes to the device must contain an even number of data bytes.

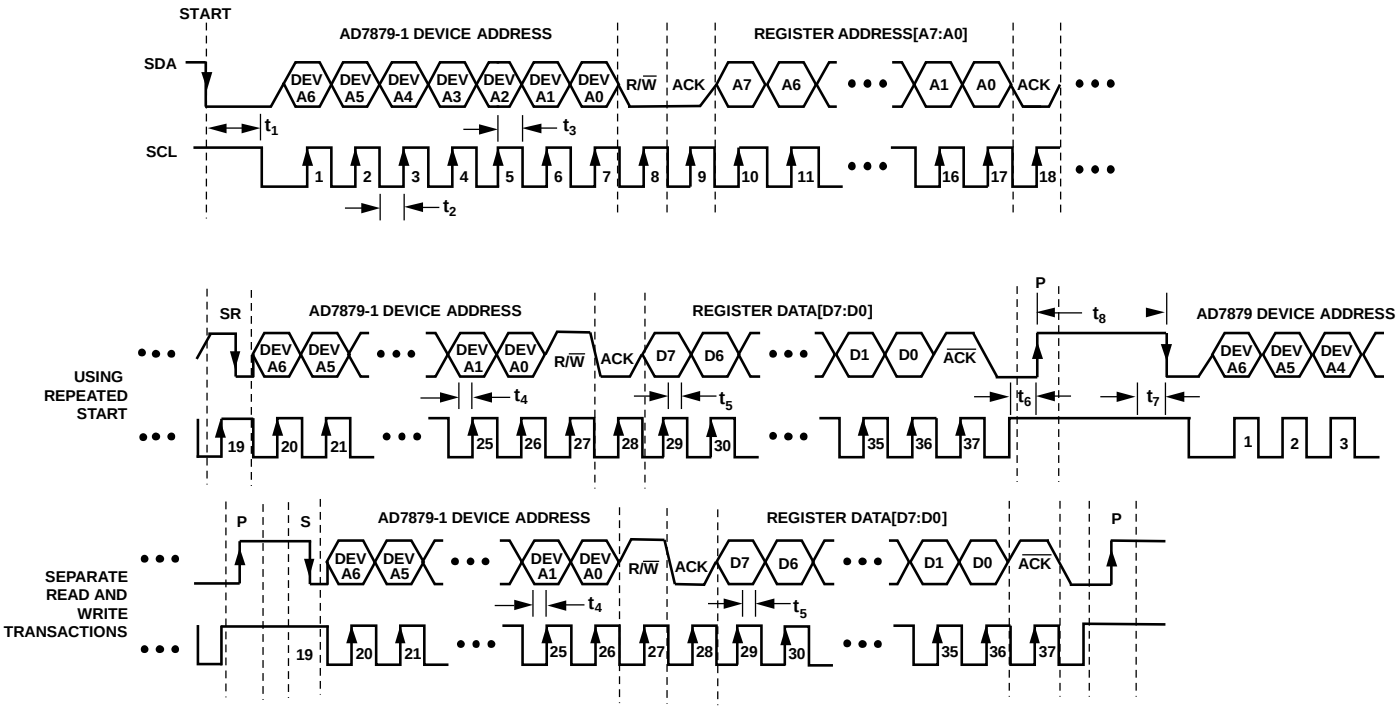
To finish the transaction, the master generates a stop condition on SDA, or generates a repeat start condition if the master is to maintain control of the bus.

Reading Data Over the I²C Bus

To read from the AD7879-1, the address pointer register must first be set to the address of the required internal register. The master performs a write transaction and writes to the AD7879-1 to set the address pointer. The master then outputs a repeat start condition to keep control of the bus, or if this is not possible, the master ends the write transaction with a stop condition. A read transaction is initiated, with the R/$\overline{W}$ bit set to 1.

The AD7879-1 supplies the upper eight bits of data from the addressed register in the first read back byte, followed by the lower eight bits in the next byte. This is shown in Figure 43 and Figure 44.

Because the address pointer automatically increases after each read, the AD7879-1 continues to output readback data until the master puts a no acknowledge and a stop condition on the bus. If the address pointer reaches its maximum value, and the master continues to read from the part, the AD7879-1 repeatedly sends data from the last register addressed.



NOTES
1. A START CONDITION AT THE BEGINNING IS DEFINED AS A HIGH-TO-LOW TRANSITION ON SDA WHILE SCL REMAINS HIGH.
2. A STOP CONDITION AT THE END IS DEFINED AS A LOW-TO-HIGH TRANSITION ON SDA WHILE SCL REMAINS HIGH.
3. THE MASTER GENERATES THE $\overline{ACK}$ AT THE END OF THE READBACK TO SIGNAL THAT IT DOES NOT WANT ADDITIONAL DATA.
4. 7-BIT DEVICE ADDRESS [DEV A6:DEV A0] = [0 1 0 1 1 X X], WHERE THE TWO LSB Xs ARE DON'T CARE BITS.
5. REGISTER DATA [D15:D8] AND REGISTER DATA [D7:D0] ARE ALWAYS SEPARATED BY A LOW ACK BIT.
6. THE R/$\overline{W}$ BIT IS SET TO A1 TO INDICATE A READBACK OPERATION.

Figure 43. Example of I²C Timing for Single Register Read Back Operation

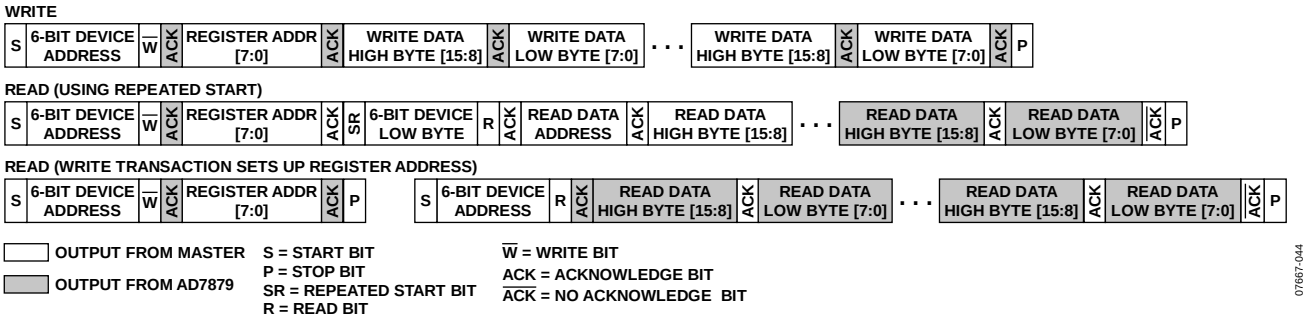


Figure 44. Example of Sequential I²C Write and Read Back Operation

GROUNDING AND LAYOUT

For detailed information on grounding and layout considerations for the AD7879, refer to the AN-577 Application Note, *Layout and Grounding Recommendations for Touch Screen Digitizers*.

CHIP SCALE PACKAGES

The lands on the chip scale package (CP-16-10) are rectangular. The printed circuit board (PCB) pad for these should be 0.1 mm longer than the package land length, and 0.05 mm wider than the package land width. Center the land on the pad to maximize the solder joint size.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. To avoid shorting, provide a clearance of at least 0.25 mm between the thermal pad and the inner edges of the land pattern on the PCB. Thermal vias can be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at a 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz. of copper to plug the via.

Connect the PCB thermal pad to GND.

WLCSP ASSEMBLY CONSIDERATIONS

For detailed information on the WLCSP PCB assembly and reliability, see the AN-617 Application Note, *MicroCSP™ Wafer Level Chip Scale Package*.

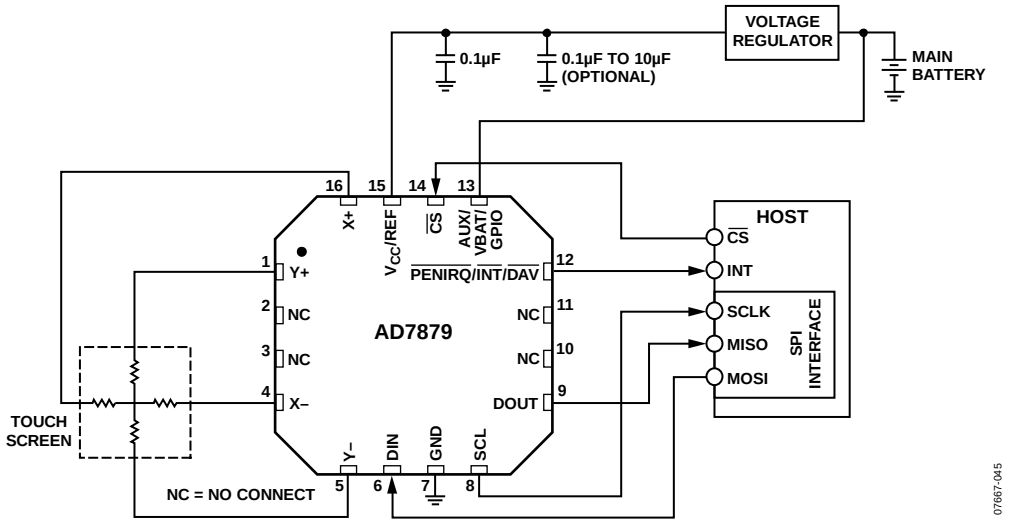


Figure 45. Typical Application Circuit

OUTLINE DIMENSIONS

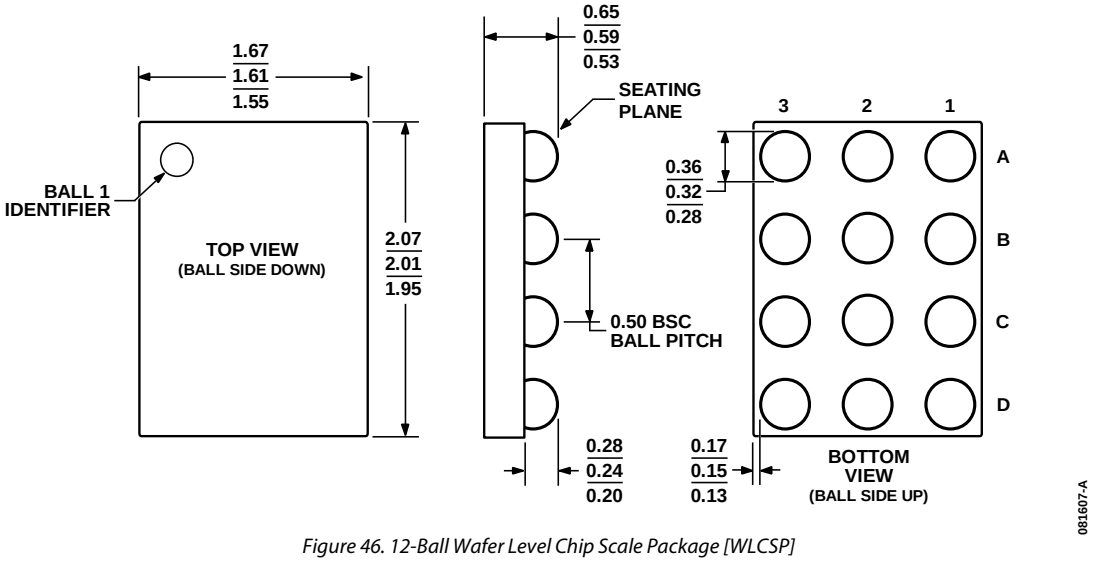


Figure 46. 12-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-12-1)
Dimensions shown in millimeters

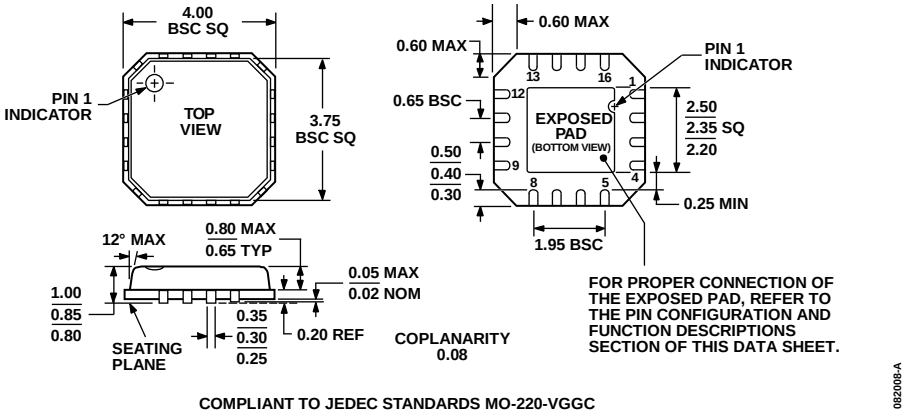


Figure 47. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm x 4mm Very Thin Quad
(CP-16-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Serial Interface Description	Package Description	Package Option	Branding
AD7879ACBZ-RL[1]	–40°C to +85°C	SPI Interface	12-Ball WLCSP	CB-12-1	T2Y
AD7879ACBZ-500R7[1]	–40°C to +85°C	SPI Interface	12-Ball WLCSP	CB-12-1	T2Y
AD7879ACPZ-RL[1]	–40°C to +85°C	SPI Interface	16-Lead LFCSP_VQ	CP-16-10	
AD7879ACPZ-500R7[1]	–40°C to +85°C	SPI Interface	16-Lead LFCSP_VQ	CP-16-10	
AD7879-1ACBZ-RL[1]	–40°C to +85°C	I²C Interface	12-Ball WLCSP	CB-12-1	T0Q
AD7879-1ACBZ-500R7[1]	–40°C to +85°C	I²C Interface	12-Ball WLCSP	CB-12-1	T0Q
AD7879-1ACPZ-RL[1]	–40°C to +85°C	I²C Interface	16-Lead LFCSP_VQ	CP-16-10	
AD7879-1ACPZ-500R7[1]	–40°C to +85°C	I²C Interface	16-Lead LFCSP_VQ	CP-16-10	
EVAL-AD7879EBZ[1]		SPI Interface	Evaluation Board		
EVAL-AD7879-1EBZ[1]		I²C Interface	Evaluation Board		

[1] Z = RoHS Compliant Part.