General-Purpose, −55°C to +125°C, Wide Bandwidth, DC-Coupled VGA

AD8336

FEATURES

- Low noise
  - Voltage noise: 3 nV/√Hz
  - Current noise: 3 pA/√Hz
- Small signal BW: 115 MHz
- Large signal BW: 2 V p-p = 80 MHz
- Slew rate: 550 V/µs, 2 V p-p
- Gain ranges (specified)
  - −14 dB to +46 dB,
  - 0 dB to 60 dB
- Gain scaling: 50 dB/V
- DC-coupled
- Single-ended input and output
- Supplies: ±3 V to ±12 V
- Temperature Range: −55°C to +125°C
- Power
  - 150 mW @ ±3 V, −55°C < T < +125°C
  - 84 mW @ ±3 V, PWRA = 3 V

APPLICATIONS

- Industrial process controls
- High performance AGC systems
- I/Q signal processing
- Video
- Industrial and medical ultrasound
- Radar receivers

FUNCTIONAL BLOCK DIAGRAM

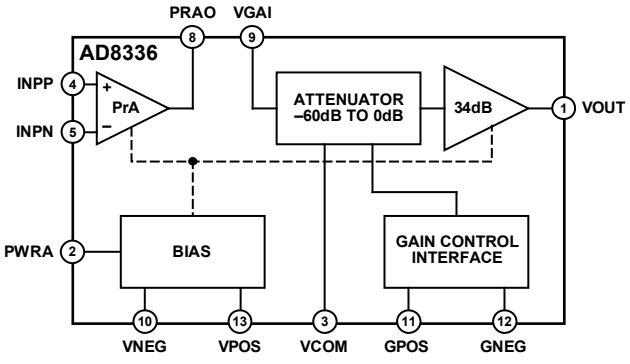

Figure 1.

GENERAL DESCRIPTION

The AD8336 is a low noise, single-ended, linear-in-dB, general-purpose variable gain amplifier, usable over a large range of supply voltages. It features an uncommitted preamplifier (preamp) with a usable gain range of 6 dB to 26 dB established by external resistors in the classical manner. The VGA gain range is 0 dB to 60 dB, and its absolute gain limits are −26 dB to +34 dB. When the preamplifier gain is adjusted for 12 dB, the combined 3 dB bandwidth of the preamp and VGA is 100 MHz, and the amplifier is fully usable to 80 MHz. With ±5 V supplies, the maximum output swing is 2 V p-p.

Thanks to its X-Amp® architecture, excellent bandwidth uniformity is maintained across the entire gain range of the VGA. Intended for a broad spectrum of applications, the differential gain control interface provides precise linear-in-dB gain scaling of 50 dB/V over the temperature span of −55°C to +125 °C. The differential gain control is easy to interface with a variety of external circuits within the common-mode voltage limits of the AD8336.

The large supply voltage range makes the AD8336 particularly suited for industrial medical applications and for video circuits. Dual-supply operation enables bipolar input signals, such as those generated by photodiodes or photomultiplier tubes.

The fully independent voltage feedback preamp allows both inverting and noninverting gain topologies, making it a fully bipolar VGA. The AD8336 can be used within the specified gain range of −14 dB to +60 dB by selecting a preamp gain between 6 dB and 26 dB and choosing appropriate feedback resistors. For the nominal preamp gain of 4×, the overall gain range is −14 dB to +46 dB.

In critical applications, the quiescent power can be reduced by about half by using the power adjust pin, PWRA. This is especially useful when operating with high supply voltages of up to ±12 V, or at high temperatures.

The operating temperature range is −55°C to +125°C. The AD8336 is available in a 16-lead LFCSP (4 mm × 4 mm).

Rev. 0

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REVISION HISTORY

10/06—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±5 V, T = 25°C, gain range = −14 dB to +46 dB, preamp gain = 4×, f = 1 MHz, C_L = 5 pF, R_L = 500 Ω, PWRA = GND, unless otherwise specified.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
PREAMPLIFIER					
−3 dB Small Signal Bandwidth	V_{OUT} = 10 mV p-p		150		MHz
−3 dB Large Signal Bandwidth	V_{OUT} = 2 V p-p		85		MHz
Bias Current, Either Input			725		nA
Differential Offset Voltage			±600		µV
Input Resistance			900		kΩ
Input Capacitance			3		pF
PREAMPLIFIER + VGA					
−3 dB Small Signal Bandwidth	V_{OUT} = 10 mV p-p		115		MHz
	V_{OUT} = 10 mV p-p, PWRA = 5 V		40		MHz
	V_{OUT} = 10 mV p-p, PrA gain = 20×		20		MHz
	V_{OUT} = 10 mV p-p, PrA gain = −3×		125		MHz
−3 dB Large Signal Bandwidth	V_{OUT} = 2 V p-p		80		MHz
	V_{OUT} = 2 V p-p, PWRA = 5 V		30		MHz
	V_{OUT} = 2 V p-p, PrA gain = 20×		20		MHz
	V_{OUT} = 2 V p-p, PrA gain = −3×		100		MHz
Slew Rate	V_{OUT} = 2 V p-p		550		V/µs
Short-Circuit Preamp Input Voltage Noise Spectral Density	±3 V ≤ V_S ≤ ±12 V		3.0		nV/√Hz
Input Current Noise Spectral Density			3.0		pA/√Hz
Output Referred Noise	V_{GAIN} = 0.7 V, PrA gain = 4×		600		nV/√Hz
	V_{GAIN} = −0.7 V, PrA gain = 4×		190		nV/√Hz
	V_{GAIN} = 0.7 V, PrA gain = 20×		2500		nV/√Hz
	V_{GAIN} = −0.7 V, PrA gain = 20×		200		nV/√Hz
	V_{GAIN} = 0.7 V, −55°C ≤ T ≤ +125°C		700		nV/√Hz
	V_{GAIN} = −0.7 V, −55°C ≤ T ≤ +125°C		250		nV/√Hz
DYNAMIC PERFORMANCE					
Harmonic Distortion	V_{GAIN} = 0 V, V_{OUT} = 1 V p-p				
HD2	f = 1 MHz		−58		dBc
HD3	f = 1 MHz		−68		dBc
HD2	f = 10 MHz		−60		dBc
HD3	f = 10 MHz		−60		dBc
Input 1 dB Compression Point	V_{GAIN} = −0.7 V		11		dBm[1]
	V_{GAIN} = +0.7 V		−23		dBm
Two-Tone Intermodulation	V_{GAIN} = 0 V, V_{OUT} = 1 V p-p, f_1 = 0.95 MHz, f_2 = 1.05 MHz		−71		dBc
Distortion (IMD3)	V_{GAIN} = 0 V, V_{OUT} = 1 V p-p, f_1 = 9.95 MHz, f_2 = 10.05 MHz		−69		dBc
	V_{GAIN} = 0 V, V_{OUT} = 2 V p-p, f_1 = 0.95 MHz, f_2 = 1.05 MHz		−60		dBc
	V_{GAIN} = 0 V, V_{OUT} = 2 V p-p, f_1 = 9.95 MHz, f_2 = 10.05 MHz		−58		dBc
Output Third-Order Intercept	V_{GAIN} = 0 V, V_{OUT} = 1 V p-p, f = 1 MHz		34		dBm
	V_{GAIN} = 0 V, V_{OUT} = 1 V p-p, f = 10 MHz		32		dBm
	V_{GAIN} = 0 V, V_{OUT} = 2 V p-p, f = 1 MHz		34		dBm
	V_{GAIN} = 0 V, V_{OUT} = 2 V p-p, f = 10 MHz		33		dBm
Overdrive Recovery	V_{GAIN} = 0.7 V, V_{IN} = 100 mV p-p to 5 mV p-p		50		ns
Group Delay Variation	1 MHz < f < 10 MHz, full gain range		±1		ns
PrA Gain = 20 ×	1 MHz < f < 10 MHz, full gain range		±3		ns

Parameter	Conditions	Min	Typ	Max	Unit
ABSOLUTE GAIN ERROR[2]	$-0.7\ V < V_{GAIN} < -0.6\ V$	0	1 to 5	6	dB
	$-0.6\ V < V_{GAIN} < -0.5\ V$	0	0.5 to1.5	3	dB
	$-0.5\ V < V_{GAIN} < 0.5\ V$	−1.25	±0.2	+1.25	dB
	$-0.5\ V < V_{GAIN} < 0.5\ V$, $\pm3\ V \le V_S \le \pm12\ V$		±0.5	1.25	dB
	$-0.5\ V < V_{GAIN} < 0.5\ V$, −55 °C ≤ T ≤ +125 °C		±0.5		dB
	$-0.5\ V < V_{GAIN} < 0.5\ V$, PrA gain = −3×		±0.5		dB
	$0.5\ V < V_{GAIN} < 0.6\ V$	−4.0	−1.5 to −3.0	0	dB
	$0.6\ V < V_{GAIN} < 0.7\ V$	−9.0	−1 to −5	0	dB
GAIN CONTROL INTERFACE					
Gain Scaling Factor		48	49.9	52	dB/V
Intercept	Preamp + VGA		16.4		dB
	VGA Only		4.5		dB
Gain Range		58	60	62	dB
Input Voltage (V_{GAIN}) Range	No foldover	$-V_S$		$+V_S$	V
Input Current			1		µA
Input Capacitance					pF
Response Time	60 dB gain change		300		ns
OUTPUT PERFORMANCE					
Output Impedance, DC to 10 MHz	$\pm3\ V \le V_S \le \pm12\ V$		2.5		Ω
Output Signal Swing	$R_L \ge 500\ \Omega$ (for $\lvert V_{SUPPLY}\rvert \le \pm5V$); $R_L \ge 1\ k\Omega$ above that		$\lvert V_{SUPPLY}\rvert - 1.5$		V
	$R_L \ge 1\ k\Omega$ (for $\lvert V_{SUPPLY}\rvert = \pm12V$)		$\lvert V_{SUPPLY}\rvert - 2.25$		V
Output Current	Linear operation − minimum discernable distortion		20		mA
Short-Circuit Current	$V_S = \pm3\ V$		+123/−72		mA
	$V_S = \pm5\ V$		+123/−72		mA
	$V_S = \pm12\ V$		+72/−73		mA
Output Offset Voltage	$V_{GAIN} = 0.7\ V$, gain = 200×	−250	−125	150	mV
	$\pm3\ V \le V_S \le \pm12\ V$		−200		mV
	−55°C ≤ T ≤ +125°C		−200		mV
PWRA Pin					
Normal Power (Logic Low)	$V_S = \pm3\ V$			0.7	V
Low Power (Logic High)	$V_S = \pm3\ V$	1.5			V
Normal Power (Logic Low)	$V_S = \pm5\ V$			1.2	V
Low Power (Logic High)	$V_S = \pm5\ V$	2.0			V
Normal Power (Logic Low)	$V_S = \pm12\ V$			3.2	V
Low Power (Logic High)	$V_S = \pm12\ V$	4.0			V
POWER SUPPLY					
Supply Voltage Operating Range		±3		±12	V
Quiescent Current					
$V_S = \pm3\ V$		22	25	30	
	−55°C ≤ T ≤ +125°C		23 to 31		mA
	PWRA = 3 V	10	14	18	
$V_S = \pm5\ V$		22	26	30	
	−55°C ≤ T ≤ +125°C		23 to 31		mA
	PWRA = 5 V	10	14	18	
$V_S = \pm12\ V$		23	28	31	
	−55°C ≤ T ≤ +125°C		24 to 33		mA
	PWRA = 5 V		16		

Parameter	Conditions	Min	Typ	Max	Unit
Power Dissipation	$V_S = \pm 3$ V		150		mW
	$V_S = \pm 5$ V		260		mW
	$V_S = \pm 12$ V		672		mW
PSRR	$V_{GAIN} = 0.7$ V, f = 1 MHz		−40		dB

[1] All dBm values are calculated with 50 Ω reference, unless otherwise noted.
[2] Conformance to theoretical gain expression (see the Setting the Gain section).

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (VPOS, VNEG)	±15 V
Input Voltage (INPP, INPN)	VPOS, VNEG
Gain Voltage (GPOS, GNEG)	VPOS, VNEG
PWRA	5 V, GND
Power Dissipation	
$V_S \leq \pm 5$ V	0.43 W
± 5 V < $V_S \leq \pm 12$ V	1.12 W
Operating Temperature Range	
± 3 V < $V_S \leq \pm 10$ V	−55°C to +125°C
± 10 V < $V_S \leq \pm 12$ V	−55°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C
Thermal Data (4-layer JEDEC board, no air flow, exposed pad soldered to PC board)	
θ_{JA}	58.2°C/W
θ_{JB}	35.9°C/W
θ_{JC}	9.2°C/W
Ψ_{JT}	1.1°C/W
Ψ_{JB}	34.5°C/W

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

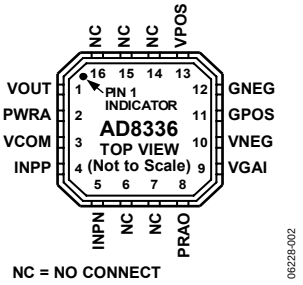


Figure 2. 16-Lead LFCSP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	VOUT	Output Voltage.
2	PWRA	Power Control. Normal power when grounded; power reduced by half if V_{PWRA} is pulled high.
3	VCOM	Common-Mode Voltage. Normally GND when using a dual supply.
4	INPP	Positive Input to Preamp.
5	INPN	Negative Input to Preamp.
6	NC	No Connect.
7	NC	No Connect.
8	PRAO	Preamp Output.
9	VGAI	VGA Input.
10	VNEG	Negative Supply.
11	GPOS	Positive Gain Control Input.
12	GNEG	Negative Gain Control Input.
13	VPOS	Positive Supply.
14	NC	No Connect.
15	NC	No Connect.
16	NC	No Connect.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±5 V, T = 25°C, gain range = −14 dB to +46 dB, PrA gain = +4×, f = 1 MHz, C_L = 5 pF, R_L = 500 Ω, PWRA = GND, unless otherwise specified.

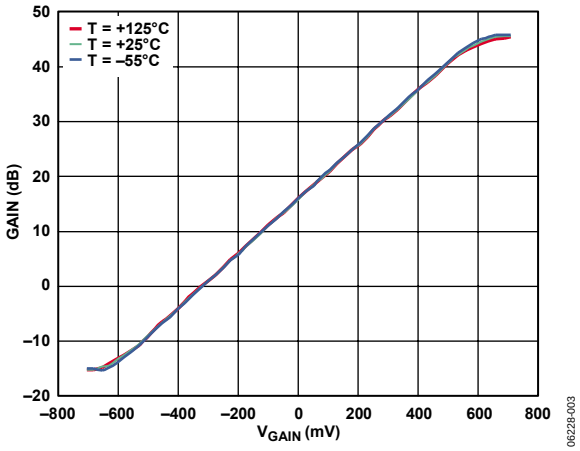


Figure 3. Gain vs. V_{GAIN} for Three Values of Temperature (T)

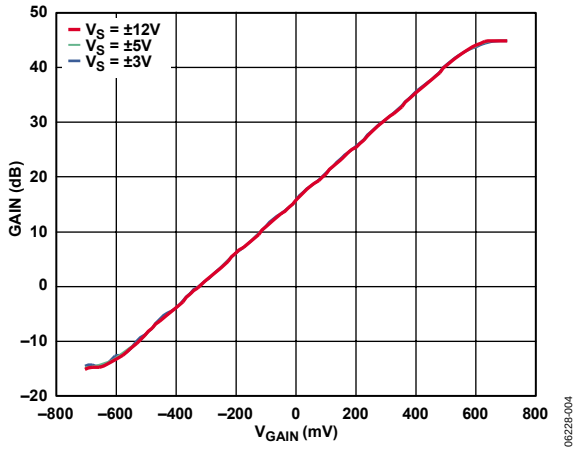


Figure 4. Gain vs. V_{GAIN} for Three Values of Supply Voltage (V_S)

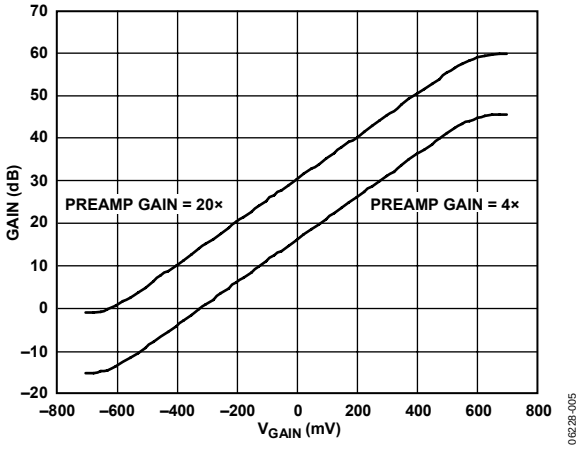


Figure 5 Gain vs. V_{GAIN} for Preamp Gains of 4× and 20×

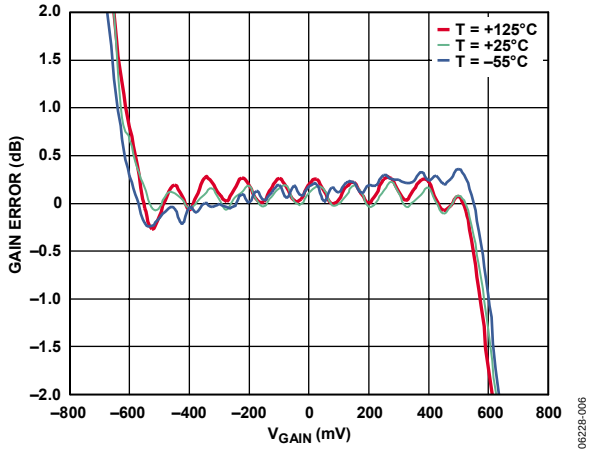


Figure 6. Gain Error vs. V_{GAIN} for Three Values of Temperature (T)

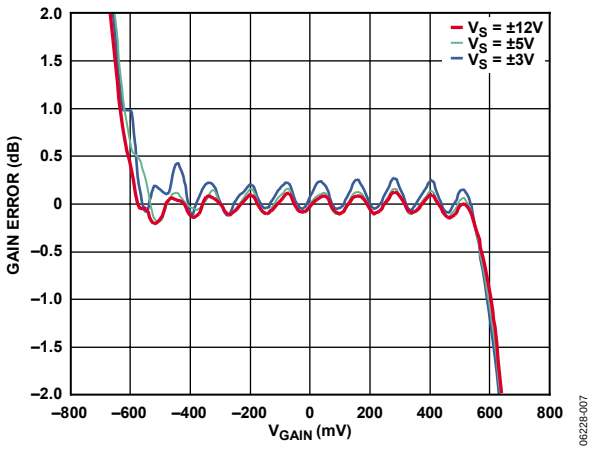


Figure 7. Gain Error vs. V_{GAIN} for Three Values of Supply Voltage (V_S)

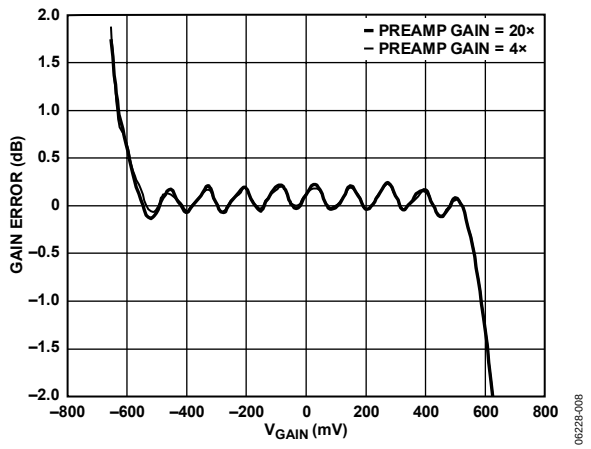


Figure 8. Gain Error vs. V_{GAIN} for Preamp Gains of 4× and 20×

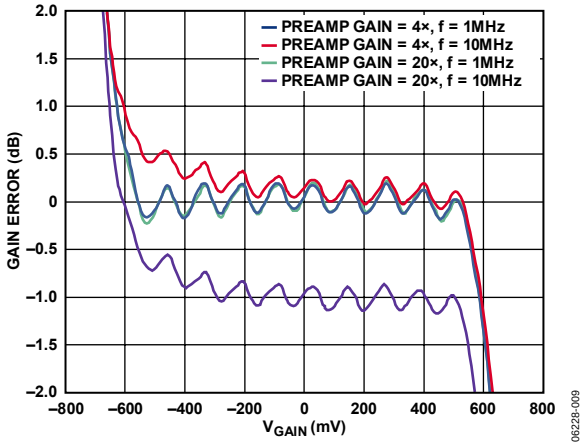


Figure 9. Gain Error vs. V_{GAIN} at 1 MHz and 10 MHz and for Preamp Gains of 4× and 20×

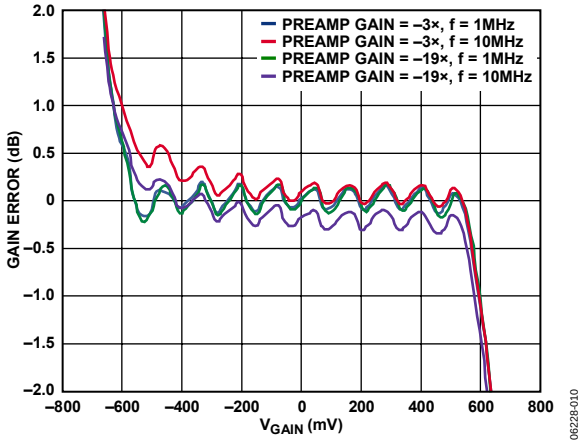


Figure 10. Gain Error vs. V_{GAIN} at 1 MHz and 10 MHz and for Inverting Preamp Gains of −3× and −19×

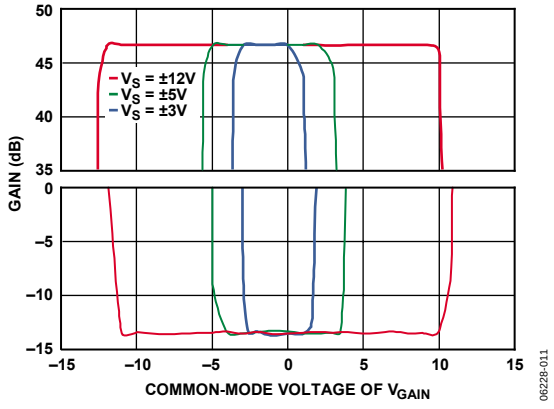


Figure 11. Common-Mode Voltage at Pin V_{GAIN} vs. V_{GAIN}

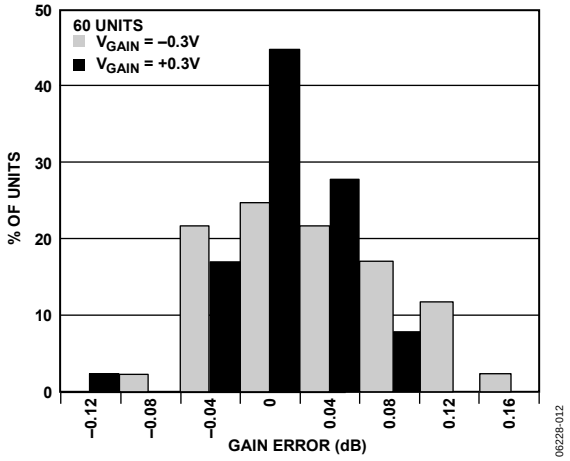


Figure 12. Gain Error Histogram

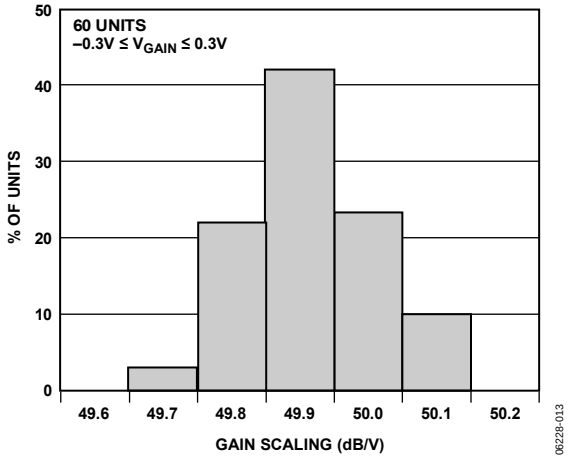


Figure 13. Gain Scaling Factor Histogram

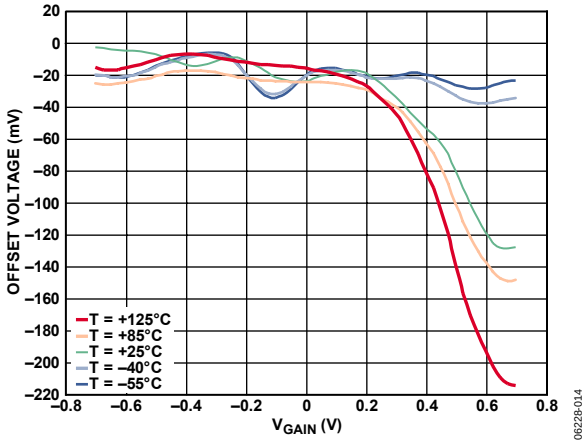


Figure 14. Output Offset Voltage vs. V_{GAIN} for Various Values of Temperature (T)

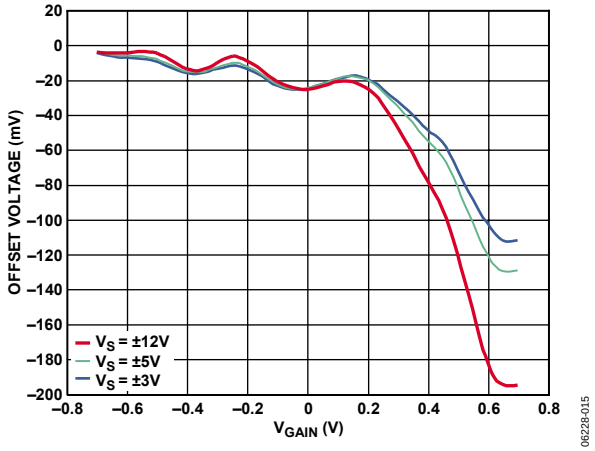


Figure 15. Output Offset Voltage vs. V_{GAIN} for Three Values of Supply Voltage (V_S)

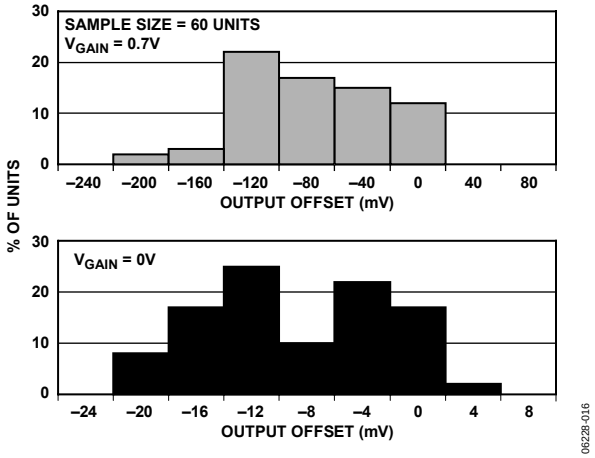


Figure 16. Output Offset Histogram

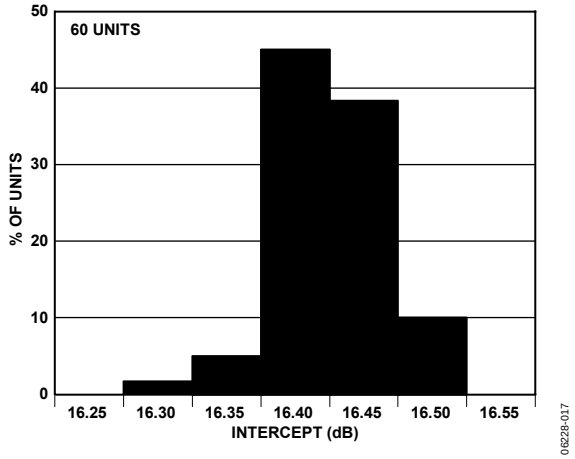


Figure 17. Intercept Histogram

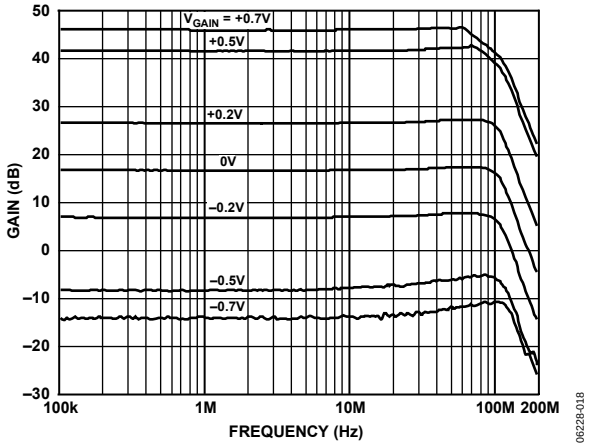


Figure 18. Frequency Response for Various Values of V_{GAIN}

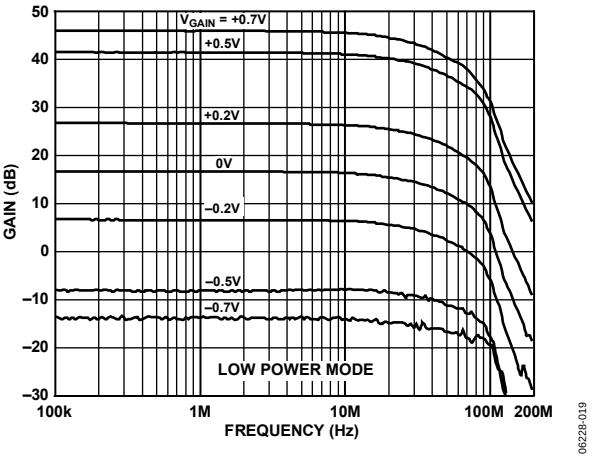


Figure 19. Frequency Response for Various Values of V_{GAIN}, Low Power Mode

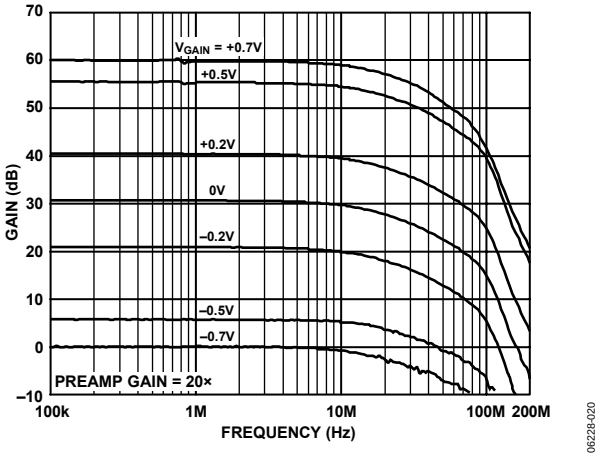


Figure 20. Frequency Response for Various Values of V_{GAIN} when the Preamp Gain is 20×

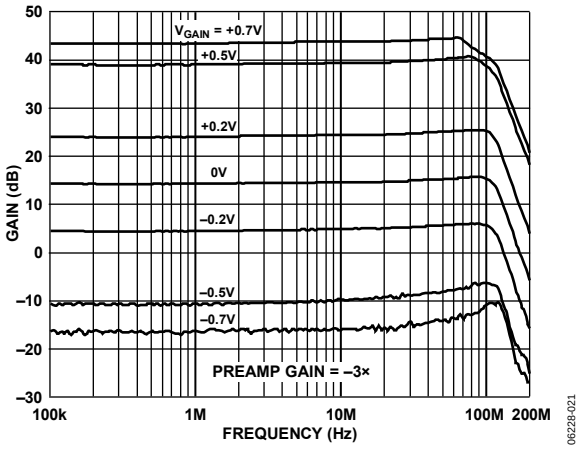


Figure 21. Frequency Response for Various Values of V_{GAIN} for Preamp Gain of –3×

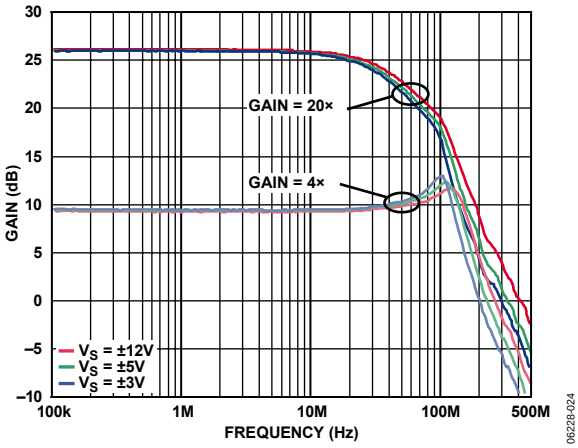


Figure 24. Preamp Frequency Response for Three Values of Supply Voltage (V_S) and Inverting Gain Values of –3× and –19×

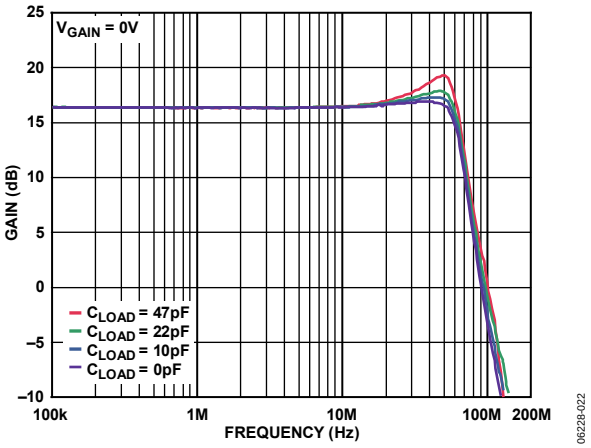


Figure 22. Frequency Response for Various Values of Load Capacitance (C_{LOAD})

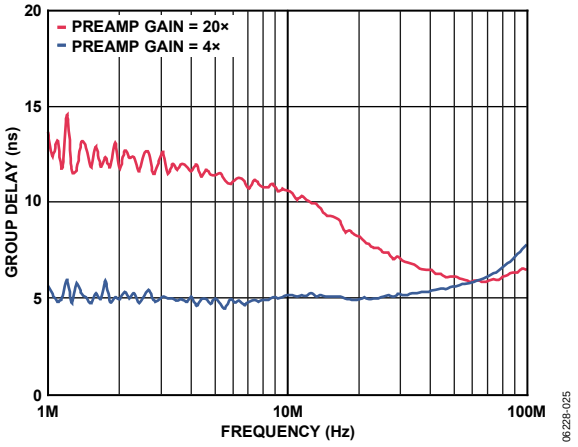


Figure 25. Group Delay vs. Frequency for Preamp Gains of 4× and 20×

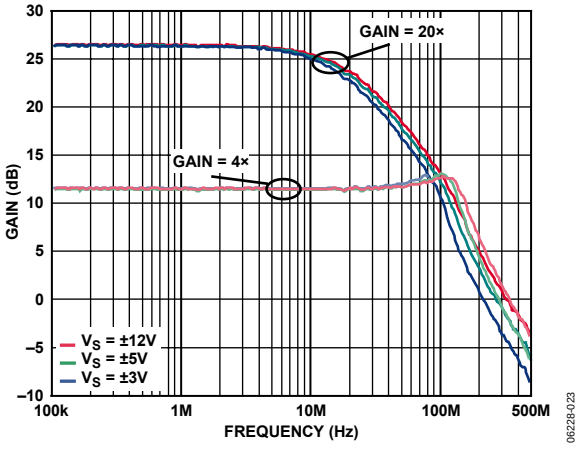


Figure 23. Preamp Frequency Response for Three Values of Supply Voltage (V_S) and for Preamp Gains of 4× and 20×

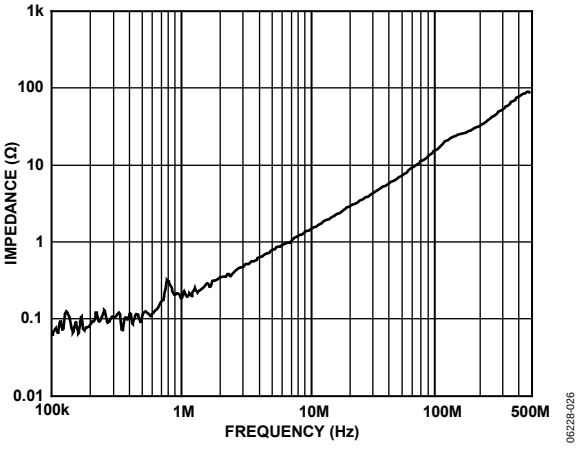


Figure 26. Output Resistance vs. Frequency of the Preamplifier

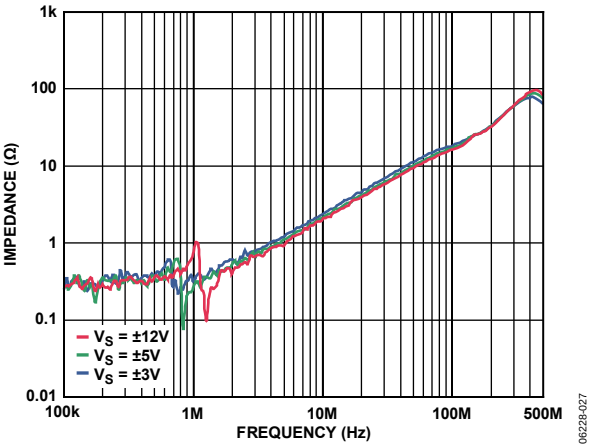


Figure 27. Output Resistance vs. Frequency of the VGA for Three Values of Supply Voltage (V_S)

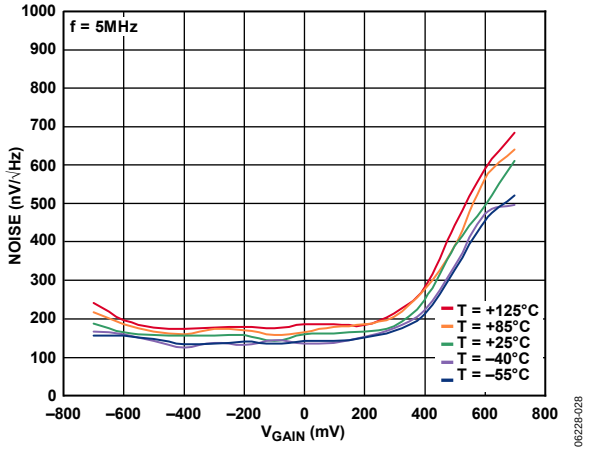


Figure 28. Output Referred Noise vs. V_{GAIN} at Various Temperatures (T)

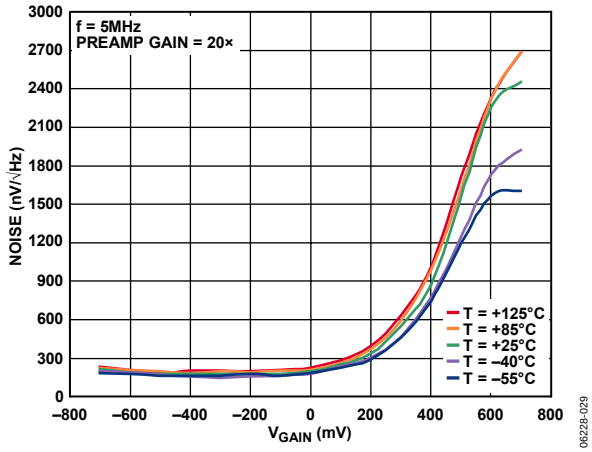


Figure 29. Output Referred Noise vs. V_{GAIN} at Various Temperatures (T) when the Preamp Gain is 20×

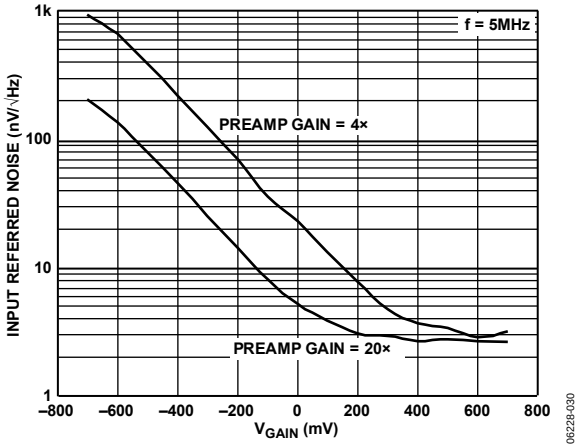


Figure 30. Input Referred Noise vs. V_{GAIN} for Preamp Gains of 4× and 20×

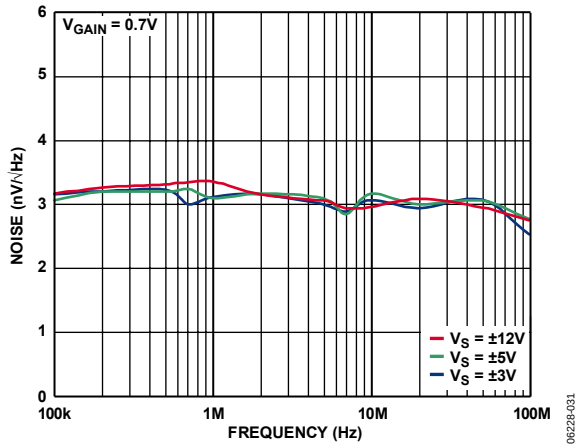


Figure 31. Short-Circuit Input Referred Noise vs. Frequency at Maximum Gain for Three Values of Power Supply Voltage (V_S)n

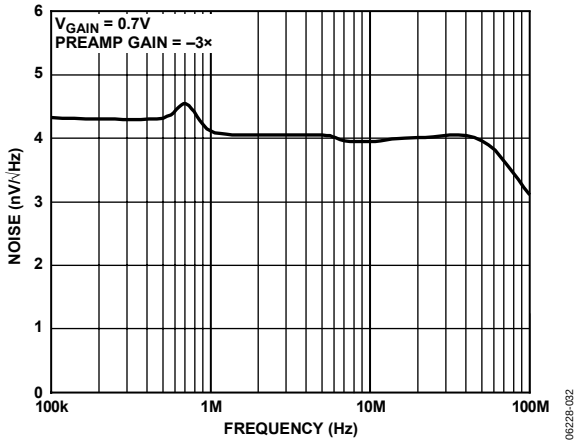


Figure 32. Short-Circuit Input Referred Noise vs. Frequency at Maximum Inverting Gain

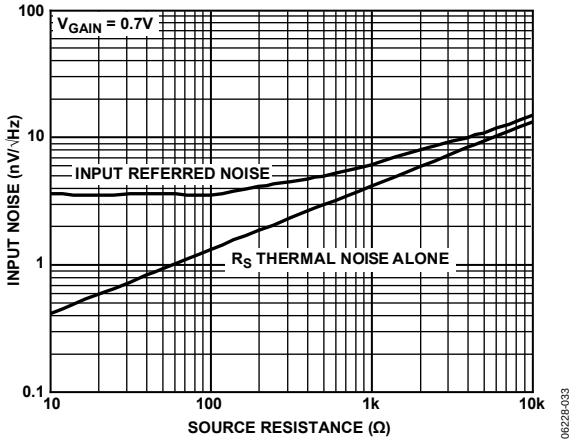


Figure 33. Input Referred Noise vs. Source Resistance

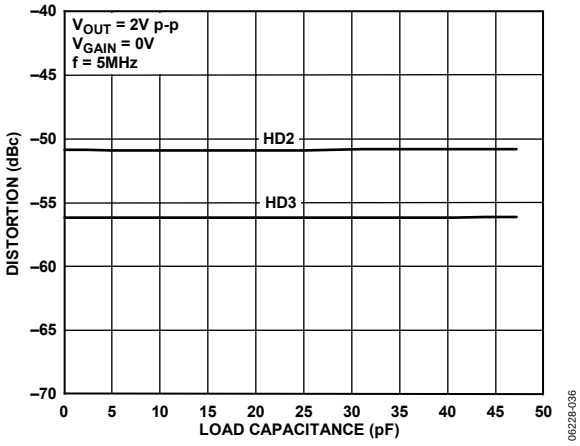


Figure 36. Harmonic Distortion vs. Load Capacitance

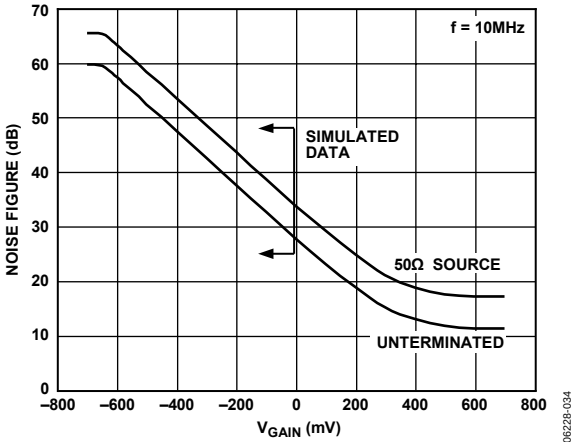


Figure 34. Noise Figure vs. V_{GAIN}

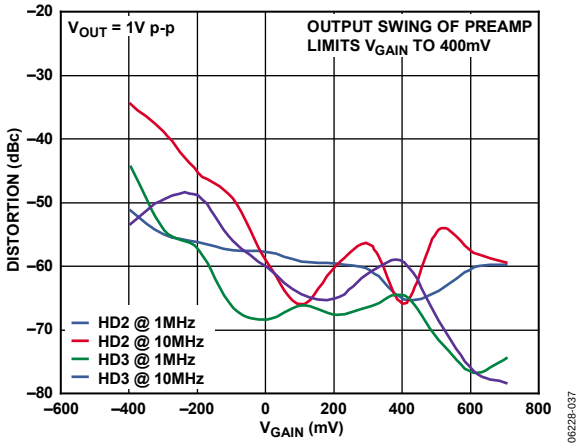


Figure 37. 2nd and 3rd Harmonic Distortion vs. V_{GAIN} at 1 MHz and 10 MHz

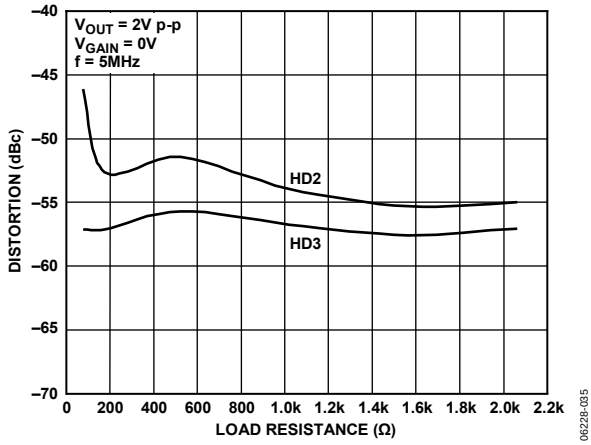


Figure 35. Harmonic Distortion vs. Load Resistance

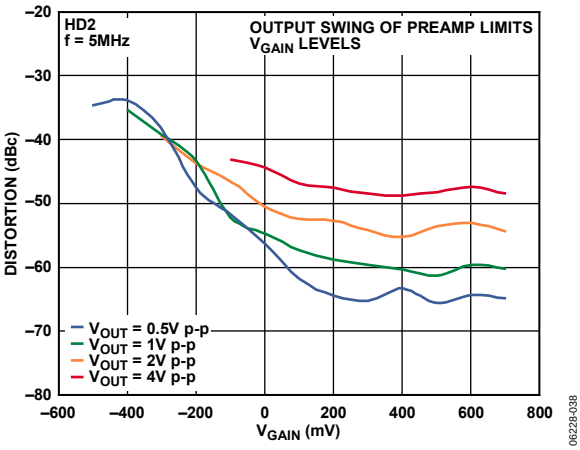


Figure 38. 2nd Harmonic Distortion vs. V_{GAIN} for Four Values of Output Voltage (V_{OUT})

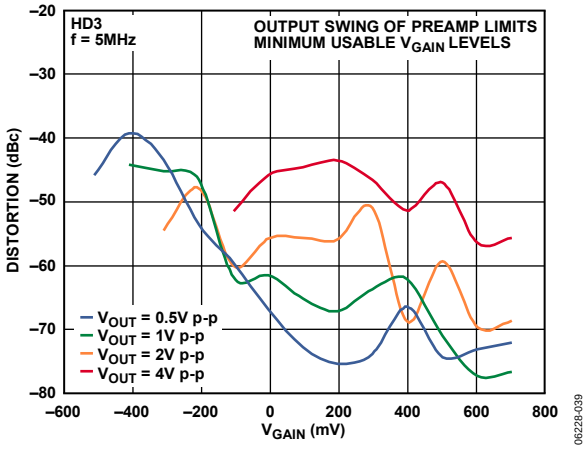


Figure 39. 3rd Harmonic Distortion vs. V_{GAIN} for Four Values of Output Voltage (V_{OUT})

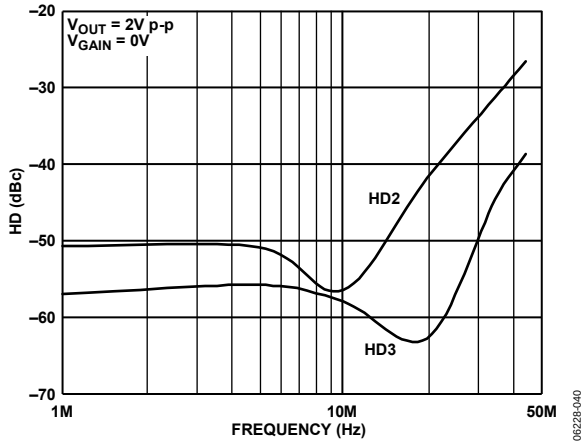


Figure 40. Harmonic Distortion vs. Frequency

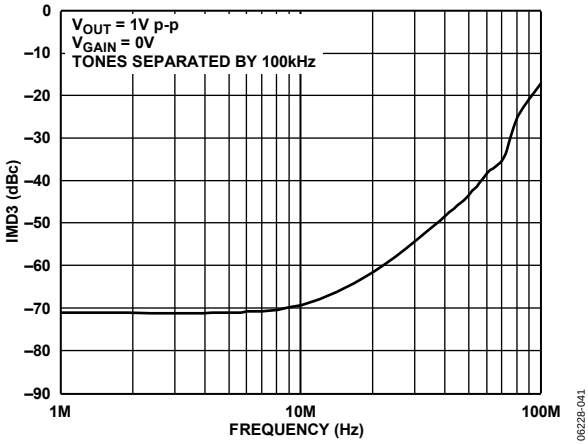


Figure 41. IMD3 vs. Frequency

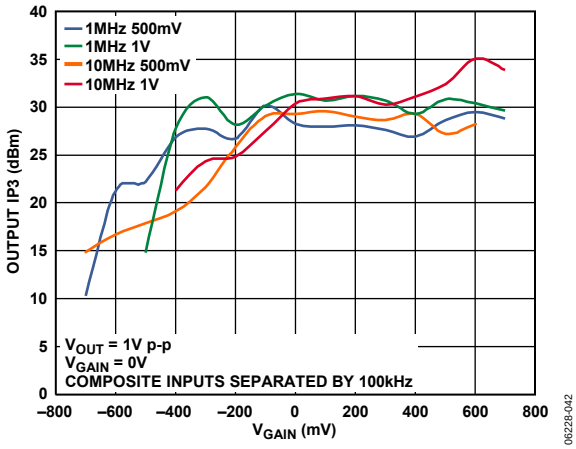


Figure 42. Output Referred IP3 (OIP3) vs. V_{GAIN} at Two Frequencies and Two Input Levels

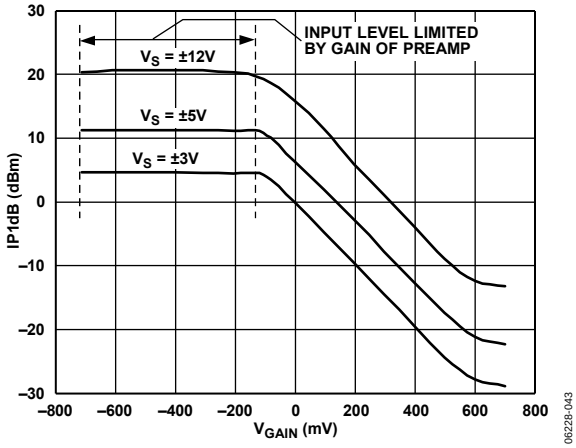


Figure 43. Input P1dB (IP1dB) vs. V_{GAIN} at Three Power Supply Values (V_S)

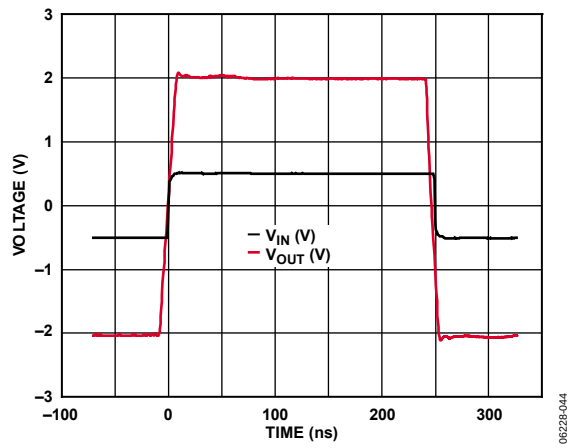


Figure 44. Large Signal Pulse Response of the Preamp

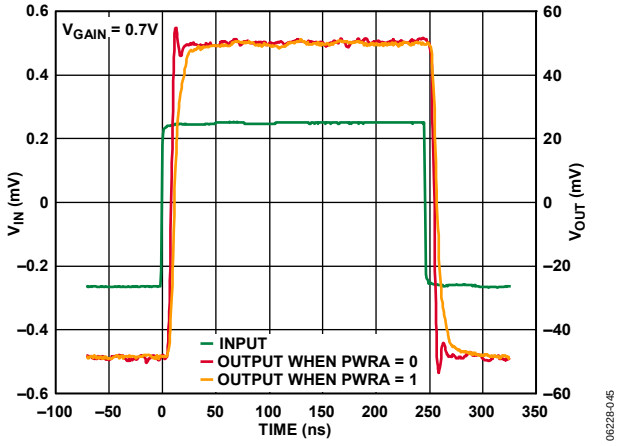


Figure 45. Noninverting Small Signal Pulse Response for Both Power Levels

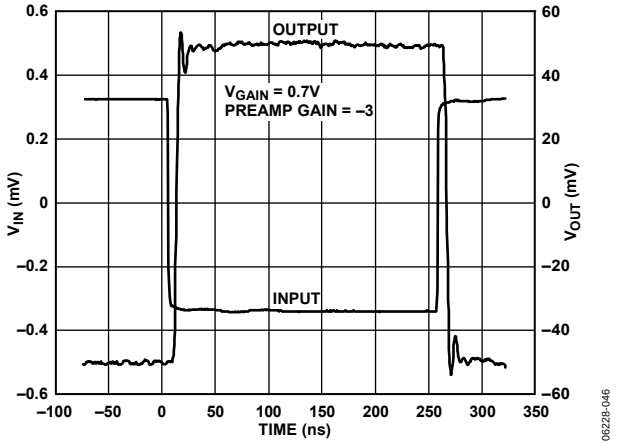


Figure 46. Inverting Gain Small Signal Pulse Response

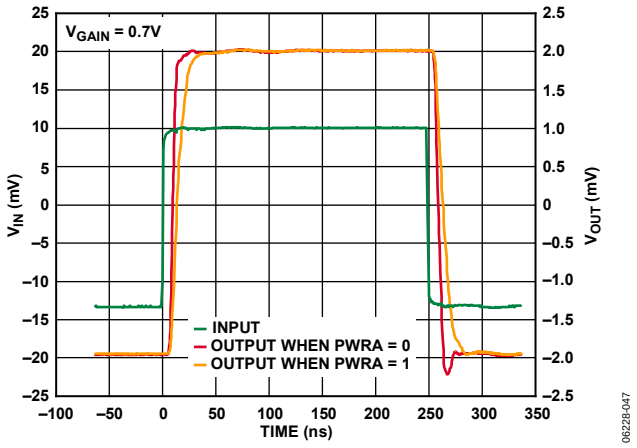


Figure 47. Large Signal Pulse Response for Both Power Levels

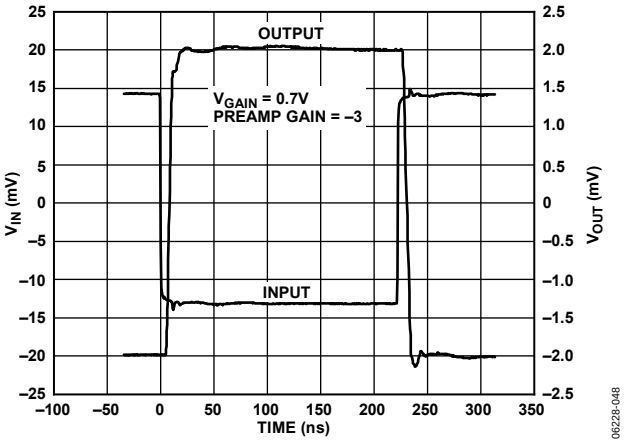


Figure 48. Inverting Gain Large Signal Pulse Response

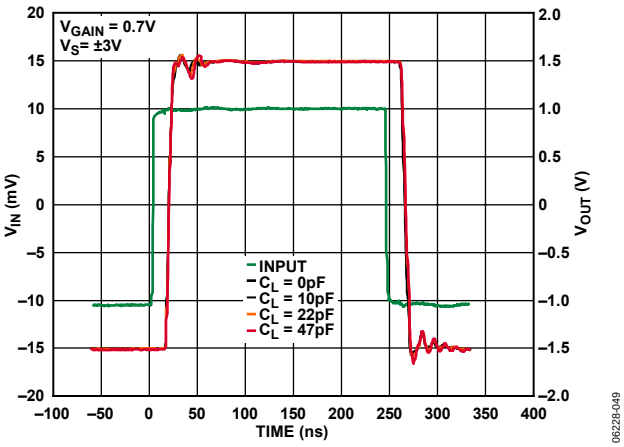


Figure 49. Large Signal Pulse Response for Various Values of Load Capacitance Using ±3V Power Supplies

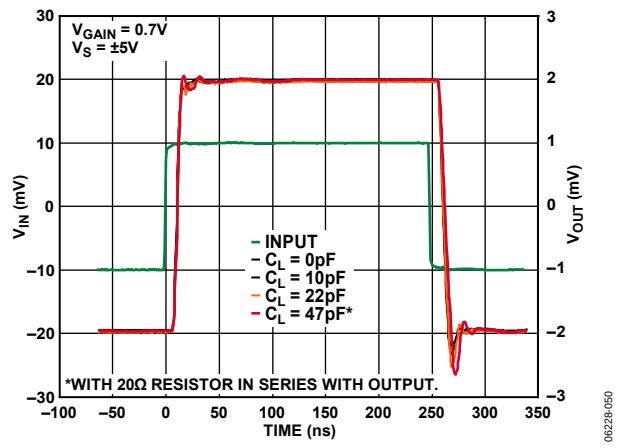


Figure 50. Large Signal Pulse Response for Various Values of Load Capacitance Using ±5V Power Supplies

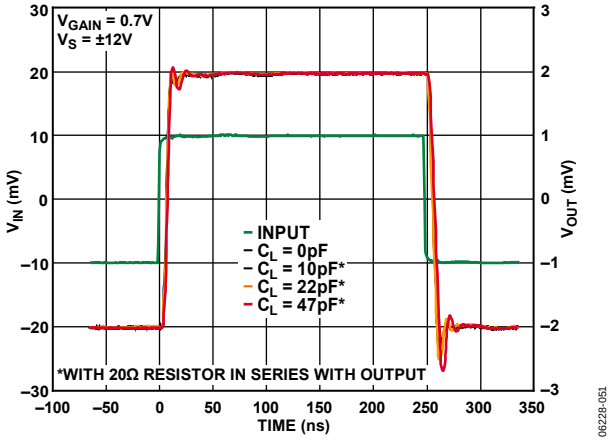


Figure 51. Large Signal Pulse Response for Various Values of Load Capacitance Using ±12V Power Supplies

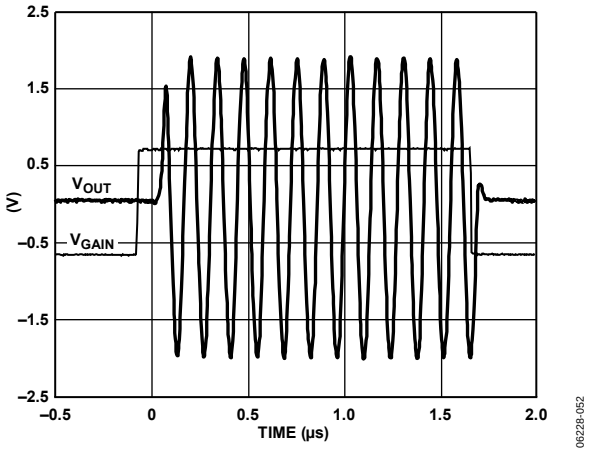


Figure 52. Gain Response

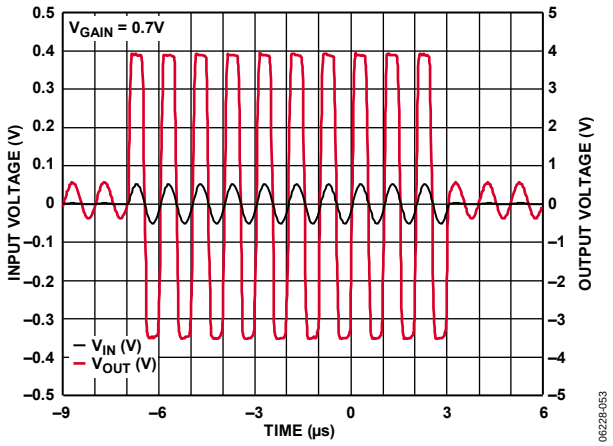


Figure 53. VGA Overdrive Recovery

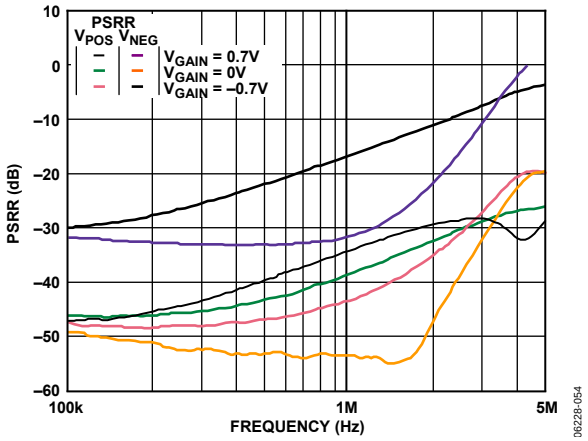


Figure 54 PSRR vs. Frequency for Three Values of V_{GAIN}

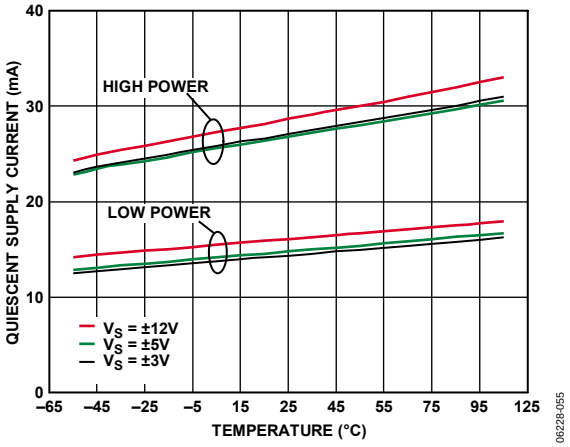


Figure 55. I_Q vs. Temperature for Three Values of Supply Voltage and High and Low Power

TEST CIRCUITS

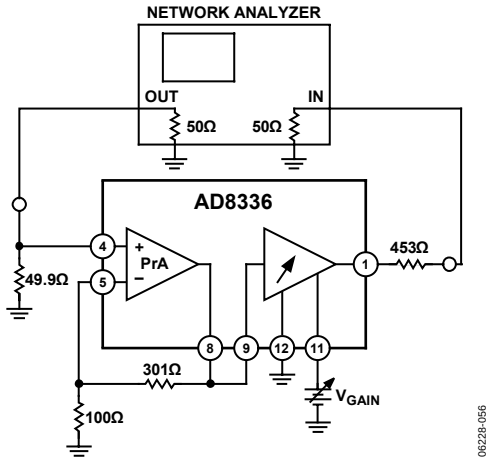


Figure 56. Gain vs. V_{GAIN} and Gain Error vs. V_{GAIN}

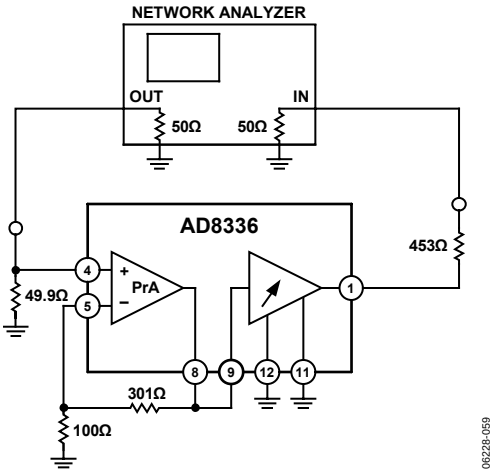


Figure 59. Group Delay

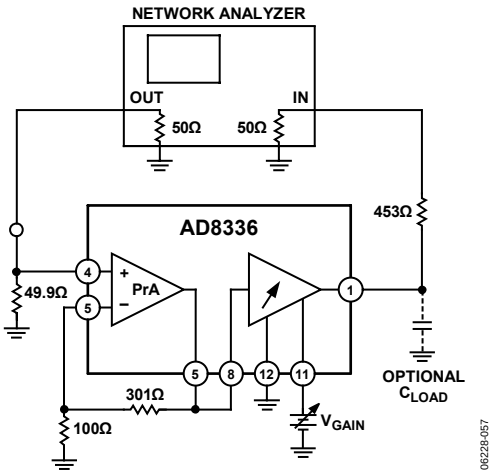


Figure 57. Frequency Response

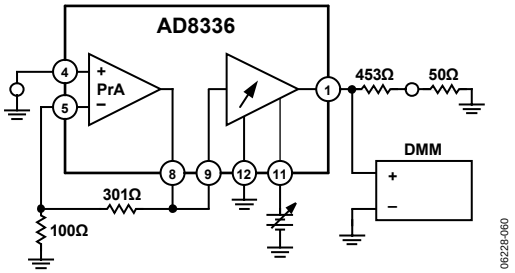


Figure 60. Offset Voltage

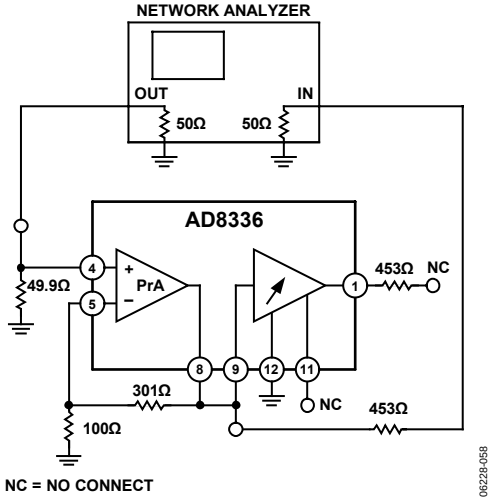


Figure 58. Frequency Response of the Preamp

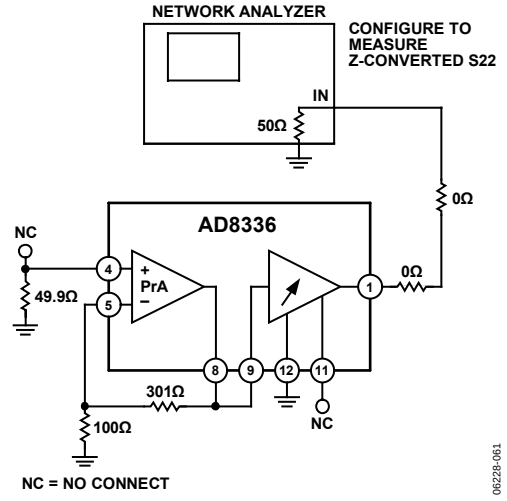


Figure 61. Output Resistance vs. Frequency

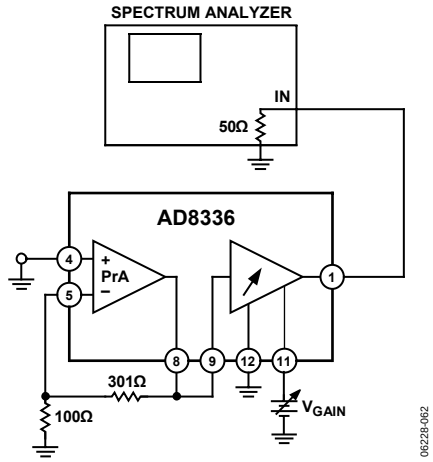


Figure 62. Input Referred Noise and Output Referred Noise

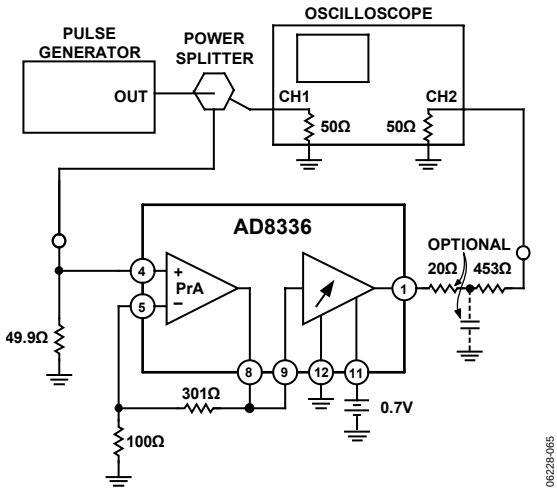


Figure 65. Pulse Response

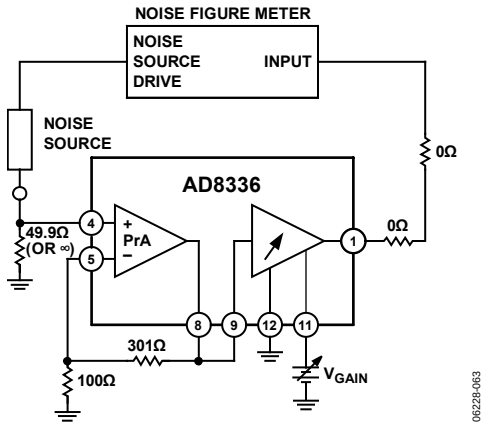


Figure 63. Noise Figure vs. V_{GAIN}

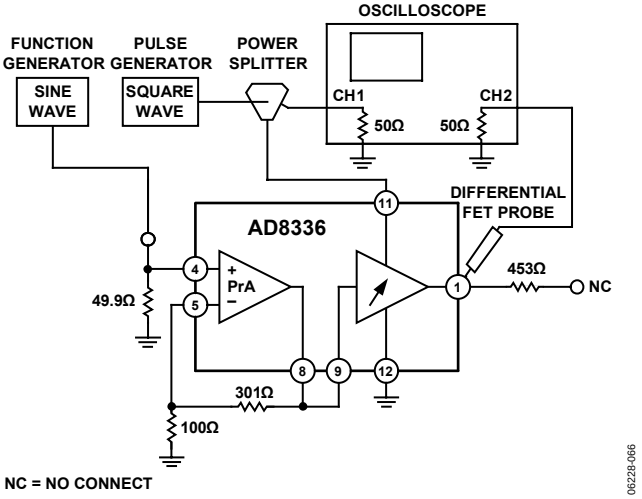


Figure 66. Gain Response

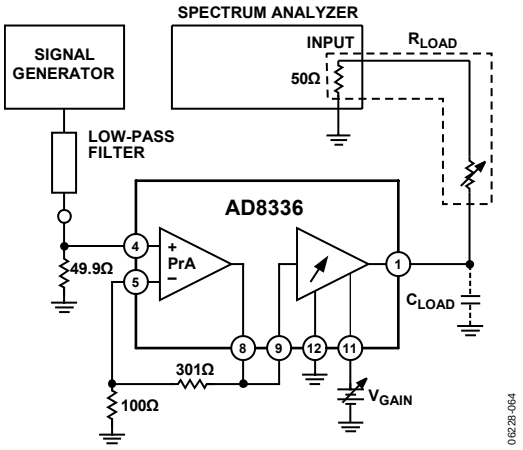


Figure 64. Harmonic Distortion

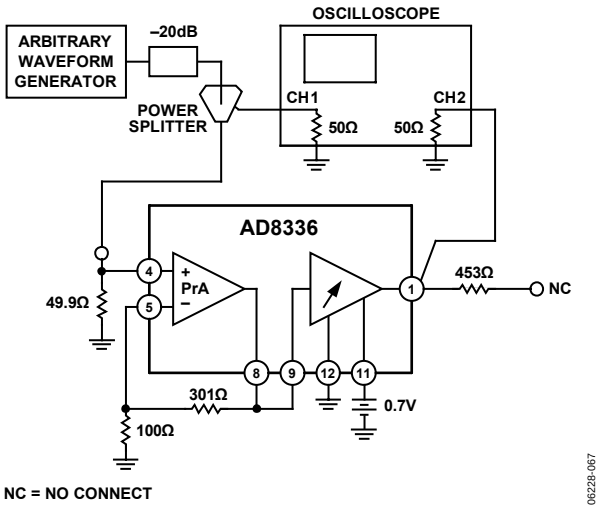


Figure 67. VGA Overdrive Recovery

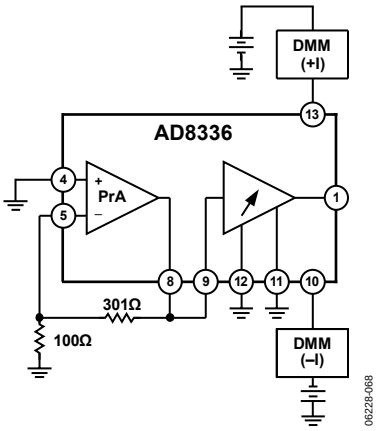


Figure 68. Supply Current

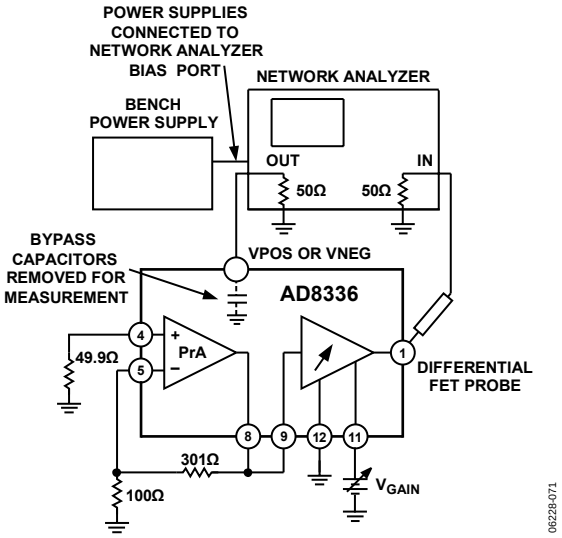


Figure 71. Power Supply Rejection Ratio

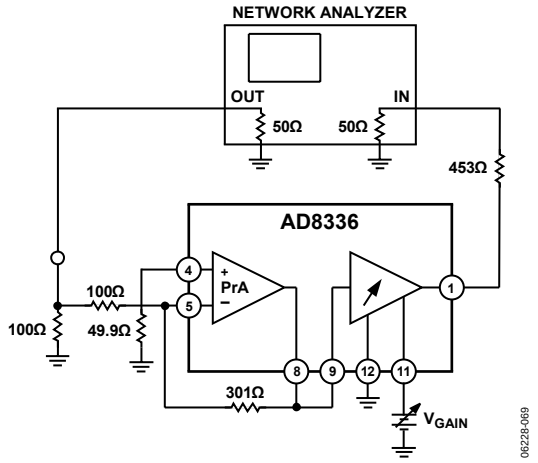


Figure 69. Frequency Response, Inverting Gain

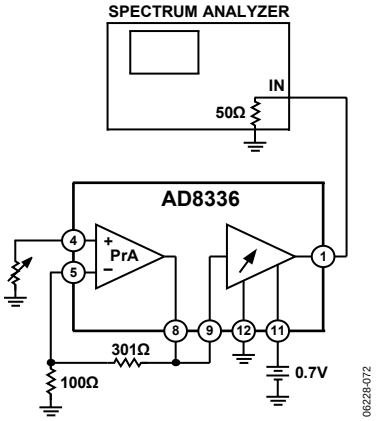


Figure 72. Input Referred Noise vs. Source Resistance

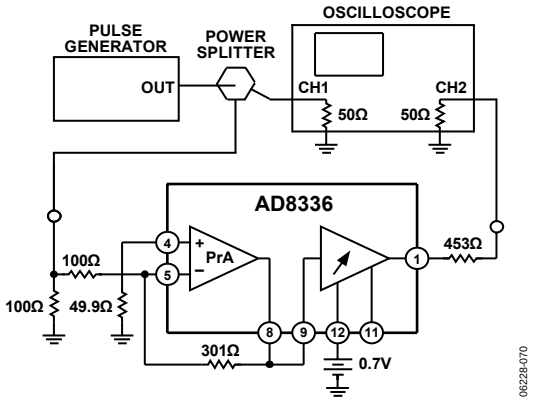


Figure 70. Pulse Response, Inverting Gain

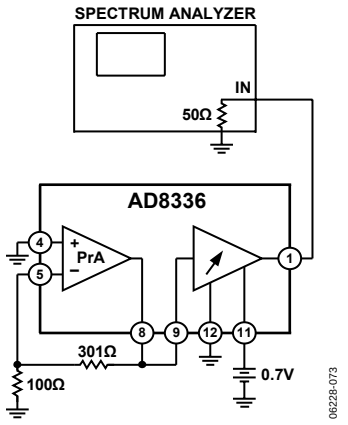


Figure 73. Short-Circuit Input Noise vs. Frequency

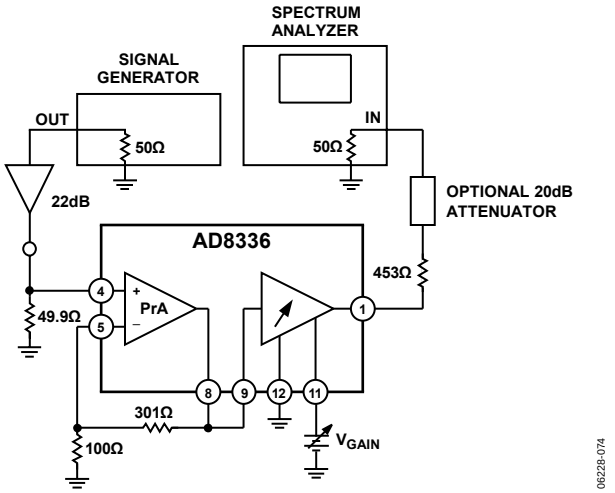


Figure 74. IP1dB vs. V_{GAIN}

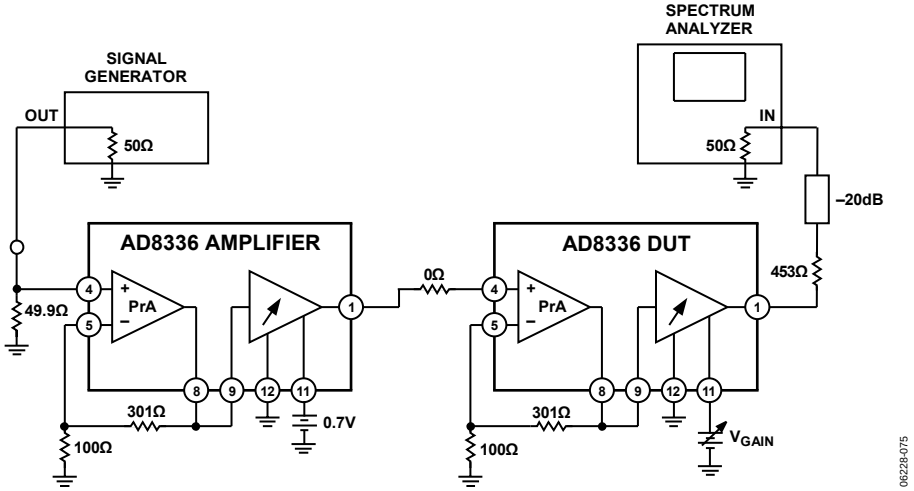


Figure 75. IP1dB vs. V_{GAIN}, High Signal Level Inputs

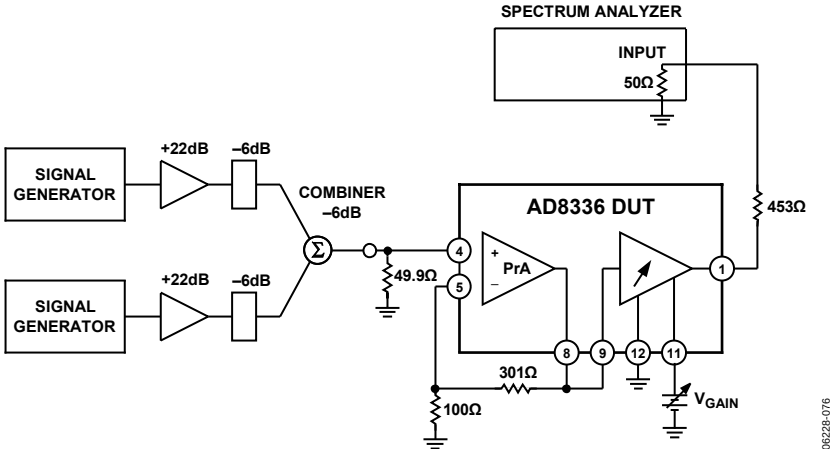


Figure 76. IMD and OIP3

THEORY OF OPERATION

OVERVIEW

The AD8336 is the first VGA designed for operation over exceptionally broad ranges of temperature and supply voltage. Its performance has been characterized from temperatures extending from −55°C to 125°C, and supply voltages from ±3 V to ±12 V. It is ideal for applications requiring dc coupling, large output voltage swings, very large gain ranges, extreme temperature variations, or a combination thereof.

The simplified block diagram is shown in Figure 77. The AD8336 includes a voltage feedback preamplifier, an amplifier with a fixed gain of 34 dB, a 60 dB attenuator, and various bias and interface circuitry. The independent voltage feedback op amp can be used in noninverting and inverting configurations, and functions as a preamplifier to the variable gain amplifier (VGA). If desired, the op amp output (PRAO) and VGA input (VGAI) pins provide for connection of an interstage filter to eliminate noise and offset. The bandwidth of the AD8336 is dc to 100 MHz with a gain range of 60 dB (−14 dB to +46 dB.)

For applications that require large supply voltages, a reduction in power is advantageous. The power reduction pin (PWRA) permits the power and bandwidth to be reduced by about half in such applications.

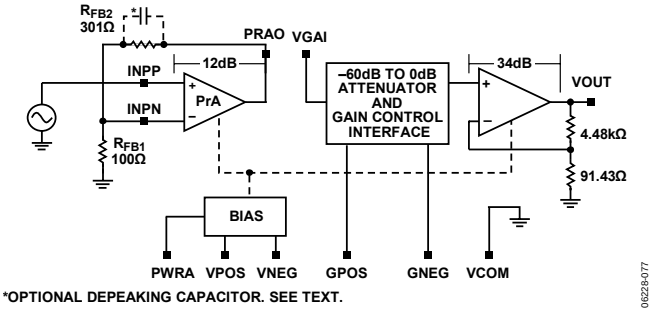


Figure 77. Simplified Block Diagram

To maintain low noise, the output stages of both the preamplifier and the VGA are capable of driving relatively small load resistances. However, at the largest supply voltages, the signal current may exceed safe operating limits for the amplifiers and the load current must not exceed 50 mA. With a ±12 V supply and ±10 V output voltage at the preamplifier or VGA output, load resistances as low as 200 Ω are acceptable.

For power supply voltages ≥ ±10 V, the maximum operating temperature range is derated to +85°C, as the power may exceed safe limits (see the Absolute Maximum Ratings section).

Since harmonic distortion products may increase for various combinations of low impedance loads and high output voltage swings, it is recommended that the user determine load and drive conditions empirically.

PREAMPLIFIER

The gain of the uncommitted voltage feedback preamplifier is set with external resistors. The combined preamplifier and VGA gain is specified in two ranges, between −14 dB to +46 dB and 0 dB to 60 dB. Since the VGA gain is fixed at 34 dB (50×), the preamp gain is adjusted for gains of 12 dB (4×) and 26 dB (200×).

With low preamplifier gains between 2× and 4×, it may be desirable to reduce the high frequency gain with a shunt capacitor across R_{FB2}, to ameliorate peaking in the frequency domain (see Figure 77). To maintain stability, the gain of the preamplifier must be 6 dB (2×) or greater.

Typical of voltage feedback amplifier configurations, the gain-bandwidth product of the AD8336 is fixed (at 400); thus, the bandwidth decreases as the gain is increased beyond the nominal gain value of 4×. For example, if the preamp gain is increased to 20×, the bandwidth reduces by a factor-of-five to about 20 MHz. The −3 dB bandwidth of the preamplifier with a gain of 4× is about 150 MHz, and for the 20× gain is about 30 MHz.

The preamp gain diminishes for an amplifier configured for inverting gain, using the same value of feedback resistors as for a noninverting amplifier, but the bandwidth remains unchanged. For example, if the noninverting gain is 4×, the inverting gain is −3×, but the bandwidth stays the same as in the noninverting gain of 4×. However, because the output referred noise of the preamplifier is the same in both cases, the input referred noise increases as the ratio of the two gain values. For the previous example, the input referred noise will increase by a factor of 4/3.

VGA

The architecture of the variable gain amplifier (VGA) section of the AD8336 is based on the Analog Devices, Inc., X-AMP (exponential amplifier), found in a wide variety of Analog Devices variable gain amplifiers. This type of VGA combines a ladder attenuator and interpolator, followed by a fixed-gain amplifier.

The gain control interface is fully differential, permitting positive or negative gain slopes. Note that the common-mode voltage of the gain control inputs increases with increasing supply.

The gain slope is 50 dB/V and the intercept is 16.4 dB when the nominal preamp gain is 4× (12 dB). The intercept changes with the preamp gain; for example, when the preamp gain is set to 20× (26 dB) the intercept becomes 30.4 dB.

Pin VGAI is connected to the input of the ladder attenuator. The ladder ratio is R/2R and the nominal resistance is 320 Ω. To reduce preamp loading and large-signal dissipation, the input resistance at Pin VGAI is 1.28 kΩ. Safe current density and power dissipation levels are maintained even when large dc signals are applied to the ladder.

The tap resistance of the resistors within the R/2R ladder is 640 Ω/3 or 213.3 Ω, the Johnson noise source of the attenuator.

SETTING THE GAIN

The overall gain of the AD8336 is the sum (in dB) or the product (magnitude) of the preamp gain and the VGA gain. The preamp gain is calculated as with any op amp, as seen in the Applications section. It is most convenient to think of the device gain in exponential terms (that is, in dB) since the VGA responds linearly-in-dB with changes in control voltage V_{GAIN} at the gain pins.

The gain equation for the VGA is

$$VGA\ Gain\ (\text{dB}) = \left[V_{GAIN}(\text{V}) \times \frac{50\ \text{dB}}{\text{V}} \right] + 4.4\ \text{dB}$$

where $V_G = V_{GPOS} - V_{GNEG}$

The gain and gain range of the VGA are both fixed at 34 dB and 60 dB, respectively; thus, the composite device gain is changed by adjusting the preamp gain. For a preamp gain of 12 dB (4×), the composite gain is −14 dB to +46 dB. Thus, the calculation for the composite gain (in dB) is

$$Composite\ Gain = G_{PRA} + [V_G(\text{V}) \times 49.9\ \text{dB/V}] + 4.4\ \text{dB}$$

For example, the midpoint gain when the preamp gain is 12 dB is

$$12\ \text{dB} + [0\ \text{V} \times 49.9\ \text{dB/V}] + 4.4\ \text{dB} = 16.4\ \text{dB}$$

Figure 3 is a plot of gain in dB vs. V_{GAIN} in mV, when the preamp gain is 12 dB (4×). Note that the computed result closely matches the plot of actual gain.

In Figure 3, the gain slope flattens at the limits of the V_G input. The gain response is linear-in-dB over the center 80% of the control range of the device. Figure 78 shows the ideal gain characteristics for the VGA stage and composite VGA + preamp.

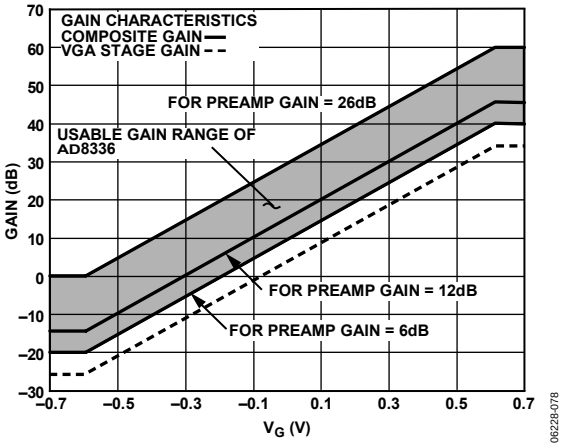


Figure 78. Ideal Gain Characteristics of the AD8336

NOISE

The noise of the AD8336 is dependent on the value of the VGA gain. At maximum V_{GAIN}, the dominant noise source is the preamp but shifts to the VGA as V_{GAIN} diminishes.

The input referred noise at the highest VGA gain and a preamp gain of 4×, with R_{FB1} =100 Ω and R_{FB2} = 301 Ω, is 3 nV/√Hz, and determined by the preamp and its gain setting resistors. See Table 4 for the noise components for the preamp.

Table 4. AD8336 Noise Components for Preamp Gain = 4×

Noise Component	Noise Voltage (nV/√Hz)
Op Amp (Gain = 4×)	2.6
R_{FB1} = 100 Ω	0.96
R_{FB2} = 301 Ω	0.55
VGA	0.77

Using the listed values, the total noise of the AD8336 is slightly less than 3 nV/√Hz, referred to the input. Although the output noise VGA is 3.1 nV/√Hz, the input referred noise is 0.77 nV/√Hz when divided by the preamplifier gain of 4×

At other than maximum gain, the noise of the VGA is determined from the output noise. The noise in the center of the gain range is about 150 nV/√Hz. Since the gain of the fixed gain amplifier that is part of the VGA is 50×, the VGA input referred noise is approximately 3 nV/√Hz, the same value as the preamp and VGA combined. This is expected since the input referred noise is the same at the input of the attenuator at maximum gain. However, the noise referred to the VGAI pin (the preamp output) increases by the amount of attenuation through the ladder network. The noise at any point along the ladder network is primarily comprised of the ladder resistance noise, the noise of the input devices, and the feedback resistor network noise. The ladder network and the input devices are the largest noise sources.

At minimum gain, the output noise increases slightly to about 180 nV/√Hz because of the finite structure of the X-AMP.

OFFSET VOLTAGE

Extensive cancellation circuitry included in the variable gain amplifier section minimizes locally generated offset voltages. However when operated at very large values of gain, dc voltage errors at the output can still result from small dc input voltages. When configured for the nominal gain range of −14 dB to 46 dB, the maximum gain is 200× and an offset of only 100 µV at the input generates 20 mV at the output.

The primary source for dc offset errors is the preamplifier; ac coupling between the PRAO and VGAI pins is the simplest solution. In applications where dc coupling is essential, a compensating current can be injected at the INPN input (Pin 5) to cancel preamp offset. The direction of the compensating current depends on the polarity of the offset voltage.

APPLICATIONS

AMPLIFIER CONFIGURATION

The AD8336 amplifiers can be configured in various options. In addition to the 60 dB gain range variable gain stage, an uncommitted voltage gain amplifier is available to the user as a preamplifier. The preamplifier connections are separate to enable noninverting or inverting gain configurations or the use of interstage filtering. The AD8336 can be used as a cascade connected VGA with preamp input, as a standalone VGA, or as a standalone preamplifier. This section describes some of the possible applications.

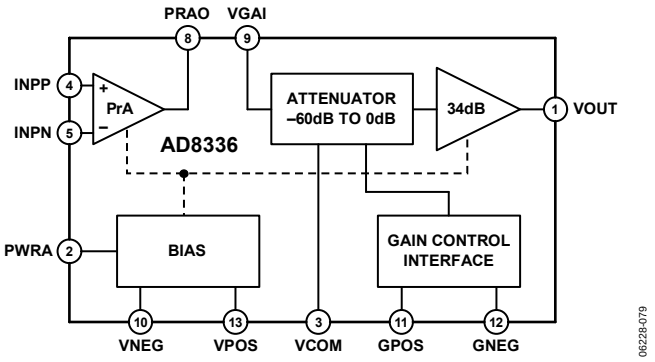


Figure 79. Application Block Diagram

PREAMPLIFIER

While observing just a few constraints, the uncommitted voltage feedback preamplifier of the AD8336 can be connected in a variety of standard high frequency op amp configurations. The amplifier is optimized for a gain of 4×, (12 dB) and has a gain bandwidth product of 600 MHz. At a gain of 4×, the bandwidth is 150 MHz. The preamplifier gain can be adjusted to a minimum gain of 2×; however, there will be a small peak in the response at high frequencies. At higher preamplifier gains, the bandwidth diminishes proportionally in conformance to the classical voltage gain amplifier GBW relationship.

While setting the overall gain of the AD8336, the user needs to consider the input referred offset voltage of the preamplifier. Although the offset of the attenuator and postamplifier are almost negligible, the preamplifier offset voltage, if uncorrected, is increased by the combined gain of the preamplifier and postamplifier. Thus for a maximum gain of 60 dB, an input offset voltage of only 200 µV results in an error of 200 mV at the output.

Circuit Configuration for Noninverting Gain

The noninverting configuration is shown in Figure 80. The preamp gain is described by the classical op amp gain equation

$$Gain = \frac{R_{FB2}}{R_{FB1}} + 1$$

The practical gain limits for this amplifier are 6 dB to 26 dB. The gain bandwidth product is about 600 MHz, so that at 150 MHz, the maximum achievable gain is 12 dB (4×). The minimum gain is established internally by fixed loop compensation, and is 6 dB (2×). This amplifier is not designed for unity gain operation. Table 5 shows the gain bandwidth for the noninverting gain configuration.

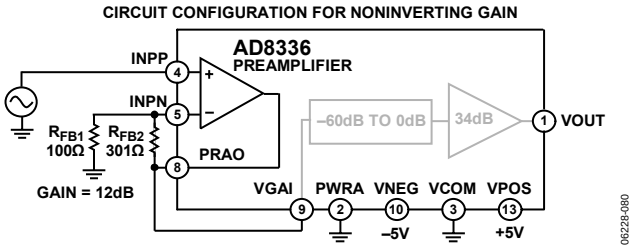


Figure 80. Circuit Configuration for Noninverting Gain

The preamplifier output reliably sources and sinks currents up to 50 mA. When using ±5 V power supplies, the suggested sum of the output resistor values is 400 Ω total for the optimal trade-off between distortion and noise. Much of the low gain value device characterization was performed with resistor values of 301 Ω and 100 Ω, resulting in a preamplifier gain of 12 dB (4×). With supply voltages between ±5 V and ±12 V, the sum of the output resistance should be increased accordingly and a total resistance of 1 kΩ is recommended. Larger resistance values, subject to a trade-off in higher noise performance, can be used if circuit power and load driving is an issue. When considering the total power dissipation, remember that the input ladder resistance of the VGA is part of the preamp load.

Table 5. Gain vs. Bandwidth for Noninverting Preamplifier Configuration.

Preamp Gain		Preamp BW (MHz)	Composite Gain (dB)
Numerical	dB		
4×	12	150	−14 to +46
8×	18	60	−8 to +52
16×	24	30	−2 to +58
20×	26	25	0 to 60

Circuit Configuration for Inverting Gain

The preamplifier can also be used in an inverting configuration, as shown in Figure 81.

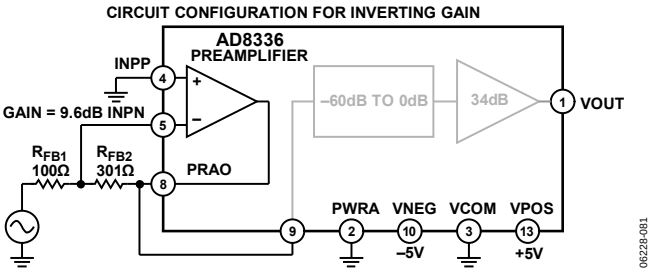


Figure 81. Circuit Configuration for Inverting Gain

The same considerations regarding total resistance vs. distortion, noise, and power as noted in the noninverting case apply, except that the amplifier can be operated at unity inverting gain. The signal gain is reduced while the noise gain is the same as for the noninverting configuration:

$$Signal\ Gain = \frac{R_{FB2}}{R_{FB1}}$$

and

$$Noise\ Gain = \frac{R_{FB2}}{R_{FB1}} + 1$$

USING THE POWER ADJUST FEATURE

The AD8336 has the provision to operate at lower power with a trade-off in bandwidth. The power reduction applies to the preamp and the VGA sections, and the bandwidth is reduced equally between them. Reducing the power is particularly useful when operating with higher supply voltages and lower values of output loading that would otherwise stress the output amplifiers. When Pin PWRA is grounded, the amplifiers operate in their default mode, and the combined 3 dB bandwidth is 80 MHz with the preamp gain adjusted to 4×. When the voltage on Pin PWRA is between 1.2 V and 5 V, the power is reduced by approximately half and the 3 dB bandwidth reduces to approximately 35 MHz. The voltage at pin PWRA must not exceed 5 V.

DRIVING CAPACITIVE LOADS

The output stages of the AD8336 are stable with capacitive loads up to 47 pF for a supply voltage of ±3 V, and capacitive loads up to 10 pF for supply voltages up to ±8 V. For larger combined values of load capacitance and/or supply voltage, a 20 Ω series resistor is recommended for stability.

The influence of capacitance and supply voltage are shown in, Figure 50 and Figure 51, where representative combinations of load capacitance and supply voltage requiring a 20 Ω resistor are marked with an asterisk. No resistor is required for the ±3 V plots in Figure 49, while a resistor is required for most of the ±12 V plots in Figure 51.

EVALUATION BOARD

An evaluation board, AD8336-EVALZ, is available online for the AD8336. Figure 82 is a photo of the board.

The board is shipped from the factory, configured for a preamp gain of 4×. To change the value of the gain of the preamp or the gain polarity to inverting is a matter of changing component values, or installing components in alternate locations provided. All components are standard 0603 size, and the board is designed for RoHS compliancy. Figure 83 shows the locations of components provided for changing the amplifier configuration to inverting gain. Simply install the components shown in red and remove those in gray.

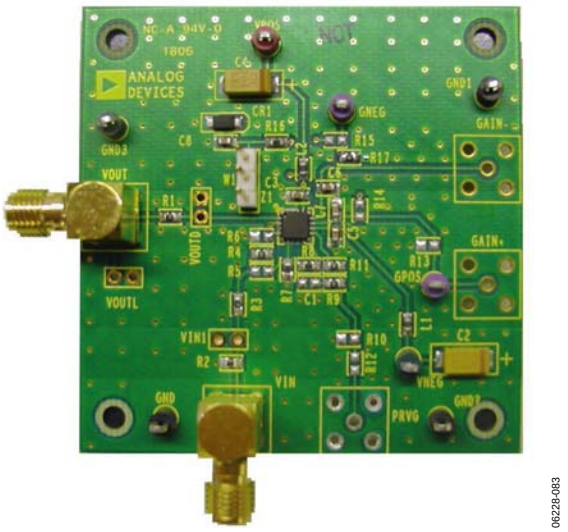


Figure 82. AD8336 Evaluation Board

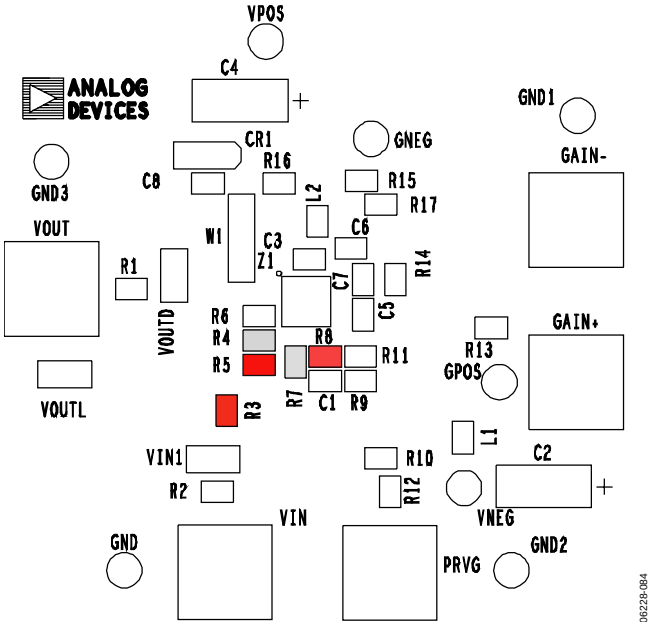


Figure 83. Components for Inverting Gain Operation

OPTIONAL CIRCUITRY

The AD8336 features differential inputs for the gain control, permitting nonzero or floating gain control inputs. In order to avoid any delay in making the board operational, the gain input circuit is shipped with Pin GNEG connected to ground via a 0 Ω resistor in location R17. The user can simply adjust the gain of the device by driving the GPOS test loop with a power supply or voltage reference. Resistor networks are provided for fixed gain bias voltages at Pin GNEG and Pin GPOS for common-mode voltages other than 0 V. If it is desired to drive the gain control with an active input such as a ramp, SMA connectors can be installed in the locations GAIN− and GAIN+. Provision is made for an optional SMA connector at PRVG for monitoring the preamp output or driving the VGA from an external source. Remove the 0 Ω resistor at R9 to isolate the preamp from an external generator.

BOARD LAYOUT CONSIDERATIONS

The evaluation board uses four layers, with power and ground planes located between two conductor layers. This arrangement is highly recommended for customers and several views of the board are provided as reference for board layout details. When laying out a printed circuit board for the AD8336, remember to provide a pad beneath the device to solder the exposed pad of the matching device. The pad in the board should have at least five vias in order to provide a thermal path for the chip scale package. Unlike leaded devices, the thermal pad is the primary means to remove heat dissipated within the device.

Table 6 is a bill of materials for the evaluation board.

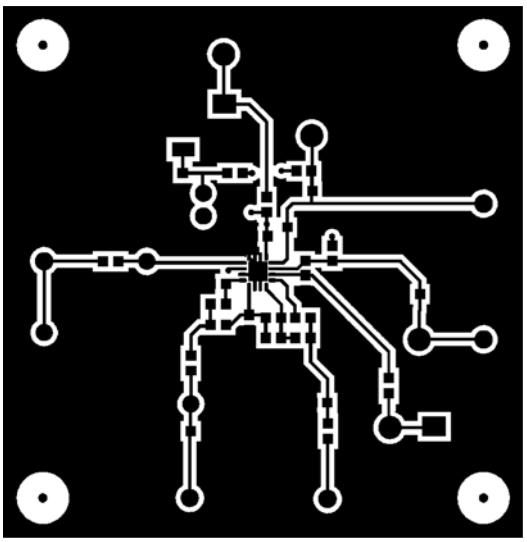


Figure 84. Component Side Copper

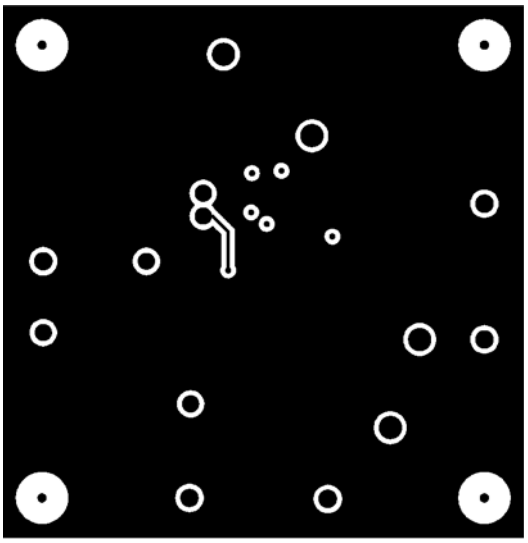


Figure 85. Secondary Side Copper

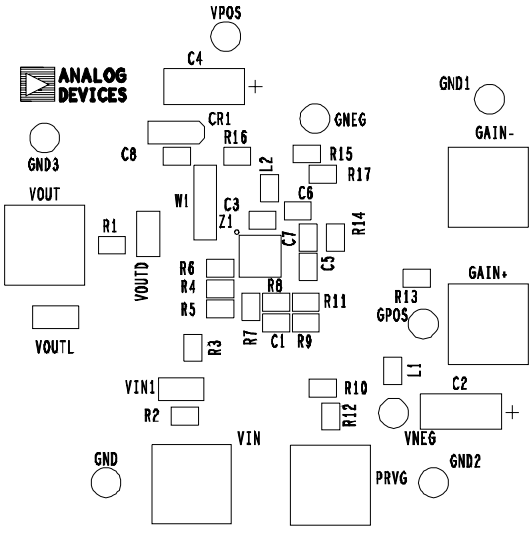


Figure 86. Component Side Silk Screen

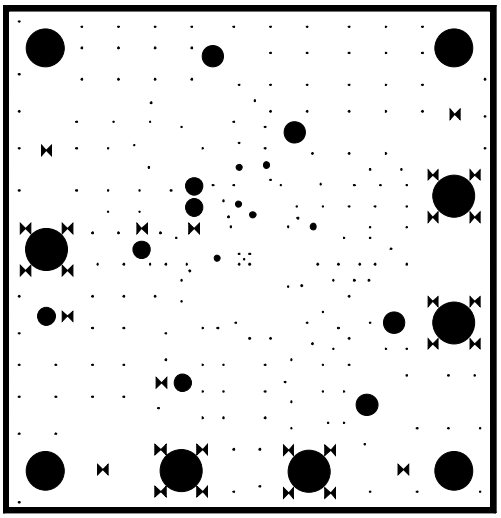


Figure 87. Internal Ground Plane

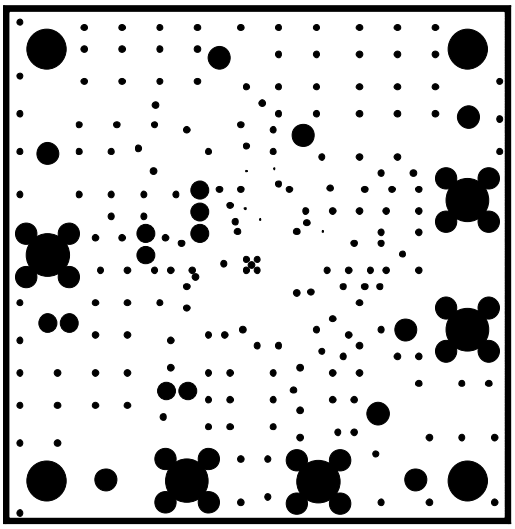


Figure 88. Internal Power Plane

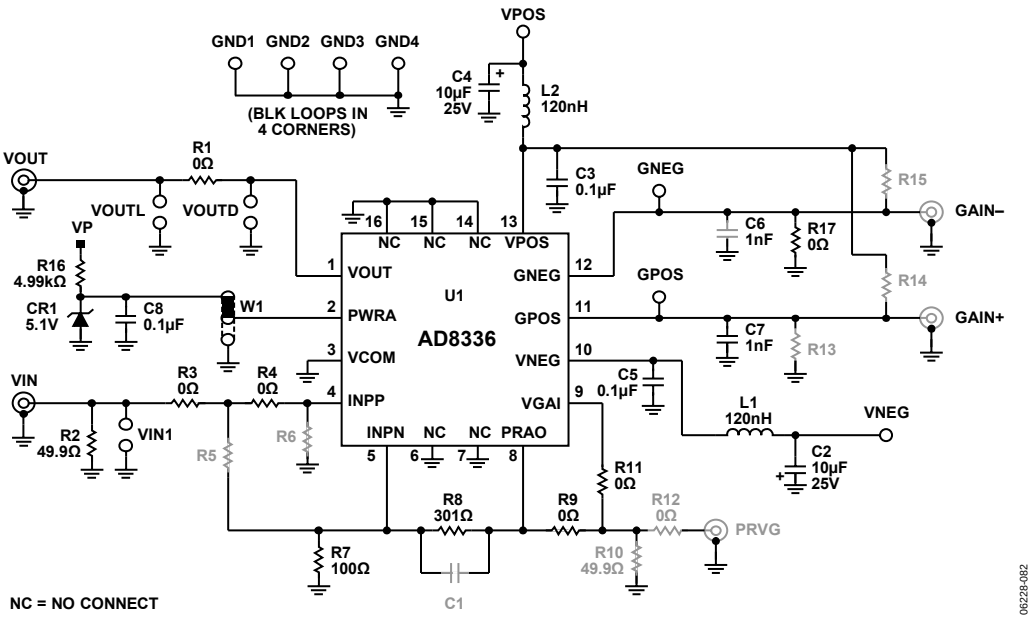
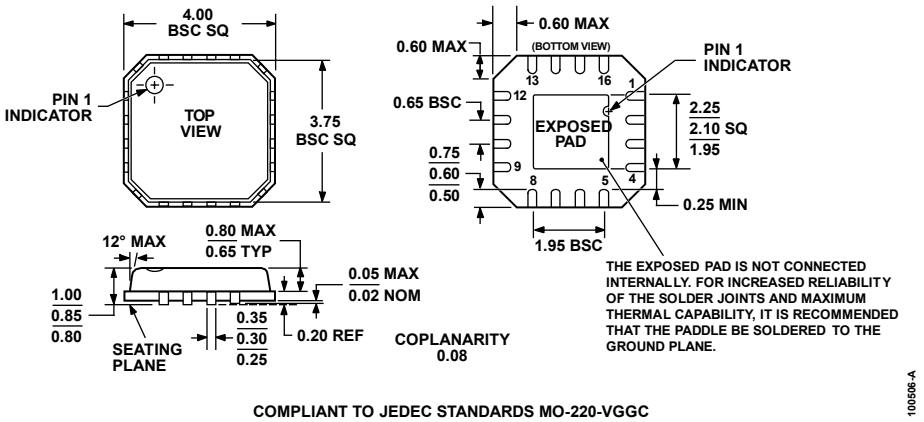


Figure 89. AD8336-EVALZ Schematic Shown as Shipped, Configured for a Noninverting Gain of 4×

Table 6. AD8336 Evaluation Board Bill of Materials

Qty	Name	Description	Reference Designator	Manufacturer	Mfg. Part Number
2	Capacitor	Tantalum 10 µF, 25 V	C2, C4	Nichicon	F931E106MCCC
3	Capacitor	0.1 µF, 16 V, 0603, X7R	C3, C5, C8	KEMET	C0603C104K4RSCTU
1	Capacitor	1 nF, 50 V, 0603, X7R	C7	Panasonic	ECJ-1VB2A102K
1	Diode	Zener, 5.1 V, 1 W	CR1	Diodes, Inc.	DFLZ5V1-7
2	Connector	SMA Fem, RA, PC Mt	VIN, VOUT	Amphenol	901-143-6RFX
4	Test Loop	Black	GND, GND1, GND2, GND3	Components Corporation	TP-104-01-00
2	Test Loop	Violet	GNEG, GPOS	Components Corporation	TP-104-01-07
2	Inductor	Ferrite Bead	L1, L2	Murata	BLM18BA750SN1D
6	Resistor	0 Ω, 5%, 0603	R1, R3, R4, R9, R11, R17	Panasonic	ERJ-2GE0R00X
1	Resistor	49.9 Ω 1% 1/16 W 0603	R2	Panasonic	ERJ-3EKF49R9V
1	Resistor	100 Ω 1% 1/16 W 0603	R7	Panasonic	ERJ-3EKF1000V
1	Resistor	301 Ω 1/16 W 1% 0603	R8	Panasonic	ERJ-3EKF3010V
1	Resistor	4.99 kΩ 1/16 W 1% 0603	R16	Panasonic	ERJ-3EKF4991V
1	Test Loop	Green	VNEG	Components Corporation	TP-104-01-05
1	Test Loop	Red	VPOS	Components Corporation	TP-104-01-02
1	Header	0.1″ Center	W1	Molex	22-10-2031
1	Integrated Circuit	VGA	Z1	Analog Devices	AD8336ACPZ
4	Rubber Bumper	Foot	NA	3M	SJ67A11

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

Figure 90. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8336ACPZ[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4
AD8336ACPZ-R7[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4
AD8336ACPZ-RL[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4
AD8336ACPZ-WP[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4
AD8336-EVALZ[1]		Evaluation Board	

[1] Z = Pb-free part.

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