FINAL

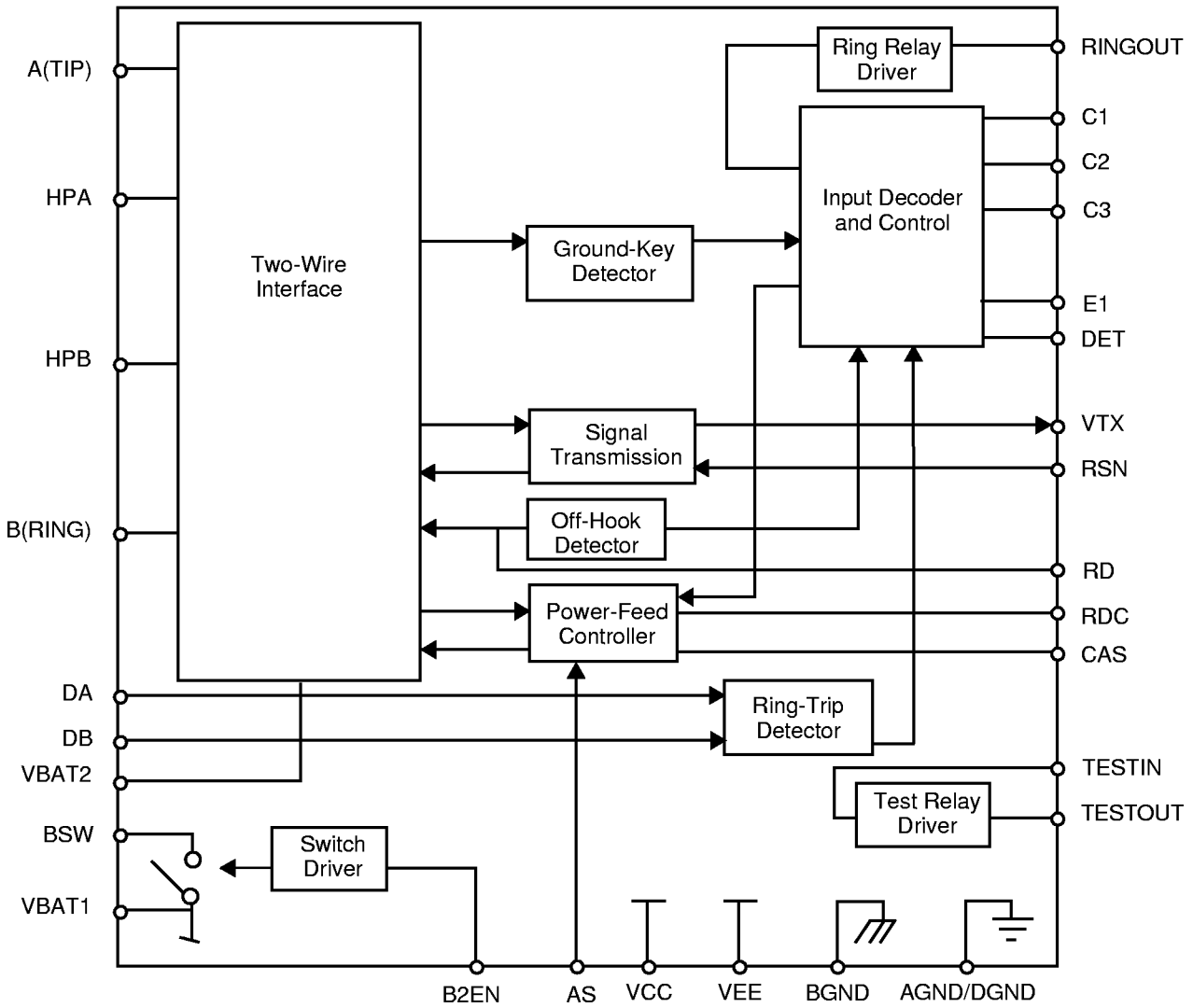
Am7949

Subscriber Line Interface Circuit

DISTINCTIVE CHARACTERISTICS

- Ideal for Fiber-In-The-Loop (FITL) applications
- Low standby power
- –21 V to –58 V battery operation
- On-chip battery switching and feed selection
- On-hook transmission
- Two-wire impedance set by single external impedance
- Programmable constant-current feed
- Current gain = 200
- Programmable loop-detect threshold
- Ground-key detector
- Tip Open state for ground-start lines
- Polarity reversal option
- On-chip ring relay driver and relay snubber circuit

BLOCK DIAGRAM



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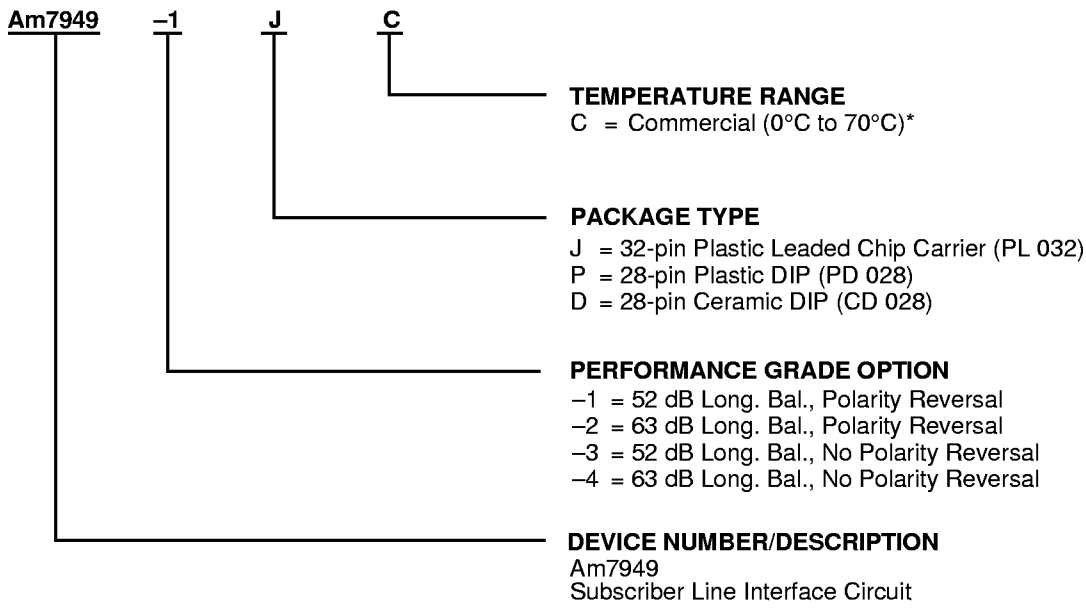
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
Am7949	–1 –2 –3 –4	JC PC DC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

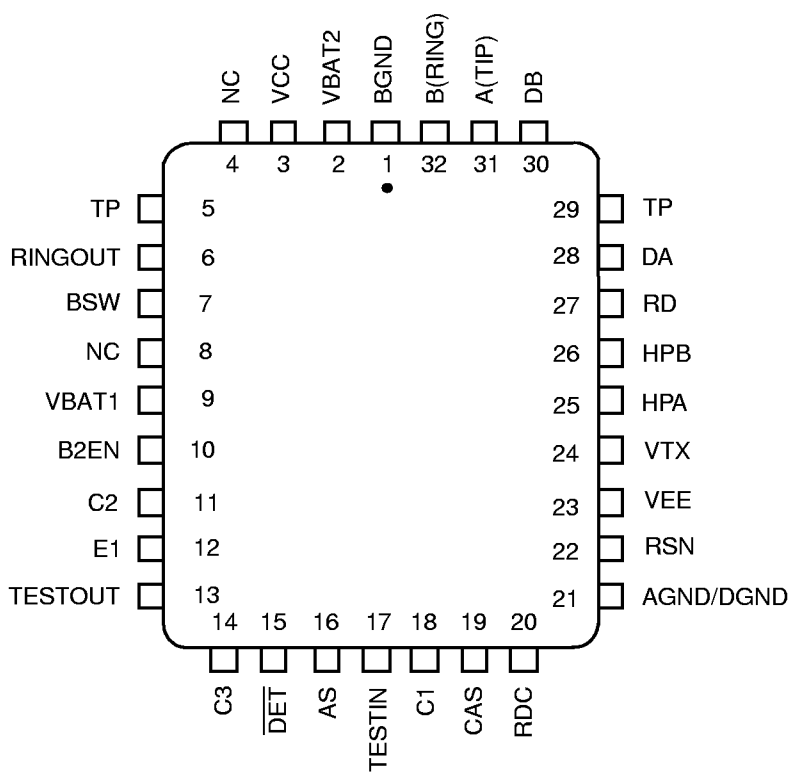
Note:

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

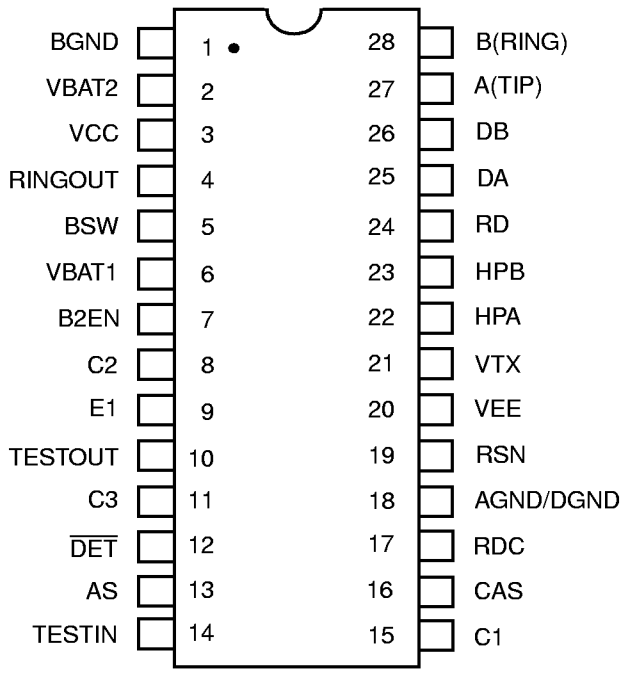
CONNECTION DIAGRAMS

Top View

32-Pin PLCC



28-Pin Plastic or Ceramic DIP



Notes:

1. *Pin 1 is marked for orientation.*
2. *TP is a thermal conduction pin tied to substrate.*
3. *NC = No Connect*

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Gnd	Analog and Digital ground.
AS	Input	Anti-saturation state select. Logic Low enables battery independent feed. Logic High enables battery tracking anti-sat. TTL compatible.
A(TIP)	Output	Output of A(TIP) power amplifier.
B2EN	Input	VBAT2 Enable. Logic Low enables low power operation from VBAT2. Logic High enables operation from VBAT1. TTL compatible.
BGND	Gnd	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
BSW	Battery Switch	Collector of battery switch.
C3–C1	Inputs	Decoder. SLIC control pins. C3 is MSB and C1 is LSB. TTL compatible.
CAS	Capacitor	Anti-saturation capacitor; Pin for capacitor to filter reference voltage when operating in anti-saturation region.
DA	Input	Ring-Trip Negative; Negative input to ring-trip comparator.
DB	Input	Ring-Trip Positive; Positive input to ring-trip comparator.
DET	Output	Switchhook Detector; A logic Low indicates that selected condition is detected. The detect condition is selected by the logic inputs (C3–C1, E1). The output is open-collector with a built-in 15 kΩ pull-up resistor.
E1	Input	Ground-key enable. A logic High selects the off-hook detector. A logic Low selects the ground key. TTL compatible.
HPA	Capacitor	High-pass filter capacitor; A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-pass filter capacitor; B(RING) side of high-pass filter capacitor.
NC	—	Pin not internally connected.
RD	Resistor	Detect resistor; Detector threshold set and filter pin.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network, which also connects to the receiver summing node (RSN). The sign of V_{RDC} is negative for normal polarity and positive for reverse polarity.
RINGOUT	Output	Ring relay driver; open-collector driver, emitter internally connected to BGND.
RSN	Input	Receive summing node; The metallic current (both AC and DC) between A(TIP) and B(RING) = 200 times the current into this pin. The networks that program receive gain, two-wire impedance, and feed resistance all connect to this node.
TESTIN	Input	Test relay driver input.
TESTOUT	Output	Open collector driver with emitter internally connected to AGND.
TP	Thermal	Thermal pin. Connection for heat dissipation. Internally connected to substrate (VBAT). Leave as open circuit or connected to VBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation
VBAT1	Battery	Battery supply and connection to substrate.
VBAT2	Battery	Power supply to output amplifiers. Connect externally to BSW. Connect to off-hook battery through a diode.
VCC	Power	+5 V power supply.
VEE	Power	–5 V power supply.
VTX	Output	Transmit Audio; Unity gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature . . . . . –55°C to +150°C

V_{CC} with respect to AGND/DGND . . . –0.4 V to +7.0 V

V_{EE} with respect to AGND/DGND . . . +0.4 V to –7.0 V

V_{BAT2} with respect to V_{BAT1} . . . . . V_{BAT1} to GND

V_{BAT1} with respect to AGND/DGND:
- Continuous . . . . . +0.4 V to –70 V
- 10 ms . . . . . +0.4 V to –75 V

BGND with respect to AGND/DGND . . . . +3 V to –3 V

A(TIP) or B(RING) to BGND:
- Continuous . . . . . –70 V to +1 V
- 10 ms (f = 0.1 Hz) . . . . . –70 V to +5 V
- 1 µs (f = 0.1 Hz) . . . . . –80 V to +8 V
- 250 ns (f = 0.1 Hz) . . . . . –90 V to +12 V

Current from A(TIP) or B(RING) . . . . . ±150 mA

RINGOUT current . . . . . 50 mA

RINGOUT voltage . . . . . BGND to +7 V

RINGOUT transient . . . . . BGND to +10 V

DA and DB inputs
- Voltage on ring-trip inputs . . . . . V_{BAT} to 0 V
- Current into ring-trip inputs . . . . . ±10 mA

C3–C1, E1, AS, B2EN
- Input voltage . . . . . –0.4 V to V_{CC} + 0.4 V

Maximum power dissipation, continuous, T_A = 85°C, No heat sink (See note):
- In 32-pin PLCC package . . . . . 1.4 W
- In 28-pin ceramic DIP package . . . . . 2.07 W
- In 28-pin plastic DIP package . . . . . 1.13 W

Thermal Data . . . . . θ_{JA}
- In 32-pin PLCC package . . . . . 43°C/W typ
- In 28-pin ceramic DIP package . . . . . 30°C/W typ
- In 28-pin plastic DIP package . . . . . 53°C/W typ

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature . . . . . 0°C to +70°C*

V_{CC} . . . . . 4.75 V to 5.25 V

V_{EE} . . . . . –4.75 V to –5.25 V

V_{BAT1} . . . . . –40.5 V to –58 V

V_{BAT2} . . . . . –21 V to V_{BAT1}

AGND/DGND . . . . . 0 V

BGND with respect to AGND/DGND . . . . . –100 mV to +100 mV

Load resistance on VTX to ground . . . . . 10 kΩ min

Operating Ranges define those limits between which device functionality is guaranteed.

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Transmission Performance						
2-wire return loss	200 Hz to 3.4 kHz (Test Circuit D)	26			dB	1, 4, 7
Z_{VTX}, Analog output impedance			3	20	Ω	4
V_{VTX}, Analog output offset voltage	0°C to +70°C –40°C to +85°C	–35 –40		+35 +40	mV	— 4
Z_{RSN}, Analog input impedance			1	20	Ω	4
Overload level, 2-wire and 4-wire	Active state	2.5			Vpk	2a
Overload level	On-hook, R_L = 600 Ω	0.88			Vrms	2b
THD (Total Harmonic Distortion)	+3 dBm, BAT2 = –24 V		–64	–50	dB	
THD, on-hook	0 dBm, R_L = 600 Ω, BAT1 = –57.5 V			–35.5		5 —
Longitudinal Performance (See Test Circuit D)						
Longitudinal to metallic L-T, L-4	200 Hz to 1 kHz –1, –3* normal polarity 0°C to +70°C –2, –4 normal polarity –40°C to +85°C –2, –4 reverse polarity –2, –4	52 63 58 54			dB	— — 4 —
	1 kHz to 3.4 kHz –1, –3* normal polarity 0°C to +70°C –2, –4 normal polarity –40°C to +85°C –2, –4 reverse polarity –2, –4	52 58 54 54			dB	— — 4 —
Longitudinal signal generation 4-L	200 Hz to 800 Hz normal polarity	42				
Longitudinal current per pin (A or B)	Active or OHT state	12	18		mArms	
Longitudinal impedance at A or B	0 to 100 Hz			35	Ω/pin	
Idle Channel Noise						
C-message weighted noise	R_L = 300 Ω DC 0°C to +70°C R_L = 300 Ω DC –40°C to +85°C		+7	+10 +12	dBrnC	— 4
Psophometric weighted noise	R_L = 300 Ω DC 0°C to +70°C R_L = 300 Ω DC –40°C to +85°C		–83	–80 –78	dBmp	— 4
Insertion Loss and Balance Return Signal (2- to 4-Wire, 4- to 2-Wire, and 4- to 4-Wire, See Test Circuits A and B)						
Gain accuracy over temperature	0 dBm, 1 kHz 0°C to +70°C –40°C to +85°C	–0.15 –0.20	0 0	+0.15 +0.20	dB	— 4
Gain accuracy over frequency	300 to 3400 Hz 0°C to +70°C relative to 1 kHz –40°C to +85°C	–0.10 –0.15		+0.10 +0.15		— 4
Gain tracking	+3 dBm to –55 dBm 0°C to +70°C relative to 0 dBm –40°C to +85°C	–0.10 –0.15		+0.10 +0.15		— 4
Gain accuracy, OHT state		–0.5		+0.5		4
Group delay	0 dBm, 1 kHz			3	µs	1, 4, 7

Note:
**P.G. = Performance Grade*

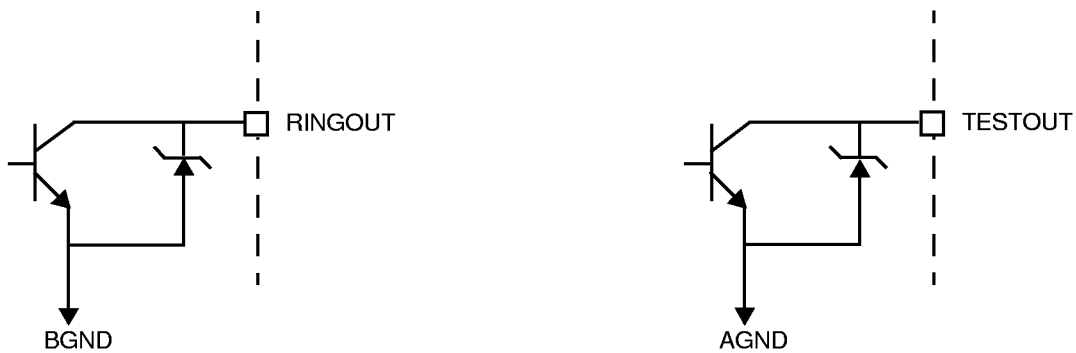
ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Line Characteristics						
I_L, Loop current accuracy	I_L in constant-current region	$0.915I_L$	I_L	$1.085I_L$	mA	
I_L, Long loops, Active or OHT state	R_{LDC} = 600 Ω	20	21.7			
I_L, Accuracy, Standby state	$I_L = \frac{\lvert V_{BAT}\rvert - 3\ V}{R_L + 1800}$ T_A = 25°C	$0.7I_L$	I_L	$1.3I_L$		
	R_L = 600 Ω	15	17.4			
I_LLIM	Active, A and B to GND OHT, A and B to GND		50 50	80		4
I_L, Loop current, Open Circuit state	R_L = 0			100	µA	
I_A, pin A leakage, Tip Open state	R_L = 0			100		
I_B, pin B current, Tip Open state	B to GND B to V_{BAT1} + 6 V		30 30		mA	
V_A, Active, ground-start signaling	A to –48 V = 7 kΩ, B to GND = 100 Ω	–7.5	–5			4
V_{AB}, Open Circuit voltage	V_{BAT1} = –51.6 V	42.8			V	
Power Supply Rejection Ratio (V_{RIPPLE} = 100 mVrms), Active Normal State						
V_{CC} V_{EE} V_{BAT}	50 Hz to 3400 Hz 50 Hz to 3400 Hz 50 Hz to 3400 Hz	33 29 30	40 35 50		dB	5
Effective internal resistance	CAS pin to GND	85	170	255	kΩ	4
Power Dissipation						
On-hook, Open Circuit state	AS & B2EN = logic high		35	70	mW	
On-hook, Standby state	AS & B2EN = logic high		45	85		
On-hook, OHT state	AS & B2EN = logic high		120	220		
On-hook, Active state	AS & B2EN = logic high		160	230		
Off-hook, Standby state	AS & B2EN = logic low, R_L = 600 Ω		860	1100		
Off-hook, OHT state	AS & B2EN = logic low, R_L = 300 Ω		500	700		
Off-hook, Active state	AS & B2EN = logic low, R_L = 300 Ω		500	700		
Supply Currents, Battery = –58 V						
I_{CC}, On-hook V_{CC} supply current	Open Circuit state OHT state Standby state Active state, BAT1 = –50 V		2.0 5.3 2.3 5.5	3.0 7.5 3.5 8.0	mA	
I_{EE}, On-hook V_{EE} supply current	Open Circuit state OHT state Standby state Active state, BAT1 = –50 V		0.82 2.0 1.1 2.0	2.0 3.5 2.0 4.0		
I_{BAT}, On-hook V_{BAT} supply current	Open Circuit state OHT state Standby state Active state, BAT1 = –50 V		0.45 2.2 0.8 2.8	1.0 4.0 2.0 4.0		

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
RFI Rejection						
RFI rejection	100 kHz to 30 MHz (See Figure E)			1.0	mVrms	4
Logic Inputs (C3–C1, E1, AS, and B2EN)						
V_{IH}, Input High voltage	C3–C1, E1, AS, B2EN TESTIN, I_{IH} = 300 µA	2.0 4.5			V	
V_{IL}, Input Low voltage				0.8		
I_{IH}, Input High current	C3–C1, AS, B2EN	–75		40	µA	
Input High current	Input E1	–75		45		
I_{IL}, Input Low current	C1, C2, C3, E1, AS B2EN	–400 –600				
Logic Output ($\overline{DET}$)						
V_{OL}, Output Low voltage	I_{OUT} = 0.8 mA, 15 kΩ to V_{CC}			0.40	V	
V_{OH}, Output High voltage	I_{OUT} = –0.1 mA, 15 kΩ to V_{CC}	2.4				
Ring-Trip Detector Input (DA, DB)						
Bias current		–500	–50		nA	
Offset voltage	Source resistance = 2 MΩ	–50	0	+50	mV	6
Ground-Key Detector Thresholds						
Ground-key resistive threshold	B to GND	2	5	10	kΩ	
Ground-key current threshold	B to GND		9		mA	
Loop Detector						
I_T, Loop-detect threshold	R_D = 35.4 kΩ, I_T = 375/R_D	9.6	10.6	11.6	mA	
Relay Driver Output (RINGOUT/TESTOUT)						
V_{OL}, On voltage, (RINGOUT)	I_{OL} = 30 mA		+0.25	+0.4	V	
V_{OL}, On voltage, (TESTOUT)	I_{OL} = 30 mA, $V_{TESTINmin}$ = 4.0 V		+0.6	+1.0		
I_{OH}, Off leakage	V_{OH} = +5 V			100	µA	
Zener breakover	I_Z = 100 µA	6	7.2		V	
Zener On voltage	I_Z = 30 mA		10			

RELAY DRIVER SCHEMATICS

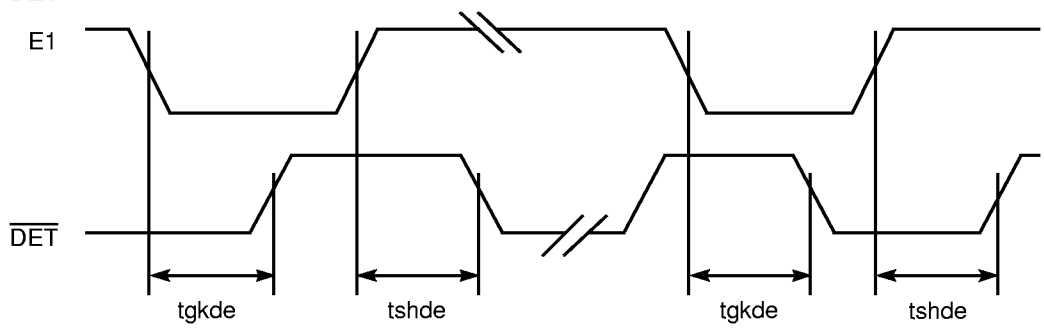


SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Temperature Ranges	Min	Typ	Max	Unit	Note
tgkde	E1 Low to $\overline{DET}$ High (E0 = 1)	Ground-Key Detect state R_L open, R_G connected (See Figure H)	0°C to +70°C			3.8	µs	4
			–40°C to +85°C			4.0		
	E1 Low to $\overline{DET}$ Low (E0 = 1)		0°C to +70°C			1.1		
			–40°C to +85°C			1.6		
tshde	E1 High to $\overline{DET}$ Low (E0 = 1)	Switchhook Detect state	0°C to +70°C			1.2		
			–40°C to +85°C			1.7		
	E1 High to $\overline{DET}$ High (E0 = 1)		0°C to +70°C			3.8		
			–40°C to +85°C			4.0		

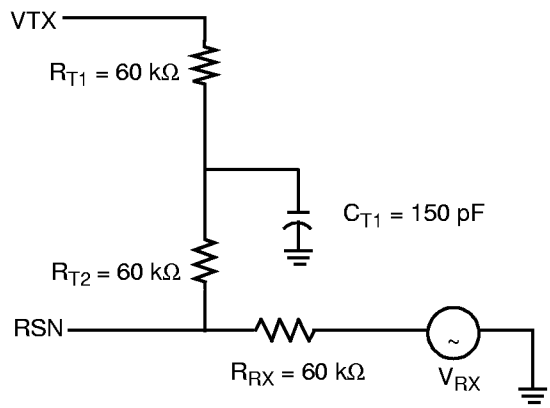
SWITCHING WAVEFORMS

E1 to $\overline{DET}$



Notes:

1. *Unless otherwise noted, test conditions are BAT1 = –52 V, BAT2 = –24 V, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 600 Ω, R_{DC1} = R_{DC2} = 10 kΩ, R_D = 35.4 kΩ, no fuse resistors, C_{HP} = 0.33 µF, C_{DC} = 0.33 µF, C_{CAS} = 0.33 µF, D_1 = 1N400x, two-wire AC input impedance is a 600 Ω resistance synthesized by the programming network shown below.*



2. *a. Overload level is defined when THD = 1%.*
   b. Overload level is defined when THD = 1.5%
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes the two-wire AC load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
6. *Tested with 0 Ω source impedance. 2 MΩ is specified for system design only.*
7. *Group delay can be greatly reduced by using a Z_T network such as that shown in Note 1 above. The network reduces the group delay to less than 2 µs. The effect of group delay on the linecard performance may also be compensated for by synthesizing complex impedance with the QSLAC™ or DSLAC™ device.*

Table 1. SLIC Decoding

State	C3 C2 C1	2-Wire Status	($\overline{DET}$) Output		Battery Selection
			E1 = 1	E1 = 0	
0	0 0 0	Open Circuit	Ring trip	Ring trip	B2EN
1	0 0 1	Ringing	Ring trip	Ring trip	
2	0 1 0	Active	Loop detector	Ground key	
3	0 1 1	On-hook TX (OHT)	Loop detector	Ground key	
4	1 0 0	Tip Open	Loop detector	Ground key	B2EN = 1**
5	1 0 1	Standby	Loop detector	Ground key	V_{BAT1}
6*	1 1 0	Active Polarity Reversal	Loop detector	Ground key	B2EN
7*	1 1 1	OHT Polarity Reversal	Loop detector	Ground key	

Notes:

** Only –1 performance grade devices support polarity reversal.*

*** For correct ground-start operation using Tip Open, V_{BAT1} on-hook battery must be used.*

Table 2. Battery Switching Decoding

AS	B2EN	Operation Status
0	0	Battery independent anti-sat, off-hook battery
1	0	Battery dependent anti-sat, off-hook battery
1	1	Battery dependent anti-sat, on-hook battery

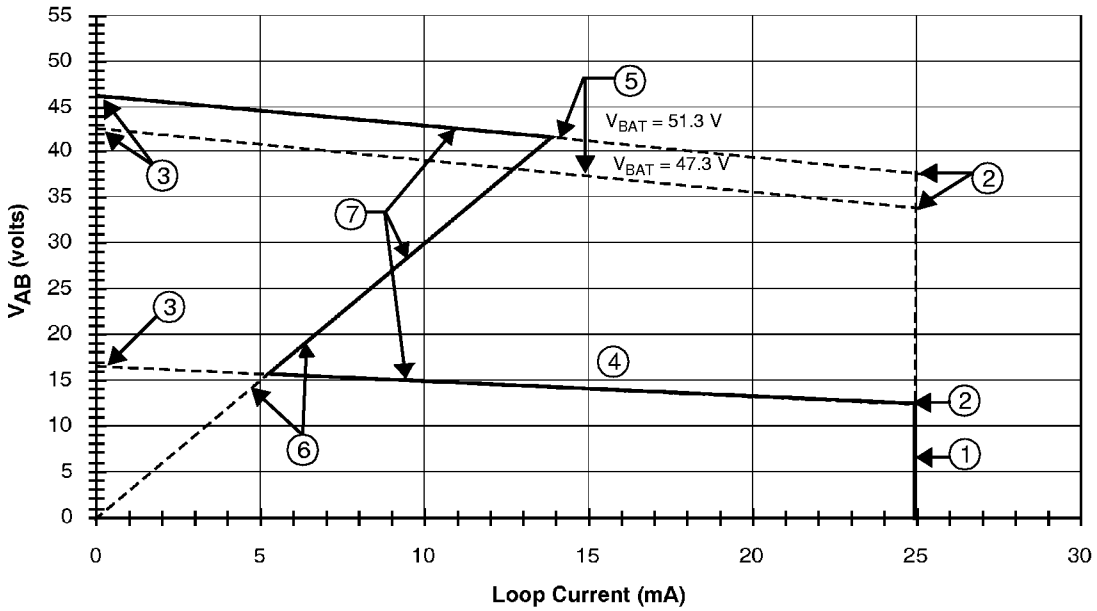
Note:

BSW and V_{BAT2} are connected together externally.

Table 3. User-Programmable Components

$Z_T = 200(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{200 \bullet Z_T}{Z_T + 200(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to R_{SN}. Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = \frac{500}{I_{LOOP}}$ $C_{DC} = 1.5\ ms \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1} \bullet R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant-current region.
$R_D = \frac{375}{I_T}, \quad CD = \frac{0.5\ ms}{R_D}$	R_D and C_D form the network connected from RD to –5 V and I_T is the threshold current between on-hook and off-hook.
$C_{CAS} = \frac{1}{3.4 \bullet 10^5 \pi f_c}$	C_{CAS} is the regulator filter capacitor and f_c is the desired filter cut-off frequency.

DC FEED CHARACTERISTICS



R_{DC} = 20 kΩ

Notes:

1. *Constant-current region:* $I_L = \frac{500}{R_{DC}}$

2. *Anti-sat turn-on point:* $V_{AB} = 12.5\ V$, *Low-Battery Anti-sat*

   $V_{AB} = 1.01|V_{BAT}| - 7.51 - \frac{500}{60}$, *High-Battery Anti-sat,* $|V_{BAT}| < 50.1\ V$

   $V_{AB} = 0.338|V_{BAT}| + 26.0 - \frac{500}{60}$, *High-Battery Anti-sat,* $|V_{BAT}| > 50.1\ V$

3. *Open Circuit voltage:* $V_{AB} = 16.7\ V$, *Low-Battery Anti-sat*

   $V_{AB} = 1.01|V_{BAT}| - 7.51$, *High-Battery Anti-sat,* $|V_{BAT}| < 50.1\ V$

   $V_{AB} = 0.338|V_{BAT}| + 26.0$, *High-Battery Anti-sat,* $|V_{BAT}| > 50.1\ V$

4. *Anti-sat region, Low battery state:* $V_{AB} = 16.7 - I_L \frac{R_{DC}}{120}$

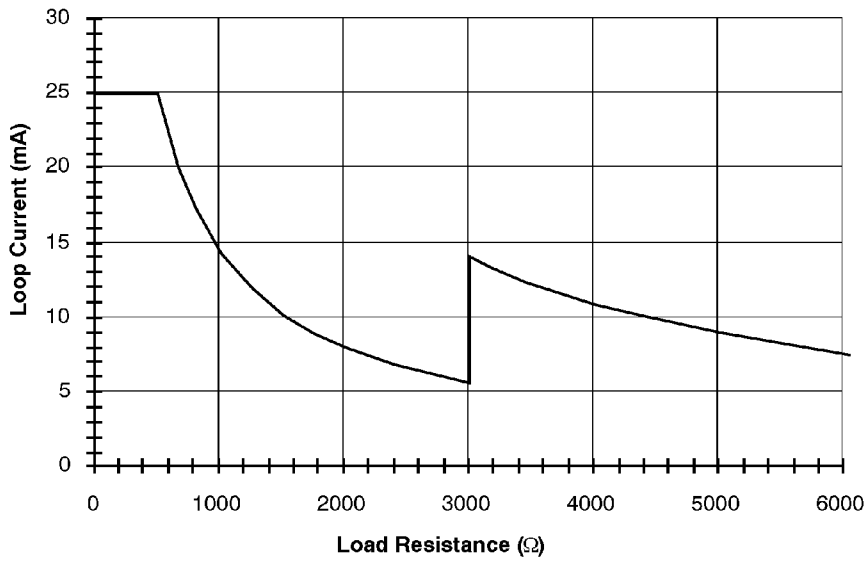
5. *Anti-sat region, High battery state:* $V_{AB} = 1.01|V_{BAT}| - 7.51 - I_L \frac{R_{DC}}{60}$, $|V_{BAT}| < 50.1\ V$

   $V_{AB} = 0.338|V_{BAT}| + 26.0 - I_L \frac{R_{DC}}{60}$, $|V_{BAT}| > 50.1\ V$

6. *Loop resistance at transition between High and Low battery states.*

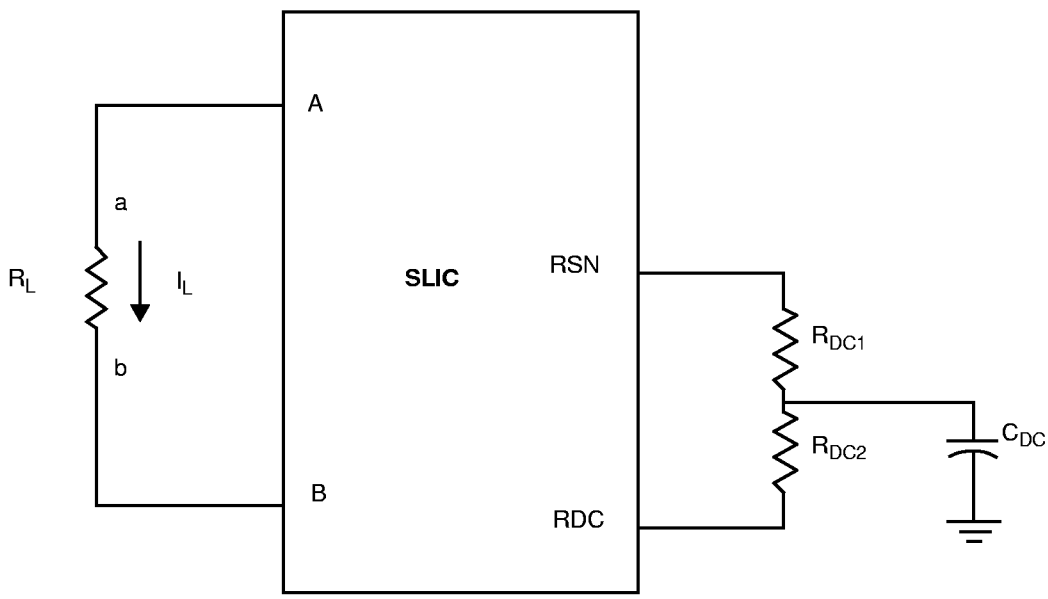
7. *DC feed characteristic through High/Low battery transitions, High/Low battery states controlled by on/off-hook states.*

a. V_A–V_B (V_{AB}) Voltage vs. Loop Current (Typical)



R_{DC} = 20 kΩ
V_{BAT}: High = 51.3 V
Low = 24 V

b. Loop Current vs. Load Resistance (Typical)

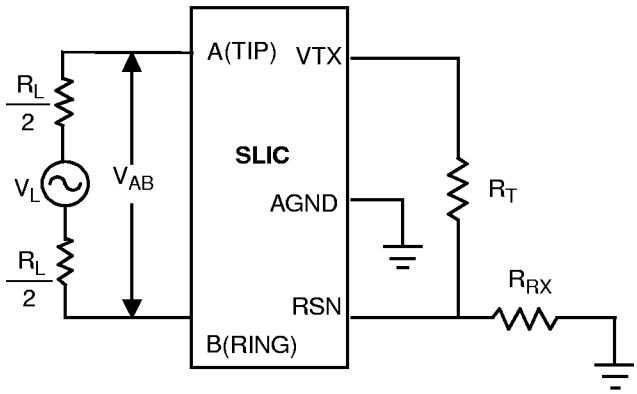


Feed current programmed by R_{DC1} and R_{DC2}

c. Feed Programming

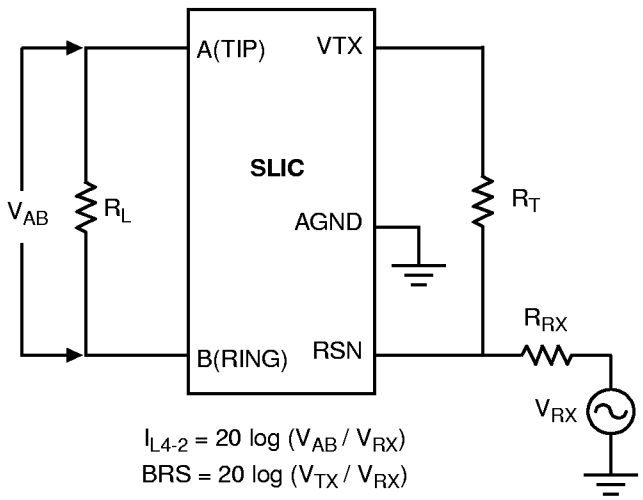
Figure 1. DC Feed Characteristics

TEST CIRCUITS



$I_{L2\text{-}4} = 20 \log (V_{TX} / V_{AB})$

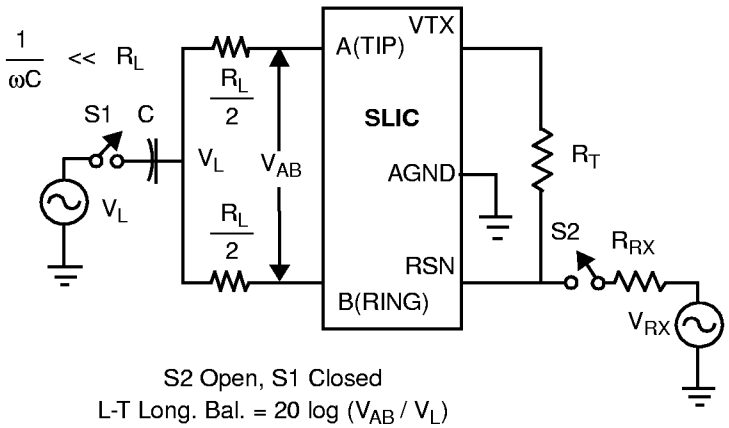
A. Two- to Four-Wire Insertion Loss



$I_{L4\text{-}2} = 20 \log (V_{AB} / V_{RX})$

$BRS = 20 \log (V_{TX} / V_{RX})$

B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed

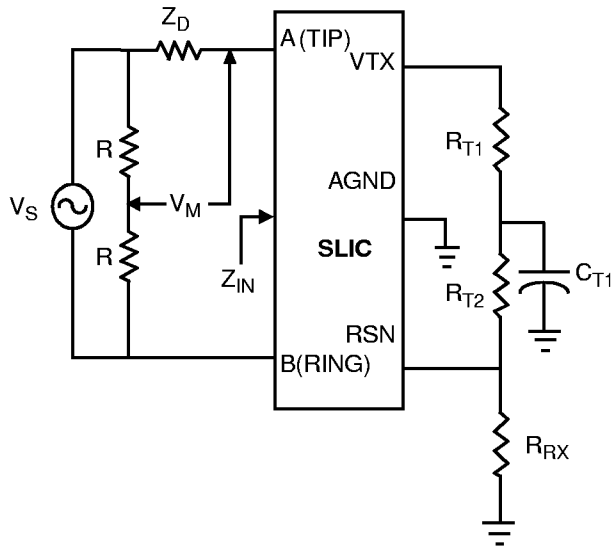
L-T Long. Bal. = 20 log (V_{AB} / V_L)

L-4 Long. Bal. = 20 log (V_{TX} / V_L)

S2 Closed, S1 Open

4-L Long. Sig. Gen. = 20 log (V_L / V_{RX})

C. Longitudinal Balance



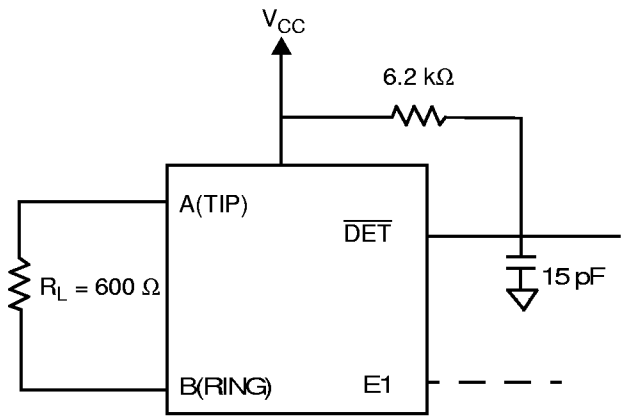
Note:

Z_D is the desired impedance (e.g., the characteristic impedance of the line).

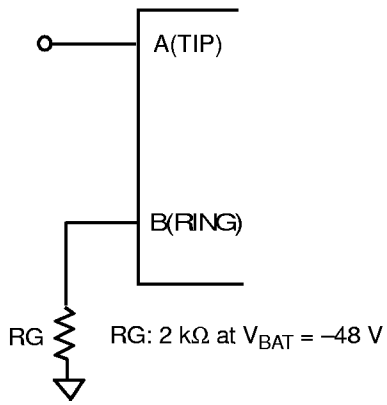
$R_L = -20 \log (2 V_M / V_S)$

D. Two-Wire Return Loss Test Circuit

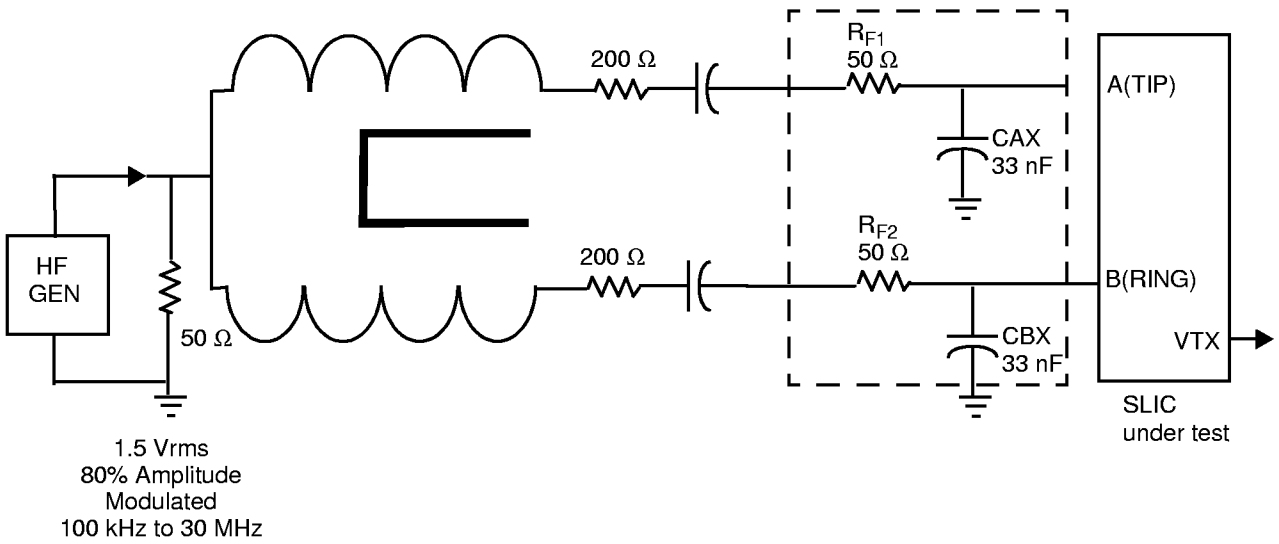
TEST CIRCUITS (continued)



E. Loop-Detector Switching

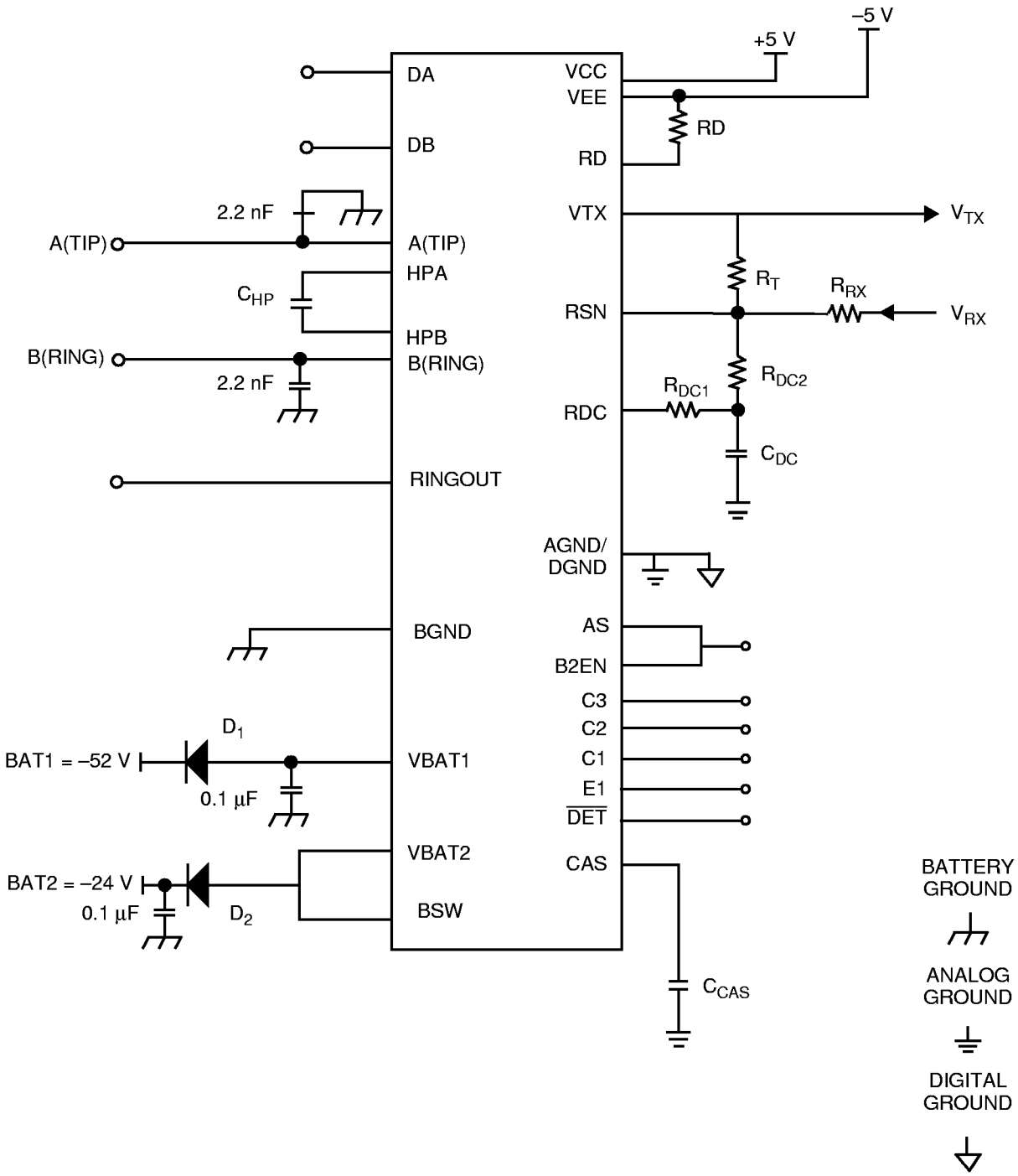


F. Ground-Key Switching



G. RFI Test Circuit

TEST CIRCUITS (continued)



H. Am7949 Test Circuit

REVISION SUMMARY

Revision A to Revision B

- Minor changes were made to the data sheet style and format to conform to AMD standards.
- Electrical Characteristics—Under Longitudinal Performance, the specifications for Longitudinal to Metallic moved from the Typ column to the Min column.
- Electrical Characteristics—Under Line Characteristics (the last row) in the Test Conditions column, V_{BAT1} = 50 V changed to V_{BAT1} = 51.6 V.
- SLIC Decoding Table—Added B2EN reference to the Battery Selection column and its corresponding note to the notes section.
- DC Feed Characteristics—Added new equations and revised existing ones.

Revision B to Revision C

- Minor changes were made to the data sheet style and format to conform to AMD standards.
- In Pin Description table, inserted/changed TP pin description to: “Thermal pin. Connection for heat dissipation. Internally connected to substrate (VBAT). Leave as open circuit or connected to VBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation.”

Count Registers

Each of the three timers has a 16-bit count register. The contents of this register may be read or written by the processor at any time. If the register is written into while the timer is counting, the new value will take effect in the current count cycle.

The count registers should be programmed before attempting to use the timers, since they are not automatically initialized to zero.

Max Count Registers

Timers 0 and 1 have two MAX COUNT registers, while Timer 2 has a single MAX COUNT register. These contain the number of events the timer will count. In timers 0 and 1, the MAX COUNT register used can alternate between the two MAX COUNT values whenever the current maximum count is reached. A timer resets when the timer count register equals the MAX COUNT value being used. If the timer count register or the MAX COUNT register is changed so that the MAX COUNT is less than the timer count the timer does not immediately reset. Instead, the timer counts up to 0FFFFH, "wraps around" to zero, counts up to the MAX COUNT value, and then resets.

Timers and Reset

Upon RESET, the Timers will perform the following actions:

- All EN (Enable) bits are reset preventing timer counting.
- For Timers 0 and 1, the RIU bits are reset to zero and the ALT bits are set to one. This results in the Timer Out pins going High.
- The contents of the count registers are indeterminate.

INTERRUPT CONTROLLER

The 80C186 can receive interrupts from a number of sources, both internal and external. The internal interrupt controller serves to merge these requests on a priority basis, for individual service by the CPU.

Internal interrupt sources (Timers and DMA channels) can be disabled by their own control registers or by mask bits within the interrupt controller. The 80C186 interrupt controller has its own control register that sets the mode of operation for the controller.

The interrupt controller will resolve priority among requests that are pending simultaneously. Nesting is provided so interrupt service routines for lower priority interrupts may themselves be interrupted by higher priority interrupts. A block diagram of the interrupt controller is shown in Figure 19.

The 80C186 has a special slave mode in which the internal interrupt controller acts as a slave to an external master. The controller is programmed into this mode by setting bit 14 in the peripheral control block relocation register (see Slave Mode section).

MASTER MODE OPERATION

Interrupt Controller External Interface

Five pins are provided for external interrupt sources. One of these pins is NMI, the non-maskable interrupt. NMI is generally used for unusual events such as power-fail interrupts. The other four pins may be configured in any of the following ways:

- As four interrupt lines with internally generated interrupt vectors.
- As an interrupt line and interrupt acknowledge line pair (cascade mode) with externally generated interrupt vectors plus two interrupt input lines with internally generated vectors.
- As two pairs of interrupt/interrupt acknowledge lines (cascade mode) with externally generated interrupt vectors.

External sources in the cascade mode use externally generated interrupt vectors. When an interrupt is acknowledged, two $\overline{\text{INTA}}$ cycles are initiated and the vector is read into the 80C186 on the second cycle. The capability to interface to external 82C59A programmable interrupt controllers is provided when the inputs are configured in cascade mode.

Interrupt Controller Modes of Operation

The basic modes of operation of the interrupt controller in master mode are similar to the 82C59A. The interrupt controller responds identically to internal interrupts in all three modes; the difference is only in the interpretation of function of the four external interrupt pins. The interrupt controller is set into one of these three modes by programming the correct bits in the INT0 and INT1 control registers. The modes of interrupt controller operation are as follows:

Fully Nested Mode

When in the fully nested mode four pins are used as direct interrupt requests as in Figure 20. The vectors for these four inputs are generated internally. An in-service bit is provided for every interrupt source. If a lower-priority device requests an interrupt while the in-service bit (IS) is set, no interrupt will be generated by the interrupt controller. In addition, if another interrupt request occurs from the same interrupt source while the in-service bit is set, no interrupt will be generated by the interrupt controller. This allows interrupt service routines to operate

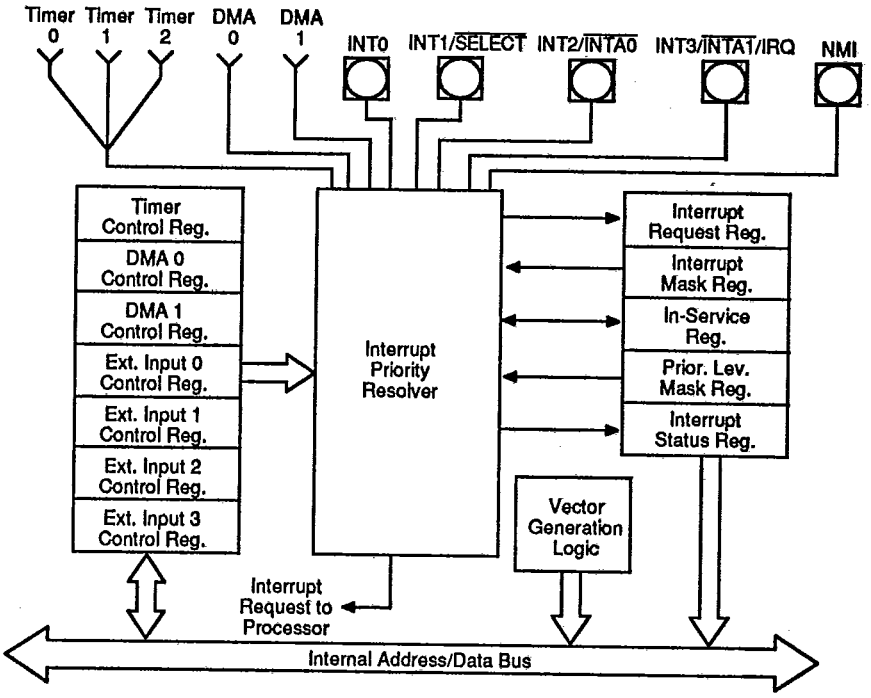


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Figure 19. Interrupt Controller Block Diagram

Master Mode Features

Programmable Priority

The user can program the interrupt sources into any of eight different priority levels. The programming is done by placing a 3-bit priority level (0–7) in the control register of each interrupt source. (A source with a priority level of 4 has higher priority over all priority levels from 5 to 7. Priority registers containing values lower than 4 have greater priority.) All interrupt sources have preprogrammed default priority levels (see Table 3).

If two requests with the same programmed priority level are pending at once, the priority ordering scheme shown in Table 3 is used. If the serviced interrupt routine reenables interrupts, it allows other interrupt requests to be serviced.

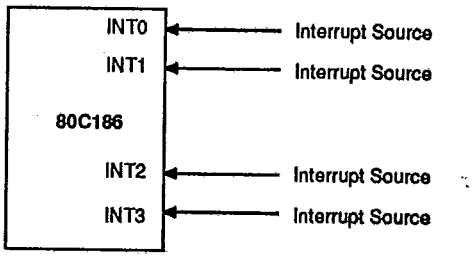

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Figure 20. Fully Nested (Direct) Mode Interrupt Controller Connections

SWITCHING CHARACTERISTICS (continued)

Ready, Peripheral, and Queue Status Timings

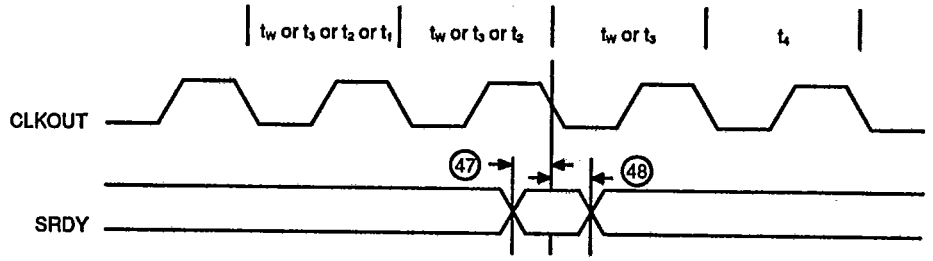
$T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 10\%$ except $V_{CC} = 5\ V \pm 5\%$ at $f > 12.5$ MHz

			Preliminary								
			80C186		80C186-12		80C186-16		80C186-20		
No	Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Unit
80C186 Ready and Peripheral Timing Requirements											
47	t_{SRYCL}	Synchronous Ready (SRDY) Transition Setup Time(1)	15		15		15		10		ns
48	t_{CLSRY}	SRDY Transition Hold Time(1)	15		15		15		10		ns
49	t_{ARYCH}	ARDY Resolution Transition Setup Time(2)	15		15		15		10		ns
50	t_{CLARX}	ARDY Active Hold Time(1)	15		15		15		10		ns
51	t_{ARYCHL}	ARDY Inactive Holding Time	15		15		15		10		ns
52	t_{ARYLCL}	Asynchronous Ready (ARDY) Setup Time(1)	25		25		25		20		ns
53	t_{INVCH}	INTx, NMI, TEST/BUSY, TMR IN Setup Time(2)	15		15		15		15		ns
54	t_{INVCL}	DRQ0, DRQ1, Setup Time(2)	15		15		15		15		ns
80C186 Peripheral and Queue Status Timing Responses											
55	t_{CLTMV}	Timer Output Delay		40		33		27		25	ns
56	t_{CHQSV}	Queue Status Delay		37		32		30		23	ns

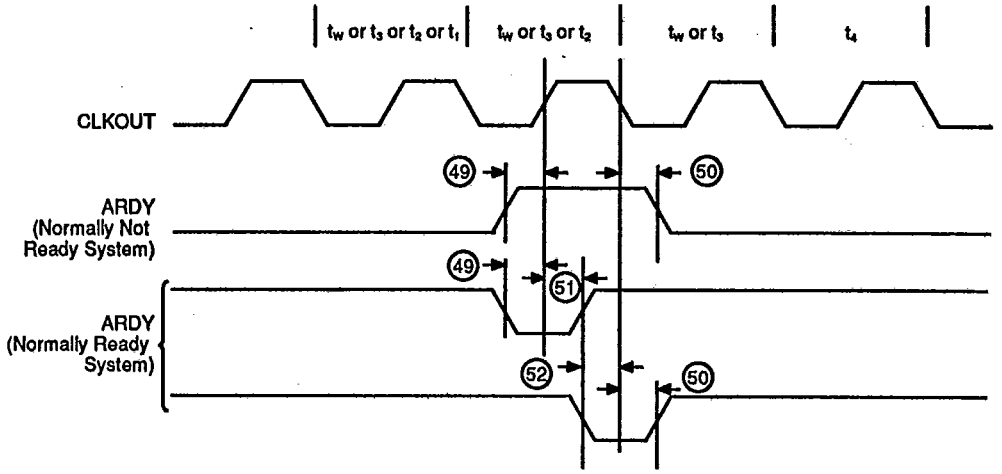
All timings are measured at 1.5 V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with $C_L = 50$–200 pF (10 MHz) and $C_L = 50$–100 pF (12.5–20 MHz).
For AC tests, input $V_{IL} = 0.45$ V and $V_{IH} = 2.4$ V except at X_1 where $V_{IH} = V_{CC} - 0.5$ V.

Notes: 1. To guarantee proper operation.
2. To guarantee recognition at clock edge.

Synchronous Ready (SRDY) Waveforms



Asynchronous Ready (ARDY) Waveforms



Peripheral and Queue Status Waveforms