AN1360
APPLICATION NOTE

Connecting the MPC56x Spanish OAK Microcontroller to the M58BW016B/D Flash Memory

CONTENTS

INTRODUCTION

This application note describes a method of connecting the M58BW016B/D Flash Memory to the Spanish OAK family of microcontrollers without using glue logic. The M58BW016B/D is an advanced 3V 16 Mbit flash memory from STMicroelectronics. It has a boot block architecture and includes a burst interface for high speed access. The M58BW016B has Tuning Block Protection (refer to Application note AN1361), whereas the M58BW016D has the Tuning Block Protection disabled.

The MPC56x is a member of Motorola's Power-PC family of integrated microprocessors. It is a low voltage high performance 32-bit microcontroller designed for advanced automotive applications. It can run at a frequency of up to 56 MHz within the full automotive temperature range using a 2.6V power supply. The M58BW016B/D can operate at the 56 MHz maximum burst frequency required by MPC56x. The internal memory controller of the MPC56x supports single read/write operations, burst read operations, and provides a programmable and flexible bus interface.

The main design consideration in connecting these two devices is the difference in the core power supplies. The electrical design flexibility of command lines, address and data bus of the MPC56x and the M58BW016B/D can be used to implement a full CMOS logic level interface.

The method explained in this document can be used as a reference for other ST burst flash memories and other Power-PC microcontrollers (for example the MPC555). The different power supply levels and timings should be considered for each case.

POWER SUPPLY MANAGEMENT

The MPC56x is a low voltage microcontroller designed for advanced automotive applications. It's bus interface can operate at 56 MHz with a core supply of 2.6V (typ). The Input lines of the MPC56x are 3.3V tolerant. Please refer to the electrical specification for full description of the required power supplies, and power-up sequence (the MPC56x also requires a 5V supply).

The M58BW016B/D is a x32 bus, 3V Flash Memory. An optional V_{PP} of 12V can be provided to speed-up program and erase operations. Like other ST Flash memories, the M58BW016B/D has separate V_{DDQ}, and V_{DDQIN} power supply pins for I/O line buffers. This is useful to interface the Flash Memory device with lower or higher power supply devices. $V_{DDQ(IN)}$ can go from 2.4V to V_{DD} (if V_{DD}=3V, V_{DDQ} can be between 2.4V and 3V).

Figure 1. Power Supply Connections

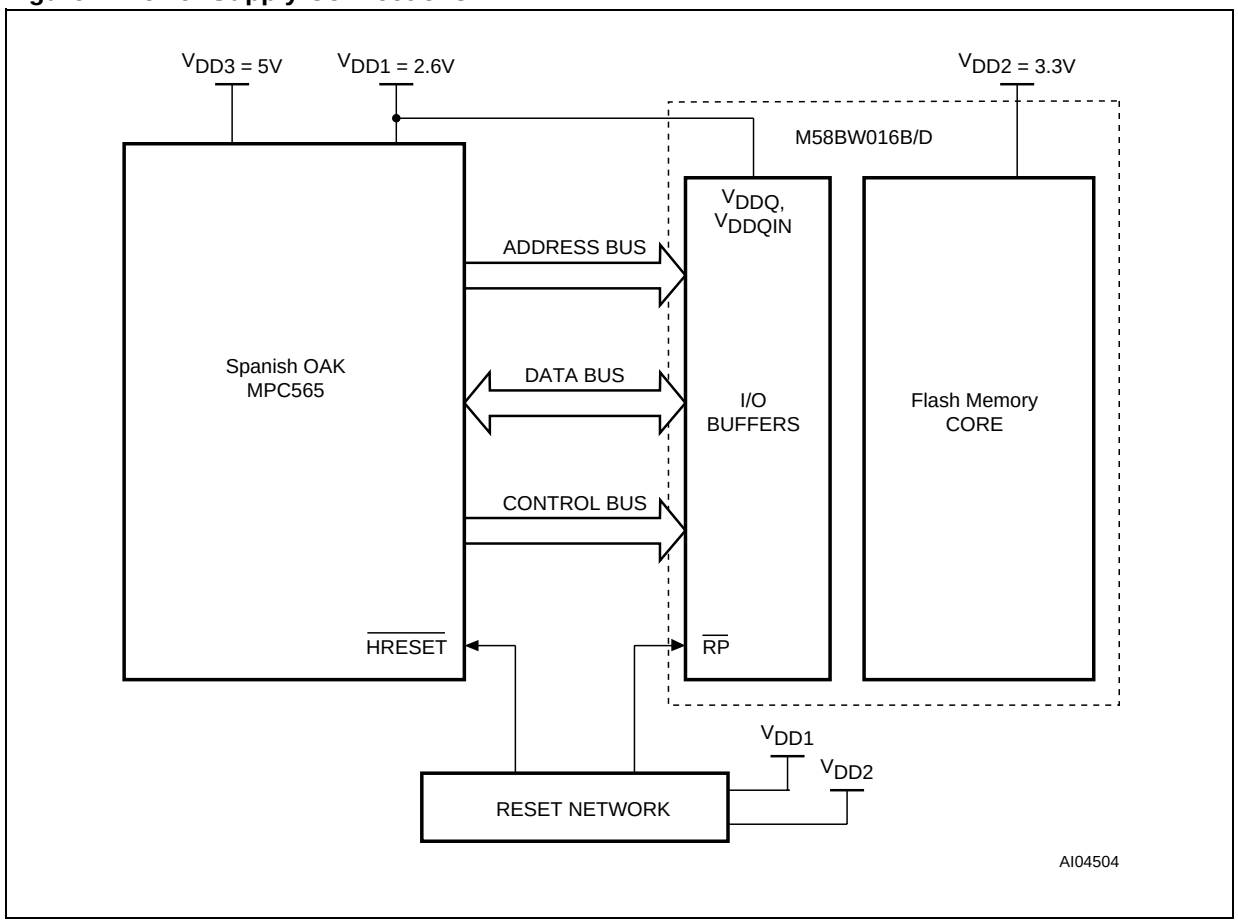


Figure1 shows the recommended way to connect the power supplies. The V_{DD1} at 2.6V is used for the MPC56x core supply and the M58BW016B/D V_{DDQ} supply. V_{DD2} at 3.3V (2.7V minimum) is mandatory to drive the core circuits of the Flash Memory. V_{DD3} (5 V) is provided for the MPC56x for its high voltage operations. Refer to the data sheets to check the minimum and maximum power supply ratings for each device.

The two typical voltage levels (V_{DD1}= 2.6V and V_{DD2}= 3V) allow the devices to reach the maximum burst read frequency of 56 MHz. The bus high logic level is higher than 2.3V, so it is recognized as a CMOS high level by the input buffers of the two devices. The power consumption is at it's lowest in this situation. The two separate power supplies can be managed with a single chip multiple line supervisor circuit, to

provide the appropriate reset signals to both devices. The reset pin on MPC56x ($\overline{\text{HRESET}}$) is connected directly to the M58BW016B/D's $\overline{\text{RP}}$ pin. If the reset network detects a drop in V_{DD} (on V_{DD1} or V_{DD2}), both devices are automatically reset.

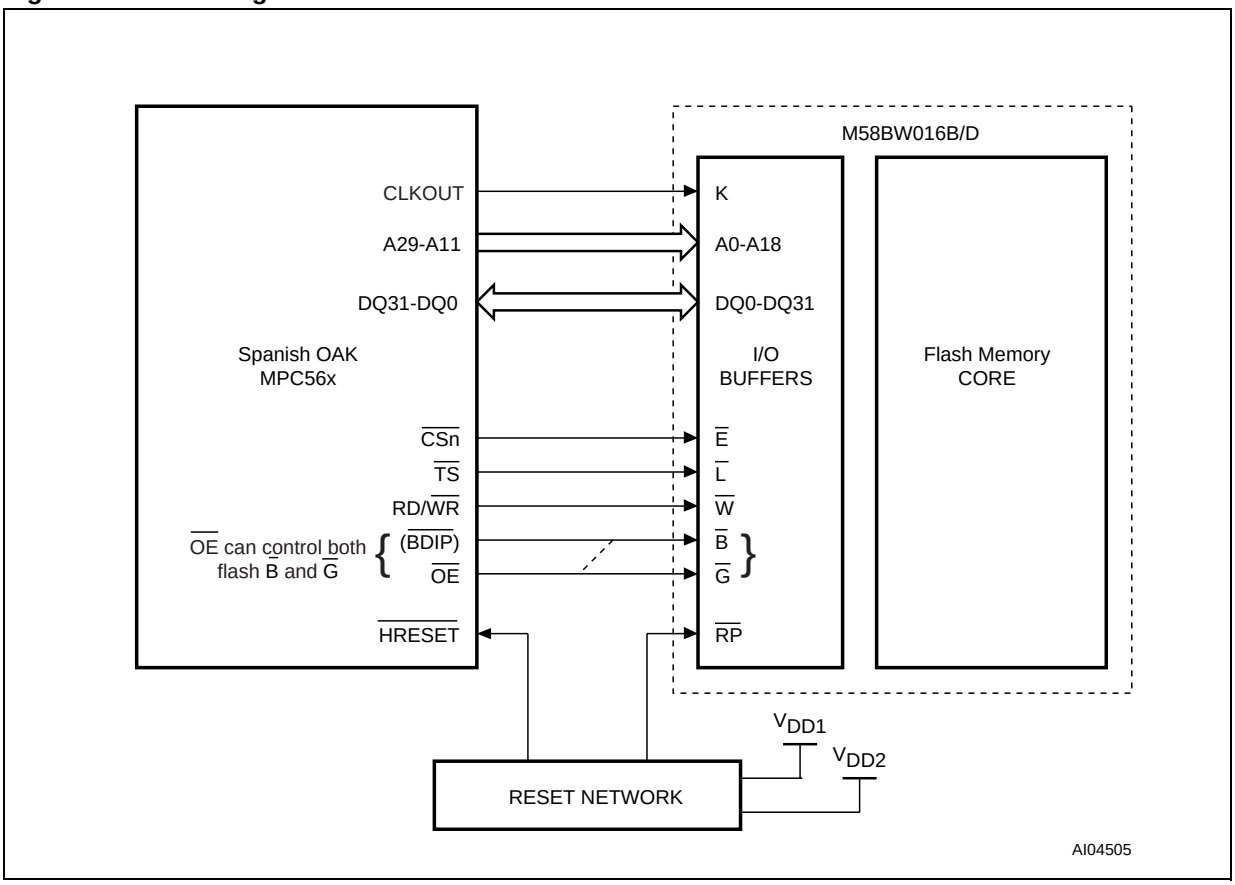
BUS ARCHITECTURE

The MPC56x is normally configured as Big-Endian. The M58BW016B/D flash memory is Little-Endian, that is the hexadecimal data used to control the command interface uses D0 to equate to the Least Significant Bit. To interface the M58BW016B/D with the MPC56x without glue logic, the Address bus and the Data bus should be reversed; A29 on the MPC56x should be connected to A0 of the M58BW016B/D, A28 to A1, A27 to A2, etc.; D31 on the MPC56x should be connected to D0 on the M58BW016B/D, D30 to D1, D29 to D2, etc. See Table 1 and Figure 2.

Table 1. Address, Data and Command Bus Connection

MPC56x	M58BW016B/D	Description
A29-A11	A0-A18	The two least significant bits of MPC56x (A31 and A30) are not connected for a X32 word data transfer. A0 of the Flash memory corresponds to A29 of the MPC56x. The most significant bit of the memory, A18, is connected to A11 of the microcontroller.
D0-D31	D31-D0	Data pins must be connected in the reverse order. Note: Flash Memory operations must be initialized with a data code (Tuning Protection code). If the scrambling between data lines is different, the command codes must be recalculated.
CLKOUT	K	Clock output of the microcontroller is the K input for the Flash Memory to synchronize the data transfer.
$\overline{\text{CSn}}$	$\overline{\text{E}}$	One of the four Chip Select pins of MPC56x must be connected to the $\overline{\text{E}}$ pin of the flash. CS0 can be configured as global boot.
$\overline{\text{TS}}$	$\overline{\text{L}}$	Transfer start pin is used as Latch address enable ($\overline{\text{L}}$ for Flash Memory) every time a read or a write operation is performed by MPC56x.
RD/$\overline{\text{WR}}$	$\overline{\text{W}}$	Read/Write pin for the MPC56x should be connected to the Write Enable pin of the Flash.
$\overline{\text{BDIP}}$	$\overline{\text{B}}$	The burst address advance pin is asserted low during a burst transfer when the next address locations are to be read during a burst sequence. The microcontroller drives it high when the address counter is not to be incremented.
$\overline{\text{OE}}$	$\overline{\text{G}}$	Output enable pin for both devices. Low when the Flash Memory is in read mode, High during a Flash write operation.
$\overline{\text{HRESET}}$	$\overline{\text{RP}}$	The microcontroller forces a reset after a voltage drop on V_{DD} supplies or a software reset. (the $\overline{\text{RP}}$ pin can also be connected to the $\overline{\text{SRESET}}$ pin of the MPC56x).

Figure 2. Connecting the MPC56x to the M58BW016B/D



Note: OE can control both Flash BAA and G.

BUS OPERATIONS AND TIMINGS

The signal timings of the two devices are compatible at the burst frequency of 56 MHz.

During the boot access an asynchronous read is performed. After the reset command, an asynchronous read access is required from the flash memory. After the boot sequence, read and write operations or a burst read operation (the Burst Configuration Register must be configured first) can be performed. Figure 3 shows example timings for these operations. Refer to the data sheets of both devices for more details.

The microcontroller default setting implies a 15 waiting states random access read. The SCY bits (number of wait states) of the MPC56x Memory Controller Option Register (ORx) must be set to 4 with a 56 MHz clock. In this way, the 4 wait states latency is used in the single cycle or in the first beat access of a burst read. During clock period 6 the data is sampled by the microcontroller strobe.

After this delay sequence, the microcontroller strobe can detect the data valid on the rising edge of the last clock cycle. OE (G) signal is asserted low one clock cycle after the TS (L) and CSx (E) falling edge. In this case OE (flash) memory has the same timing as BDIP in normal assertion. A late BDIP can be also used (in this case flash OE can be connected to micro OE).

Figure 4 shows a burst read at 56 MHz. The Burst Configuration Register of the M58BW016B/D (bits 13:11) is set to '1,0,0,2' in order to have 6 clock periods from the address latch to the first data beat. According to MPC56x ORx notation, the user must specify 4 extra wait states (SCY field) in the Memory Controller Option Register. The address latch clock period (1st) and data latch clock period (6th) are not considered to be wait states for the external memory interface of the MPC56x.The data beat can be held

for just one clock period to perform a linear burst with a 1 period beat length (see Appendix A, Registers Configuration). These two settings (ORx and Flash Data Stream Register) define a 6-1-1-1 burst sequence.

An example of a write cycle is provided in Figure 5. All write operations in both the MPC56x and the M58BW016B/D are asynchronous. After execution of the write cycles to initialize a program or erase operation in the flash memory, the result of that operation can be detected in the Status Register. Issue the Read Status Register command to output the contents of the Status Register. If the operation is still in progress a Read command will also output the contents of the Status Register. Refer to the M58BW016B/D data sheet for more details on the Program, Erase and Read Status Register commands.

Figure 3. Single Read

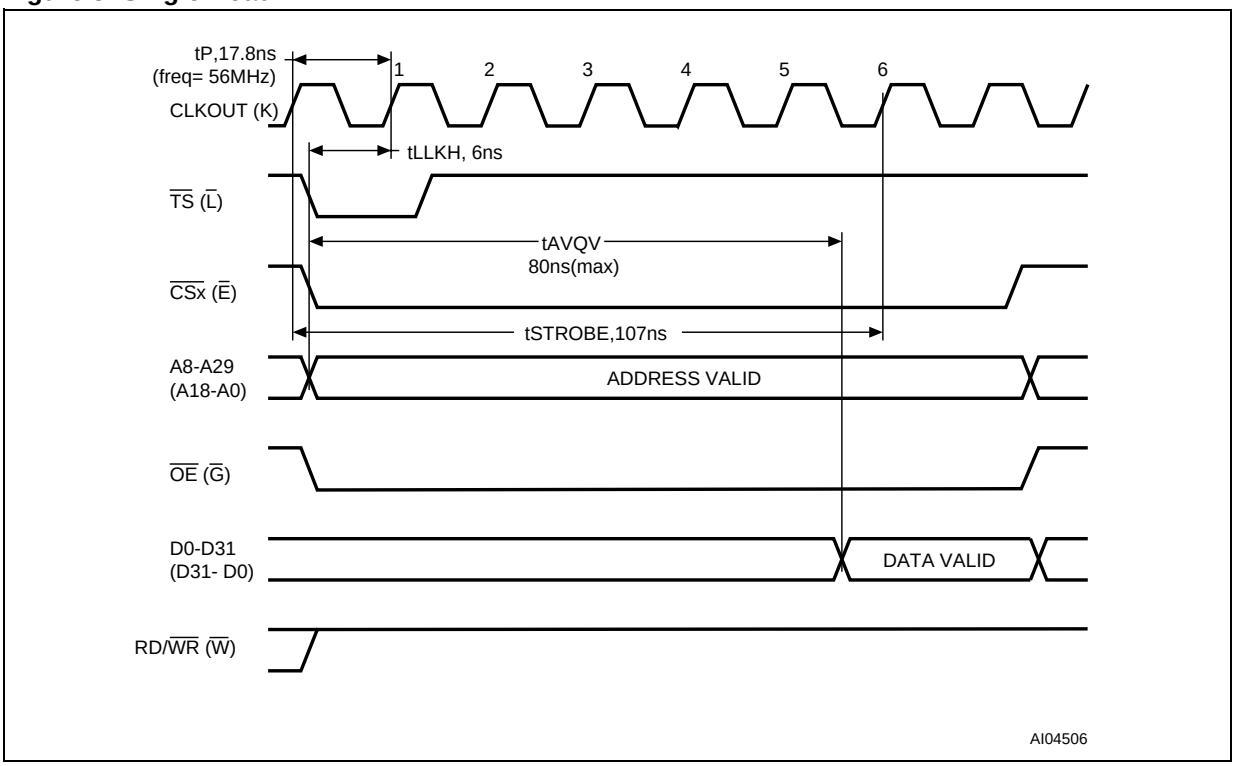


Figure 4. 56MHz 6-1-1-1 Burst Read

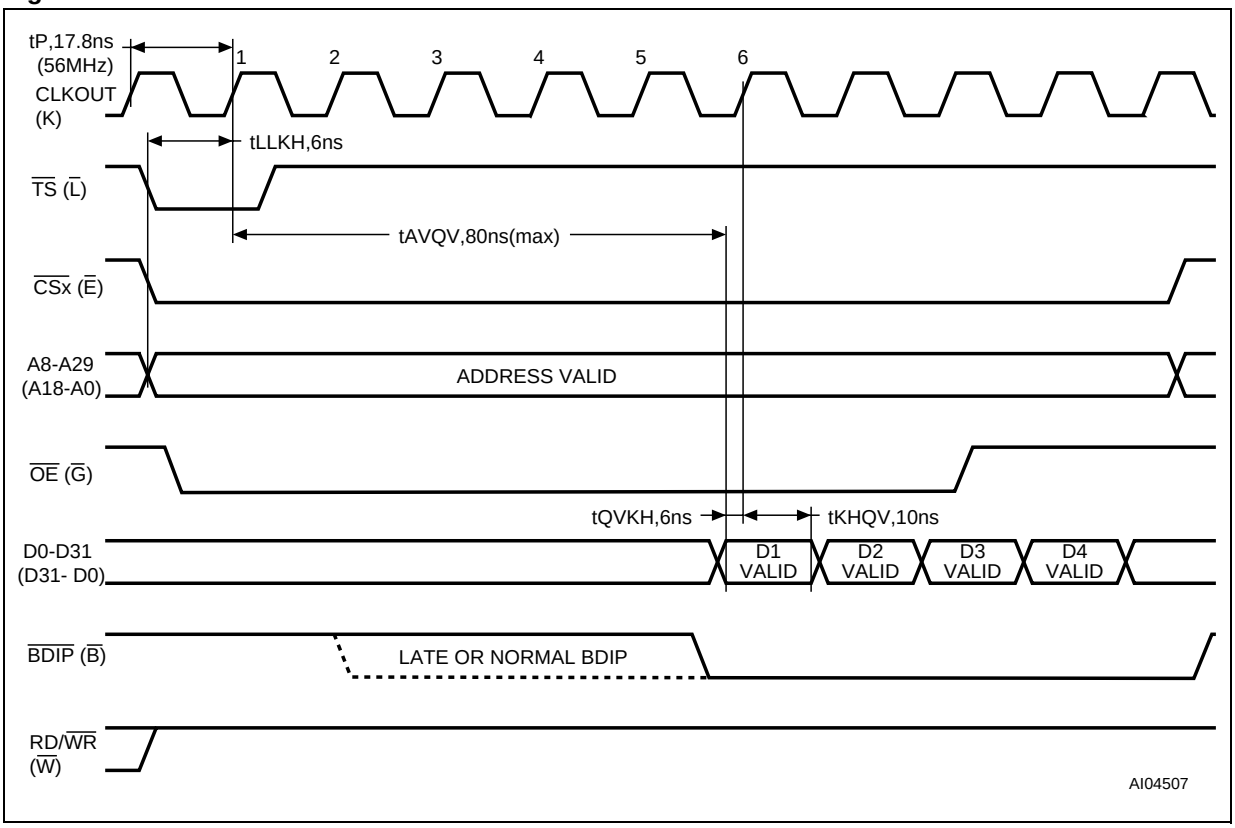
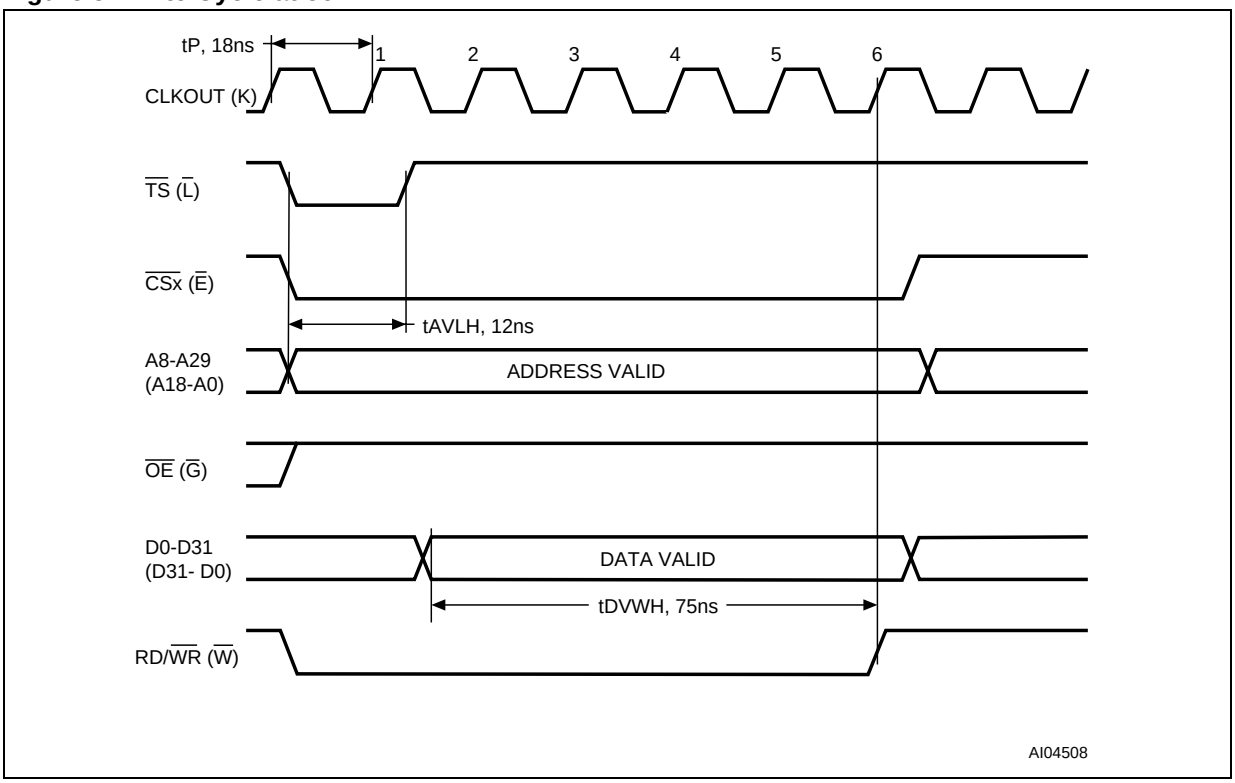


Figure 5. Write Cycle at 56 MHz



APPENDIX A. REGISTERS CONFIGURATION

Table 2. M58BW016B/D: Burst Configuration Register

Bit	Description	Value	Description
M15	Read Select	0	Synchronous Burst Read
		1	Asynchronous Read (Default at power-on)
M14			Reserved
M13-M11	X-Latency (2)	001	Reserved
		010	4, 4-1-1-1 (1)
		011	5, 5-1-1-1, 5-2-2-2
		100	6, 6-1-1-1, 6-2-2-2
		101	7, 7-1-1-1, 7-2-2-2
		110	8, 8-1-1-1, 8-2-2-2
M10			Reserved
M9	Y-Latency (3)	0	One Burst Clock cycle
		1	Two Burst Clock cycles
M8	Valid Data Ready	0	R valid Low during valid Burst Clock edge
		1	R valid Low one data cycle before valid Burst Clock edge
M7	Burst Type	0	Interleaved
		1	Sequential
M6	Valid Clock Edge	0	Falling Burst Clock edge
		1	Rising Burst Clock edge
M5-M4			Reserved
M3	Wrapping	0	Wrap
		1	No wrap
M2-M0	Burst Length	001	4 Double-Words
		010	8 Double-Words
		111	Continuous

Note: The 16 bit Burst Configuration Register is used to configure the read access of the Flash Memory.

Table 3. MPC56x: External Memory Base Register (BRx)(1) Configuration

Bit	Name	Value	Description
0-16	Base Address	User defined	The Flash Memory base address
17-19	Address Type	User defined	The user assigns the flash to any address space.
20-21	Port Size	00	32 bit port size
22	Reserved	0	
23	Write Protect	User Defined	0 = Flash can be programmed 1 = Flash Memory Read Only
24-26	Reserved	000	
27	TBDIP	0	No toggle BDIP
28	LBDIP	0	No late BDIP
29	SETA	0	No external TA
30	Burst Inhibit	User Defined	0 = Enable Burst Access (instruction fetch only) 1 = Disable Burst Access
31	Valid	1	To activate the current Bank

Note: 1. "x" is the number of the chip select assigned to the Flash Memory address space.

Table 4. MPC56x: External Memory Option Register (ORx)(1) Configuration

Bit	Name	Value	Description
0-15	Address Mask	User defined	0xffe0 for mask in 16 Mbit X32 bit setup
16	Address Mask bit 16	0	Base Address mask bit 16 is always turned on for all setups
17-19	Address Type Mask	User defined	More than one address space type can be assigned to a chip select.
20	CSNT	0	Chip select negation time
21-22	ACS	00	No delay needed
23	EHTR	0	Extended hold time not needed
24-26	SCY	100	4 wait states + 2 = 6 clocks for first access or burst initial latency. Same wait states used for the write cycle.
28-30	BSCY	0	0 wait states clock per data beat
31	TRLX	0	No TRLX needed

Note: 1. "x" is the number of the chip select assigned to Flash Memory address space.

CONCLUSION

The M58BW016B/D can be connected to the MPC56x in a glue-less configuration, providing burst performance at 56MHz in the full automotive temperature range (-40 to 125°C).

REVISION HISTORY

Date	Version	Revision Details
05-Jun- 2001	-01	First Issue

If you have any questions or suggestion concerning the matters raised in this document please send them to the following electronic mail address:

ask.memory@st.com (for general enquiries)

Please remember to include your name, company, location, telephone number and fax number.