

CDP1800-Series and CDP6805-Series Peripherals (Continued)

Input Levels: CMOS for All Types

Type	Description and Function	Features	Operating Voltage Range	Operating Temp Range (T _A) †	Fanout (TTL Loads)	No. of Pins* Package
			Volts	°C		
MEMORY I/O INTERFACE						
CDP1853 CDP1853C	N Bit 1-of-8 Decoder	<ul style="list-style-type: none"> Provides direct control of up to 7 input & 7 output devices Chip Enable (CE) allows easy expansion for multi-level I/O systems 	4 to 10.5 4 to 6.5	-40 to +85	1	16 D E
CDP1881 CDP1881C	6-Bit Latch and Decoder Memory Interface	<ul style="list-style-type: none"> Performs memory address latch and decoder functions multiplexed or non-multiplexed Decodes up to 16K bytes of memory Interfaces directly with CDP 1800-series μPs at maximum clock frequency 	4 to 10.5 4 to 6.5	-40 to +85	1	20 E
CDP1882 CDP1882C	6-Bit Latch and Decoder Memory	<ul style="list-style-type: none"> Performs memory address latch and decoder functions multiplexed or non-multiplexed Decodes up to 16K bytes of memory Interfaces directly with CDP1800-series μPs at maximum clock frequency 	4 to 10.5 4 to 6.5	-40 to +85	1	18 D E
CDP1883 CDP1883C	7-Bit Latch and Decoder Memory Interface	<ul style="list-style-type: none"> Performs memory address latch and decoder functions multiplexed or non-multiplexed Interfaces directly with the CDP1800-series μPs Allows decoding for systems up to 32K bytes 	4 to 10.5 4 to 6.5	-40 to +85	1	20 E
SERIAL I/O						
CDP1854A CDP1854AC	Programmable Universal Asynchronous Receiver/Transmitter (UART)	<ul style="list-style-type: none"> Two operating modes: <ul style="list-style-type: none"> Mode 0: functionally compatible with industry types such as the TR1602A Mode 1: interfaces directly with CDP1800-series μPs without additional components Full or half duplex operation Parity, framing, and overrun error detection Baud rate: <ul style="list-style-type: none"> DC to 200K bits/s at V_{DD} = 5V DC to 400K bits/s at V_{DD} = 10V Fully programmable with externally selectable word length (5-8 bits), parity inhibit, even/odd parity, and 1, 1.5 or 2 stop bits False start bit detection 	4 to 10.5 4 to 6.5	-40 to +85	1	40 D E 44 Q
CDP6402 CDP6402C	UART	<ul style="list-style-type: none"> Low-power CMOS circuitry: 7.5mW typ at 3.2MHz (max freq) at V_{DD} = 5V Baud rate: <ul style="list-style-type: none"> DC to 200K bits/s (max) at V_{DD} = 5V, 85°C DC to 400K bits/s (max) at V_{DD} = 10V, 85°C Automatic data formatting and status generation Fully programmable with externally selectable word length (5-8 bits), parity inhibit, even/odd parity, and 1, 1.5 or 2 stop bits Operating temperature range: <ul style="list-style-type: none"> (CDP6402D, CD) -55°C to +125°C (CDP6402E, CE) -40°C to +85°C Replaces industry types IM6402 and HD6402 	4 to 10.5 4 to 6.5	-40 to +85	1	40 D E

† T_A indicates operating temperature range over which the published electrical data are specified

* See interpretation guide and packaging section