LH521032

PRELIMINARY

256K × 4 Separate I/O Static RAM

FEATURES

- Separate Data In and Data Out
- Reduces Chip Count and Increases Performance
- Fast Access Times: 20/25/35 ns
- Space Saving 32-Pin, 400-mil SOJ
- Low Power Standby When Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation

FUNCTIONAL DESCRIPTION

The LH521032 is a high-speed 1,048,576-bit static RAM organized as 256K × 4 with separate Data Input and Output buses.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) gates power to the chip when $\overline{E}$ is HIGH. Standby power (I_{SB1}) drops to its lowest level when $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both $\overline{E}$ and Write Enable ($\overline{W}$) are LOW. Data is transferred from the Data In pins to the memory location specified by the 18 address lines.

Read cycles occur when $\overline{E}$ is LOW and $\overline{W}$ is HIGH. A Read cycle will begin upon an address transition, on a falling edge of $\overline{E}$, or on a rising edge of $\overline{W}$. Data will be output on the Data Out pins. The Data Out pins become high-impedance during Write operations, with the contents of the Data In bus flowing-through to the Data Out bus.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

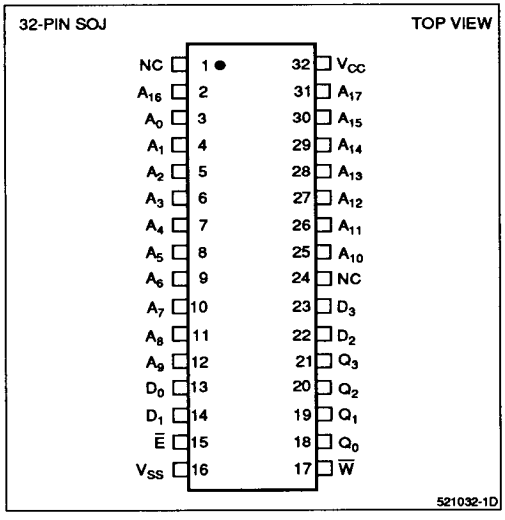

Figure 1. Pin Connections for SOJ Package

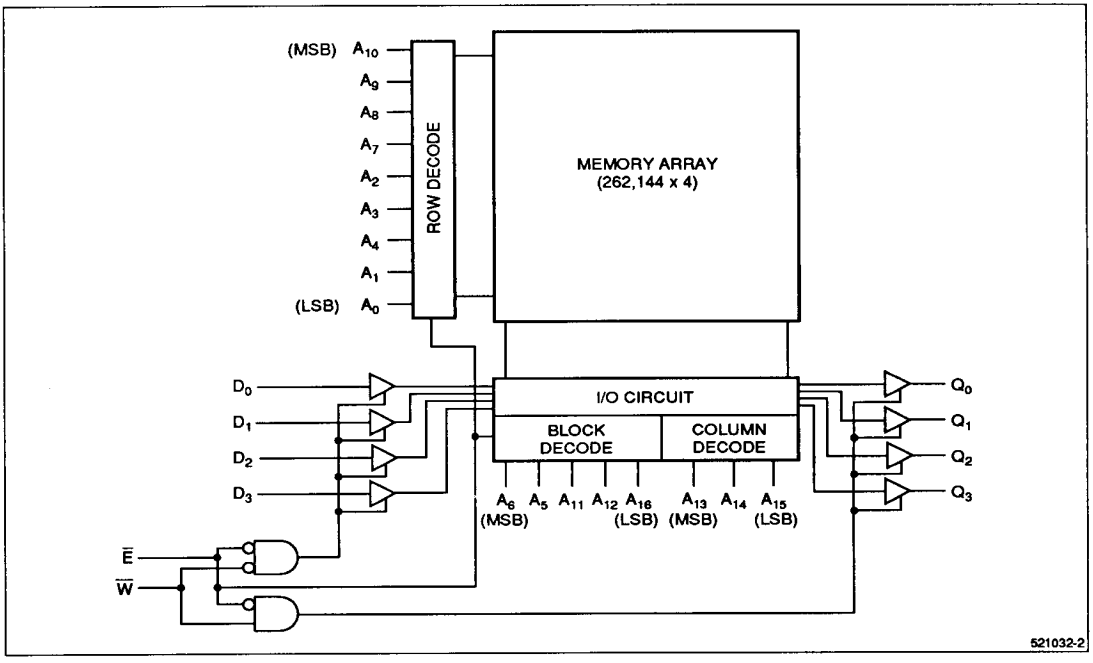

Figure 2. LH521032 Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{W}$	MODE	$D_0 - D_3$	$Q_0 - Q_3$	I_{CC}
H	X	Not Selected	Don't Care	High-Z	Standby
L	H	Read	Don't Care	Data Out	Active
L	L	Write	Data In	High-Z	Active

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{17}$	Address Inputs
$D_0 - D_3$	Data Inputs
$Q_0 - Q_3$	Data Outputs
$\overline{E}$	Chip Enable input

PIN	DESCRIPTION
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5		5.5	V
V_{SS}	Supply Voltage	0		0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	Outputs open, t_{RC} = min				mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V				mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$				mA
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V

NOTE:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

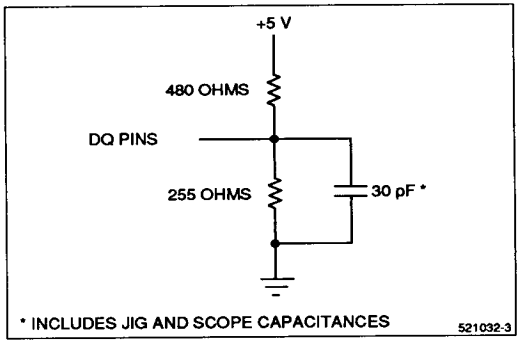

Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	
C_{DQ} (I/O Capacitance)	

NOTES:
1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-20		-25		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
t_{RC}	Read Cycle Timing	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{OH}	Output Hold from Address Change	5		5		5		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	5		5		5		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		10		15		20	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		20		25		35	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		30		ns
t_{AW}	Address Valid to End of Write	15		20		30		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from End of Write	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	15		20		30		ns
t_{DW}	Input Data Setup Time	10		12		15		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		10		15		20	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	0		0		0		ns

NOTES:
1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±200 mV transition from steady state levels into the test load.
3. Guaranteed but not tested.

TIMING DIAGRAMS — READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, and $\overline{E}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of $D_0 - D_3$ implies that data lines are in the Low-Z state and the data may not be valid.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid while $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, but may become valid as soon as t_{ELZ}.

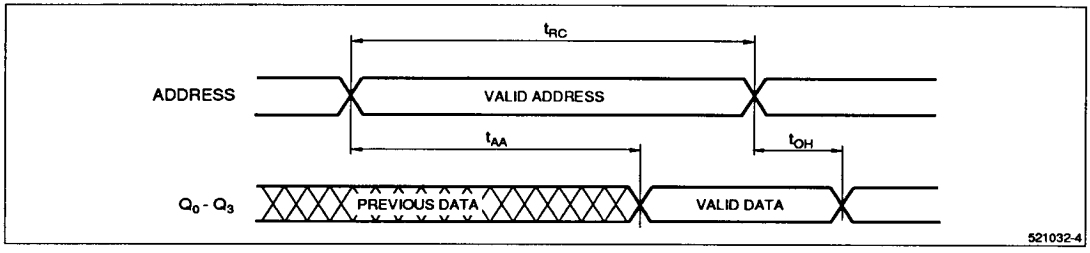

Figure 4. Read Cycle No. 1

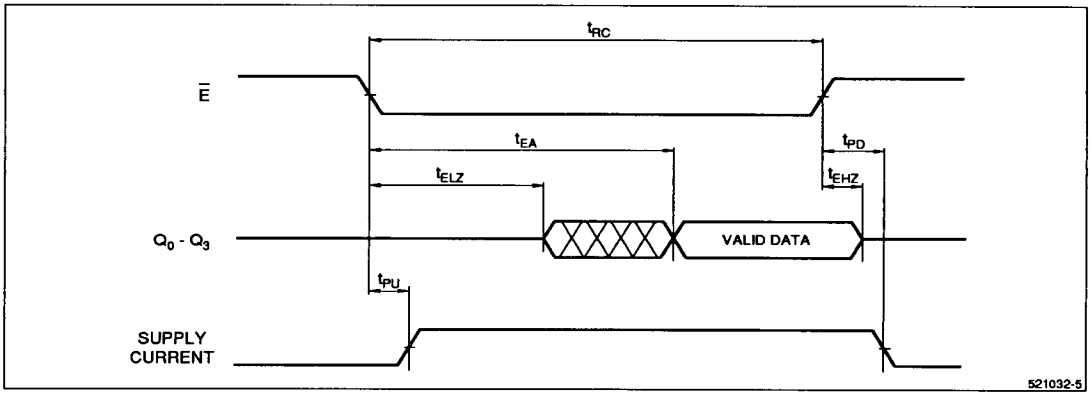

Figure 5. Read Cycle No. 2

TIMING DIAGRAMS — WRITE CYCLE

Addresses must be stable during Write cycles. $\overline{E}$ or $\overline{W}$ must be high during address transitions. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW.

Write Cycle No. 2 ($\overline{E}$ Controlled)

DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

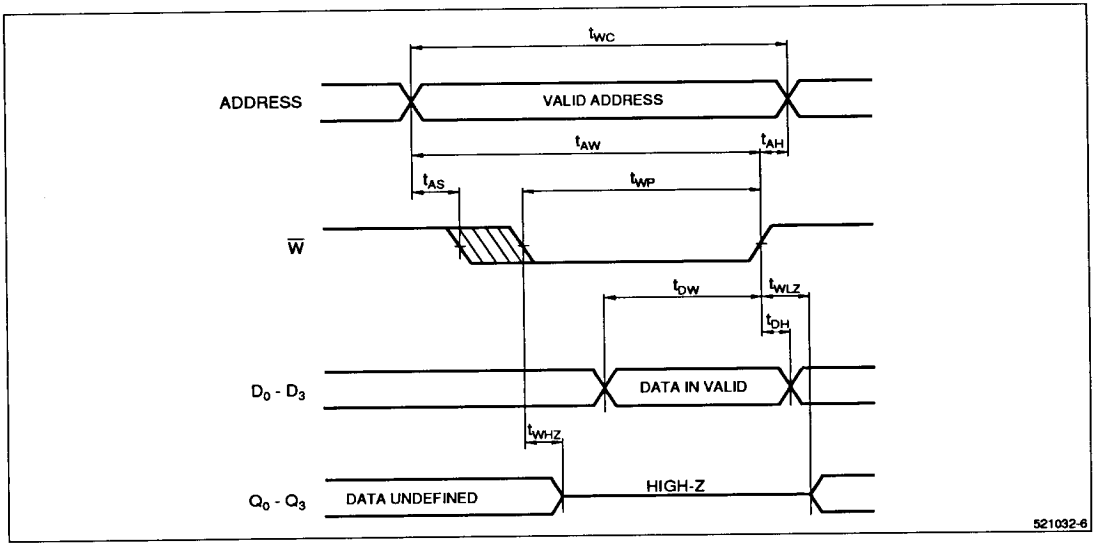

Figure 6. Write Cycle No. 1

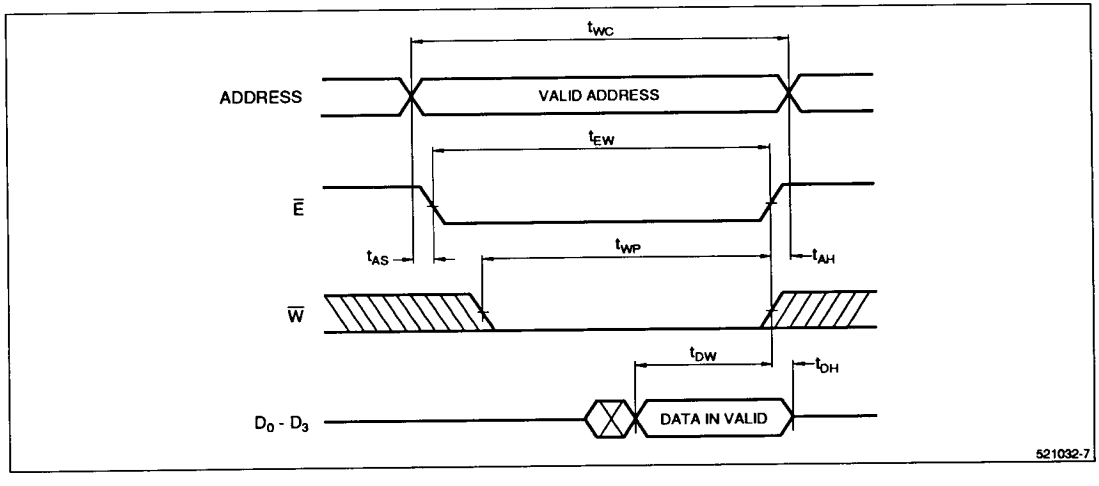

Figure 7. Write Cycle No. 2

ORDERING INFORMATION