NEC

TFT COLOR LCD MODULE

NL10276AC28-01E

36 cm (14.1 type), 1024 × 788 pixels, FULL-COLOR, MULTI-SCAN FUNCTION INCORPORATED BACKLIGHT WITH INVERTER

DESCRIPTION

NL10276AC28-01E is a TFT (thin film transistor) active matrix color liquid crystal display (LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight. NL10276AC28-01E has a built-in backlight with inverter.

The 36cm diagonal display area contains 1024 × 768 pixels and can display full-color (more than 16 million colors simultaneously).

NL1276AC28-01E is a sucessor model of NL10276AC28-01.

FEATURES

- High luminance and Low reflection
- Analog RGB signals
- Contrast and brightness control function
- Multi-scan function: e.g., XGA, SVGA, VGA, VGA-TEXT, PC-9801, MAC
- Incorporated edge-light type backlight with inverter (Two long life CCFLs per lamp holder)
- Replaceable lamp holder (Part number: 141LHS08)

APPLICATIONS

- Engineering workstation(EWS), Desk-top type of PC
- Display terminals for control system
- Monitors for process controller

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STRUCTURE AND FUNCTIONS

A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. The TFT panel structure is created by sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate. After the driver LSIs are connected to the panel, the backlight assembly is attached to the backside of the panel.

RGB (red, green, blue) data signals from a source system is modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cells.

Acting as an electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by the data source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

OUTLINE OF CHARACTERISTICS (at room temperature)

Display area	285.696 (H) × 214.272 (V) mm
Drive system	a-Si TFT active matrix
Display colors	Full-color
Number of pixels	1024 × 768
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.279 (H) × 0.279 (V) mm
Module size	330.0 (H) × 255.0 (V) × 19.0 typ. (D) mm
Weight	1220 g (typ.)
Contrast ratio	150:1 (typ.)

Viewing angle (more than the contrast ratio of 10:1)

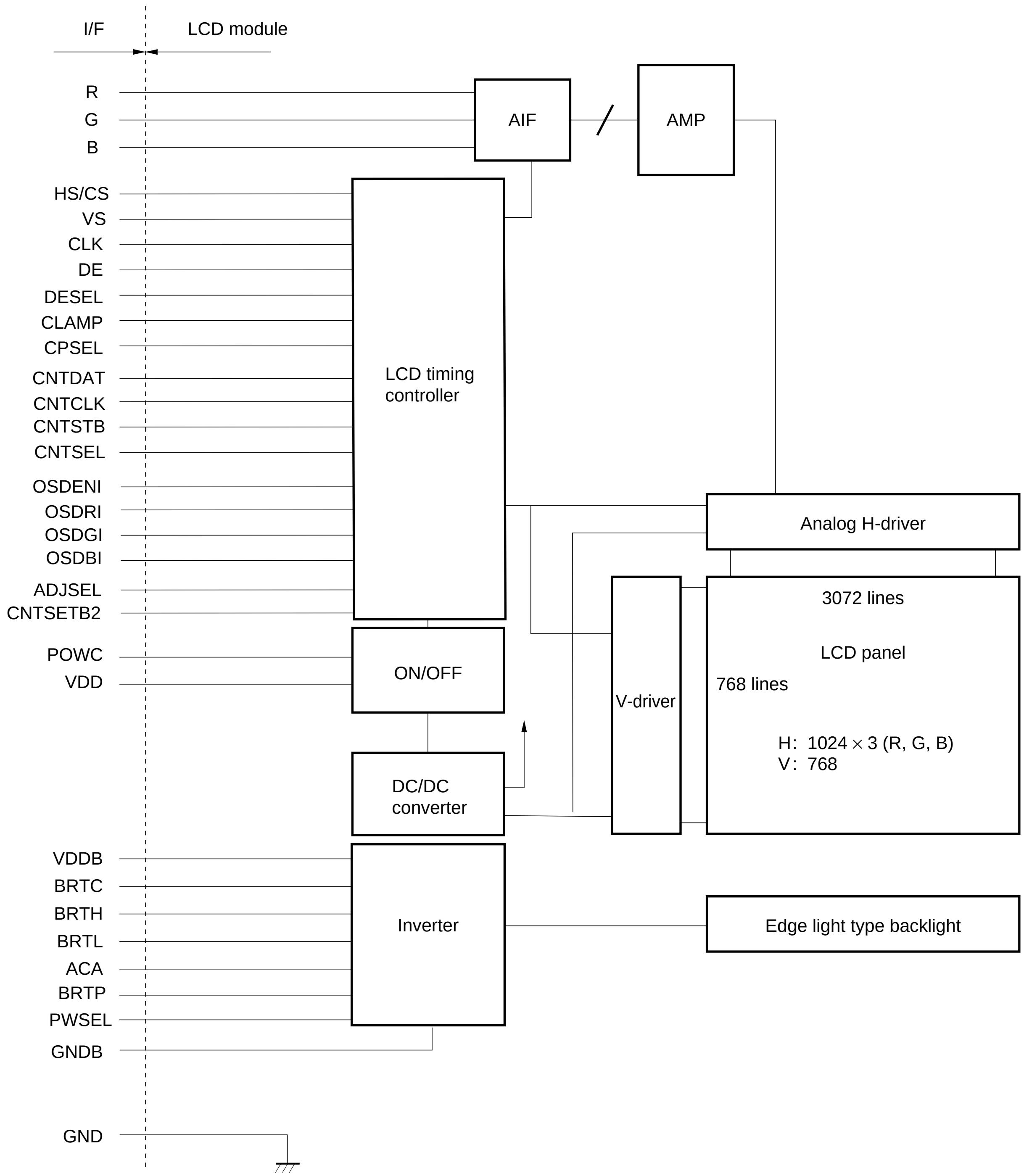
- Horizontal : 50° (typ., left side, right side)
- Vertical : 20° (typ., up side), 35° (typ., down side)

Designed viewing direction

- Wider viewing angle with contrast ratio : down side (6 o'clock)
- Wider viewing angle without image reversal : up side (12 o'clock)
- Optimum grayscale (γ= 2.2) : 0° (typ.)

Polarizer hardness	2H (min. with JIS K5400)
Color gamut	40 % (typ.. At center, To NTSC)
Response time	25 ms (max.), "white" to "black"
Luminance	200 cd/m^2 (typ.)
Signal system	Analog RGB signals, Synchronous signals (Hsync, Vsync), Dot clock (CLK)
Supply voltage	12 V, 12 V (Logic/LCD driving, Backlight)
Backlight	Edge light type: Two cold cathode fluorescent lamps with inverter [Replacement parts] • Lamp holder: 141LHS08 • Inverter: 141PW111
Power consumption	15 W (typ.)

BLOCK DIAGRAM



Note Neither GND nor GNDB is connected to the Frame.

SPECIFICATIONS

GENERAL SPECIFICATIONS

Item	Contents	Unit
Module size	330.0 ± 0.5 (H) × 255.0 ± 0.5 (V) × 20.5 (max.) (D)	mm
Display area	285.696 (H) × 214.272 (V)	mm
Number of dots	1024 × 3 (H) × 768 (V)	dots
Pixel pitch	0.279 (H) × 0.279 (V)	mm
Dot pitch	0.093 (H) × 0.279 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	—
Display colors	full-color	color
Weight	1300 (max.)	g

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit	Remarks
Supply voltage	VDDB	–0.3 to +14	V	Ta = 25 °C
	VDD	–0.3 to +14	V	
Logic input voltage	Vin1	–0.3 to +5.5	V	Ta = 25 °C VDD = 12 V
R, G, B input voltage	Vin2	–6.0 to +6.0	V	
CLK input voltage	Vin3	–7.0 to +7.0	V	
BRTL input voltage	Vin4	–0.3 to +1.5	V	
Storage temp.	Tst	–20 to +60	°C	—
Operating temp.	Top	0 to +50	°C	Module surface Note
Humidity (no condensation)	≦ 95 % relative humidity			Ta ≦ 40 °C
	≦ 85 % relative humidity			40 < Ta ≦ 50 °C
	Absolute humidity shall not exceed Ta = 50 °C, 85 % relative humidity level.			Ta > 50 °C

Note Measured at the LCD panel

ELECTRICAL CHARACTERISTICS

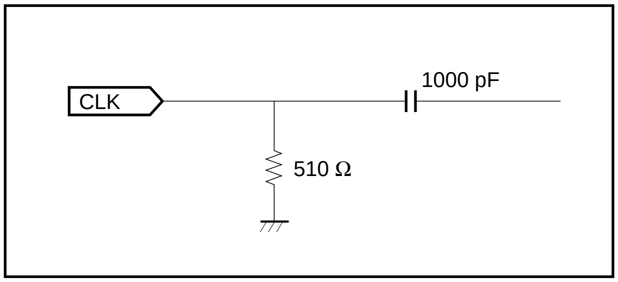
(1) Logic, LCD driving, Backlight

(Ta = 25 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	VDDB	11.4	12.0	12.6	V	for backlight
	VDD	11.4	12.0	12.6	V	for Logic and LCD driving
Logic input “L” voltage 1	ViL1	0	—	0.6	V	for BRTP
Logic input “H” voltage 1	ViH1	4.5	—	5.25	V	
Logic input “L” voltage 2	ViL2	0	—	0.8	V	for Logic except BRTP
Logic input “H” voltage 2	ViH2	2.2	—	5.25	V	
CLK input voltage	ViCLK	0.6	—	1.0	Vp-p	for CLK
CLK DC input level	ViDCCLK	–4.5	—	+4.5	V	
Logic input “L” current 1	IiL1	–10	—	—	μA	for HS and VS
Logic input “H” current 1	IiH1	—	—	160	μA	
Logic input “L” current 2	IiL2	–1400	—	—	μA	for CNTSEL, CPSEL, POWC, ADJSEL
Logic input “H” current 2	IiH2	—	—	10	μA	
Logic input “L” current 3	IiL3	–1.0	—	—	mA	for ACA
Logic input “H” current 3	IiH3	—	—	0.8	mA	
Logic input “L” current 4	IiL4	–1.0	—	—	mA	for BRTC, BRTLC, ACA, POSEL, BRTP
Logic input “H” current 4	IiH4	—	—	10	μA	
Logic input “L” current 5	IiL5	–10	—	—	μA	for Logic except above input
Logic input “H” current 5	IiH5	—	—	10	μA	
Supply current	IDDB	—	700	900	mA	VDDB = 12.0 V (Max. luminance)
Note	IDD	—	530	800	mA	VDD = 12.0 V

Note Dot - checkered pattern

(2) CLK input equivalent circuit



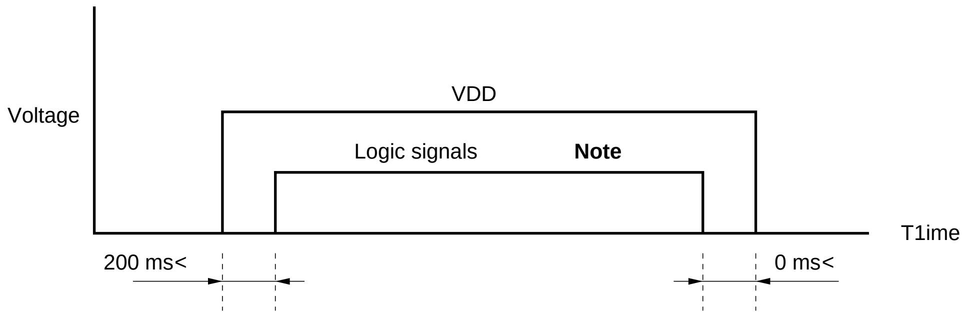
(3) Video signal (R, G, B) input

(Ta = 25 °C)

Item	Min.	Typ.	Max.	Unit	Remarks
Maximum amplitude (white - black)	0 (black)	0.7 (white)	0.9	Vp-p	Need to adjust the contrast in case of >0.7Vp-p
DC input level (black)	–3.5	—	+3.5	V	—

POWER SUPPLY

(1) Supply Sequence



Note Synchronous signal, Control signals and CLK

> **CAUTION**
> Wrong power sequence may damage to the module.

(a) Logic signals (synchronous signals and control signals) should be “0” voltage (V), when VDD is not input. If higher than 0.3 V is input to signal lines, the internal circuit will be damaged.

(b) LCD module will shut down the power supply of driving voltage to LCD panel internally, when one of CLK, Hsync, and Vsync, DE (at DE mode) is not input more than 90 ms typically. As the display data are unstable in this period, the display is disordered. But the backlight works correctly event this period. So the backlight ON/OFF should be controlled by BRTC signal.

(c) The ON/OFF switching of backlight while logic signals are supplied. The backlight power supply (VDDB) is not related to the power supply sequence. However, unstable data will be displayed when the backlight power is turned ON/OFF with no logic signals.

(d) Keep POWC signal “L” more than 200 ms after the power supply (VDD) is input, if POWC signal is controlled.

(e) Analog RGB input are independent from this power supply sequence.

(f) The power supply of backlight VDDB should be the rated voltage witin 80ms after turn-on. Otherwise, the protection circuit makes the backlight turn off.

(2) Ripple of supply voltage

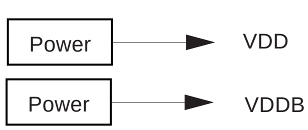
Please note that the ripple at the input connector of the module should be within the values shown below. If the ripple would be beyond these values, the noise might appear on the screen.

	VDD (for Logic and LCD driver)	VDDB (for Backlight)
Acceptable range	≤ 100 mVp-p	≤ 200 mVp-p

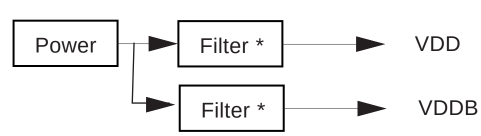
Note A coaxial cable shield should be connected with GND.

Example of rhe power supply connection

(a) Separate power supply



(b) Put filters

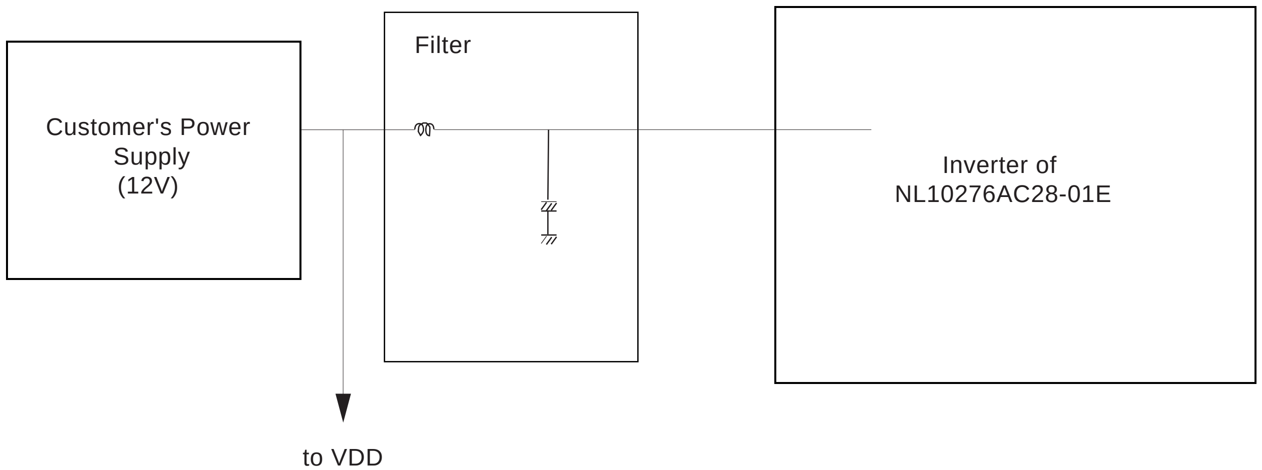


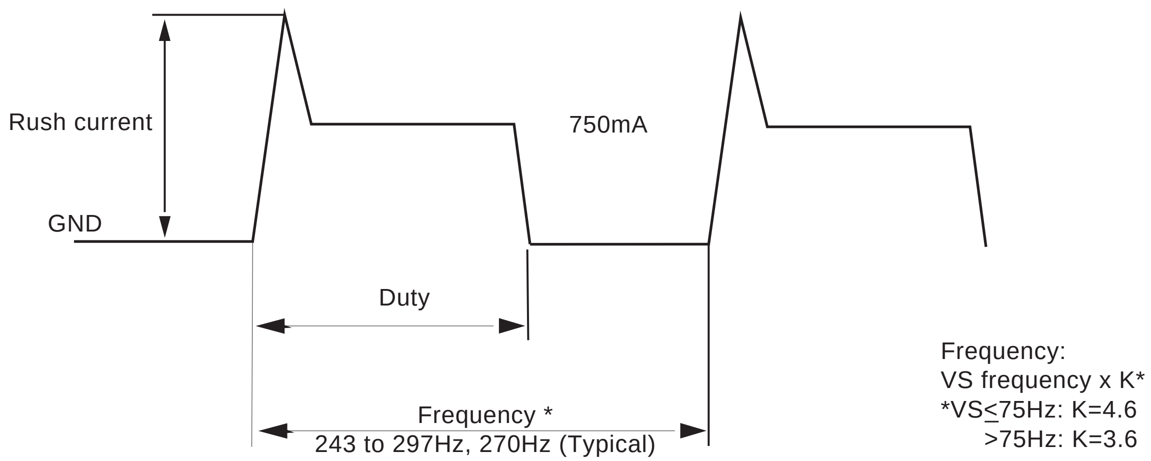
* Filter reference value
L = 10 mH to 100 mH
C = 10 mF to 100 mF

(3) Inverter Current Waveform

In the luminance control mode, the rush current below flows into the inverter of the module. The duty cycle varies from 100% through 30% depending on the luminance control level. This might cause the noise on the screen.

Please evaluate the appropriate value of the capacitor in the filter to eliminate the noise.





INTERFACE PIN CONNECTION

(1) CN1

Part No. : MRF03-6R-SMT
Adaptable socket : MRF03-2 × 6P-1.27 (For cable type) or MRF03-6PR-SMT (For board to board type)
Supplier : HIROSE ELECTRIC CO.,LTD. (coaxial type)

Coaxial cable : UL20537PF75VLAS
Supplier : HITACHI CO., LTD.

Note A coaxial cable shield should be connected with GND.

Pin No.	Symbol	Pin No.	Symbol
1	B	4	VS
2	G	5	HS/CS
3	R	6 ▼	CLK

Figure from socket view

▼
1 2 · · 5 6

(2) CN3

Part No. : IL-Z-15PL1-SMTY
Adaptable socket : IL-Z-15S-S125C3
Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	VDD	9	GND
2	VDD	10	CNTCLK
3	GND	11	CPSEL
4	GND	12	GND
5	POWC	13	GND
6	CNTSEL	14	N.C.
7	CNTDAT	15 ▼	GND
8	CNTSTB		

Note N.C. (No connection) should be open.

Figure from socket view

▼
15 14 · · · · 2 1

(3) CN4

Part No. : DF14A-20P-1.25H
Adaptable socket : DF14-20S-1.25C
Supplier : HIROSE ELECTRONIC CO., LTD

Pin No.	Symbol	Pin No.	Symbol
1	GND	11	ADJSEL
2	OSDENI	12	N.C.
3	GND	13	CNTSTB2
4	OSDBI	14	GND
5	GND	15	N.C.
6	OSDGI	16	GND
7	GND	17	N.C.
8	OSDRI	18	N.C.
9	GND	19	N.C.
10	N.C.	20 ▼	N.C.

Figure from socket view

▼
1 2 · · · 19 20

Note N.C. (No connection) should be open.

(4) CN201

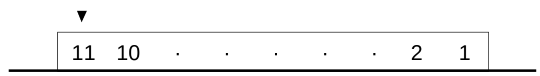
Part No. : IL-Z-11PL1-SMTY

Adaptable socket : IL-Z-11S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	VDDB	7	ACA
2	VDDB	8	BRTC
3	VDDB	9	BRTH
4	GNDB	10	BRTL
5	GNDB	11 ▼	N.C.
6	GNDB		

Figure from socket view



Note N.C. (No connection) should be open.

(5) CN202

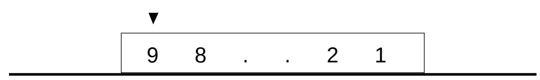
Part No. : IL-Z-9PL-SMTY

Adaptable socket : IL-Z-9S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	GNDB	6	BRTL
2	GNDB	7	BRTP
3	ACA	8	GNDB
4	BRTC	9 ▼	PWSEL
5	BRTH		

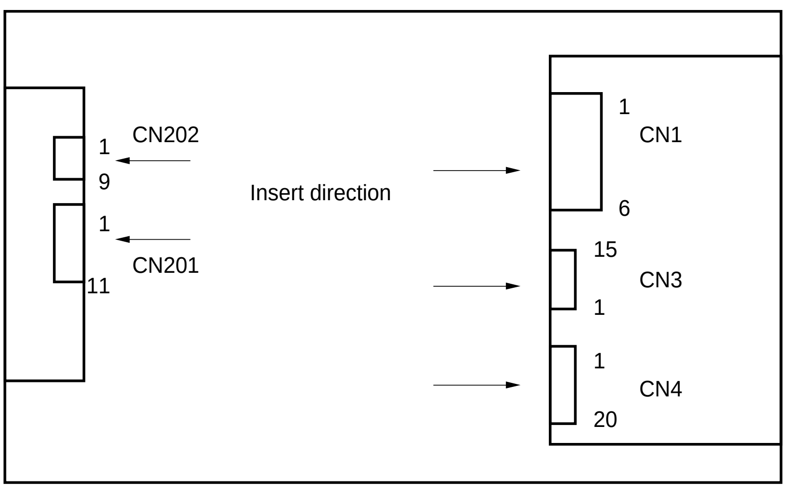
Figure from socket view



Note N.C. (No connection) should be open.

Caution: Use one of CN201 or CN202.

Rear view



PIN FUNCTION

Symbol	I/O	Logic	Description
CLK	Input	Negative	Dot clock input. (ECL level) This timing-signal is for display data.
HS/CS	Input	Negative	Horizontal synchronous signal input (TTL level)
VS	Input	Negative	Vertical synchronous signal input (TTL level)
R	Input	—	Red video signal input (0.7 Vp-p, 75 Ω)
G	Input	—	Green video signal input (0.7 Vp-p, 75 Ω)
B	Input	—	Blue video signal input (0.7 Vp-p, 75 Ω)
POWC	Input	Positive	Power control signal (TTL level) "H" or "Open" : Logic and LCD power are on. "L" : Logic and LCD power are off. When POWC is "L" , serial communication data is clear. Please set again. **Note 1**
CNTSEL	Input	—	Display control signal in case of serial communications. (TTL level) "H" or "Open": Default , "L": External control Serial communications set external control up.
CNTDAT	Input	Positive	Display control data (TTL level) Detail of CNTDAT is mentioned in **FUNCTIONS**.
CNTCLK	Input	Positive	CLK for display control data (TTL level) Detail of CNTCLK is mentioned in **FUNCTIONS**.
CNTSTB	Input	Positive	Latch pulse for display control data (TTL level) Detail of CNTSTB is mentioned in **FUNCTIONS**.
CPSEL	Input	—	Clamp signal function select signal (TTL level) "H" or "Open": Default, "L": External control
CLAMP	Input	Negative	Clamp timing signal of black level (TTL level) This mode works in CPSEL = "L".
ADJSEL	Input	Positive	Contrast, brightness select control signal (TTL level)
CNTSTB2	Input	Positive	Latch pulse 2 for display control data Detail of CNTSTB2 is mentioned in **FUNCTIONS**.
OSDRI	Input	---	Input OSD-R data. Detail of OSD-R is mentioned in **OSD FUNCTIONS**.
OSDGI	Input	---	Input OSD-G data. Detail of OSD-G is mentioned in **OSD FUNCTIONS**.
OSDRI	Input	---	Input OSD-R data. Detail of OSD-R is mentioned in **OSD FUNCTIONS**.
OSDENI	Input	Positive	Enable signal for OSD. Detail of OSDENI is mentioned in **OSD FUNCTIONS**.
ACA	Input	Positive	Luminance control signal (TTL level) "H" or "Open": Normal luminance "L" : Low luminance (1/2 of normal luminance)
BRTC	Input	Positive	Backlight ON/OFF control signal (TTL level) "H" or "Open": Backlight ON, "L": Backlight OFF
BRTH BRTL	Input	—	Variable resistor or Voltage controls Refer to the next page in detail.
BRTP	Input	—	Luminance control signal by Pulse Modulation Width. Refer to the next page.
PWSEL	Input	Positive	Select the control of luminance (TTL level) Refer to the next page.
VDD	—	—	Power supply for Logic and LCD driving +12 V (±5 %)
VDDB	—	—	Power supply for backlight. +12 V (±5 %)
GND	—	—	Signal ground for Logic and LCD driving (Connect to a system ground)
GNDB	—	—	Ground for backlight. GNDB is not connected to the flame ground of LCD module.

Notes 1. When POWC is "L" logic input signal is all "0 V". If input more than "0.3 V", inside circuits of the LCD module may be broken.

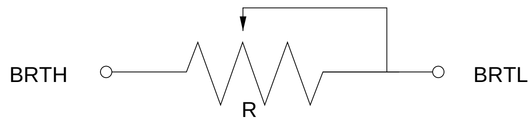
2 The frame ground, signal ground (GND) and backlight ground (GNDB) are not connected in the LCD module.

3 The power supply (VDDB) should rise the specific voltage within 80ms, otherise, the protection circuit makes the backlight off.

[FUNCTION SELECT]

Form	Terminal	How to adjust	
BRTP signal is "Valid"	PWSEL="L"	Luminance can be controlled by BRTP signal. Refer to **OUTSIDE CONTROL FOR LUMINANCE** in detail.	
BRTP signal should be "Open"	PWSEL="H" or "L"	Resistor	Please connect BRTH and BRTL with the variable resistor discribed as follows.
		Voltage	BRTH is "0V", and BRTL input voltage controls brightness. When BRTL input voltage is"1V", the luminance becomes maximum. And when BRTL input voltage is "0V', the luminance becomes minimum.

Notes 1. The variable resistor for luminance control should be 10 kΩ type, and zero point of the resistor corresponds to the minimum luminance.



Maximum luminance (100 %) : R = 10 kΩ
Minimum luminance (30 %) : R = 0 Ω

Mating variable resistor: 10 kΩ ±5 %, B curve

FUNCTIONS

This LCD module has following functions by serial data input (table 1)

(1) Display position control (VERTICAL) : See table 3
(2) Display position control(HORIZONTAL): See table 6
(3) CLK delay control : See table 4
(4) CLK fall/rise synchronous change : See table 5
(5) Contrast control
(6) Sub-Contrast control
(7) Sub-Brightness control
} See table 9, 10 and **COLOR CONTROL FUNCTION AND GRAPHIC IMAGE**

Set up the following items to work the above functions

(A) Expansion mode : See table 2 and **EXPANSION FUNCTION**
(B) CLK counts of horizontal period : See table 7
(C) CLK frequency range : See table 8

HOW TO USE THE FUNCTIONS

If CNTSEL is “L”, the above functions are valid. (CNTSEL is “H” or open, default values are valid.) After serial data are transferred, the data is latched by CNTSTB. Once, the data is latched, the above functions are effective. Please keep CNTSTB to be “L” during transferring data. Input data can be changed during power on, but LCD display may be disturbed. When the serial data are changed, we recommend that the backlight power is off using BRTC function.

HOW TO USE THE FUNCTIONS

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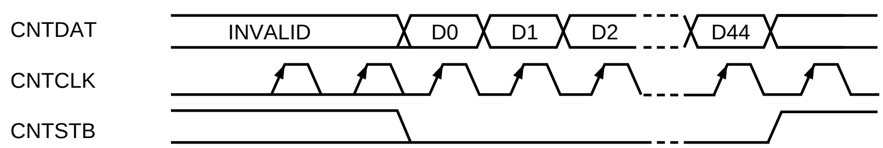
SERIAL COMMUNICATION TIMING AND WAVEFORM

SERIAL COMMUNICATION TIMING



Parameter	Symbol	Min.	Max.	Unit	Remark
CLK pulse-width	Twck	50	—	ns	CNTCLK
CLK frequency	Fclk	—	5	MHz	
DATA set-up-time	Tdst	50	—	ns	CNTDAT
DATA hold-time	Tdhl	50	—	ns	
Latch pulse-width	Twlp	50	—	ns	CNTSTB
Latch set-up-time	T1st	50	—	ns	
Rise/fall time	Tr, Tf	—	50	ns	CNT xxx

SERIAL COMMUNICATION WAVEFORM

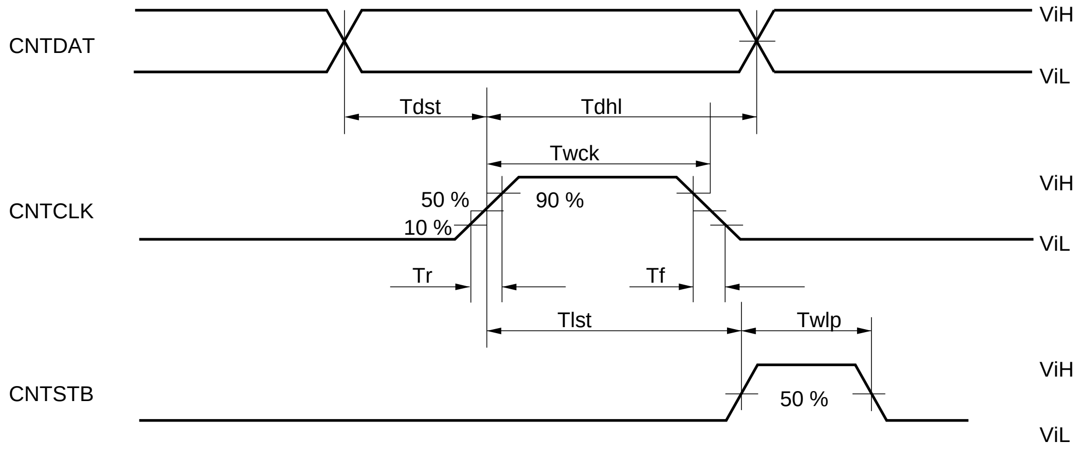


Table 1. CNTDAT Composition

DATA	DATA name	Function	
D0	VEX3	Expansion mode	See table 2
D1	VEX2	Expansion mode	
D2	VEX1	Expansion mode	
D3	VEX0	Expansion mode	
D4	VD10	Vertical display position (MSB)	See table 3
D5	VD9	Vertical display position	
D6	VD8	Vertical display position	
D7	VD7	Vertical display position	
D8	VD6	Vertical display position	
D9	VD5	Vertical display position	
D10	VD4	Vertical display position	
D11	VD3	Vertical display position	
D12	VD2	Vertical display position	
D13	VD1	Vertical display position	
D14	VD0	Vertical display position (LSB)	
D15	DELAY6	CLK delay (MSB)	See table 4
D16	DELAY5	CLK delay	
D17	DELAY4	CLK delay	
D18	DELAY3	CLK delay	
D19	DELAY2	CLK delay	
D20	DELAY1	CLK delay	
D21	DELAY0	CLK delay (LSB)	
D22	CK S	CLK reverse signal	See table 5
D23	HD8	Horizontal display position (MSB)	See table 6
D24	HD7	Horizontal display position	
D25	HD6	Horizontal display position	
D26	HD5	Horizontal display position	
D27	HD4	Horizontal display position	
D28	HD3	Horizontal display position	
D29	HD2	Horizontal display position	
D30	HD1	Horizontal display position	
D31	HD0	Horizontal display position (LSB)	
D32	HSE10	CLK count of horizontal period (MSB)	See table 7
D33	HSE9	CLK count of horizontal period	
D34	HSE8	CLK count of horizontal period	
D35	HSE7	CLK count of horizontal period	
D36	HSE6	CLK count of horizontal period	
D37	HSE5	CLK count of horizontal period	
D38	HSE4	CLK count of horizontal period	
D39	HSE3	CLK count of horizontal period	
D40	HSE2	CLK count of horizontal period	
D41	HSE1	CLK count of horizontal period	
D42	HSE0	CLK count of horizontal period (LSB)	
D43	MOD1	CLK frequency select	See table 8
D44	MOD0	CLK frequency select	
AD11	DAA0	Color adjust select data (LSB)	
AD10	DAA1	Color adjust select data	
AD9	DAA2	Color adjust select data	
AD8	DAA3	Color adjust select data (MSB)	
AD7	DAD7	Color adjust data (MSB)	
AD6	DAD6	Color adjust data	
AD5	DAD5	Color adjust data	
AD4	DAD4	Color adjust data	
AD3	DAD3	Color adjust data	
AD2	DAD2	Color adjust data	
AD1	DAD1	Color adjust data	
AD0	DAD0	Color adjust data (LSB)	

Table 2. Display Mode (VEX3 to VEX0: 4 bit)

VEX3	VEX2	VEX1	VEX0	Vertical magnification	Display mode	Display image
0	0	0	0	1	XGA	Standard **Note**
0	0	0	1	1.25	SVGA	
0	0	1	0	1.6	TEXT, PC98, VGA	
0	0	1	1	ó	Prohibit	
0	1	0	1	ó	Prohibit	
0	1	1	0	ó	Prohibit	
0	1	1	1	ó	Prohibit	
1	0	0	0	ó	Prohibit	See **DISPLAY IMAGE**
1	0	0	1	1.2	832 × 624 (MAC)	
1	0	1	0	ó	Prohibit	
1	0	1	1	ó	Prohibit	
1	1	0	0	ó	Prohibit	
1	1	0	1	ó	Prohibit	
1	1	1	0	ó	Prohibit	
1	1	1	1	ó	Prohibit	

Note When CNTSEL is ìHî or ìOpenî, display mode is XGA.

Table 3. Vertical Position (VD10 to VD0: 11 bit)

VD10	VD9	VD8	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0	Vertical position [H] **Note 1**
0	0	0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	0	0	1	Prohibit
0	0	0	0	0	0	0	0	0	1	0	Prohibit
0	0	0	0	0	0	0	0	0	1	1	Prohibit
0	0	0	0	0	0	0	0	1	0	0	4
0	0	0	0	0	0	0	0	1	0	1	5
∑	∑	∑	∑	∑	∑	∑	∑	∑	∑	∑	∑ ∑
∑	∑	∑	∑	∑	∑	∑	∑	∑	∑	∑	∑ ∑
∑	∑	∑	∑	∑	∑	∑	∑	∑	∑	∑	∑ ∑
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047 **Note 2**

Notes 1. This is horizontal line number for effective VIDEO signal from Vsync-fall.

2. The maximum vertical position is Vsync total.

3. When CNTSEL is ìHî or ìOpenî, vertical position is fixed at 35 [H].

Table 4. CLK Delay (DELAY6 to DELAY0: 7 bit)

DELAY[6..0]	Delay	Unit
00H	11.1	ns
01H	11.3	ns
02H	11.6	ns
03H	11.8	ns
04H	12.1	ns
05H	12.3	ns
06H	12.6	ns
07H	12.8	ns
08H	13.1	ns
09H	13.4	ns
0AH	13.6	ns
0BH	13.9	ns
0CH	14.1	ns
0DH	14.4	ns
0EH	14.6	ns
0FH	14.9	ns
10H	15.2	ns
11H	15.5	ns
12H	15.7	ns
13H	16.0	ns
14H	16.2	ns
15H	16.5	ns
16H	16.7	ns
17H	17.0	ns
18H	17.3	ns
19H	17.5	ns
1AH	17.8	ns
1BH	18.1	ns
1CH	18.3	ns
1DH	18.6	ns
1EH	18.8	ns
1FH	19.1	ns
20H	19.4	ns
21H	19.6	ns
22H	19.9	ns
23H	20.2	ns
24H	20.4	ns
25H	20.7	ns
26H	20.9	ns
27H	21.2	ns
28H	21.5	ns
29H	21.7	ns
2AH	22.0	ns
2BH	22.3	ns
2CH	22.5	ns
2DH	22.7	ns
2EH	23.0	ns
2FH	23.3	ns

DELAY[6..0]	Delay	Unit
30H	23.6	ns
31H	23.8	ns
32H	24.1	ns
33H	24.3	ns
34H	24.6	ns
35H	24.8	ns
36H	25.1	ns
37H	25.3	ns
38H	25.6	ns
39H	25.8	ns
3AH	26.1	ns
3BH	26.4	ns
3CH	26.6	ns
3DH	26.8	ns
3EH	27.1	ns
3FH	27.4	ns
40H	27.7	ns
41H	28.0	ns
42H	28.3	ns
43H	28.5	ns
44H	28.8	ns
45H	29.0	ns
46H	29.3	ns
47H	29.5	ns
48H	29.8	ns
49H	30.1	ns
4AH	30.3	ns
4BH	30.6	ns
4CH	30.8	ns
4DH	31.1	ns
4EH	31.3	ns
4FH	31.6	ns
50H	31.9	ns
51H	32.1	ns
52H	32.4	ns
53H	32.7	ns
54H	32.9	ns
55H	33.2	ns
56H	33.4	ns
57H	33.7	ns
58H	34.0	ns
59H	34.3	ns
5AH	34.5	ns
5BH	34.8	ns
5CH	35.0	ns
5DH	35.3	ns
5EH	35.5	ns
5FH	35.8	ns

DELAY[6..0]	Delay	Unit
60H	36.0	ns
61H	36.3	ns
62H	36.6	ns
63H	36.8	ns
64H	37.1	ns
65H	37.3	ns
66H	37.6	ns
67H	37.8	ns
68H	38.1	ns
69H	38.4	ns
6AH	38.7	ns
6BH	38.9	ns
6CH	39.2	ns
6DH	39.4	ns
6EH	39.7	ns
6FH	39.9	ns
70H	40.2	ns
71H	40.4	ns
72H	40.7	ns
73H	41.0	ns
74H	41.2	ns
75H	41.4	ns
76H	41.7	ns
77H	42.0	ns
78H	42.3	ns
79H	42.5	ns
7AH	42.8	ns
7BH	43.1	ns
7CH	43.3	ns
7DH	43.5	ns
7EH	43.8	ns
7FH	44.0	ns

Notes 1. When CNTSEL is "H" or "Open", DELAY[6..0] is fixed at 00H.

2. This delay value is typical value at Ta = 25 °C. By changing ambient temperature and power supply, the delay will be changed.

Please set up a preferable display position. See the following references.

<1> Variation of CLK delay by temperature drift. (as reference) The temperature constant of CLK delay is 0.2 %/°C.

Calculated example:

In case of delay time is 20 ns at Ta = 25 °C;

(a) In case Ta rising to 50 °C.

Increase of delay time → (50 °C ñ 25 °C) × 0.002 × 20 ns = +1 ns

So, the total delay time is 21 ns at Ta = 50 °C.

(b) In case Ta falling to 0 °C.

Decrease of delay time → (0 °C ñ 25 °C) × 0.002 × 20 ns = ñ1 ns

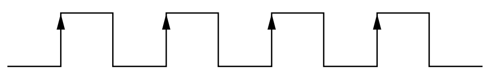
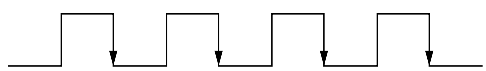
So, the total delay time is 19 ns at Ta = 0 °C.

<2> Variation of CLK delay time against each LCD module. (as reference)

ñ10.5 % to +14.4 %

	MOD setting			
	0, 0	0, 1	1, 0	1, 1
The upper limit of CLK delay; DELAY[6..0]	Prohibit	59H	6BH	7FH

Table 5. CLK Reverse Signal

CKS	FUNCTION
0	DATA is sampled on rising edge of CLK 
1	DATA is sampled on falling edge of CLK 

Note When CNTSEL is ìHî or ìOpenî, CKS is ì0î.

Table 6. Display Horizontal Position (HD8 to HD0: 9 bit)

HD8	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	Horizontal position [CLK] **Note 1**
0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	1	Prohibit
∑	∑	∑	∑	∑	∑	∑	∑	∑	∑
∑	∑	∑	∑	∑	∑	∑	∑	∑	∑
0	0	1	1	1	1	1	1	1	Prohibit
0	1	0	0	0	0	0	0	0	64
0	1	0	0	0	0	0	0	1	65
∑	∑	∑	∑	∑	∑	∑	∑	∑	∑
∑	∑	∑	∑	∑	∑	∑	∑	∑	∑
1	1	1	1	1	1	1	0	1	509
1	1	1	1	1	1	1	1	0	510
1	1	1	1	1	1	1	1	1	511

Notes 1. This is CLK number from Hsync-fall to effecting VIDEO signal.

2. When CNTSEL is ìHî or ìOpenî, Horizontal position is set at 296 [CLK].

Table 7. CLK Count of Horizontal Period (HSE10 to HSE0: 11 bit)

HSE10	HSE9	HSE8	HSE7	HSE6	HSE5	HSE4	HSE3	HSE2	HSE1	HSE0	CLK count **Note 1**
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047

Notes 1. This is CLK number from Hsync to next Hsync.
2. When CNTSEL is “H” or “Open”, CLK count is set at 1344 [CLK].
3. This CLK count must be equal to CLK count of input signal.

Table 8. CLK Frequency Select (MOD1 to MOD0: 2 bit)

MOD1	MOD0	CLK frequency [MHz]
0	0	Prohibit
0	1	65 to 80
1	0	50 to 65
1	1	20 to 50

Notes 1. Set up the MOD1 and MOD0 complying with input CLK frequency.
2. When CNTSEL is “H” or “Open”, CLK frequency is set 65 to 80 MHz.

Table 9. Color control data (DAD7 to DAD0: 8 bit)

DAD7	DAD6	DAD5	DAD4	DAD3	DAD2	DAD1	DAD0	Adjustment value
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	
1	1	1	1	1	1	0	1	253
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

Notes 1. The adjustment value for selecting function is above table.
2. Different D/A-range depends on the fucntion select.
3. See more detail on **Color control function and graph image**.

Table 10. Color adjust select data (DAA3 to DAA0: 4 bit)

DAA3	DAA2	DAA1	DAA0	Function
0	0	0	0	Prohibit
0	0	0	1	Main contrast
0	0	1	0	Prohibit
0	0	1	1	Prohibit
0	1	0	0	Sub-contrast R
0	1	0	1	Sub-contrast G
0	1	1	0	Sub-contrast B
0	1	1	1	Sub-brightness R
1	0	0	0	Sub-brightness G
1	0	0	1	Sub-brightness B
1	0	1	0	Prohibit
1	1	0	0	Prohibit
1	1	0	1	Prohibit
1	1	1	0	Prohibit
1	1	1	1	Prohibit

Notes 1. See more detail on **Color control function and graph image**.

EXPANSION FUNCTION

HOW TO USE EXPANSION MODE

Expansion mode is a function to expand screen. For example, VGA signal has 640 × 480 pixels. But, if the display data can expanded to 1.6 times vertically and horizontally, VGA screen image can be displayed fully on the screen of XGA resolution.

This LCD module has the function of expanding vertical direction as shown in Table 1. And expanding horizontal direction is possible by setting input CLK frequency which is equivalent to the magnification. It is necessary to make this CLK outside of this LCD module.

The below image is display example, when DE function is default and HD and VD is set to most suitable frequency. And when DE function is used, HD and VD become default. Adjustment the display to the best position by DE signal. Please adopt this mode after evaluating display quality, because the appearance of expansion mode is happened to become bad some cases.

The followings show display magnifications for each mode.

Input display	Number of pixels	Magnification	
		Vertical	Horizontal **Note**
XGA	1024 × 768	1	1
SVGA	800 × 600	1.25	1.25
VGA	640 × 480	1.6	1.6
VGA text	720 × 400	1.6	1.4
PC9801	640 × 400	1.6	1.6
MAC	832 × 624	1.2	1.2

Note The horizontal magnification multiples the input clock (CLK).
Input CLK = system CLK × horizontal magnification

Example In case of XGA and VGA, CLK frequency can be decided as follows.
XGA: (system CLK (65 MHz)) × 1.0 = 65 MHz
VGA: (system CLK (25.175 MHz)) × 1.6 = 40.28 MHz

SETTING SERIAL DATA

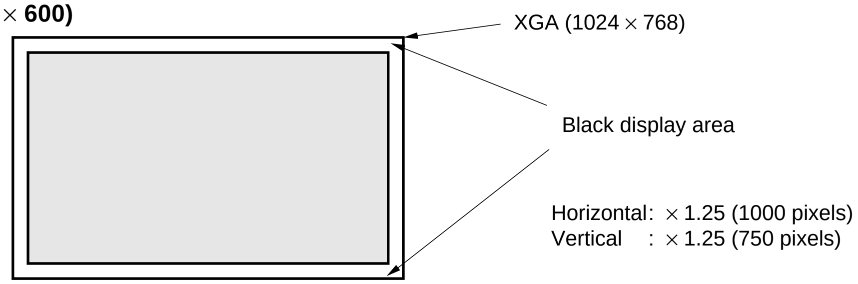
Input signal								Module serial data setting		
Mode	System CLK [MHz]	Hsync [kHz]	Vsync [Hz]	Horizontal		Vertical		HSE	HD	VD
				Count number [CLK]	DSP* [CLK]	Count number [H]	DSP* [H]	Calculation formula		
				(A)	(B)	ó	(C)	(A) × Ver. mag.	(B) × Hor. mag.	= (C)
XGA (1024 × 768)	65	48.363	60.004	1344	296	806	35	(A) × 1	(B) × 1	= (C)
	75	56.476	70.069	1328	280	806	35			
	78.75	60.023	75.029	1312	272	800	31			
MAC (832 × 624)	57.283	49.725	74.5	1152	288	667	42	(A) × 1.2	(B) × 1.2	
SVGA (800 × 600)	36*	35.156	56.25	1024	200	625	24	(A) × 1.25	(B) × 1.25	
	40*	37.879	60.317	1056	216	628	27			
	50*	48.077	72.188	1040	184	666	29			
	49.5*	46.875	75	1056	240	666	24			
VGA (640 × 480)	25.175*	31.469	59.94	800	144	525	35	(A) × 1.6	(B) × 1.6	
	31.5*	37.861	72.809	832	168	520	31			
	31.5*	37.5	75	840	184	500	19			
	30.24*	35.0	66.667	864	160	525	42			
VGA text (720 × 400)	28.322*	31.469	70.087	900	153	449	37	(A) × 1.4	(B) × 1.4	
	31.5*	37.927	85.04	936	180	446	45			
PC9801 (640 × 400)	21.053*	24.827	56.432	848	144	440	33	(A) × 1.6	(B) × 1.6	443

***** DSP = Display Start Period. DSP is the total of ìpulse-widthî and ìback-porchî.

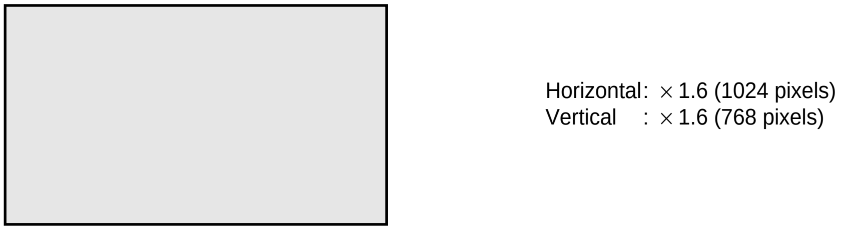
Notes 1. HD and VD are approximate value. Set HD and VD in case of adjusting display to the screen center.
2. The pulse-width of Hsync, Vsync and back-porch are the same as XGA-mode. (Standard-mode).
3. HSE see CLK number of Table 7.
4. HD see horizontal position of Table 6.
5. VD see vertical position of Table 3.

DISPLAY IMAGE

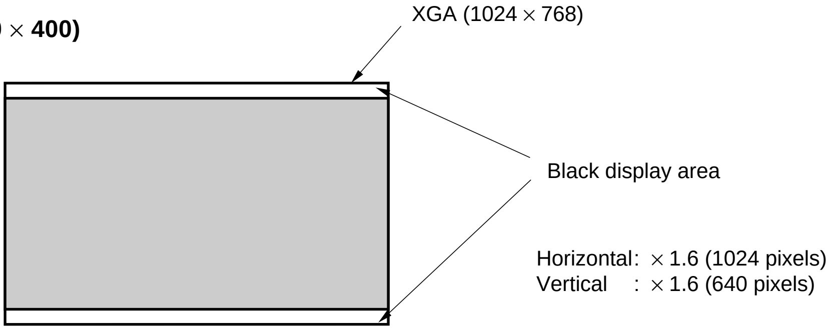
1) SVGA mode (800 × 600)



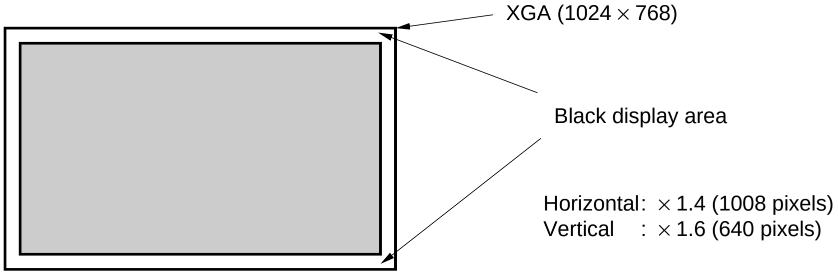
2) VGA mode (640 × 480)



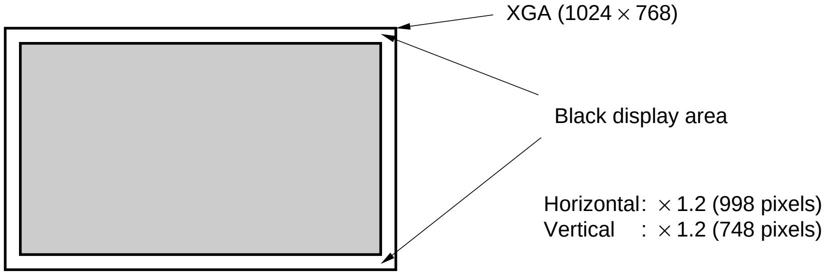
3) PC9801 mode (640 × 400)



4) VGA text mode (720 × 400)



5) 832 × 624 MAC mode (832 × 624)



COLOR CONTROL FUNCTION AND GRAPH IMAGE

This LCD module can adjust the following fucntions by serial data input (Table 1)
(1) Main contast:
(2) Sub-contrast each R, G, B:
(3) Sub-brightness each R, G, B:

(1) Main Contrast
Main contrast adusts R/G/B contrast simalteniously. Contrast controls the amplitude of input video signal.
Defalut value: 128, Valid range: 78 to 198
Contrast minimum: 198
Contrast maximum: 78
ADJSEL="H" or "Open": Main contrast =128

(2) Sub-contrast R, G, B
Sub-contrast adjusts each R/G/B. Sub-ontrast controls each amplitude of input video signal.
Default value: 128, Valid range: 78 to 198
Contrast minimum: 198
Contrast maximum: 78
ADJSEL="H" or "Open": Main contrast=128

(3) Sub-brightness R, G, B
Sub-brightness adjusts each R/G/B. Brightness adjusts the black level of input video signal.
Default value: 128, Valid range: 55 to 163
Brightness minimum: 55
Brightness maximum: 163
ADJSEL="H" or "Open": Main contrast=128

Note1: If the LCD module is used over the above valid range, it will not be destroied. However, it will be inferiority.
Please set each values within the specifed range.
Note 2:

COLOR CONTROL FUNCTION AND GRAPH IMAGE

Expansion mode is a function to expand screen. For example, VGA signal has 640 × 480 pixels. But, if the display

COLOR CONTROL FUNCTION AND GRAPH IMAGE

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COLOR CONTROL FUNCTION AND GRAPH IMAGE

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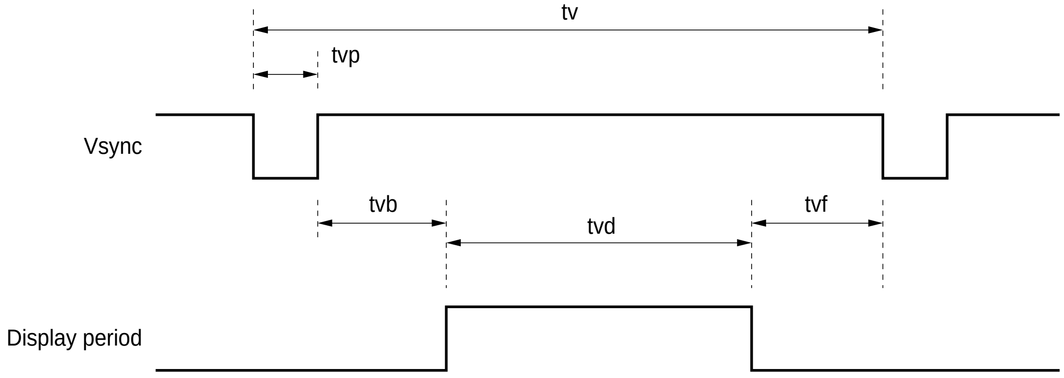
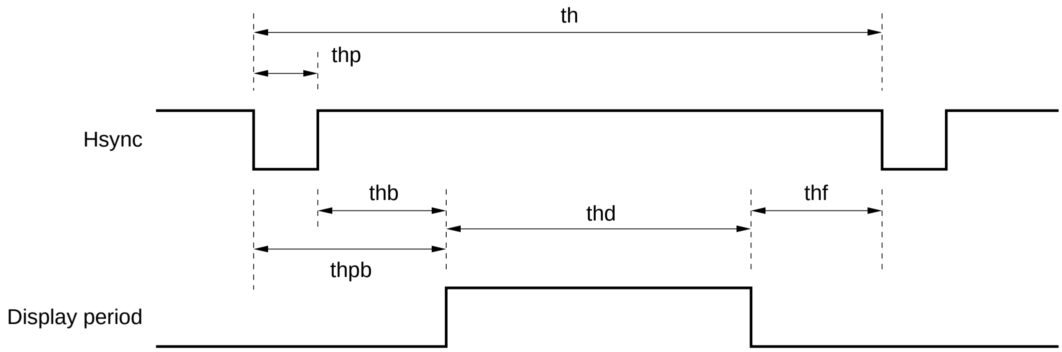
INPUT SIRIAL TIMING

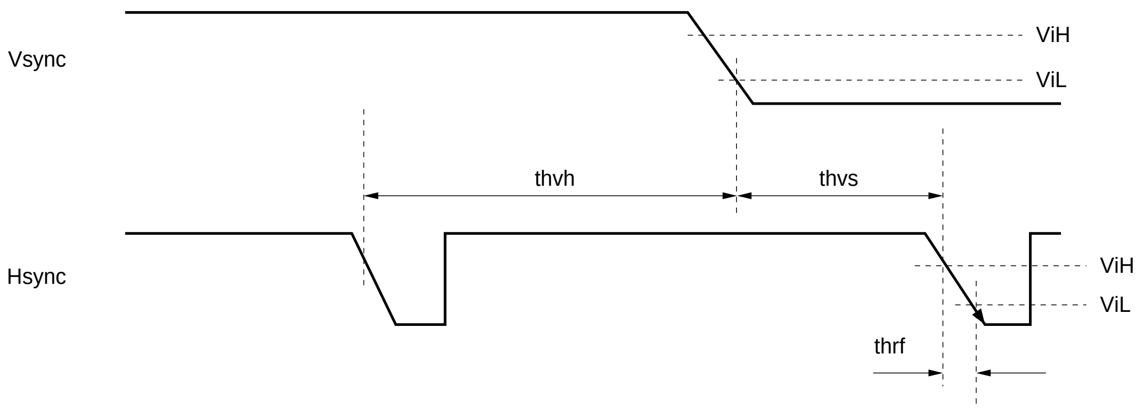
XGA MODE (STANDARD)

	Name	Symbol	Min.	Typ.	Max.	Unit	Remark
CLK	Frequency	1/tc	52.0 ó	65.0 15.385	79.0 ó	MHz ns	XGA standard
	Rise / Fall	tcrf	ó	ó	10	ns	ó
	Pulse-width	tcl/tc	0.4	0.5	0.6	ó	ó
Hsync	Period	th	16.0 ó	20.677 1344	22.7 ó	μs CLK	48.363 kHz (typ.)
	Display	thd	ó ó	15.754 1024	ó ó	μs CLK	ó
	Front-porch	thf	ó 10	0.369 24	ó ó	μs CLK	ó
	Pulse-width	thp	ó 16	2.092 136	ó ó	μs CLK	ó
	Back-porch	thb	1.0 44	2.462 160	ó ó	μs CLK	**Note**
	Pulse-width + Back-porch	thpb	1.8	ó	ó	μs	ó
	Vsync ñ Hsync timing	thvh	4	ó	ó	ns	ó
		thvs	1	ó	ó	CLK	ó
	Rise / Fall	thrf	ó	ó	10	ns	ó
Vsync	Period	tv	13.3 ó	16.665 806	18.5 ó	ms H	60.004 Hz (typ.)
	Display	tvd	ó ó	15.880 768	ó ó	μs H	ó
	Front-porch	tvf	ó 1	62.031 3	ó ó	μs H	ó
	Pulse-width	tvp	ó 2	124.06 6	ó ó	μs H	ó
	Back-porch	tvb	ó 5	599.63 29	ó ó	μs H	ó
DE	Set-up time	tds	2	ó	ó	ns	ó
	Hold time	tdh	4	ó	ó	ns	ó
	Rise / Fall	tdrf	ó	ó	10.0	ns	ó
Analog R, G, B	ó	tda	4	ó	ó	ns	ó

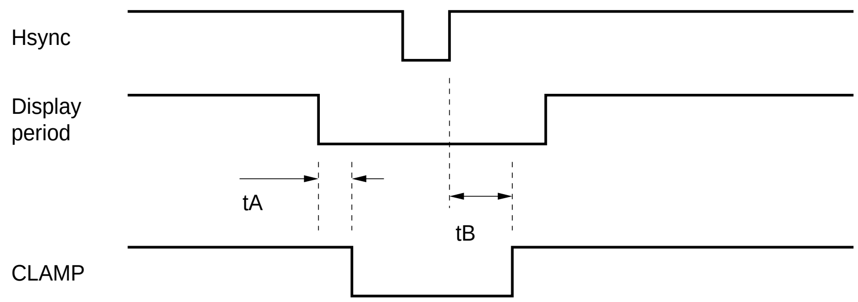
Note Minimum values of Back-porch (thb) must be satisfied with both 1.0 μs and 44 CLK.


tv
tvp
Vsync
tvb
tvd
tvf
Display period


th
thp
Hsync
thb
thd
thf
thpb
Display period


Vsync
ViH
ViL
thvh
thvs
Hsync
ViH
ViL
thrf

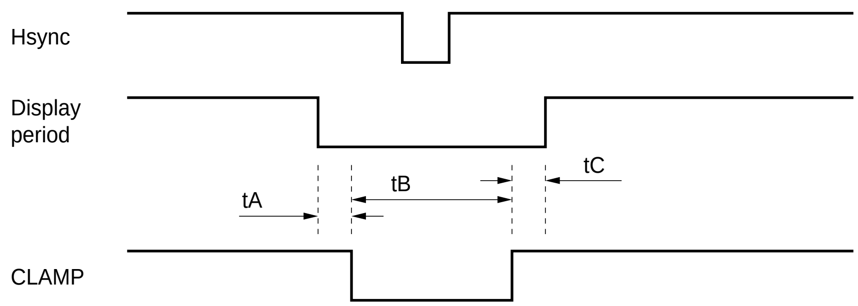
TIMING FOR GENERATING CLAMP SIGNAL INTERNALLY



MOD1	MOD2	tA [CLK]	tB [ns]
0	0	Prohibit	
0	1	2	27
1	0	2	20
1	1	2	15

Note Exclude noises on analog R, G, B signal, because analog R, G, B signals are the black level reference during CLAMP = "L". If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

TIMING FOR INPUTING CLAMP SIGNAL FROM OUTSIDE



Item	Min.	Typ.	Max.	Unit	Remarks
tA	0.1	—	—	μs	—
tB	0.3	—	—	μs	—
tC	0.2	—	—	μs	—

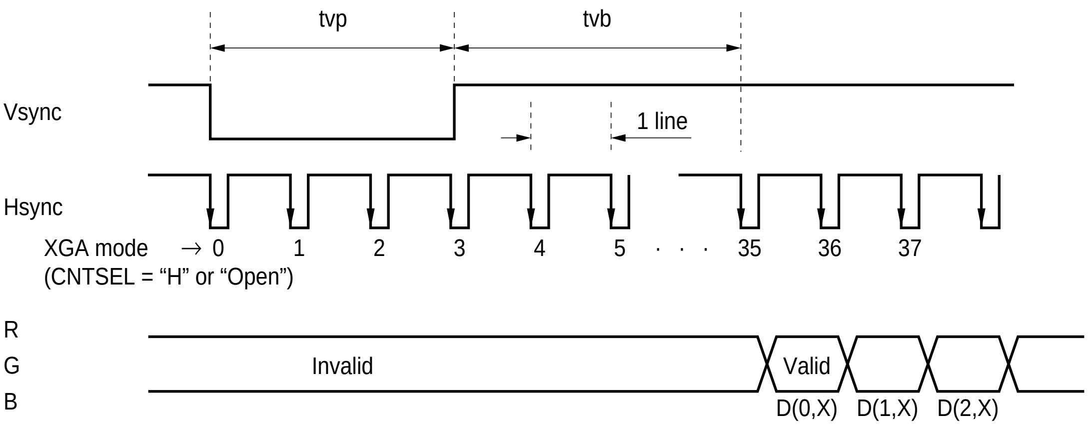
Note Exclude noises on analog R, G, B signal, because analog R, G, B signals are the black level reference during CLAMP = "L". If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

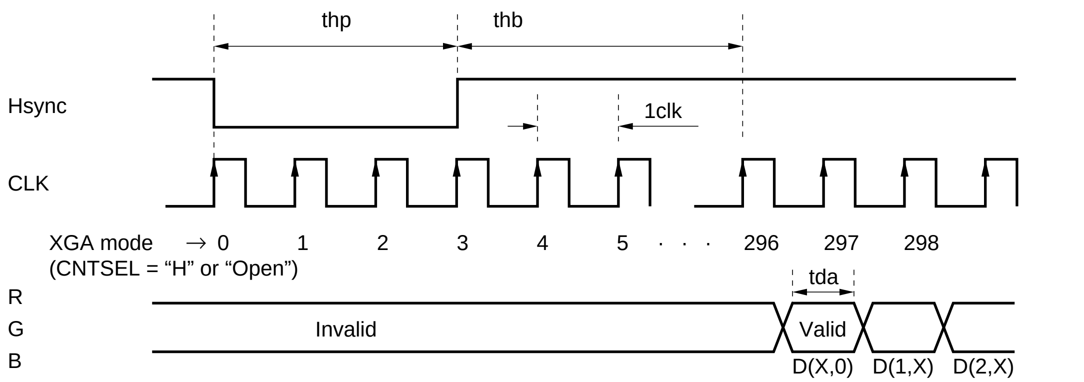
INPUT SIGNAL AND DISPLAY POSITION

XGA standard timing

Pixels

D(0,0)	D(0,1)	D(0,2)	· · ·	· · ·	D(0,1023)
D(1,0)	D(1,1)	D(1,2)	· · ·	· · ·	D(1,1023)
D(2,0)	D(2,1)	D(2,2)	· · ·	· · ·	D(2,1023)
· · · ·	· · · ·	· · · ·			· · · ·
D(767,0)	D(767,1)	D(767,2)	· · ·	· · ·	D(767,1023)





Note tda should be minimum 4ns

OPTICAL CHARACTERISTICS

(Ta = 25 °C, VDD = 12 V, VDDB = 12 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Contrast ratio	CR	Best contrast angle θR = 0°, θL = 0°, θU = 7°, White/Black	—	300	—	—	**Note 1**
		γ = 2.2 viewing angle θR = 0°, θL = 0°, θD = 5°, White/Black	80	150	—	—	
Luminance	Lvmax	White	150	200	—	cd/m^2	**Note 2**
Luminance uniformity	—	White	—	—	1.30	—	**Note 3**
Color gamut	C	θR = 0°, θL = 0°, θU = 0° θD = 0°, At center, to NTSC	35	40	—	%	
Response time	Ton	White to black	—	11	25	ms	**Note 4**
	Toff	White to black	—	40	80	ms	

Reference data

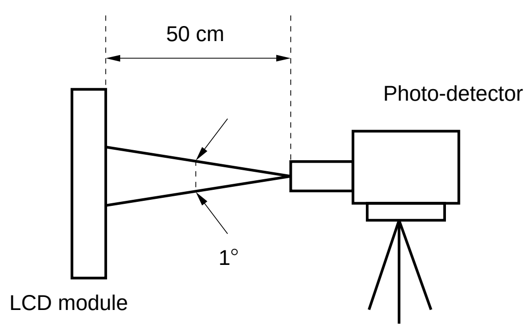
(Ta = 25 °C, VDD = 12 V, VDDB = 12 V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Chromaticity Coordinates	W	White (x, y)		—	0.30, 0.31	—	—
	R	Red (x, y)		—	0.57, 0.33	—	—
	G	Green (x, y)		—	0.32, 0.51	—	—
	B	Blue (x, y)		—	0.15, 0.11	—	—
Viewing angle range	θR	CR > 10, θU = 0°, θD = 0°		40	50	—	deg.
	θL			40	50	—	deg.
	θU	CR > 10, θR = 0°, θL = 0°		15	20	—	deg.
	θD			25	35	—	deg.
Luminance control range by BRTH/BRTL	—	Maximum luminance: 100 %	ACA = H	—	30 to 100	—	%
			ACA = L	—	40 to 100	—	

Notes 1. The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance with all pixels in “white”}}{\text{Luminance with all pixels in “black”}}$$

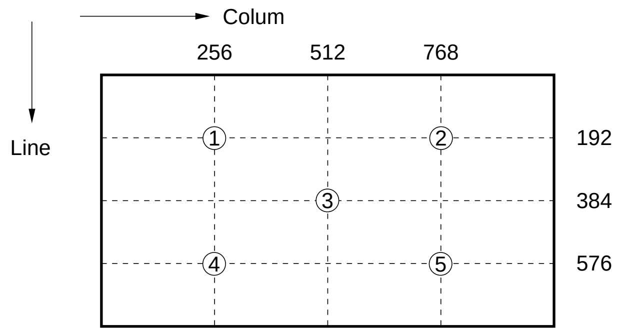
2. The luminance is measured after 20 minutes from the module works, with all pixels in “white”. The typical value is measured after luminance saturation.



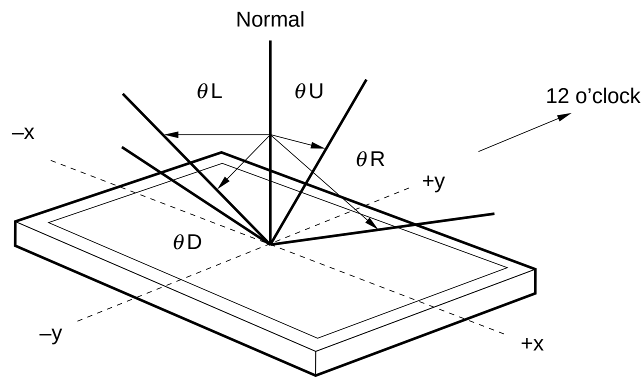
Notes 3. Luminance uniformity is calculated by using the following formula.

$$\text{Luminance uniformity} = \frac{\text{Maximum luminance}}{\text{Minimum luminance}}$$

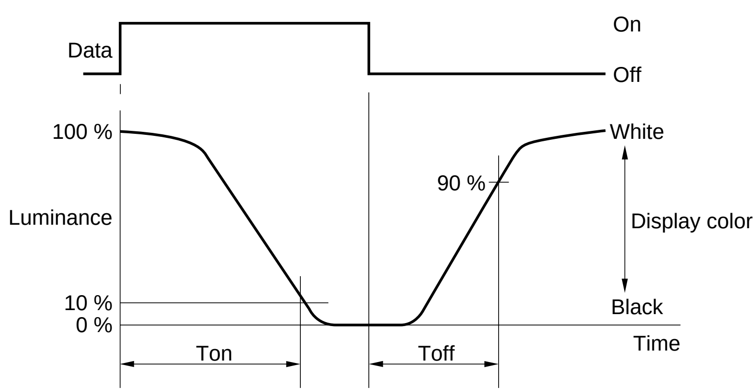
The luminance is measured at near the five points shown below.



4. Definitions of viewing angle are as follows.



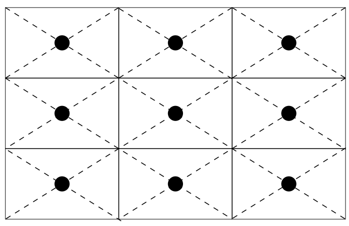
5. Definitions of response time is as follows.
Photo-detector out put signal is measured when the luminance changes "white" to "black". Response time is the time between 10 % and 100 % of the photo-detector output amplitude.



RELIABILITY TEST

Test item	Test condition
High temperature/humidity operation **Note 1**	50 ± 2°C, 85% relative humidity 240 hours Display data is black.
Heat cycle (operation) **Note 1**	<1> 0°C ± 3°C ··· 1 hour 55°C ± 3°C ··· 1 hour <2> 50 cycles, 4 hours/cycle <3> Display data is black.
Thermal shock (non-operation) **Note 1**	<1> –20°C ± 3°C ··· 30 minutes 60°C ± 3°C ··· 30 minutes <2> 100 cycles <3> Temperature transition time within 5 minutes
Vibration (non-operation) **Notes 1, 2**	<1> 5 - 100 Hz, 2G 1 minute/cycle X, Y, Z direction <2> 50 times each direction
Mechanical shock (non-operation) **Notes 1, 2**	<1> 55 G, 11 ms X, Y, Z direction <2> 3 times each direction
ESD (operation) **Notes 1, 3**	150 pF, 150 Ω, ±10 kV 9 places on a panel 10 times each place at one-second intervals
Dust (operation) **Note 1**	15 kinds of dust (JIS Z 8901) Hourly 15 seconds stir, 8 times repeat

Notes 1. Display function is checked by the same condition as LCD module out-going inspection.
2. Physical damage.
3. Discharge points "●" are shown in the figure.



Next figures and sentence are very important. Please understand these, then read the text of a book.

CAUTION This figure is a mark that you will get hurt and/or the module will have damages when you make a mistake to operate.

	This figure is a mark that you will get an electric shock when you make a mistake to operate.
	This figure is a mark that the LCD module will give out smoke or catch fire when you make a mistake to operate.
	This figure is a mark that you will get hurt when you make a mistake to operate.

CAUTION

Do not touch an inverter --on which is stuck a caution label-- while the LCD module is under the operation, because of dangerous high voltage.

(1) Caution when taking out the module

<1> Pick the pouch only, in taking out module from a carrier box.

(2) Caution for handling the module

<1> As the electrostatic discharges may break the LCD module, handle the LCD module with care against electrostatic discharges.

<2> As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.

<3> As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.

<4> Do not pull the interface connectors in or out while the LCD module is operating.

<5> Put the module display side down on a flat horizontal plane.

<6> Handle connectors and cables with care.

<7> When the module is operating, do not lose CLK, Hsync, or Vsync signal. If any one of these signals is lost, the LCD panel would be damaged.

<8> The torque of mounting screw should be 0.392 N·m (4 Kgf·cm) less.

(3) Caution for the atmosphere

<1> Dew drop atmosphere should be avoided.

<2> Do not store and/or operate the LCD module in a high temperature and/or high humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

<3> This module uses cold cathode fluorescent lamps. Therefore, the life time of lamps becomes short conspicuously at low temperature.

<4>  Do not operate the LCD module in a high magnetic field.

(4) Caution for the module characteristics

<1> Do not apply fixed pattern data signal to the LCD module at product aging. Applying fixed pattern for a long time may cause image sticking.

(5) Other cautions

<1> Do not disassemble and/or reassemble LCD module.

<2> Do not readjust variable resistor or switch etc.

<3> When returning the module for repair or etc., please pack the module not to be broken. We recommend to the original shipping packages.

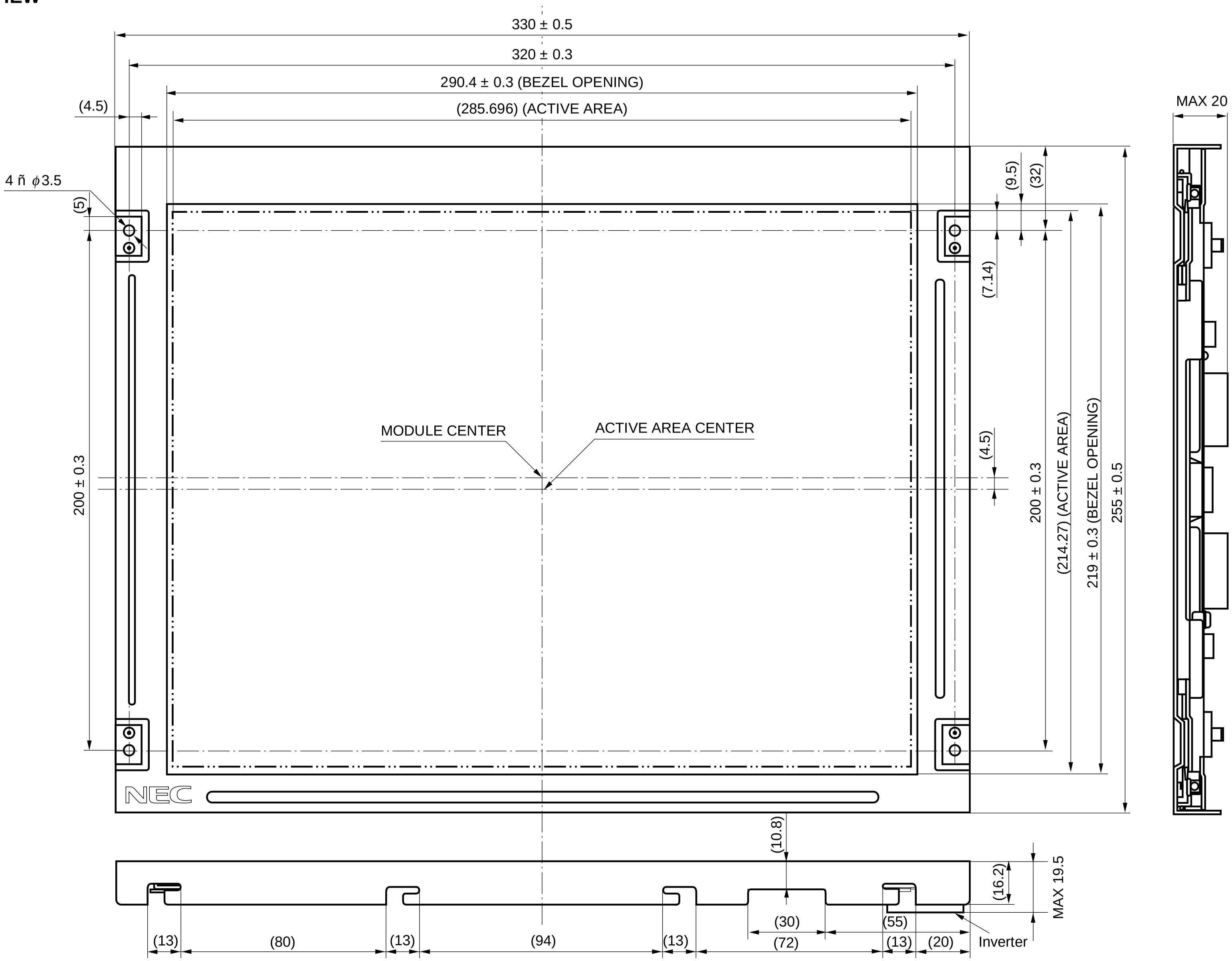
Liquid Crystal Display has the following specific characteristics. There are not defects or malfunctions.

The display condition of LCD module may be affected by the ambient temperature.
The LCD module uses cold cathode tube for backlight. Optical characteristics, like luminance or uniformity, will change during time.

Uneven brightness and/or small spots may be noticed depending on different display patterns.

OUTLINE DRAWING (Unit in mm)

FRONT VIEW

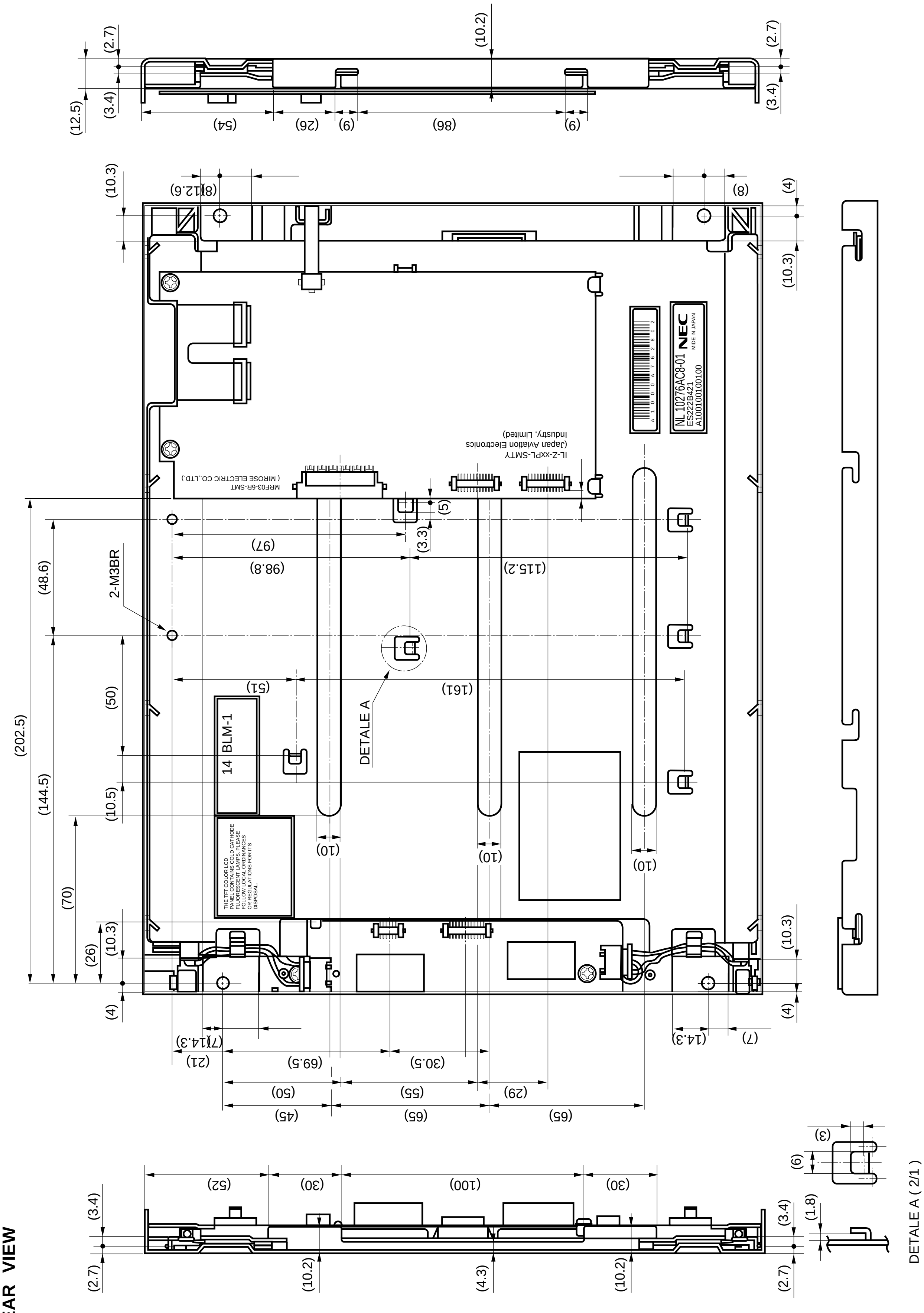


Notes 1. The value in parentheses are for reference.

2. The torque to mounting screw should never exceed 0.392 N∑m (4 Kgf∑m).

OUTLINE DRAWING (Unit in mm)

REAR VIEW



[MEMO]