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The CS5322 Digital Filter

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Delta-Sigma A/D converters have become widely accepted by data acquisition designers because of their high performance. One of the highest dynamic range Delta-Sigma converters is the Crystal Semiconductor CS5321/CS5322 chip set. The CS5321 is a fourth order modulator. The CS5322 is a linear phase FIR decimation filter. The purpose of this Technical Brief is to compare the architecture of a general purpose DSP chip with that of the CS5322.

General purpose DSPs are available which support either fixed-point arithmetic or floating-point arithmetic. Fixed-point processors are lower cost but floating-point processors have more horsepower. Fixed point processors work with either 16, 20, or 24-bit data words, while floating-point processors operate with 32-bit data words. The size of the data word greatly influences the cost of the chip and the cost of the overall system. This is because data word length determines the size of the registers used in the processor, the number of pins required on the package, and the word-width of the external memory. If low cost is the number one goal in a DSP design, the designer will specify a DSP which has the smallest word size that the application can tolerate.

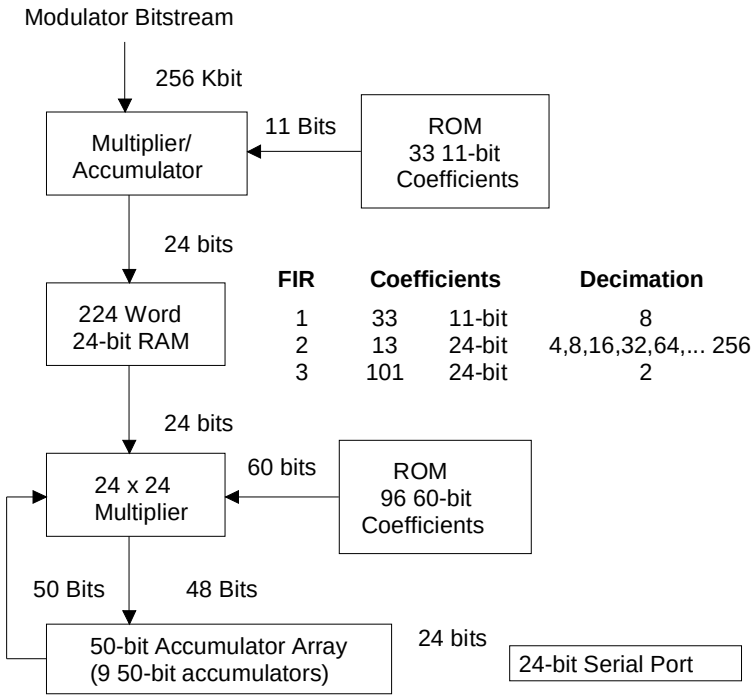

Figure 1. Digital Filter Block Diagram

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Output Word Rate(Hz) (CLKIN = 1.024 MHz)	-3dB Bandwidth (Hz)	Dynamic Range* (dB)
4000	1652.3	103
2000	824.3	118
1000	411.9	120
500	205.9	123
250	102.9	126
125	51.5	128
62.5	25.7	130

* Modulator and Filter Combination; limited by the modulator

Table 1 CS5322 Filter Bandwidth Selections

Most general purpose processors, whether they be fixed-point, or floating point, use a central ALU (Arithmetic Logic Unit), through which all processing occurs.

The CS5322 is a "signal processing chip" which performs a dedicated FIR low pass filter function. Figure 1 illustrates the block diagram of the CS5322. When the CS5322 is operated from a 1.024 MHz clock, the filter provides seven deferent selectable decimation rates as shown in Table 1. The -3 dB bandwidth of each decimation rate is approximately 82% of the nyquist frequency. The filter achieves a minimum of 130 dB attenuation at the nyquist frequency for all filter selections.

The filter offers selection of any one of seven filter frequencies by means of hardware pins on the chip or by means of writing a control word into the configuration register via the serial port.

The CS5322 is architecturally quite different from a general purpose DSP. The CS5322 contains three FIR filter stages. The 256 kHz 1-bit stream from the modulator enters FIR1 and is multiplied by 33 11-bit coefficients. The bit stream is decimated by eight as it is processed and the output data is placed in RAM. FIR2 and FIR3 are executed using a common multiplier. FIR2 is a 13 coefficient (24-bit) variable decimation stage. FIR2 can be programmed to decimate at rates of 4, 8, 16, 32, 64, 128, and 256. Computations for FIR2 are processed in a low power 24-bit by 24-bit multiplier and accumulated in eight successive 50-bit accumulators. The decimation rate is controlled by the choice of which of the accumulators feeds back to the multiplier. The output of FIR2 is then processed by the 24-bit by 24-bit multiplier and accumulated in a ninth 50-bit accumulator. The decimate by 2 output result of FIR3 is placed into the 24-bit serial port register in two's complement format.

Each of the seven filter output selections is designed to ensure that, given an impulse input, that one of the output words will provide a sample point at the peak of the impulse response. Because of this design feature, the clock cycle lengths of each of the actual seven filters are not binary multiples of each other. Instead, the filters are designed to buffer input data (each filter has a different buffer length to ensure it provides a sample at the impulse peak) to facilitate proper operation. The filter is designed that to the user the filters actually take

c1(1)=0.0d0	c1(12)=204.0d0	c1(23)=161.0d0
c1(2)=0.0d0	c1(13)=246.0d0	c1(24)=120.0d0
c1(3)=1.0d0	c1(14)=284.0d0	c1(25)=84.0d0
c1(4)=4.0d0	c1(15)=315.0d0	c1(26)=56.0d0
c1(5)=10.0d0	c1(16)=336.0d0	c1(27)=35.0d0
c1(6)=20.0d0	c1(17)=344.0d0	c1(28)=20.0d0
c1(7)=35.0d0	c1(18)=336.0d0	c1(29)=10.0d0
c1(8)=56.0d0	c1(19)=315.0d0	c1(30)=4.0d0
c1(9)=84.0d0	c1(20)=284.0d0	c1(31=1.0d0
c1(10)=120.0d0	c1(21)=246.0d0	c1(32)=0.0d0
c1(11)=161.0d0	c1(22)=204.0d0	c1(33 =0.0d0

Table 2. FIR1 Filter Coefficients

c2(1)=8192.0d0	c2(6)=6488064.0d0	c2(11)=540672.0d0
c2(2)=98304.0d0	c2(7)=7569408.0d0	c2(12)=98304.0d0
c2(3)=540672.0d0	c2(8 =6488064.0d0	c2(13)=8192.0d0
c2(4)=1802240.0d0	c2(9)=4055040.0d0	
c2(5)=4055040.0d0	c2(10)=1802240.0d0	

Table 3. FIR2 Filter Coefficients

binary multiples of clock cycles relative to each other, going from slowest to the fastest, but because of the internal data buffering the filter actually takes one more filter output word to settle than a strict analysis of the filter coefficients would imply. The filter settles to full accuracy to a input step in 57 output words.

Tables 2, 3 and 4 list the filter coefficients for the three FIR filter stages.

The CS5322 digital filter consumes only 11 milliwatt power although it consist of approximately 76,000 transistors. An analog filter of comparable complexity would consist of over 233,000 reactive elements.

c3(1)=-26.0d0	c3(35)=139856.0d0	c3(69)=-175718.0d0
c3(2)=-247.0d0	c3(36)=270573.0d0	c3(70)=43678.0d0
c3(3)=-822.0d0	c3(37)=-29083.0d0	c3(71)=156296.0d0
c3(4)=-1362.0d0	c3(38)=-360427.0d0	c3(72)=33416.0d0
c3(5)=-839.0d0	c3(39)=-162173.0d0	c3(73)=-106905.0d0
c3(6)=1012.0d0	c3(40)=371807.0d0	c3(74)=-71982.0d0
c3(7)=2197.0d0	c3(41)=417807.0d0	c3(75)=51056.0d0
c3(8)=212.0d0	c3(42)=-246840.0d0	c3(76)=77065.0d0
c3(9)=-3443.0d0	c3(43)=-693181.0d0	c3(77)=-5404.0d0
c3(10)=-3077.0d0	c3(44)=-78388.0d0	c3(78)=-60427.0d0
c3(11)=3156.0d0	c3(45)=902497.0d0	c3(79)=-22177.0d0
c3(12)=7168.0d0	c3(46)=685231.0d0	c3(80)=35194.0d0
c3(13)=-256.0d0	c3(47)=-865217.0d0	c3(81)=31641.0d0
c3(14)=-10709.0d0	c3(48)=-1713558.0d0	c3(82)=-11826.0d0
c3(15)=-7644.0d0	c3(49)=-262.0d0	c3(83)=-28007.0d0
c3(16)=10713.0d0	c3(50)=3276208.0d0	c3(84)=-3873.0d0
c3(17)=18055.0d0	c3(51)=4950471.0d0	c3(85)=18055.0d0
c3(18)=-3873.0d0	c3(52)=3276208.0d0	c3(86)=10713.0d0
c3(19)=-28007.0d0	c3(53)=-262.0d0	c3(87)=-7644.0d0
c3(20)=-11826.0d0	c3(54)=-1713558.0d0	c3(88)=-10709.0d0
c3(21)=31641.0d0	c3(55)=-865217.0d0	c3(89)=-256.0d0
c3(22)=35194.0d0	c3(56)=685231.0d0	c3(90)=7168.0d0
c3(23)=-22177.0d0	c3(57)=902497.0d0	c3(91)=3156.0d0
c3(24)=-60427.0d0	c3(58)=-78388.0d0	c3(92)=-3077.0d0
c3(25)=-5404.0d0	c3(59)=-693181.0d0	c3(93)=-3443.0d0
c3(26)=77065.0d0	c3(60)=-246840.0d0	c3(94)=212.0d0
c3(27)=51056.0d0	c3(61)=417807.0d0	c3(95)=2197.0d0
c3(28)=-71982.0d0	c3(62)=371807.0d0	c3(96)=1012.0d0
c3(29)=-106905.0d0	c3(63)=-162173.0d0	c3(97)=-839.0d0
c3(30)=33416.0d0	c3(64)=-360427.0d0	c3(98)=-1362.0d0
c3(31)=156296.0d0	c3(65)=-29083.0d0	c3(99)=-822.0d0
c3(32)=43678.0d0	c3(66)=270573.0d0	c3(100)=-247.0d0
c3(33)=-175718.0d0	c3(67)=139856.0d0	c3(101)=-26.0d0
c3(34)=-152409.0d0	c3(68)=-152409.0d0	

Table 4. FIR3 Filter Coefficients