TECHNICAL MANUAL

L80227
10BASE-T/
100BASE-TX
Ethernet PHY

October 2002

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Preface

This book is the primary reference and technical manual for the L80227 10BASE-T/100BASE-TX Ethernet Physical Layer Device (PHY). It contains a complete functional description for the device and includes complete physical and electrical specifications for the product.

Audience

This document assumes that you have some familiarity with Ethernet devices and related support devices. The people who benefit from this book are:

- Engineers and managers who are evaluating the device for possible use in a system
- Engineers who are designing the device into a system

Organization

This document has the following chapters:

- Chapter 1, **Introduction**, describes the device in general terms and gives a block diagram and lists the device features.
- Chapter 2, **Functional Description**, describes each of the internal blocks in the device in some detail.
- Chapter 3, **Signal Descriptions**, lists and describes the device input and output signals.
- Chapter 4, **Registers**, gives a register summary and describes each of the bits in each register.
- Chapter 5, **Management Interface**, describes the device Management Interface, which allows the registers to be read and written.

- Chapter 6, **Specifications**, lists the AC and DC characteristics and gives typical timing parameters.
- Appendix A, **Application Information**, gives practical guidelines for incorporating the device into a design.

Abbreviations Used in This Manual

Below is a list of abbreviations used throughout this manual.

100BASE-T	100 Mbit/s Twisted-Pair Ethernet
10BASE-T	10 Mbit/s Twisted-Pair Ethernet
4B5B	4-Bit 5-Bit
CLK	Clock
CRC	Cyclic Redundancy Check
CRS	Carrier Sense
CSMA	Carrier Sense Multiple Access
CWRD	Codeword
DA	Destination Address
ECL	Emitter-Coupled Logic
EOF	End of Frame
ESD	End of Stream Delimiter
FCS	Frame Check Sequence
FDX	Full-Duplex
FEF	Far End Fault
FIFO	First In - First Out
FLP	Fast Link Pulse
FX	Fiber
HDX	Half-Duplex
HIZ	High Impedance
I/G	Individual/Group
IETF	Internet Engineering Task Force
IPG	Inter-Packet Gap
IREF	Reference Current
L/T	Length and Type
LSB	Least-Significant Bit
MIB	Management Information Base
MLT3	Multi-Level Transmission (3 levels)
ms	millisecond
MSB	Most-Significant Bit
mV	millivolt
NLP	Normal Link Pulse
NRZI	Non-Return to Zero Inverted
NRZ	Non-Return to Zero
OP	Opcode
PCB	Printed Circuit Board
pF	picofarad

PRE	Preamble
R/LH	Read Latched High
R/LHI	Read Latched High with Interrupt
R/LL	Read Latched Low
R/LLI	Read Latched Low with Interrupt
R/LT	Read Latched Transition
R/LTI	Read Latched Transition with Interrupt
R/WSC	Read/Write Self Clearing
RFC	Request for Comments
RJ-45	Registered Jack-45
RMON	Remote Monitoring
SA	Start Address or Station Address
SFD	Start of Frame Delimiter
SNMP	Simple Network Management Protocol
SOI	Start of Idle
SSD	Start of Stream Delimiter
STP	Shielded Twisted Pair
TP	Twisted Pair
µH	microhenry
µP	microprocessor
UTP	Unshielded Twisted Pair

Conventions Used in This Manual

The first time a word or phrase is defined in this manual, it is *italicized.*

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive.

Hexadecimal numbers are indicated by the prefix “0x” —for example, 0x32CF. Binary numbers are indicated by the prefix “0b” —for example, 0b0011.0010.1100.1111.

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Chapter 1
Introduction

This chapter contains a brief introduction to the L80227 10BASE-T/100BASE-TX Ethernet Physical Layer Device (PHY). It contains the following sections:

1.1 Overview

This manual describes the L80227 device. The device contains a single PHY channel. The convention used in this manual is that *device* refers to the IC, and *channel* refers to the PHY in the device.

The L80227 is a highly-integrated analog interface IC for twisted-pair Ethernet applications and can be configured for either 100 Mbits/s (100BASE-TX) or 10 Mbits/s (10BASE-T) Ethernet operation.

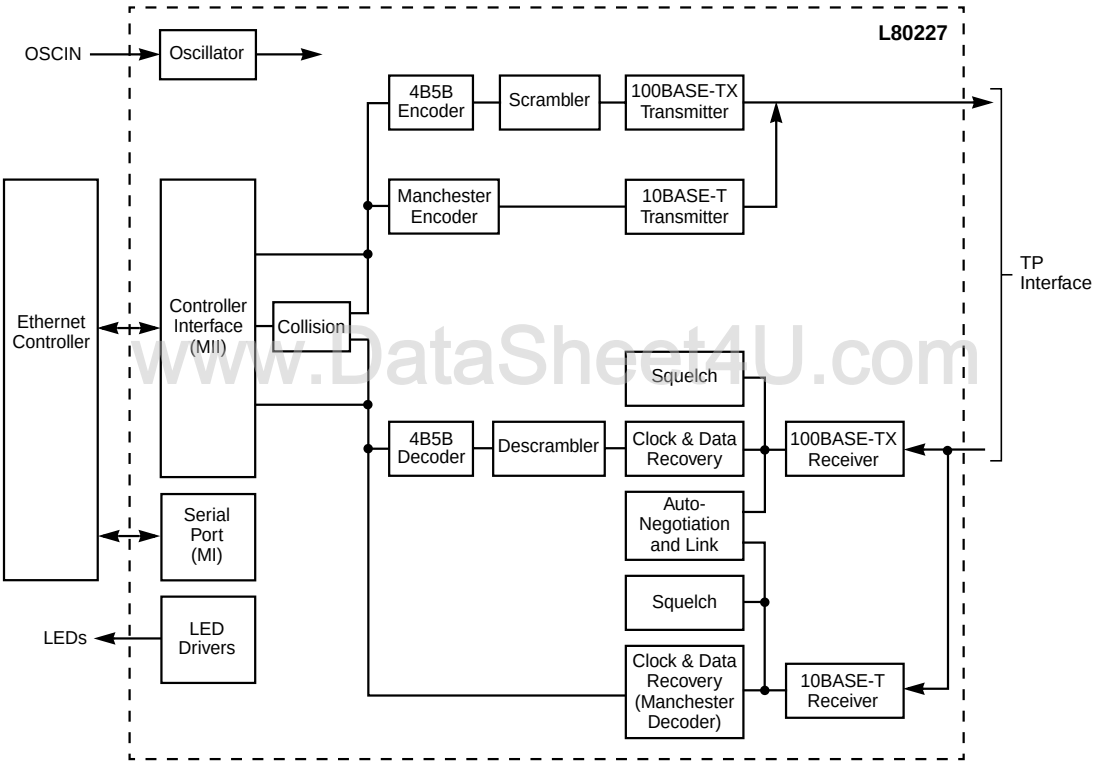
The PHY channel contains the following blocks:

- 4B5B Encoder/Manchester Encoder
- Scrambler
- 10BASE-T Transmitter
- 100BASE-TX Transmitter
- 10BASE-T Receiver
- 100BASE-TX Receiver
- Squelch
- Clock and Data Recovery
- Link Integrity and Autonegotiation

- Descrambler
- 4B5B Decoder/Manchester Decoder
- MII Controller Interface
- Management Interface (MI)
- Collision Detection

Figure 1.1 is a simplified top-level block diagram of the L80227 device.

Figure 1.1 Top Level Block Diagram



Internal output waveshaping circuitry and on-chip filters in the PHY eliminates the need for external filters normally required in 100BASE-TX and 10BASE-T applications.

Using the on-chip AutoNegotiation algorithm, the device can automatically configure the PHY channel to independently operate in 100 Mbits/s or 10 Mbits/s operation in either full- or half-duplex mode.

The device uses the Management Interface (MI) serial port to access eight 16-bit registers in the PHY. These registers comply to Clause 22 of IEEE 802.3u and contain bits and fields that reflect configuration inputs, status outputs, and device capabilities.

The device is ideally suited as a media interface for 10BASE-T/100BASE-TX repeaters, routers, PCMCIA cards, NIC cards, networked modems, and other end station applications.

The device is implemented in either 0.35 or 0.30 micron CMOS technology and operates on a 3.3 V power supply.

1.2 Features

The following list summarizes the salient features of the devices:

- Single-chip solution for a 10BASE-T/100BASE-TX PHY
- Dual speed: 10/100 Mbit/s
- Half-duplex or full-duplex operation
- MII interface to Ethernet MAC
- Management Interface (MI) for configuration and status
- AutoNegotiation for 10/100 Mbit/s, full/half duplex operation
- AutoNegotiation Advertisement control through pins
- All applicable IEEE 802.3, 10BASE-T and 100BASE-TX specifications are met
- On-chip wave shaping (no external filters required)
- Adaptive equalizer for 100BASE-TX operation
- Baseline wander correction
- Minimum number of external components
- LEDs are individually programmable to reflect any the following events:
  - Link

  - Activity
  - Collision
  - Full-Duplex
  - 10/100 Mbits/s
- 3.3 V power supply, 5 V tolerant I/O
- 64-pin LQFP
- Operating temperature ranges available:
  - Commercial (L80227): 0˚ to +70˚ C
  - Industrial (L80227 I): -40˚ to +85˚ C

Chapter 2
Functional Description

This chapter contains a functional description of the PHY device. It has the following sections:

2.1 Device Differences

This manual describes the L80227 PHY. It is similar to the L80223 and L80225 PHY devices. Each of these devices is similar with respect to Ethernet operation. Table 2.1 shows the similarities and differences in the devices.

Table 2.1 Device Differences

Function	L80223	L80225	L80227
Power Supply	3.3V	3.3V	3.3V
RESET Pin	Yes	Yes	Yes
FX Interface	Yes	No	No
Transmit Transformer Winding Ratio	1:1	1:1	1:1
Speed Pin	Yes	Yes	Yes
Duplex Pin	Yes	Yes	Yes
Hardware Advertisement Control	No	Yes	No
Registers 16 – 20	Yes	#18	#17, #18
Available in industrial temperature range	No	No	Yes

2.2 Overview

This section gives a brief overview of the device functional operation.

The L80227 is a complete 100/10 Mbits/s Ethernet Media Interface IC. A block diagram is shown in Figure 2.1.

Note: Unless otherwise noted, the operation and specifications for the industrial temperature devices are identical to the commercial temperature range device.

2.2.1 Channel Operation

The PHY operates in the 100BASE-TX mode at 100 Mbits/s mode, or in the 10BASE-T mode at 10 Mbits/s. The 100 Mbits/s mode and the 10 Mbits/s mode differ in data rate, signaling protocol, and allowed wiring as follows:

- 100BASE-TX mode uses two pairs of category 5 or better UTP or STP twisted-pair cable with 4B5B encoded, scrambled, and MLT3 coded 62.5 MHz ternary data to achieve a throughput of 100 Mbits/s.
- 10 Mbits/s mode uses two pairs of category 3 or better UTP or STP twisted-pair cable with Manchester encoded 10 MHz binary data to achieve a 10 Mbits/s throughput

The data symbol format on the twisted-pair cable for the 100 and 10 Mbits/s modes is defined in IEEE 802.3 specifications and shown in Figure 2.2.

2.2.2 Data Paths

In each device, there is a transmit data path and a receive data path associated with each PHY channel. The transmit data path is from the Controller Interface to the twisted-pair transmitter. The receive data path is from the twisted-pair receiver to the Controller Interface.

Figure 2.1 L80227 Device Block Diagram

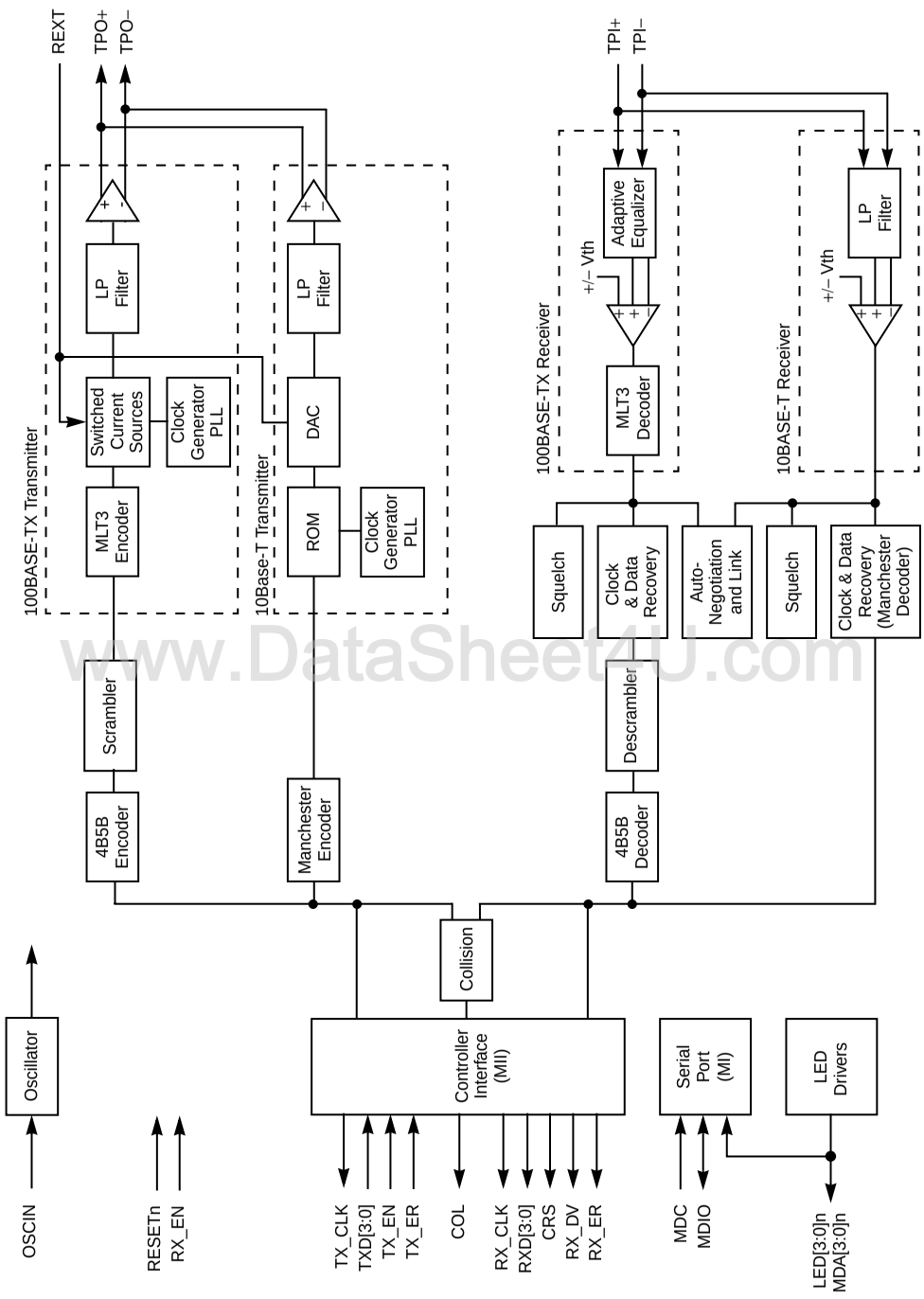
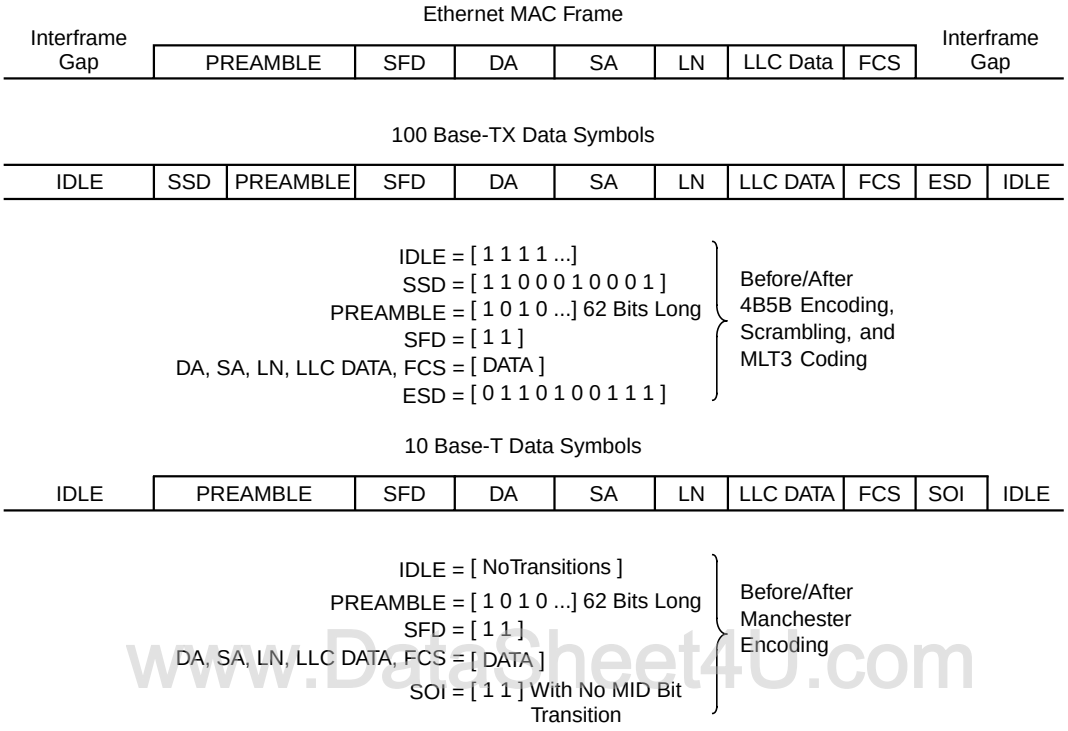


Figure 2.2 100BASE-TX and 10BASE-T Frame Format



2.2.2.1 100BASE-TX Operation

In 100BASE-TX transmit operation, data is received on the Controller Interface from an external Ethernet controller according to the format shown in Figure 2.3 and Table 2.2. The data is sent to the 4B5B encoder, which scrambles the encoded data. The scrambled data is then sent to the TP transmitter. The TP transmitter converts the encoded and scrambled data into MLT3 ternary format, preshapes the output, and drives the twisted-pair cable.

Figure 2.3 MII Frame Format

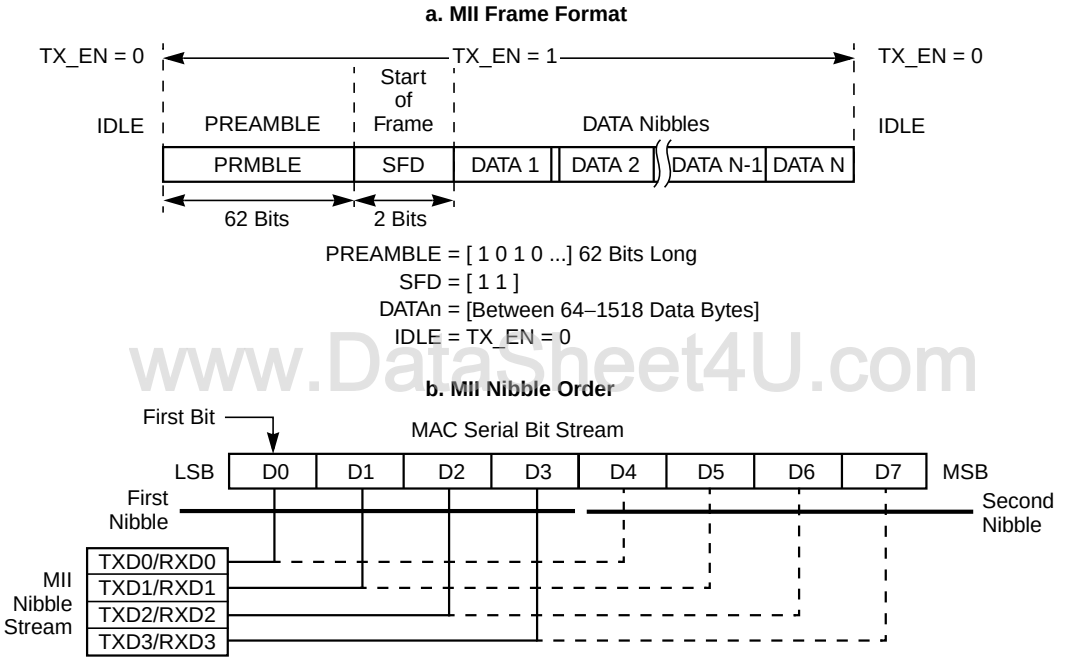


Table 2.2 Transmit Preamble and SFD Bits at MAC Nibble Interface

Signals	Bit Value																			
TXDO	X	X	1[1]	1	1	1	1	1	1	1	1	1	1	1	1	1	1[2]	1	D0[3]	D4[4]
TXD1	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
TXD2	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
TXD3	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
TX_EN	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

1. 1st preamble nibble transmitted.
2. 1st SFD nibble transmitted.
3. 1st data nibble transmitted.
4. D0 through D7 are the first 8 bits of the data field.

In 100BASE-TX receive operation, the TP receiver takes incoming encoded and scrambled MLT3 data from the twisted-pair cable, removes any high-frequency noise from the input, equalizes the input signal to compensate for the effects of the cable, performs baseline wander correction, qualifies the data with a squelch algorithm, and converts the data from MLT3-encoded levels to internal digital levels. The output of the receiver then goes to a clock and data recovery block that recovers a clock from the incoming data, uses the clock to latch valid data into the device, and converts the data back to NRZ format. The 4B5B decoder and descrambler then decodes and descrambles the NRZ data, respectively, and sends it out of the Controller Interface to an external Ethernet controller. The format of the received data at the Controller interface is as shown in Table 2.3.

Table 2.3 Receive Preamble and SFD Bits at MAC Nibble Interface

Signals	Bit Value																		
RXDO	X	1[1]	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1[2]	1	D0[3]	D4[4]
RXD1	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
RXD2	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
RXD3	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
RX_DV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

1. First preamble nibble received. Depending on the mode, the device may eliminate either all or some of the preamble nibbles, up to the first SFD nibble.
2. First SFD nibble received.
3. First data nibble received.
4. D0 through D7 are the first 8 bits of the data field.

2.2.2.2 10BASE-T Operation

10BASE-T operation is similar to the 100BASE-TX operation except

- there is no scrambler/descrambler
- the encoder/decoder is Manchester instead of 4B5B
- the data rate is 10 Mbits/s instead of 100 Mbits/s,
- the twisted-pair symbol data is two-level Manchester instead of ternary MLT-3.
- the transmitter generates link pulses during the idle period
- the transmitter detects the jabber condition
- the receiver detects link pulses and implements the AutoNegotiation algorithm

2.3 Block Diagram Description

The L80227 PHY device has the following main blocks:

- Oscillator and Clock
- Controller Interface
- 4B5B/Manchester Encoder/Decoder
- Scrambler/Descrambler
- Twisted-Pair Transmitter
- Twisted-Pair Receiver
- Clock and Data Recovery
- Link Integrity/AutoNegotiation
- Descrambler
- Link Indication
- Collision Detection
- LED Drivers

A Management Interface (MI) serial port provides access to eight internal PHY registers.

Figure 2.1 shows the main blocks, along with their associated signals. The following sections describe each of the blocks in Figure 2.1. The performance of the device in both the 10 and 100 Mbits/s modes is described.

2.3.1 Oscillator and Clock

The L80227 requires a 25 MHz reference frequency for internal signal generation. This 25 MHz reference frequency is generated with either an external 25 MHz crystal connected between OSCIN and GND or with the application of an external 25 MHz clock to OSCIN.

The device provides either a 2.5 MHz or 25 MHz reference clock at the TX_CLK or RX_CLK output pins for 10-MHz or 100 MHz operation, respectively.

2.3.2 Controller Interface

This section describes the controller interface operation.

2.3.2.1 High Impedance Control

When the RX_EN pin is LOW, the following controller interface outputs are placed in the high impedance state:

- RX_CLK
- RXD[3:0]
- RX_DV
- RX_ER
- COL

2.3.2.2 MII Interface

The device has an MII interface to an external Ethernet Media Access Controller (MAC).

MII (100 Mbits/s) – The MII is a nibble-wide packet data interface defined in IEEE 802.3 and shown in Figure 2.3. The L80227 meets all the MII requirements outlined in IEEE 802.3. The L80227 can directly connect, without any external logic, to any Ethernet controller or other device that also complies with the IEEE 802.3 MII specifications.

The MII interface contains the following signals:

- Transmit data bits (TXD[3:0])
- Transmit clock (TX_CLK)
- Transmit enable (TX_EN)
- Transmit error (TX_ER)
- Receive data bits (RXD[3:0])
- Receive clock (RX_CLK)
- Carrier sense (CRS)
- Receive data valid (RX_DV)
- Receive data error (RX_ER)
- Collision (COL).

The transmit and receive clocks operate at 25 MHz in 100 Mbits/s mode.

On the transmit side, the TX_CLK output runs continuously at 25 MHz. When no data is to be transmitted, TX_EN must be deasserted. While TX_EN is deasserted, TX_ER and TXD[3:0] are ignored and no data is clocked into the device. When TX_EN is asserted on the rising edge of TX_CLK, data on TXD[3:0] is clocked into the device on the rising edge of the TX_CLK output clock. TXD[3:0] input data is nibble-wide packet data whose format must be the same as specified in IEEE 802.3 and shown in Figure 2.3. When all data on TXD[3:0] has been latched into the device, TX_EN must be deasserted on the rising edge of TX_CLK.

TX_ER is also clocked in on the rising edge of TX_CLK. TX_ER is a transmit error signal. When this signal is asserted, the device substitutes an error nibble in place of the normal data nibble that was clocked in on TXD[3:0]. The error nibble is defined to be the /H/ symbol, which is defined in IEEE 802.3 and shown in Table 2.4.

Table 2.4 4B/5B Symbol Mapping

Symbol Name	Description	5B Code	4B Code
0	Data 0	0b11110	0b0000
1	Data 1	0b01001	0b0001
2	Data 2	0b10100	0b0010
3	Data 3	0b10101	0b0011
4	Data 4	0b01010	0b0100
5	Data 5	0b01011	0b0101
6	Data 6	0b01110	0b0110
7	Data 7	0b01111	0b0111
8	Data 8	0b10010	0b1000
9	Data 9	0b10011	0b1001
A	Data A	0b10110	0b1010
B	Data B	0b10111	0b1011
C	Data C	0b11010	0b1100
D	Data D	0b11011	0b1101

Table 2.4 4B/5B Symbol Mapping (Cont.)

Symbol Name	Description	5B Code	4B Code
E	Data E	0b11100	0b1110
F	Data F	0b11101	0b1111
I	Idle	0b11111	0b0000
J	SSD #1	0b11000	0b0101
K	SSD #2	0b10001	0b0101
T	ESD #1	0b01101	0b0000
R	ESD #2	0b00111	0b0000
H	Halt	0b00100	Undefined
–	Invalid codes	All others[1]	0b0000*

1. These 5B codes are not used. The decoder decodes these 5B codes to 4B 0000. The encoder encodes 4B 0000 to 5B 11110, as shown in symbol Data 0.

Because the OSCIN input clock generates the TX_CLK output clock, the TXD[3:0], TX_EN, and TX_ER signals are also clocked in on rising edges of OSCIN.

On the receive side, as long as a valid data packet is not detected, CRS and RX_DV are deasserted and the RXD[3:0] signals are held LOW. When the start of packet is detected, CRS and RX_DV are asserted on the falling edge of RX_CLK. The assertion of RX_DV indicates that valid data is clocked out on RXD[3:0] on the falling edge of the RX_CLK. The RXD[3:0] data has the same frame structure as the TXD[3:0] data and is specified in IEEE 802.3 and shown in Figure 2.3. When the end of the packet is detected, CRS and RX_DV are deasserted, and RXD[3:0] is held LOW. CRS and RX_DV also stay deasserted if the device is in the Link Fail State.

RX_ER is a receive error output that is asserted when certain errors are detected on a data nibble. RX_ER is asserted on the falling edge of RX_CLK for the duration of that RX_CLK clock cycle during which the nibble containing the error is output on RXD[3:0].

The collision output, COL, is asserted whenever the collision condition is detected.

MII (10 Mbits/s) – MII 10 Mbits/s operation is identical to 100 Mbits/s operation except

- TX_CLK and RX_CLK clock frequency is reduced to 2.5 MHz
- TX_ER is ignored
- RX_ER is disabled and always held LOW
- Receive operation is modified as follows:

  On the receive side, when the squelch circuit determines that invalid data is present on the TP inputs, the receiver is idle. During idle, RX_CLK follows TX_CLK, RXD[3:0] is held LOW, and CRS and RX_DV are deasserted. When a start of packet is detected on the TP receive inputs, CRS is asserted and the clock recovery process starts on the incoming TP input data. After the receive clock is recovered from the data, the RX_CLK is switched over to the recovered clock and the data valid signal RX_DV is asserted on a falling edge of RX_CLK. Once RX_DV is asserted, valid data is clocked out on RXD[3:0] on the falling edge of RX_CLK. The RXD[3:0] data has the same packet structure as the TXD[3:0] data and is formatted on RXD[3:0] as specified in IEEE 802.3 and shown in Figure 2.3. When the end of packet is detected, CRS and RX_DV are deasserted. CRS and RX_DV also stay deasserted as long as the device is in the Link Fail State.

MII Disable – To disable the MII inputs and outputs, set the MII_DIS bit in the MI serial port Control register. When the MII is disabled, the MII inputs are ignored, and the MII and TP outputs are placed in a high-impedance state.

If the MI address lines, MDA[3:0]n, are pulled HIGH during reset or powerup, the L80227 powers up and resets with the MII disabled. Otherwise, the L80227 powers up and resets with the MII enabled.

2.3.3 Encoder

This section describes the 4B5B encoder, which is used in 100 Mbits/s operation. It also describes the Manchester Encoder, used in 10BASE-T operation.

2.3.3.1 4B5B Encoder (100 Mbits/s)

100BASE-TX operation requires that the data be 4B5B encoded. The 4B5B Encoder block shown in Figure 2.1 converts the four-bit data nibbles into five-bit data words. The mapping of the 4B nibbles to 5B codewords is specified in IEEE 802.3 and is shown in Table 2.4.

The 4B5B encoder takes 4B (four-bit) nibbles from the Transmit MAC block, converts them into 5B (five-bit) words according to Table 2.4, and sends the 5B words to the scrambler. The 4B5B encoder also substitutes the first eight bits of the preamble with the Start of Stream Delimiter (SSD) (/J/K/ symbols) and adds an End of Stream Delimiter (ESD) (/T/R/ symbols) to the end of each packet, as defined in IEEE 802.3 and shown in Figure 2.2. The 4B5B encoder also fills the period between packets (idle period), with a continuous stream of idle symbols, as shown in Figure 2.2.

2.3.3.2 Manchester Encoder (10 Mbits/s)

The Manchester Encoder shown in Figure 2.1 is used for 10 Mbits/s operation. It combines clock and non-return to zero inverted (NRZI) data such that the first half of the data bit contains the complement of the data, and the second half of the data bit contains the true data, as specified in IEEE 802.3. This process guarantees that a transition always occurs in the middle of the bit cell. The Manchester encoder on the device converts the 10 Mbits/s NRZI data from the Ethernet controller interface into a single data stream for the TP transmitter and adds a start of idle pulse (SOI) at the end of the packet as specified in IEEE 802.3 and shown in Figure 2.2. The Manchester encoding process is only done on actual packet data; during the idle period between packets, no signal is transmitted except for periodic link pulses.

2.3.4 Decoder

This section describes the 4B5B decoder, used in 100 Mbits/s operation, which converts 5B encoded data to 4B nibbles. It also describes the Manchester Decoder, used in 10BASE-T operation.

2.3.4.1 4B5B Decoder (100 Mbits/s)

Because the TP input data is 4B5B encoded on the transmit side, the 4B5B decoder must decode it on the receive side. The mapping of the

5B codewords to the 4B nibbles is specified in IEEE 802.3. The 4B5B decoder takes the 5B codewords from the descrambler, converts them into 4B nibbles according to Table 2.4, and sends the 4B nibbles to the receive Ethernet controller.

The 4B5B decoder also strips off the SSD delimiter (/J/K/ symbols), and replaces it with two 4B Data 5 nibbles (/5/ symbol). It also strips off the ESD delimiter (/T/R/ symbols), and replaces it with two 4B Data 0 nibbles (/I/ symbol), per IEEE 802.3 specifications (see Figure 2.2).

The 4B5B decoder detects SSD, ESD, and codeword errors in the incoming data stream as specified in IEEE 802.3. To indicate these errors, the device asserts the RX_ER output while the errors are being transmitted across RXD[3:0].

2.3.4.2 Manchester Decoder (10 Mbits/s)

In Manchester coded data, the first half of the data bit contains the complement of the data, and the second half of the data bit contains the true data. The Manchester Decoder converts the single data stream from the TP receiver into non-return to zero (NRZ) data for the controller interface. To do this, it decodes the data and strips off the SOI pulse. Because the Clock and Data Recovery block has already separated the clock and data from the TP receiver, that block inherently performs the the Manchester decoding.

2.3.5 Scrambler

100BASE-TX transmission requires scrambling to reduce the radiated emissions on the twisted pair. The scrambler takes the NRZI encoded data from the 4B5B encoder, scrambles it per the IEEE 802.3 specifications, and sends it to the TP transmitter. A scrambler is not used for 10 Mbits/s operation.

2.3.6 Descrambler

The descrambler block shown in Figure 2.1 is used in 100BASE-TX operation. The device descrambler takes the scrambled NRZI data from the data recovery block, descrambles it according to IEEE 802.3 specifications, aligns the data on the correct 5B word boundaries, and sends it to the 4B5B decoder.

The algorithm for synchronization of the descrambler is the same as the algorithm outlined in the IEEE 802.3 specification.

After the descrambler is synchronized, it maintains synchronization as long as enough descrambled idle pattern ones are detected within a given interval. To stay in synchronization, the descrambler needs to detect at least 25 consecutive descrambled idle pattern ones in a 1 ms interval. If 25 consecutive descrambled idle pattern ones are not detected within the 1 ms interval, the descrambler goes out of synchronization and restarts the synchronization process.

The descrambler is disabled for 10BASE-T operation.

2.3.7 Twisted-Pair Transmitters

This section describes the operation of the 10 and 100 Mbits/s TP transmitters.

2.3.7.1 100 Mbits/s TP Transmitter

The TP transmitter consists of an MLT3 encoder, waveform generator, and line driver.

The MLT3 encoder converts the NRZI data from the scrambler into a three-level code required by IEEE 802.3. MLT3 coding uses three levels, converting ones to transitions between the three levels, and zeros to no transitions or changes in level.

The purpose of the waveform generator is to shape the transmit output pulse. The waveform generator takes the MLT3 three-level encoded waveform and uses an array of switched current sources to control the shape of the twisted-pair output signal. The waveform generator consists of switched current sources, a clock generator, filter, and logic. The switched current sources control the rise and fall time as well as signal level to meet IEEE 802.3 requirements. The output of the switched current sources goes through a second order low-pass filter that “smooths” the current output and removes any high-frequency components. In this way, the waveform generator preshapes the output waveform transmitted onto the twisted-pair cable such that the waveform meets the pulse template requirements outlined in IEEE 802.3. The waveform generator eliminates the need for any external filters on the TP transmit output.

The line driver converts the shaped and smoothed waveform to a current output that can drive greater than 100 meters of category 5 unshielded twisted-pair cable or 150-ohm shielded twisted-pair cable.

2.3.7.2 10 Mbits/s TP Transmitter

Even though the 10 Mbits/s transmitter operation is much different than that of 100 Mbits/s, it also consists of a waveform generator and line driver (see Figure 2.1).

The waveform generator, which consists of a ROM, DAC, clock generator, and filter, shapes the output transmit pulse. The DAC generates a stair-stepped representation of the desired output waveform. The stair-stepped DAC output then is passed through a low-pass filter to “smooth” the DAC output and remove any high-frequency components. The DAC values are determined from the data at the ROM addresses. The data is chosen to shape the pulse to the desired template. The clock generator clocks the data into the DAC at high speed. In this way, the waveform generator preshapes the output waveform to be transmitted onto the twisted-pair cable to meet the pulse template requirements outlined in IEEE 802.3 Clause 14 and shown in Figure 2.4. The waveshaper replaces and eliminates external filters on the TP transmit output.

The line driver converts the shaped and smoothed waveform to a current output that can drive greater than 100 meters of category 3/4/5 100-ohm unshielded twisted-pair cable or 150-ohm shielded twisted-pair cable without any external filters.

During the idle period, no output signals are transmitted on the TP outputs except for link pulses.

Figure 2.4 TP Output Voltage Template

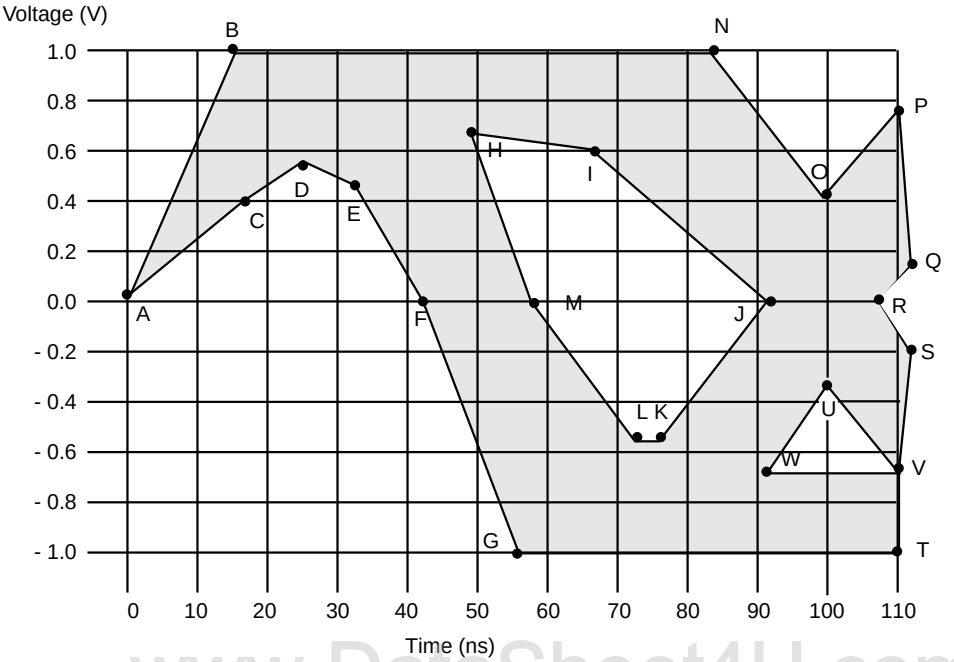


Table 2.5 TP Output Voltage (10 Mbits/s)

Reference	Time (ns) Internal MAU	Voltage (V)
A	0	0
B	15	1.0
C	15	0.4
D	25	0.55
E	32	0.45
F	42	0
G	57	–1.0
H	48	0.7
I	67	0.6
J	92	0
K	74	–0.55
L	73	–0.55

Table 2.5 TP Output Voltage (10 Mbits/s) (Cont.)

Reference	Time (ns) Internal MAU	Voltage (V)
M	58	0
N	85	1.0
O	100	0.4
P	110	0.75
Q	111	0.15
R	108	0
S	111	–0.15
T	110	–1.0
U	100	–0.3
V	110	–0.7
W	90	–0.7

2.3.8 Twisted-Pair Receiver

The device is capable of operating at either 10- or 100-Mbits/s. This section describes the twisted-pair receivers and squelch operation for both modes of operation.

2.3.8.1 100 Mbits/s TP Receiver

The TP receiver detects input signals from the twisted-pair input and converts them to a digital data bit stream ready for clock and data recovery. The receiver can reliably detect 100BASE-TX compliant transmitter data that has been passed through 0 to 100 meters of 100-ohm category 5 UTP or 150-ohm STP cable.

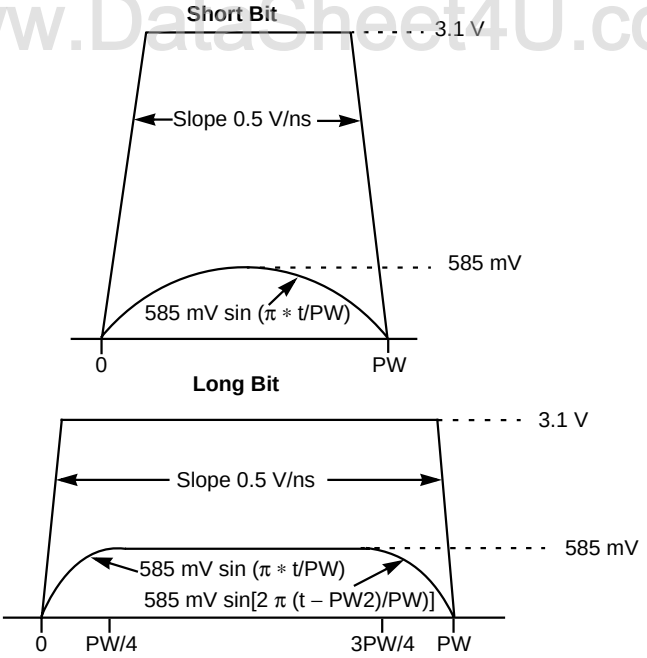
The 100 Mbits/s receiver consists of an adaptive equalizer, baseline wander correction circuit, comparators, and an MLT3 decoder. The TP inputs first go to an adaptive equalizer. The adaptive equalizer compensates for the low-pass characteristics of the cable and can adapt and compensate for 0 to 100 meters of category 5, 100-ohm or 150-ohm STP cable. The baseline wander correction circuit restores the DC component of the input waveform that the external transformers have removed. The comparators convert the equalized signal back to digital levels and qualify the data with the squelch circuit. The MLT3 decoder

takes the three-level MLT3 encoded output data from the comparators and converts it to normal digital data to be used for clock and data recovery.

2.3.8.2 10 Mbits/s TP Receiver

The 10 Mbits/s receiver detects input signals from the twisted-pair cable that are within the template shown in Figure 2.5. The TP inputs are biased by internal resistors and go through a low-pass filter designed to eliminate any high-frequency input noise. The output of the receive filter goes to two different types of comparators: squelch and zero crossing. The squelch comparator determines whether the signal is valid, and the zero-crossing comparator senses the actual data transitions after the signal is determined to be valid. The output of the squelch comparator goes to the squelch circuit and is also used for link pulse detection, SOI detection, and reverse polarity detection. The output of the zero-crossing comparator is used for clock and data recovery in the Manchester decoder.

Figure 2.5 TP Input Voltage Template (10 Mbits/s)



2.3.8.3 Squelch (100 Mbits/s)

The Squelch block determines if the TP input contains valid data. The 100 Mbits/s TP squelch is one of the criteria used to determine link integrity. The squelch comparators compare the TP inputs against fixed positive and negative thresholds called squelch levels. The output from the squelch comparator goes to a digital squelch circuit, which determines whether the receive input data on that port is valid. If the data is invalid, the receiver is in the squelched state. If the input voltage exceeds the squelch levels at least four times with alternating polarity within a 10 µs interval, the squelch circuit determines that the data is valid and the receiver enters into the unsquelch state.

In the unsquelch state, the receive threshold level is reduced by approximately 30% for noise immunity reasons and is called the unsquelch level. When the receiver is in the unsquelch state, the input signal is considered valid.

The device stays in the unsquelch state until loss of data is detected. Loss of data is detected if no alternating polarity unsquelch transitions are detected during any 10 µs interval. When a loss of data is detected, the receive squelch is turned on again.

2.3.8.4 Squelch (10 Mbits/s)

The TP squelch algorithm for 10 Mbits/s mode is identical to the 100 Mbits/s mode, except

- the 10 Mbits/s TP squelch algorithm is not used for link integrity, but to sense the beginning of a packet
- the receiver goes into the unsquelch state if the input voltage exceeds the squelch levels for three bit times with alternating polarity within a 50 to 250 ns interval
- the receiver goes into the squelch state when SOI is detected
- unsquelch detection has no effect on link integrity (link pulses are used in 10 Mbits/s mode for that purpose)
- start of packet is determined when the receiver goes into the unsquelch state and CRS is asserted
- the receiver meets the squelch requirements defined in IEEE 802.3 Clause 14.

2.3.9 Clock and Data Recovery

This section describes clock and data recovery methods implemented in the device for both the 100 Mbits/s and 10 Mbits/s modes.

2.3.9.1 100 Mbits/s Clock and Data Recovery

Clock recovery is accomplished with a phase-locked-loop (PLL). If valid data is not present on the receive inputs, the PLL is locked to the 25 MHz TX_CLK signal. When the squelch circuit detects valid data on the receive TP input, and if the device is in the Link Pass state, the PLL input is switched to the incoming data on the receive inputs. The PLL then locks on to the transitions in the incoming signal to recover the clock. The recovered data clock is then used to generate the 25 MHz RX_CLK, which clocks data into the controller interface section.

The recovered clock extracted by the PLL latches in data from the TP receiver to perform data recovery. The data is then converted from a single bit stream into nibble-wide data words according to the format shown in Figure 2.3

2.3.9.2 10 Mbits/s Clock and Data Recovery

The clock recovery process for 10 Mbits/s mode is identical to the 100 Mbits/s mode except

- the recovered clock frequency is a 2.5 MHz nibble clock
- the PLL is switched from TX_CLK to the TP input when the squelch indicates valid data
- the PLL takes up to 12 transitions (bit times) to lock onto the preamble, so some of the preamble data symbols are lost. However, the clock recovery block recovers enough preamble symbols to pass at least six nibbles of preamble to the receive controller interface as shown in Figure 2.3.

The data recovery process for 10 Mbits/s mode is identical to that of the 100 Mbits/s mode. As mentioned in the Manchester Decoder section, the data recovery process inherently performs decoding of Manchester encoded data from the TP inputs.

2.3.10 Link Integrity and AutoNegotiation

The device can be configured to implement either the standard link integrity algorithms or the AutoNegotiation algorithm.

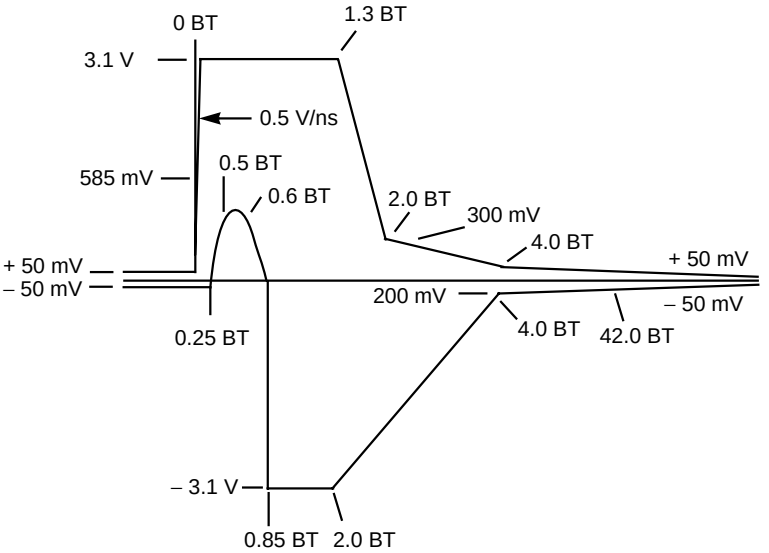
The standard link integrity algorithms are used solely to establish a link to and from a remote device. The AutoNegotiation algorithm is used to establish a link to and from a remote device *and* automatically configure the device for 10 or 100 Mbits/s and Half- or Full-Duplex operation. The different standard link integrity algorithms for 10 and 100 Mbits/s modes are described in following subsections.

The AutoNegotiation algorithm in the device meets all requirements specified in IEEE 802.3.

2.3.10.1 10BASE-T Link Integrity Algorithm (10 Mbits/s)

The device implements the same 10BASE-T link integrity algorithm that is defined in IEEE 802.3. This algorithm uses normal link pulses (NLPs), which are transmitted during idle periods, to determine if a device has successfully established a link with a remote device (called Link Pass state). The transmit link pulse meets the template requirements defined in IEEE 802.3 and shown in Figure 2.6. Refer to IEEE 802.3 for more details if needed.

Figure 2.6 Link Pulse Output Voltage Template (10 Mbits/s)



2.3.10.2 100BASE-TX Link Integrity Algorithm (100 Mbits/s)

Because the IEEE 802.3 specification defines 100BASE-TX to have an active idle signal, the device uses the squelch criteria and descrambler synchronization algorithm on the input data to determine if the device has successfully established a link with a remote device (called Link Pass state). Refer to IEEE 802.3 for more details if needed.

2.3.10.3 AutoNegotiation Algorithm

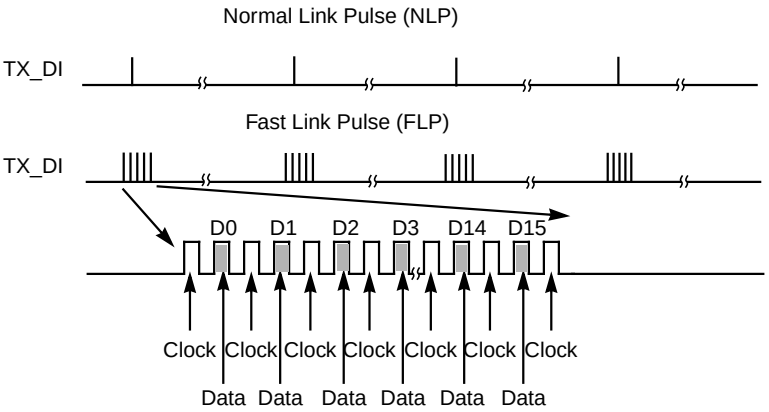
As stated previously, the AutoNegotiation algorithm is used for two purposes:

- to establish a link to and from a remote device
- to automatically configure the device for either 10 or 100 Mbits/s operation and either Half- or Full-Duplex operation.

The AutoNegotiation algorithm is the same algorithm defined in IEEE 802.3 Clause 28. AutoNegotiation uses a burst of link pulses, called fast link pulses (FLPs), to pass up to 16 bits of signaling data back and forth between the device and a remote device. The transmit FLP pulses meet

the template specified in IEEE 802.3 and shown in Figure 2.6. A timing diagram contrasting NLPs and FLPs is shown in Figure 2.7.

Figure 2.7 NLP vs FLP Link Pulse



To enable AutoNegotiation for a channel, assert the AutoNegotiation pin (ANEG), or set the AutoNegotiation Enable (ANEG_EN) bit in the MI serial port Control register (register 0). If AutoNegotiation is enabled, any of the following events initiates the AutoNegotiation algorithm for the channel:

- Power up
- Device reset
- Channel enters the Link Fail state
- AutoNegotiation Enable (ANEG_EN) bit in the MI serial port Control register for that port is cleared, then set
- AutoNegotiation Reset (ANEG_RST) bit in the MI serial port Control register is set

Once a negotiation has been initiated, the device first determines if the remote device has AutoNegotiation capability. If the remote device is not AutoNegotiation-capable and is just transmitting either 10BASE-T or 100BASE-TX signals, the device senses it and places itself in the same mode as the remote device. If the device detects FLPs from the remote device, the remote device is determined to have AutoNegotiation capability, and the device then uses the value from the PHY AutoNegotiation Advertisement for that port to advertise its capabilities to

the remote device. The device negotiation algorithm matches its capabilities to the remote device's capabilities and determines what mode the device should be configured for according to the priority resolution algorithm defined in IEEEE 802.3 Clause 28. After the negotiation process is completed, the device configures itself for either 10 or 100 Mbits/s modes and either Half- or Full-Duplex modes (depending on the outcome of the negotiation process), and switches to either the 10BASE-T or 100BASE-TX link integrity algorithms (depending on which mode AutoNegotiation enabled). Refer to IEEE 802.3 Clause 28 for more details.

2.3.10.4 AutoNegotiation Outcome Indication

The outcome or result of the AutoNegotiation process is stored in the 10/100 Speed Detect (SPD_DET) and Duplex Detect (DPLX_DET) bits in the MI serial port Status Output 0 register.

2.3.10.5 AutoNegotiation Status

To monitor the status of the AutoNegotiation process, read the AutoNegotiation Acknowledgement (ANEG_ACK) bit in the MI serial port Status register.

2.3.10.6 AutoNegotiation Enable/Disable

To enable the AutoNegotiation algorithm, set the AutoNegotiation Enable bit (ANEG_EN) in the MI serial port Control register, or assert the ANEG pin. To disable the AutoNegotiation algorithm, clear the ANEG_EN bit or deassert the ANEG pin.

When the AutoNegotiation algorithm is enabled, the device halts all transmissions including link pulses for 1200 to 1500 ms, enters the Link Fail State, and restarts the negotiation process. When the AutoNegotiation algorithm is disabled, the selection of 100 Mbits/s or 10 Mbits/s mode is determined with the state of the SPEED bit in the MI serial port Control register and the half- or full-duplex mode is determined with the state of the DPLX bit in the MI serial port Control register.

2.3.10.7 AutoNegotiation Reset

Appropriately setting the AutoNegotiation Reset (ANEG_RST) bit in the MI serial port Control register can initiate or reset the AutoNegotiation algorithm at any time.

2.3.11 Link Indication

Receive link detect activity can be monitored two ways:

1. The link detect bit (LINK) in the MI serial port Status register indicates link activity when it is set.
2. The LED output pins can be programmed to indicate link activity.

In the MI serial port Configuration register, set the LED function select bits (LED_DEF_[1:0]) so that link activity is indicated at the PLED3n or PLED0n output. Set the PLED3_[1:0] and PLED0_[1:0] bits in the same register to 0b11 (normal). With these settings, LEDs connected to the PLED3n and PLED0n pins will reflect link activity.

When either the PLED3n or PLED0n pins are programmed to be a link detect output, they are driven LOW whenever the device is in the Link Pass State. The PLED3n output is open-drain with a pullup resistor and can drive an LED from V_{DD}. The PLED0n output has both pullup and pulldown driver transistors in addition to a weak pullup resistor, so it can drive an LED from either V_{DD} or GND. Both the PLED3n and PLED0n outputs can also drive another digital input.

See Section 2.3.13, “LED Drivers,” page 2-28 for more details on how to program the LED output pins to indicate various conditions.

2.3.12 Collision

Collisions occur whenever transmit and receive operations occur simultaneously while the device is in Half-Duplex mode.

2.3.12.1 100 Mbits/s

In 100 Mbits/s operation, a collision occurs and is sensed whenever there is simultaneous transmission (packet transmission on TPO+/-) and reception (non-idle symbols detected at the TP+/- input). When a

collision is detected, the COL output is asserted, TP data continues to be transmitted on the twisted-pair outputs, TP data continues to be received on the twisted-pair inputs, and internal CRS loopback is disabled. After a collision is in process, CRS is asserted and stays asserted until the receive and transmit packets that caused the collision are terminated.

The collision function is disabled if the device is in the Full-Duplex mode, is in the Link Fail state, or if the device is in the diagnostic loopback mode.

2.3.12.2 10 Mbits/s

A collision in the 10 Mbits/s mode is identical to one the 100 Mbits/s mode except

- the 10 Mbits/s squelch criteria determines reception
- the RXD[3:0] outputs are forced to all zeros
- the collision signal (COL) is asserted when the SQE test is performed
- the collision signal (COL) is asserted when the jabber condition has been detected.

2.3.12.3 Collision Test

To test the Controller Interface collision signal (COL), set the COLTST bit in the MI serial port Control register. When this bit is set, TX_EN is looped back onto COL and the TP outputs are disabled.

2.3.12.4 Collision Indication

Collisions are indicated through the COL pin, which is asserted HIGH every time a collision occurs. The device can also be programmed to indicate collisions on the PLED2n output.

In the MI serial port Configuration register, set the LED function select bits (LED_DEF_[1:0]) so that collision activity is indicated at the PLED2n output. Set the PLED2_[1:0] bits in the same register to 0b11 (normal). With these settings, an LED connected to the PLED2n pin will reflect collision activity.

When the PLED2n pin is programmed to be a collision detect output, it is asserted LOW for 100 ms every time a collision occurs. The PLED2n output is open drain with a pullup resistor and can drive an LED from V_{DD} or can drive another digital input.

See Section 2.3.13, “LED Drivers,” page 2-28 for more details on how to program the LED output pins to indicate various conditions.

2.3.13 LED Drivers

The PLED[5:2]n outputs are open-drain with a pullup resistor and can drive LEDs tied to V_{DD}. The PLED[1:0]n outputs have both pullup and pulldown driver transistors with a pullup resistor, so the PLED[1:0]n outputs can drive LEDs tied to either V_{DD} or GND.

The PLED[5:0]n outputs can be programmed through the MI serial port Configuration register for the following functions:

- Normal Function
- On
- Off
- Blink

The PLED[5:0]n outputs are programmed with the LED output select bits (PLEDn_[1:0]) and the LED Normal Function select bits (LED_DEF[1:0]) in the MI serial port Configuration register.

2.3.13.1 LED Output Select Bits

There are four sets of output select bits in MI serial port Configuration register, one set for each LED output pin:

- PLED3_[1:0] control the PLED3n output
- PLED2_[1:0] control the PLED2n output
- PLED1_[1:0] control the PLED1n output
- PLED0_[1:0] control the PLED0n output

The PLEDn_[1:0] bits program the outputs to operate in the following modes:

- Normal operation (see Section 2.3.13.2, “LED Normal Function Select Bits”)
- Blink
- Steady On (PLED[3:0]n pin LOW)
- Steady Off (PLED[3:0]n pin HIGH)

Table 2.6 shows the encoding of the output select bits.

Table 2.6 PLEDn_[1:0] Output Select Bit Encoding

PLEDn_[1]	PLEDn_[0]	LED State	LED Pin
1	1	Normal	LED pin reflects the functions selected with the LED_DEF[1:0] bits
1	0	LED Blink	LED output driver continuously toggles at a rate of 100 ms on, 100 ms off
0	1	LED On	LED output driver is LOW
0	0	LED Off	LED output driver is HIGH

2.3.13.2 LED Normal Function Select Bits

When the PLED[5:0]n pins are programmed for their normal functions (PLEDn_[1:0] = 0b11), the pin output states indicate four specific types of events. The LED Normal Function select bits (LED_DEF[1:0]) in the MI serial port Configuration register determine the states of the pins, as indicated in Table 2.7 and Table 2.8.

Table 2.7 LED Normal Function Definition

LED_DEF[1:0]	PLED5n	PLED4n	PLED3n	PLED2n	PLED1n	PLED0n
0b11	RCV ACT	XMT ACT	LINK	COL	FDX	10/100
0b10	RCV ACT	XMT ACT	LINK	ACT	FDX	10/100
0b01	RCV ACT	XMT ACT	LINK + ACT	COL	FDX	10/100
0b00[1]	RCV ACT	XMT ACT	LINK 100	ACT	FDX	LINK10

1. The L80227 powers up with the LED_DEF[1:0] bits set to the default value of 0b00.

The default Normal Functions for PLED[5:0]n are Receive Activity, Transmit Activity, Link 100, Activity, Full Duplex, and Link 10, respectively.

Table 2.8 LED Event Definition

Symbol	Definition
RCV ACT	Receive activity occurred; stretch pulse to 100 ms
XMT ACT	Transmit activity occurred; stretch pulse to 100 ms
LINK	100 or 10 Mbits/s link detected
LINK+ACT	100 or 10 Mbits/s link detected or activity occurred; stretch pulse to 100 ms (link detect causes LED to be on, activity causes LED to blink)
ACT	Activity occurred; stretch pulse to 100 ms
LINK100	100 Mbit/s link detected
COL	Collision occurred; stretch pulse to 100 ms
FDX	Full-Duplex mode enabled
10/100	10 Mbits/s mode enabled (HIGH), or 100 Mbits/s mode enabled (LOW)
LINK10	10 Mbits/s link detected

2.4 Start of Packet

This section describes start of packet operation for both the 100 Mbits/s and 10 Mbits/s modes.

2.4.1 100 Mbits/s

A unique Start of Stream Delimiter (SSD) indicates the start of packet for 100 Mbits/s mode. The SSD pattern consists of two /J/K/ 5B symbols inserted at the beginning of the packet in place of the first two preamble symbols, as defined in IEEE 802.3 Clause 24 and shown in Table 2.4 and Figure 2.2.

The 4B5B encoder generates the transmit SSD and inserts the /J/K/ symbols at the beginning of the transmit data packet in place of the first two 5B symbols of the preamble, as shown in Figure 2.2.

The 4B5B decoder detects the receive pattern. To do this, the decoder examines groups of 10 consecutive code bits (two 5B words) from the descrambler. Between packets, the receiver detects the idle pattern (5B /I/ symbols). When in the idle state, the device deasserts the CRS and RX_DV pins.

If the receiver is in the idle state and 10 consecutive code bits from the receiver consist of the /J/K/ symbols, the start of packet is detected, data reception begins, and /5/5/ symbols are substituted in place of the /J/K/ symbols.

If the receiver is in the idle state and 10 consecutive code bits from the receiver are a pattern that is neither /I/I/ nor /J/K/ symbols, but contain at least two noncontiguous zeros, activity is detected but the start of packet is considered to be faulty and a False Carrier Indication (also referred to as bad SSD) is signaled to the controller interface.

When False Carrier is detected, CRS is asserted, RX_ER is asserted, RX_DV remains deasserted, and the RXD[3:0] output state is 0b1110 while RX_ER is asserted.

If the receiver is in the idle state and 10 consecutive code bits from the receiver consist of a pattern that is neither /I/I/ nor /J/K/ symbols but does not contain at least two noncontiguous zeros, the data is ignored and the receiver stays in the idle state.

2.4.2 10 Mbits/s

Because the idle period in 10 Mbits/s mode is defined to be when there is no valid data on the TP inputs, the start of packet for 10 Mbits/s mode is detected when the TP squelch circuit detects valid data. When the start of packet is detected, CRS is asserted as described in Section 2.3.2, “Controller Interface,” page 2-9. See Section 2.3.8.4, “Squelch (10 Mbits/s),” page 2-20 for details on the squelch algorithm.

2.5 End of Packet

This section describes end of packet operation for both the 100 Mbits/s and 10 Mbits/s modes.

2.5.1 100 Mbits/s

The End of Stream Delimiter (ESD) indicates the end of packet for 100 Mbits/s mode. The ESD pattern consists of two /T/R/ 4B5B symbols inserted after the end of the packet, as defined in IEEE 802.3 Clause 24 and shown in Table 2.4 and Figure 2.2.

The 4B5B encoder generates the transmit ESD and inserts the /T/R/ symbols after the end of the transmit data packet, as shown in Figure 2.2.

The 4B5B decoder detects the ESD pattern when there are groups of 10 consecutive code bits (two 5B words) from the descrambler during valid packet reception.

If the 10 consecutive code bits from the receiver during valid packet reception consist of the /T/R/ symbols, the end of packet is detected, data reception is terminated, the CRS and RX_DV pins are asserted, and /I/I/ symbols are substituted in place of the /T/R/ symbols.

If the 10 consecutive code bits from the receiver during valid packet reception do not consist of /T/R/ symbols, but instead consist of /I/I/ symbols, the packet is considered to have been terminated prematurely and abnormally, and the end of packet condition is signalled to the controller interface.

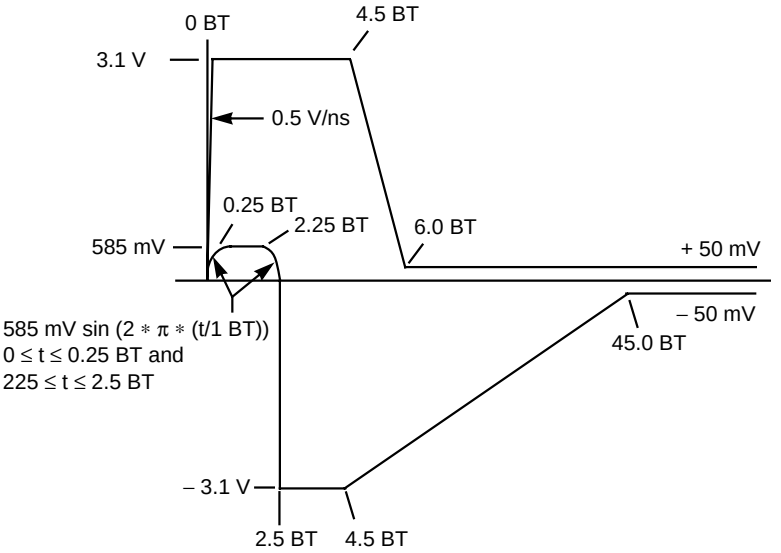
When the premature end of packet condition is detected, the RX_ER signal is asserted for the nibble associated with the first /I/ symbol detected, then the CRS and RX_DV pins are deasserted.

2.5.2 10 Mbits/s

The end of packet for 10 Mbits/s mode is indicated with the Start of Idle (SOI) pulse. The SOI pulse is a positive double wide pulse containing a Manchester code violation inserted at the end of every packet.

The TP transmitter generates the transmit SOI pulse and inserts it at the end of the data packet after TX_EN has been deasserted. The transmit waveshaper shapes the transmitted SOI output pulse at the TP output to meet the pulse template requirements specified in IEEE 802.3 Clause 14 and shown in Figure 2.8.

Figure 2.8 SOI Output Voltage Template (10 Mbits/s)



The TP receiver senses missing data transitions in order to detect the receive SOI pulse. Once the SOI pulse is detected, data reception is ended and the CRS and RX_DV pins are deasserted.

2.6 Full-/Half-Duplex Mode

Half-Duplex mode is the CSMA/CD operation defined in IEEE 802.3. It allows transmission or reception, but not both at the same time. Full-Duplex operation is a mode that allows simultaneous transmission and reception. Full duplex in the 10 Mbits/s mode is identical to operation in the 100 Mbits/s mode.

The device can be forced into either the Full- or Half-Duplex mode, or the device can use AutoNegotiation to autoselect Full-/Half-Duplex operation. When a channel is placed in Full-Duplex mode:

- The collision function is disabled, and
- TX_EN to CRS loopback is disabled

2.6.1 Forcing Full-/Half-Duplex Operation

To independently force a channel into either the Full- or Half-Duplex mode, set the Duplex Mode Select (DPLX) bit in the MI serial port Control register, assuming that AutoNegotiation is not enabled with the ANEG_EN bit in the MI serial port Control register.

The device automatically configures itself for Full- or Half-Duplex mode. To do this, the device uses the AutoNegotiation algorithm to advertise and detect Full- and Half-Duplex capabilities to and from a remote device. To enable AutoNegotiation, set the AutoNegotiation Enable (ANEG_EN) bit in the MI serial port Control register.

To select the advertised Full/-Half-Duplex capability, appropriately set the bits in the MI serial port AutoNegotiation Advertisement register. AutoNegotiation functionality is described in more detail in Section 2.3.10, “Link Integrity and AutoNegotiation”.

2.6.2 Full/Half Duplex Indication

Full-Duplex detection can be monitored through the DPLX_DET bit in the MI serial port Status Output register, or it can also be programmed to appear on the PLED1n pin.

In the MI serial port Configuration register, set the LED function select bits (LED_DEF[1:0]) so that the Full-Duplex condition activity is indicated at the PLED1n output. Set the PLED2_[1:0] bits in the same register to 0b11 (normal). When the PLED1n pin is programmed to be a Full-Duplex detect output, it is asserted LOW when the device is configured for Full-Duplex operation. The PLED1n output has both pullup and pulldown driver transistors and a weak pullup resistor, so it can drive an LED from either V_{DD} or GND and can also drive a digital input.

See Section 2.3.13, “LED Drivers,” page 2-28 for more details on how to program the LED output pins to indicate various conditions.

2.6.3 Loopback

2.6.3.1 Internal CRS Loopback

TX_EN is internally looped back onto CRS during every transmit packet. This internal CRS loopback is disabled during collision, in Full-Duplex

mode, and in the Link Fail State. In 10 Mbits/s mode, internal CRS loopback is also disabled when jabber is detected.

2.6.3.2 Diagnostic Loopback

Setting the loopback bit (LPBK) in the MI serial port Control register selects the diagnostic loopback mode. When diagnostic loopback is enabled, the TXD[3:0] data is looped back onto RXD[3:0], TX_EN is looped back onto CRS, RX_DV operates normally, the TP receive and transmit paths are disabled, the transmit link pulses are halted, and the Half-/Full-Duplex modes do not change.

2.7 10/100 Mbits/s Selection

The device can be forced into either the 10 or 100 Mbits/s mode, or it can use AutoNegotiation to autoselect 10 or 100 Mbits/s operation.

2.7.1 Forcing 10/100 Mbits/s Operation

To independently force each channel into either the 10 Mbits/s or 100 Mbits/s mode

- clear the ANEG_EN bit in the MI serial port Control register, and
- set the Speed Select (SPEED) bit in the MI serial port Control register

2.7.2 Autoselecting 10/100 Mbits/s Operation

The device can automatically configure itself for 10 or 100 Mbits/s mode. To do this, it uses the AutoNegotiation algorithm to advertise and detect 10 and 100 Mbits/s capabilities to and from a remote device. Setting the AutoNegotiation Enable (ANEG_EN) bit in the MI serial port Control register enables AutoNegotiation. Appropriately setting the bits in the MI serial port AutoNegotiation Advertisement register selects the advertised speed capability. AutoNegotiation functionality is described in more detail in Section 2.3.10, “Link Integrity and AutoNegotiation”.

2.7.3 10/100 Mbits/s Indication

The channel 10/100 Mbits/s speed can be monitored through the SPD_DET bit in the MI serial port Channel Status Output register.

In the MI serial port Configuration register, set the LED function select bits (LED_DEF[1:0]) so that the 10/100 speed condition is indicated at the PLED0n output. Set the PLED_2[1:0]n bits in the same register to 0b11 (normal). When the PLED0n pin is programmed to be a speed detect output, it is asserted LOW when the device is configured for 100 Mbits/s operation. The PLED0n output has both pullup and pulldown driver transistors and a weak pullup resistor, so it can drive an LED from either V_{DD} or GND and can also drive a digital input.

See Section 2.3.13, “LED Drivers,” page 2-28 for more details on how to program the LED output pins to indicate various conditions.

2.8 Jabber

A jabber condition occurs in 10 Mbits/s mode when the transmit packet exceeds a predetermined length. When jabber is detected, the TP transmit outputs are forced to the idle state, a collision is asserted, and the JAB register bit is set in the MI serial port Status register.

Clearing the Jabber Disable (JAB_DIS) bit to 0 in the MI serial port Configuration register disables the jabber function.

The jabber function is disabled in the 100 Mbits/s mode.

2.9 Reset

The device is reset when

1. V_{DD} is applied to the device, or
2. the reset bit (RST) is set in the MI serial port Control register, or
3. the RESETn pin is asserted (LOW).

When reset occurs because of (1) or (2), an internal power-on reset pulse is generated that resets all internal circuits, forces the MI serial port

bits to their default values, and latches in new values for the MI address. After the power-on reset pulse has finished, the reset bit (RST) in the MI serial port Control register is cleared and the device is ready for normal operation.

When reset is initiated because of (3), the same procedure occurs except the device stays in the reset state as long as the RESETn pin is held LOW. The RESETn pin has an internal pullup to V_{DD}. The device is guaranteed to be ready for normal operation 50 ms after the reset sequence is initiated.

2.10 Receive Polarity Correction

In 10 Mbits/s mode, the polarity of the signal on the TP receive input is continuously monitored.

A start of idle (SOI) pulse is sent at the end of transmission in order to signal to a receiver that transmission has ended and the idle period has started. The SOI pulse is a positive pulse. When the SOI pulse is detected, it indicates that receive data is no longer valid and causes the device to turn on the receive squelch mechanism. Link pulses are transmitted occasionally during the idle period.

When the device is powered up, it is assumed that the polarity is correct and no polarity correction occurs. After that, receive polarity is continuously monitored by checking the polarity of the SOI pulses (they are always expected to be positive pulses). If three consecutive SOI pulses indicate incorrect polarity on the TP receive input, the polarity is internally determined to be incorrect. In this case, the Reverse Polarity Detect bit (RPOL) is set in the MI serial port Status Output register.

The device automatically corrects for the reverse polarity condition, provided the autopolarity feature is not disabled. To disable autopolarity, set the Autopolarity Disable bit (APOL_DIS) in the MI serial port Configuration register.

No polarity detection or correction is needed in the 100 Mbits/s mode.

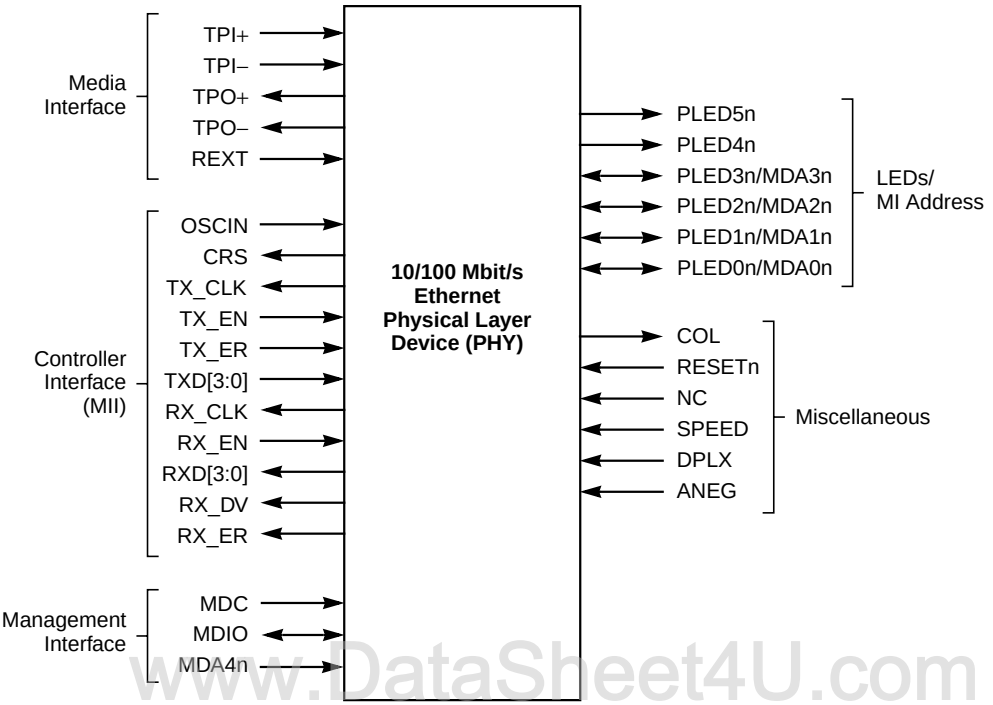
Chapter 3
Signal Descriptions

This chapter describes the device signals. It contains the following sections:

- Section 3.1, “Media Interface Signals”
- Section 3.2, “Controller Interface Signals (MII)”
- Section 3.3, “Management Interface (MI)/LED Signals”
- Section 3.4, “LED Signals”
- Section 3.5, “Miscellaneous Signals”
- Section 3.6, “Power Supply”

Figure 3.1 is a logic diagram for the device.

Figure 3.1 Device Logic Diagram



3.1 Media Interface Signals

REXT — **Transmit Current Set** — **I**

A resistor connected between the REXT pin and GND sets the output current for the TP transmit outputs.

TPO+ — **Twisted-Pair Transmit Output (Positive)** — **O**

The TPO+ pin functions as the positive signal in the twisted-pair output.

TPO- — **Twisted-Pair Transmit Output (Negative)** — **O**

The TPO- pin functions as the negative signal in the twisted-pair output.

TPI+	**Twisted-Pair Receive Input (Positive)** The TPI+ pin functions as the positive signal in the twisted-pair input.	**I**
TPI-	**Twisted-Pair Receive Input (Negative)** The TPI- pin functions as the negative signal in the twisted-pair input.	**I**

3.2 Controller Interface Signals (MII)

CRS	**Carrier Sense Output** The CRS output is asserted HIGH when valid data is detected on the receive TP inputs. CRS is clocked out on the falling edge of RX_CLK.	**O**
OSCIN	**Clock Oscillator Input** There must be either a 25 MHz crystal between this pin and GND or a 25 MHz clock applied to this pin. TX_CLK output is generated from this input.	**I**
RX_CLK	**Receive Clock Output** Receive data on RXD, RX_DV, and RX_ER is clocked out to an external controller on the falling edge of RX_CLK.	**O**
RXD[3:0]	**Receive Data Output** RXD[3:0] contain receive nibble data from the TP input, and they are clocked out on the falling edge of RX_CLK.	**O**
RX_DV	**Receive Data Valid Output** RX_DV is asserted HIGH when valid decoded data is present on the RXD outputs. RX_DV is clocked out on the falling edge of RX_CLK.	**O**
RX_EN	**Receive Enable Input** When RX_EN is HIGH, all of the receive outputs (RX_CLK, RXD[3:0], RX_DV, RX_ER, COL) are enabled. When RX_EN is LOW, the outputs are in a high-impedance state.	**I**
RX_ER	**Receive Error Output** RX_ER is asserted HIGH when a coding error or other specified errors are detected on the receive twisted-pair inputs. The signal is clocked out on the falling edge of RX_CLK.	**O**

TX_CLK **Transmit Clock Output** **O**

Transmit data from the controller on TXD, TX_EN, and TX_ER is clocked in on the rising edge of TX_CLK and OSCIN.

TXD[3:0] **Transmit Data Input** **I**

TXD[3:0] contain input nibble data to be transmitted on the TP outputs, and they are clocked in on the rising edge of TX_CLK and OSCIN when TX_EN is asserted.

TX_EN **Transmit Enable Input** **I**

TX_EN must be asserted HIGH to indicate that data on TXD and TX_ER is valid. TX_ER is clocked in on the rising edge of TX_CLK and OSCIN.

TX_ER **Transmit Error Input** **I**

The TXER pin, when asserted, causes a special pattern to be transmitted on the twisted-pair outputs in place of normal data, and it is clocked in on the rising edge of TX_CLK when TX_EN is asserted.

3.3 Management Interface (MI)/LED Signals

MDC **MI Clock** **I**

The MDC clock shifts serial data for the internal registers into and out of the MDIO pin on its rising edge.

MDA4n

Address 4 Input **Pullup O.D. I**

During powerup or reset, this pin is high-impedance and the level on this pin is latched in as the physical device address MDA4 for the MI serial port

MDIO **MI Data** **I/O**

This bidirectional pin contains serial data for the internal registers. The data on this pin is clocked in and out of the device on the rising edge of MDC.

PLED3n/MDA3n **Pullup O.D. I/O**

Programmable LED Output/MI Address Bit

The default function of this pin is to be a 100 Mbits/s Link Detect output. This pin can also be programmed through the MI serial port to indicate other events or be user controlled. This pin can drive an LED from V_{DD}.

When programmed as a 100 Mbits/s Link Detect Output (default):

Pin	Function
HIGH	No Link Detect
LOW	100 Mbits/s Link Detected

During powerup or reset, this pin is high-impedance and the level on this pin is latched in as the physical device address MDA3n for the MI serial port.

PLED2n/MDA2n **Pullup O.D. I/O**

Programmable LED Output/MI Address Bit

The default function of this pin is to be an Activity Detect output. This pin can also be programmed through the MI serial port to indicate other events or be user controlled. This pin can drive an LED from V_{DD}.

When programmed as an Activity Detect Output (default):

Pin	Function
HIGH	No Activity
LOW	Transmit or receive packet occurred (held LOW for 100 ms)

During powerup or reset, this pin is high-impedance and the level on this pin is latched in as the physical device address MDA2n for the MI serial port.

PLED1n/MDA1n **Pullup O.D. I/O**

Programmable LED Output/MI Address Bit

The default function of this pin is to be a Full Duplex Detect output. This pin can also be programmed through the MI serial port to indicate other events or be user controlled. This pin can drive an LED from both V_{DD} and GND.

When programmed as Full Duplex Detect Output (default):

Pin	Function
HIGH	Half-Duplex
LOW	Full-Duplex

During powerup or reset, this pin is high-impedance and the level on this pin is latched in as the physical address device address MDA1n for the MI serial port.

PLED0n/MDA0n **Pullup O.D. I/O**

Programmable LED Output/MI Address Bit

The default function of this pin is to be a 10 Mbits/s Link Detect output. This pin can also be programmed through the MI serial port to indicate other events or be user controlled.

This pin can drive an LED from both V_{DD} and GND.

When programmed as 10 Mbits/s Link Detect Output (default):

Pin	Function
HIGH	No Detect
LOW	10 Mbits/s Link Detected

During powerup or reset, this pin is high-impedance and the value on this pin is latched in as the address MDA0n for the MI serial port.

3.4 LED Signals

PLED5n **Receive LED Output** **Pullup O.D. O**

The function of this pin is to be a Receive Activity Detect output. This pin can also drive an LED from V_{DD}.

HIGH = No Receive Activity

LOW = Receive packet occurred: hold LOW for 100 ms

PLED4n **Transmit LED Output** **Pullup O.D. O**

The function of this pin is to be a Transmit Activity Detect output. This pin can also drive an LED from V_{DD}.

HIGH = No Transmit Activity

LOW = Transmit packet occurred: hold LOW for 100 ms

3.5 Miscellaneous Signals

ANEG **AutoNegotiation Input** **I**

This pin control AutoNegotiation operation.

Pin	Meaning
HIGH	AutoNegotiation is on. AutoNegotiation Enable is controlled from the ANEG_EN bit, 10/100 Mbits/s operation is controlled from the SPEED bit, and Half/Full Duplex operation is controlled from the DPLX bit.
LOW	AutoNegotiation is off. 10/100 Mbits/s operation is controlled from the SPEED pin and Half/Full Duplex operation is controlled from the DPLX pin.

COL **Collision Output** **O**

COL is asserted HIGH when a collision between transmit and receive data is detected.

DPLX **Full/Half Duplex Select Input** **I**

When the ANEG pin is LOW, the DPLX pin selects Half/Full Duplex operation.

Pin	Meaning
HIGH	Full Duplex operation
LOW	Half Duplex operation

When the ANEG pin is HIGH, the DPLX pin is ignored and the Half/Full Duplex operation is controlled from the Duplex Mode Select bit (DPLX) in the MI serial port Control register or the AutoNegotiation outcome.

NC **No Connect**

These pins are reserved for future use and should be left floating for proper operation.

RESETn **Hardware Reset Input** **Pullup I**

Pin	Meaning
HIGH	Normal
LOW	Device in reset state. Reset is finished 100 ms after RESETn goes HIGH.

SPEED **Speed Select Input** **I**

When the ANEG pin is LOW, the SPEED pin selects 10/100 Mbits/s operation.

Pin	Meaning
HIGH	100 Mbits/s operation
LOW	10 Mbits/s operation

When the ANEG pin is HIGH, this pin is ignored and the speed is determined from the Speed Select bit (SPEED) in the MI serial port Control register or the AutoNegotiation outcome.

3.6 Power Supply

GND **Ground** **I**

The ground pins must be connected to ground (0 Volts).

VDD **Positive Supply** **I**

The V_{DD} pins must be connected to 3.3 ± 5% Volts.

Chapter 4
Registers

This chapter contains a description of the registers accessed over the management interface (MI) serial interface. It contains the following sections:

- Section 4.1, “Bit Types”
- Section 4.2, “MI Serial Port Register Summary”
- Section 4.3, “Registers”

For further information about the operation of the MI serial interface, see Chapter 5, “Management Interface.”

4.1 Bit Types

Because the serial port is bidirectional (capable of both read and write operations), there are many types of bits. The following bit type definitions are summarized in Table 4.1:

- Write bits (W) are inputs during a write cycle and are high impedance during a read cycle
- Read bits (R) are outputs during a read cycle and high impedance during a write cycle
- Read/Write bits (R/W) are actually write bits that can be read out during a read cycle
- R/WSC bits are R/W bits that are self-clearing after a set period of time or after a specific event has completed
- R/LL bits are read bits that latch themselves when they go LOW, and they stay LOW until read. After they are read, they are reset HIGH.
- R/LH bits are the same as R/LL bits, except that they latch HIGH.

- R/LT are read bits that latch themselves whenever they make a transition or change value, and they stay latched until they are read. After R/LT bits are read, they are updated to their current value.

Table 4.1 MI Register Bit Type Definition

Symbol	Name	Definition	
		Write Cycle	**Read Cycle**
W	Write	Input	No operation, Hi-Z
R	Read	No operation, Hi-Z	Output
R/W	Read/Write	Input	Output
R/WSC	Read/Write, Self-Clearing	Input	Output (clears itself after the operation completes)
R/LL	Read/Latching LOW	No operation, Hi-Z	Output When the bit goes LOW, it is latched. When the bit is read, it is updated.
R/LH	Read/Latching HIGH	No operation, Hi-Z	Output When the bit goes HIGH, it is latched. When the bit is read, it is updated.
R/LT	Read/Latching on transition	No operation, Hi-Z	Output When the bit transitions, the bit is latched. When the bit is read, the bit is updated.

4.2 MI Serial Port Register Summary

The following tables summarize the device registers accessible through the MI serial port.

Control Register (Register 0)

15	14	13	12	11	10	9	8
RST	LPBK	SPEED	ANEG_EN	PDN	MII_DIS	ANEG_RST	DPLX

7	6	0
COLTST	Reserved	

Status Register (Register 1)

15	14	13	12	11	10	8
CAP_T4	CAP_TXF	CAP_TXH	CAP_TF	CAP_TH	Reserved	

7	6	5	4	3	2	1	0
Reserved	CAP_SUPR	ANEG_ACK	REM_FLT	CAP_ANEG	LINK	JAB	EXREG

PHY ID #1 Register (Register 2) –

15	14	13	12	11	10	9	8
OUI3	OUI4	OUI5	OUI6	OUI7	OUI8	OUI9	OUI10

7	6	5	4	3	2	1	0
OUI11	OUI12	OUI13	OUI14	OUI15	OUI16	OUI17	OUI18

PHY ID #2 Register (Register 3)

15	14	13	12	11	10	9	8
OUI19	OUI20	OUI21	OUI22	OUI23	OUI24	PART5	PART4

7	6	5	4	3	2	1	0
PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0

AutoNegotiation Advertisement Register (Register 4)

15	14	13	12 10	9	8
NP	ACK	RF	Reserved	T4	TX_FDX

7	6	5	4 1	0
TX_HDX	10_FDX	10_HDX	Reserved	CSMA

AutoNegotiation Remote End Capability Register (Register 5)

15	14	13	12 10	9	8
NP	ACK	RF	Reserved	T4	TX_FDX

7	6	5	4 1	0
TX_HDX	10_FDX	10_HDX	Reserved	CSMA

Configuration Register (Register 17)

15	14	13	12	11	10	9	8
PLED3_1	PLED3_0	PLED2_1	PLED2_0	PLED1_1	PLED1_0	PLED0_1	PLED0_0

7	6	5	4	3	2 1	0
LED_DEF1	LED_DEF0	APOL_DIS	JAB_DIS	MREG	Reserved	

Status Output Register (Register 18)

15 8
Reserved

7 5	4	3	2 0
Reserved	SPD_DET	DPLX_DET	Reserved

4.3 Registers

This section contains a description of each of the bits in each register.

4.3.1 Control Register (Register 0)

The default value for this register is 0x3400.

15	14	13	12	11	10	9	8
RST	LPBK	SPEED	ANEG_EN	PDN	MII_DIS	ANEG_RST	DPLX

7	6	0
COLTST	Reserved	

RST **Reset** **R/WSC 15**

Bit	Meaning
1	Reset. The bit is bit self-clearing in less than or equal to 200 µs after reset finishes.
0	Normal (Default)

LPBK **Loopback Enable** **R/W 14**

Bit	Meaning
1	Loopback mode enabled
0	Normal (Default)

SPEED **Speed Select** **R/W 13**

Bit[1]	Meaning
1	100 Mbit/s (100BASE-TX) (default)
0	10 Mbit/s (10BASE-T)

1. The SPEED bit is effective only when AutoNegotiation is off

ANEG_EN **AutoNegotiation Enable** **R/W 12**

Bit	Meaning
1	1 = AutoNegotiation enabled (default)
0	0 = Disabled

PDN **Power Down Enable** **R/W 11**

Bit	Meaning
1	Power down
0	Normal (default)

MII_DIS **MII Interface Disable** **R/W 10**

Bit[1]	Meaning
0	MII interface disable
1	Normal (default)

1. If MDA[4:0]n is not read as 0b11111, the MII_DIS default value is changed to 0.

ANEG_RST **AutoNegotiation Reset** **R/WSC 9**

Bit	Meaning
1	Restart AutoNegotiation process. The bit is self-clearing after reset is finished
0	Normal (default)

DPLX **Duplex Mode Select** **R/W 8**

Bit[1]	Meaning
1	Full-duplex (default)
0	Half-duplex

1. This bit is effective only when AutoNegotiation is off

COLTST **Collision Test Enable** **R/W 7**

Bit	Meaning
1	Collision test enabled
0	Normal (default)

R **Reserved** **R [6:0]**

These bits are reserved and must remain at the default value of 0x00 for proper device operation.

4.3.2 Status Register (Register 1)

The default value of this register is 0x7809.

15	14	13	12	11	10		8
CAP_T4	CAP_TXF	CAP_TXH	CAP_TF	CAP_TH	Reserved		

7	6	5	4	3	2	1	0
Reserved	CAP_SUPR	ANEG_ACK	REM_FLT	CAP_ANEG	LINK	JAB	EXREG

CAP_T4 **100BASE-T4 Capable** **R 15**

Bit	Meaning
1	Capable of 100BASE-T4 operation
0	Not capable of 100BASE-T4 Operation (default)

CAP_TXF **100BASE-TX Full Duplex Capable** **R 14**

Bit	Meaning
1	Capable of 100BASE-TX Full-Duplex (default)
0	Not capable of 100BASE-TX Full-Duplex

CAP_TXH **100BASE-TX Half Duplex Capable** **R 13**

Bit	Meaning
1	Capable of 100BASE-TX Half-Duplex (default)
0	Not capable of 100BASE-TX Half-Duplex

CAP_TF **10BASE-T Full Duplex Capable** **R 12**

Bit	Meaning
1	Capable of 10BASE-T Full-Duplex (default)
0	Not capable of 10BASE-T Full-Duplex

CAP_TH **10BASE-T Half Duplex Capable** **R 11**

Bit	Meaning
1	Capable of 10BASE-T Half Duplex (default)
0	Not capable of 10BASE-T Half Duplex

R **Reserved** **R [10:7]**

These bits are reserved and must remain at the default value of 0x0 for proper device operation

CAP_SUPR **MI Preamble Suppression Capable** **R 6**

Bit	Meaning
1	Capable of accepting MI frames with preamble suppression
0	Not capable of accepting MI frames with preamble suppression (default)

ANEG_ACK **AutoNegotiation Acknowledgment** **R 5**

Bit	Meaning
1	AutoNegotiation acknowledgment process complete
0	AutoNegotiation not complete (default)

REM_FLT **Remote Fault Detect** **R/LH 4**

Bit	Meaning
1	Remote fault detect. The REM_FLT bit is set when Remote Fault (RF) bit is set in the AutoNegotiation Remote End Capability register.
0	No remote fault (default)

CAP_ANEG **AutoNegotiation Capable** **R 3**

Bit	Meaning
1	Capable of AutoNegotiation (default)
0	Not capable of AutoNegotiation

LINK **Link Status** **R/LL 2**

Bit	Meaning
1	Link detected.
0	Link not detected (default)

JAB **Jabber Detect** **R/LH 1**

Bit	Meaning
1	Jabber detected
0	Normal (default)

EXREG **Extended Register Capable** **R 0**

Bit	Meaning
1	Extended registers exist (default)
0	Extended registers do not exist

4.3.3 PHY ID 1 Register (Register 2)

15	14	13	12	11	10	9	8
OUI3	OUI4	OUI5	OUI6	OUI7	OUI8	OUI9	OUI10

7	6	5	4	3	2	1	0
OUI11	OUI12	OUI13	OUI14	OUI15	OUI16	OUI17	OUI18

OUI[3:18] **Company ID, Bits 3–18** **R [15:0]**

OUI[3:18] in this register and OUI[19:24] of the PHY ID 2 register make up the LSI OUI, whose default value is 0x00.A07D. The table below shows the default bit positions for the entire OUI field:

Bit	Default Value	Hex Value
OIU24	0	0x7
OIU23	1	
OIU22	1	
OIU21	1	
OIU20	1	0xD
OIU19	1	
OIU18	0	
OIU17	1	
OIU16	1	0xA
OIU15	0	
OIU14	1	
OIU13	0	
OIU12	0	0x0
OIU11	0	
OIU10	0	
OIU9	0	

Bit	Default Value	Hex Value
OIU8	0	0x0
OIU7	0	
OIU6	0	
OIU5	0	
OIU4	0	0x0
OUI3	0	

4.3.4 PHY ID 2 Register (Register 3)

15	14	13	12	11	10	9	8
OUI19	OUI20	OUI21	OUI22	OUI23	OUI24	PART5	PART4

7	6	5	4	3	2	1	0
PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0

OUI[19:24] **Company ID, Bits 19–24** **R [15:10]**
OUI[19:24] in this register and OUI[3:18] of the PHY ID 1 register make up the LSI OUI, whose default value is 0x00.A07D. See the table in the PHY ID 1 description for a description of the entire OUI field.

PART[5:0] **Manufacturer's Part Number** **R [9:4]**
The default value for this field is 0x04. The table below shows the default bit positions for the PART[5:0] field:

Bit	Default Value	Hex Value
PART[5]	0	0x0
PART[4]	0	
PART[3]	0	0x4
PART[2]	1	
PART[1]	0	
PART[0]	0	

REV[3:0] **Manufacturer's Revision Number** **R [3:0]**
The default value for this field is 0x0.

4.3.5 AutoNegotiation Advertisement Register (Register 4)

The default value for this register is 0x01E1.

15	14	13	12 10	9	8
NP	ACK	RF	Reserved	T4	TX_FDX

7	6	5	4 1	0
TX_HDX	10_FDX	10_HDX	Reserved	CSMA

NP **Next Page Enable** **R 15**

Bit	Meaning
1	Next page
0	No next page (default)

ACK **Acknowledge** **R 14**

Bit	Meaning
1	AutoNegotiation word recognized
0	Not recognized (default)

RF **Remote Fault** **R/W 13**

Bit	Meaning
1	AutoNegotiation remote fault detect
0	No remote fault detect (default)

R **Reserved** **R/W[12:10]**

These bits are reserved and must remain at the default value of 0b00 for proper device operation

T4 **100BASE-T4 Capable** **R/W 9**

Bit	Meaning
1	Capable of 100BASE-T4 operation
0	Not capable (default)

TX_FDX **100BASE-TX Full Duplex Capable** **R/W 8**

Bit	Meaning
1	Capable of 100BASE-TX Full Duplex operation (default)
0	Not capable

TX_HDX **100BASE-TX Half Duplex Capable** **R/W 7**

Bit	Meaning
1	Capable of 100BASE-TX Half Duplex operation (default)
0	Not capable

10_FDX **10BASE-TX Full Duplex Capable** **R/W 6**

Bit	Meaning
1	Capable of 10BASE-T Full-Duplex operation (default)
0	Not capable

10_HDX **10BASE-TX Half Duplex Capable** **R/W 5**

Bit	Meaning
1	Capable of 10BASE-T Half-Duplex operation (default)
0	Not capable

R **Reserved** **R/W [4:1]**

These bits are reserved and must remain at the default value of 0x0 for proper device operation

CSMA **CSMA 802.3 Capable** **R/W 0**

Bit	Meaning
1	Capable of 802.3 CSMA[1] operation (default)
0	Not capable

1. Carrier-Sense, Multiple-Access

4.3.6 AutoNegotiation Remote End Capability Register (Register 5)

The default value for this register is 0x0000.

15	14	13	12 10	9	8
NP	ACK	RF	Reserved	T4	TX_FDX

7	6	5	4 1	0
TX_HDX	10_FDX	10_HDX	Reserved	CSMA

NP **Next Page Enable** **R 15**

Bit	Meaning
1	Next Page exists
0	No Next Page (default)

ACK **Acknowledge** **R 14**

Bit	Meaning
1	Received AutoNegotiation Word recognized
0	Not Recognized (default)

RF **Remote Fault** **R 13**

Bit	Meaning
1	AutoNegotiation Remote Fault detect
0	No Remote Fault (default)

R **Reserved** **R [12:10]**

These bits are reserved and must remain at the default value of 0b00 for proper device operation

T4 **100BASE-T4 Capable** **R 9**

Bit	Meaning
1	Capable of 100BASE-T4 operation
0	Not capable (default)

TX_FDX **100BASE-TX Full Duplex Capable** **R 8**

Bit	Meaning
1	Capable of 100BASE-TX Full Duplex operation
0	Not capable (default)

TX_HDX **100BASE-TX Half Duplex Capable** **R 7**

Bit	Meaning
1	Capable of 100BASE-TX Half Duplex operation
0	Not capable (default)

10_FDX **10BASE-TX Full Duplex Capable** **R 6**

Bit	Meaning
1	Capable of 10BASE-T Full Duplex operation
0	Not capable (default)

10_HDX **10BASE-TX Half Duplex Capable** **R 5**

Bit	Meaning
1	Capable of 10BASE-T Half Duplex operation
0	Not capable (default)

R **Reserved** **R [4:1]**

These bits are reserved and must remain at the default value of 0x0 for proper device operation

CSMA **CSMA 802.3 Capable** **R 0**

Bit	Meaning
1	Capable of 802.3 CSMA[1] Operation
0	Not capable (default)

1. Carrier-Sense, Multiple-Access

4.3.7 Configuration Register (Register 17)

The default value for this register is 0xFF00.

15	14	13	12	11	10	9	8
PLED3_1n	PLED3_0n	PLED2_1n	PLED2_0n	PLED1_1n	PLED1_0n	PLED0_1n	PLED0_0n

7			4	3	2	1	0
LED_DEF1	LED_DEF0	APOL_DIS	JAB_DIS	MREG	Reserved		

PLED3_[1:0]n Programmable LED 3 Output Select R/W [15:14]

PLED3_1n	PLED3_0n	Meaning
1	1	Normal: PLED3n pin state is determined from the LED_DEF[1:0] bits (default is LINK100). 0b11 is the default for these bits
1	0	LED tied to PLED3n blinks (toggles 100 ms LOW, then 100 ms HIGH)
0	1	LED tied to PLED3n ON steady (PLED3n output LOW)
0	0	LED tied to PLED3n OFF steady (PLED3n output HIGH)

PLED2_[1:0]n Programmable LED 2 Output Select R/W [13:12]

PLED2_1n	PLED2_0n	Meaning
1	1	Normal: PLED2n pin state is determined from the LED_DEF[1:0] bits (default is Activity). 0b11 is the default for these bits
1	0	LED tied to PLED2n blinks (toggles 100 ms LOW, then 100 ms HIGH)
0	1	LED tied to PLED2n ON steady (PLED2n output LOW)
0	0	LED tied to PLED2n OFF steady (PLED2n output HIGH)

PLED1_[1:0]n Programmable LED 1 Output Select **R/W [11:10]**

PLED1_1n	PLED1_0n	Meaning
1	1	Normal: PLED1n pin state is determined from the LED_DEF[1:0] bits (default is Full-Duplex). 0b11 is the default for these bits
1	0	LED tied to PLED1n blinks (toggles 100 ms LOW, then 100 ms HIGH)
0	1	LED tied to PLED1n ON steady (PLED1n output LOW)
0	0	LED tied to PLED1n OFF steady (PLED1n output HIGH)

PLED0_[1:0]n Programmable LED 0 Output Select **R/W [9:8]**

PLED3_1n	PLED3_0n	Meaning
1	1	Normal: PLED0n pin state is determined from the LED_DEF[1:0] bits (default is Link 10). 0b11 is the default for these bits
1	0	LED tied to PLED0n blinks (toggles 100 ms LOW, then 100 ms HIGH)
0	1	LED tied to PLED0n ON steady (PLED0n output LOW)
0	0	LED tied to PLED0n OFF steady (PLED0n output HIGH)

LED_DEF_[1:0]

LED Normal Function Select **R/W [7:6]**

See Table 2.7 on page 2-29 for these bit definitions.

APOL_DIS Autopolarity Disable **R 5**

Bit	Meaning
1	Autopolarity correction disabled
0	Normal (default)

JAB_DIS **Jabber Disable** **R 4**

Bit	Meaning
1	Jabber disabled
0	Jabber enabled (default)

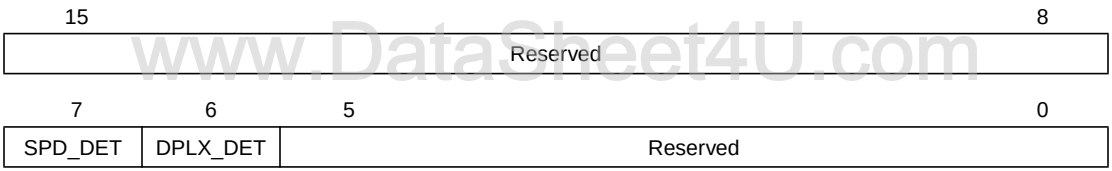
MREG **Multiple Register Access Enable** **R 3**

Bit	Meaning
1	Multiple register access enabled
0	No multiple register access (default)

R **Reserved** **R [2:0]**
These bits are reserved and must remain at the default value of 0x0 for proper device operation.

4.3.8 Channel Status Output 0 Register (Register 18)

The default value for this register is 0x0000.



SPD_DET **100/10 Mbits/s Speed Detect** **R 7**

Bit	Meaning
1	Device is in 100 Mbits/s mode (100BASE-TX)
0	Device is in 10 Mbits/s mode (10 BASE-T)

DPLX_DET **Duplex Detect** **R 6**

Bit	Meaning
1	Device is operating in Full-Duplex
0	Device is operating in Half-Duplex

R **Reserved** **R [5:0]**
These bits are reserved and must remain at the default value of 0x0 for proper device operation.

Chapter 5
Management Interface

This chapter describes the Management Interface, over which the internal device registers are accessed. It contains the following sections:

The Management Interface, referred to as the MI serial port, is a 7-pin bidirectional link through which the internal device registers are accessed. The internal register bits control the configuration and capabilities of the device, and reflect device status.

The MI serial port provides access to eight internal registers and meets all IEEE 802.3 specifications for the Management Interface.

5.1 Signal Description

The MI serial port has six pins:

- MDC – serial shift clock input pin
- MDIO – bidirectional data pin
- MDA[3:0]n – physical address pins

The MDA[3:0]n pins configure the device for a particular address, from 0b0000 to 0b1111, such that 16 devices can exist in the same address domain and each can be addressed separately over the MI serial port. When an MI read or write cycle occurs, the device compares the internally inverted and latched state of the MDA[4:0]n pins to the

PHYAD[4:0] address bits of the MI frame. If the states compare, the device knows it is being addressed.

The MDA[3:0]n inputs share the same pins as the PLED[3:0]n LED outputs, respectively. At powerup or reset, the LED output drivers are 3-stated for an interval called the power-on reset time. During the power-on reset time, the level of these pins is latched into the device, inverted, and used as the MI serial port physical device address.

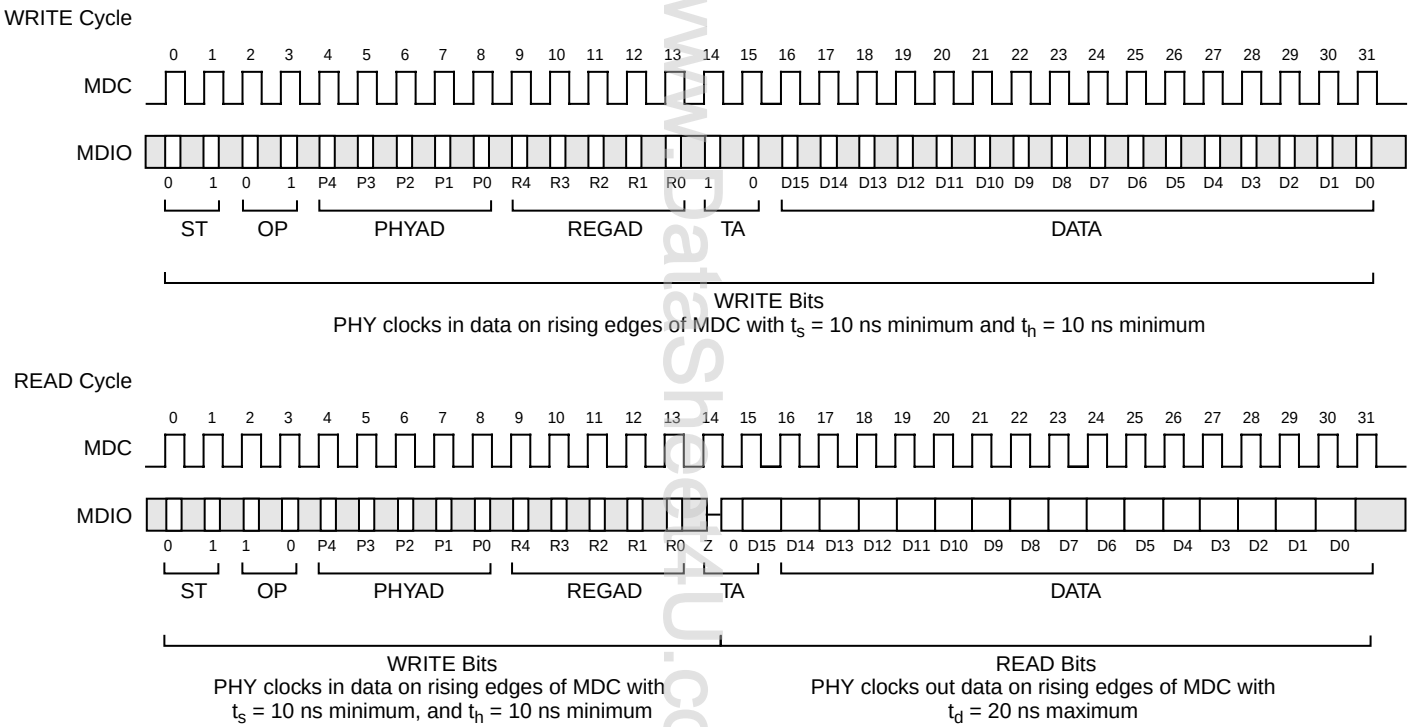
5.2 General Operation

The MI serial port is idle when at least 32 continuous 1s are detected on the bidirectional MDIO data pin and remains idle as long as continuous 1s are detected. During idle, the MDIO output driver is in the high-impedance state. When the MI serial port is in the idle state, a 0b01 pattern on the MDIO pin initiates a serial shift cycle. Control and address bits are clocked into MDIO on the next 14 rising edges of MDC (the MDIO output driver is still in a high-impedance state). If multiple register access is not enabled, data is either shifted in or out on MDIO on the next 16 rising edges of MDC, depending on whether a write or read cycle was selected with the READ and WRITE operation bits. After the 32 MDC cycles have been completed

- one complete register has been read or written
- the serial shift process is halted
- data is latched into the device
- the MDIO output driver goes into a high-impedance state.

Another serial shift cycle cannot be initiated until the idle condition is detected again (at least 32 continuous 1s). Figure 5.1 shows a timing diagram for a MI serial port cycle.

Figure 5.1 MI Serial Port Frame Timing Diagram



Note: ST = start bits, OP = operation bits (read or write), PHAD = PHY address, REGAD = register address, TA = turnaround bits
For more detailed information on the timing related to t_s, t_h, and t_d, please see Chapter 6, “Specifications.”

5.3 Frame Structure

The structure of the serial port frame is shown in Figure 5.2 and a timing diagram is shown in Figure 5.1. Each serial port access cycle consists of 32 bits (or 144 bits if multiple register access is enabled and REGAD[4:0] = 0b11111), exclusive of idle. The first 16 bits of the serial port cycle are always write bits and are used for control and addressing. The last 16 bits are data that is written to or read from a data register.

The first two bits in Figure 5.2 and Figure 5.1 are start bits (ST[1:0]) and must be written as a 0b01 for the serial port cycle to continue. The next two bits are the READ and WRITE bits, which determine whether the registers are being read or written. The next five bits are the PHY device address bits (PHYAD[4:0]), and they must match the inverted values latched from the MDA[4:0]n pins during the power on reset time for access to continue.

The next five bits are register address select (REGAD[4:0]) bits, which select one of the eight registers for access. The next two bits are turnaround (TA) bits, which are not actual register bits but provide the device extra time to switch the MDIO pin function from a write pin to a read pin, if necessary. The final 16 bits of the MI serial port cycle are written to or read from the specific data register that the register address bits (REGAD[4:0]) designate. Figure 5.2 shows the MI frame structure.

Figure 5.2 MI Serial Frame Structure

IDLE	ST[1:0]	READ	WRITE	PHYAD[4:0]	REGAD[4:0]	TA[1:0]	D[15:0]

IDLE **Idle Pattern** **W**
These bits are an idle pattern. The device does not initiate an MI cycle until it detects an idle pattern of at least 32 consecutive 1s.

ST[1:0] **Start Bits** **W**
When ST[1:0] = 01, a MI serial port access cycle starts.

READ **Read Select** **W**
When the READ bit is 1, it designates a read cycle.

WRITE	**Write Select** When the WRITE bit is 1, it designates a write cycle.	**W**
PHYAD[4:0]	**Physical Device Address** When the PHYAD[4:0] bits match the inverted latched value of the MDA[4:0]n pins, the device's MI serial port is selected for operation.	**W**
REGAD[4:0]	**Register Address** The REGAD[4:0] bits determine the specific register to access.	**W**
TA[1:0]	**Turnaround Time** These bits provide some turnaround time for MDIO to allow it to switch to a write input or read output, as needed. When READ = 1, TA[1:0] = Z0; when WRITE = 1, TA[1:0] = 0b10**.**	**R/W**
D[15:0]	**Data** These 16 bits contain data to or from one of the registers selected with the register address bits REGAD[4:0].	**R or W**

5.4 Register Structure

The device has eight 16-bit registers. A map of the registers is shown in Section 4.2, "MI Serial Port Register Summary". See Chapter 4, Registers for a complete description of each register.

The eight registers consist of six registers that are defined by IEEE 802.3 specifications (registers 0 to 5) and two registers that are unique to the device (registers 17 and 18). Table 5.1 gives a summary of the functions of each register

Table 5.1 MI Serial Port Register Summary

Register	Name	Description
0	Control Register	Stores various configuration bits
1	Status Register	Contains device capability and status output bits
2	PHY ID 1	Contain an identification code unique to the device
3	PHY ID 2	
4	AutoNegotiation Advertisement	Contains bits that control the operation of the AutoNegotiation algorithm
5	AutoNegotiation Remote End Capability	Contains bits that reflect the AutoNegotiation capabilities of the link partner's PHY
17	Configuration	Stores various configuration bits
18	Channel Status Output 0	Contains status

Chapter 6
Specifications

This chapter contains the complete electrical, timing, and mechanical specifications for the device. It contains the following sections:

6.1 Absolute Maximum Ratings

Table 6.1 shows the device absolute maximum ratings. These are limits which, if exceeded, could cause permanent damage to the device or affect device reliability. All voltages are specified with respect to GND unless otherwise specified.

Table 6.1 Absolute Maximum Ratings

Parameter	Range	Units
V_{DD} Supply Voltage	–0.3V to +4.0V	V
All Inputs and Outputs	–0.3V to 5.5V	V
Package Power Dissipation	2.0 @ 70˚C	W
Storage Temperature	–65 to +150	˚C
Temperature Under Bias	–10 to +80	˚C
Commercial Temperature	-10 to +80	˚C
Industrial Temperature	-40 to +85	˚C
Lead Temperature (soldering, 10 sec)	260	˚C
Body Temperature (soldering, 30 sec)	220	˚C

6.2 Electrical Characteristics

Table 6.2 lists the device DC electrical characteristics. Unless otherwise noted, all test conditions are as follows:

TA = 0 to + 70 ˚C (commercial), -40 to + 85 ˚C (industrial)
V_{DD} = 3.3 V ±5%
Clock = 25 MHz + 0.01%
REXT = 10 KΩ + 1%, no load

Table 6.2 DC Characteristics

Sym	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
VIL	Input Low Voltage			0.8	Volt	All except OSCIN, MDA[3:0]n
				V_{DD} – 1.0	Volt	MDA[3:0]n
				1.5	Volt	OSCIN
VIH	Input High Voltage	2		5.5	Volt	All except OSCIN, MDA[3:0]n
		V_{DD} – 200			mV	MDA[3:0]n
		2.3			Volt	OSCIN
IIL	Input Low Current			–1	µA	VIN=GND. All except OSCIN, MDA[3:0]n, RESETn
		–4		–25	µA	VIN = GND. MDA[3:0]n
		–12		–120	µA	VIN = GND. RESETn
				–150	µA	VIN = GND. OSCIN
IIH	Input High Current			1	µA	VIN = V_{DD}. All except OSCIN
				150	µA	VIN = V_{DD}. OSCIN
VOL	Output Low Voltage			0.4	Volt	IOL = –4 mA. All except PLED[5:0]n
				1	Volt	IOL = –10 mA. PLED[5:0]n

Table 6.2 DC Characteristics (Cont.)

Sym	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
VOH	Output High Voltage	V_{DD} – 1.0			Volt	IOH = 4 mA. All Except PLED[5:0]n
		2.4			Volt	IOH = 4 µA. PLED[5:2]n
		V_{DD} – 1.0			Volt	IOH = 10mA. PLED[1:0]n
CIN	Input Capacitance		5		pF	
IDD	V_{DD} Supply Current			120	mA	Transmitting, 100 Mbits/s
				140	mA	Transmitting, 10 Mbits/s
IGND	GND Supply Current			190	mA	Transmitting, 100 Mbits/s[1], Note 1
				220	mA	Transmitting, 10 Mbits/s[1]
IPDN	Powerdown Supply Current			200	µA	Powerdown, either IDD or IGND

1. IGND includes current flowing into GND from the external resistors and transformer on TPO as shown in Figure A.1

6.2.1 Twisted-Pair DC Characteristics

Unless otherwise noted, all test conditions for TP transmit and receive operations are as follows:

TA = 0 to + 70 ˚C (commercial), -40 to + 85 ˚C (industrial)
V_{DD} = 3.3 V ±5%
Clock = 25 MHz ±0.01%
REXT = 10 KΩ ±%, no load
TPO+/- loading is as shown in Figure A.1 or equivalent
62.5/10 MHz Square Wave on TP+/- inputs in 100/10 Mbits/s modes

Table 6.3 shows the twisted-pair characteristics for transmit operation.

Table 6.3 Twisted Pair Characteristics (Transmit)

Sym	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
T_{OV}	TP Differential Output Voltage	0.950	1.000	1.050	V pk	100 Mbits/s, UTP mode, 100 ohm load
		2.2	2.5	2.8	V pk	10 Mbits/s, UTP mode, 100 ohm load
T_{OVS}	TP Differential Output Voltage Symmetry	98		102	%	100 Mbits/s, ratio of positive and negative amplitude peaks on TPO
T_{ORF}	TP Differential Output Rise And Fall Time	3.0		5.0	ns	100 Mbits/s
T_{ORFS}	TP Differential Output Rise And Fall Time Symmetry			±0.5	ns	100 Mbits/s, difference between rise and fall times on TPO
T_{ODC}	TP Differential Output Duty Cycle Distortion			±0.25	ns	100 Mbits/s, output data = 0b 0101... NRZ pattern unscrambled, measure at 50% points
T_{OJ}	TP Differential Output Jitter			±1.4	ns	100 Mbits/s, output data = scrambled /H/
T_{OO}	TP Differential Output Overshoot			5.0	%	100 Mbits/s
T_{OVT}	TP Differential Output Voltage Template	See Figure 2.4				10 Mbits/s
T_{SOI}	TP Differential Output SOI Voltage Template	See Figure 2.6				10 Mbits/s
T_{LPT}	TP Differential Output Link Pulse Voltage Template	See Figure 2.7				10 Mbits/s, NLP and FLP
T_{OIV}	TP Differential Output Idle Voltage			±50	mV	10 Mbits/s. measured on secondary side of transformer in Figure A.1.
T_{OIA}	TP Output Current	38	40	42	mA pk	100 Mbits/s
		88	100	112	mA pk	10 Mbits/s
T_{OIR}	TP Output Current Adjustment Range	0.80		1.2		V_{DD} = 3.3 V, adjustable with REXT, relative to TOIA with REXT = 10 K
T_{OR}	TP Output Resistance		10 K		Ohm	
T_{OC}	TP Output Capacitance		15		pF	

Table 6.4 shows the twisted-pair characteristics for receive operation.

Table 6.4 Twisted Pair Characteristics (Receive)

Sym	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
R_{ST}	TP Input Squelch Threshold	166		500	mV pk	100 Mbits/s, RLVL = 0
		310		540	mV pk	10 Mbits/s, RLVL = 0
R_{UT}	TP Input Unsquelch Threshold	100		300	mV pk	100 Mbits/s, RLVL = 0
		186		324	mV pk	10 Mbits/s, RLVL = 0
R_{OCV}	TP Input Open Circuit Voltage		V_{DD} – 2.4 ± 0.2		Volt	Voltage on either TPI+ or TPI– with respect to GND.
R_{CMR}	TP Input Common-Mode Voltage Range		R_{OCV} ± 0.25			Voltage on TPI± with respect to GND.
R_{DR}	TP Input Differential Voltage Range			V_{DD}	Volt	
R_{IR}	TP Input Resistance	5K			Ohm	
R_{IC}	TP Input Capacitance		10		pF	

6.3 AC Electrical Characteristics

Unless otherwise noted, all test conditions are as shown in Table 6.5.

Table 6.5 Test Conditions

Test Condition	Parameter	Value
Temperature (commercial)	TA	0 to +70 C
Temperature (industrial)	TA	-40 to +85 C
Voltage	V_{DD}	3.3V ± 5%
Clock Frequency		25 MHz 0.01%
External Resistor	REXT	10K 1%, no load
Input Conditions (all inputs)	tr, tf	≤ 10 ns, 20-80% points
Output Loading		
TPO	Same as Figure A.1 or equivalent	10 pF
Open-drain outputs		1K pullup, 50 pF
All other digital outputs		25 pF
Measurement Points		
TPO ,TPI		0.0 V during data, 0.3 V at start/end of packet
All other inputs and outputs		1.4 V

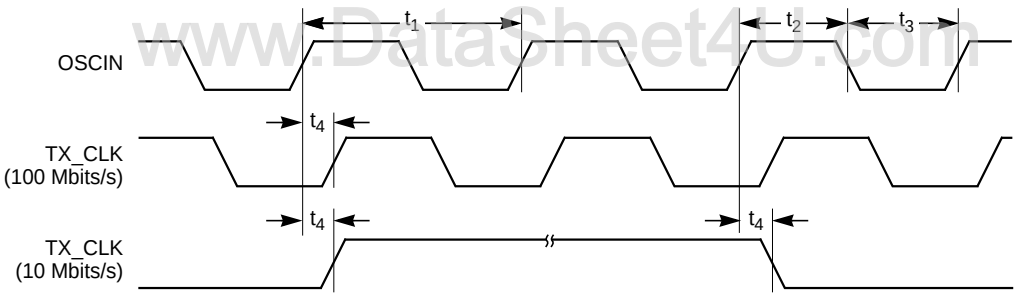
6.3.1 25 MHz Input/Output Clock Timing Characteristics

Table 6.6 shows the 25 MHz input/Output Clock timing parameters. See Figure 6.1 for the timing diagram.

Table 6.6 25 MHz Input/Output Clock

Sym	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t1	OSCIN Period	39.996	40	40.004	ns	Clock applied to OSCIN
t2	OSCIN High Time	16			ns	Clock applied to OSCIN
t3	OSCIN Low Time	16			ns	Clock applied to OSCIN
t4	OSCIN to TX_CLK Delay			10	ns	100 Mbits/s
				20	ns	10 Mbits/s

Figure 6.1 25 MHz Output Timing



6.3.2 Transmit Timing Characteristics

Table 6.7 shows the Transmit AC timing parameters. See Figure 6.2 and Figure 6.3 for the 100 Mbits/s and 10 Mbits/s transmit timing diagrams.

Table 6.7 Transmit Timing

Sym	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t11	TX_CLK Period	39.996	40	40.004	ns	100 Mbits/s
		399.96	400	400.04	ns	10 Mbits/s
t12	TX_CLK Low Time	16	20	24	ns	100 Mbits/s
		160	200	240	ns	10 Mbits/s
t13	TX_CLK High Time	16	20	24	ns	100 Mbits/s
		160	200	240	ns	10 Mbits/s
t14	TX_CLK Rise/Fall Time			10	ns	
t15	TX_EN Setup Time	15			ns	Note[1]
t16	TX_EN Hold Time	0			ns	
t17	CRS During Transmit Assert Time			40	ns	100 Mbits/s
				400	ns	10 Mbits/s
t18	CRS During Transmit Deassert Time			160	ns	100 Mbits/s
				900	ns	10 Mbits/s
t19	TXD Setup Time	15			ns	Note 1
t20	TXD Hold Time	0			ns	
t21	TX_ER Setup Time	15			ns	Note 1
t22	TX_ER Hold Time	0			ns	
t23	Transmit Propagation Delay	60		140	ns	100 Mbits/s, MII
				600	ns	10 Mbits/s
t24	Transmit Output Jitter			±0.7	ns pk-pk	100 Mbits/s
				±5.5	ns pk-pk	10 Mbits/s
t25	Transmit SOI Pulse Width To 0.3 V	250			ns	10 Mbits/s
t26	Transmit SOI Pulse Width to 40 mV			4500	ns	10 Mbits/s
t27	PLEDn Delay Time			25	ms	PLEDn programmed for activity
t28	PLEDn Pulse Width	80		105	ms	PLEDn programmed for activity

1. Setup time measured with 5 pF loading on TXC. Additional leading will create delay on TXC rise time which will require increased setup times.

Figure 6.2 Transmit Timing (100 Mbits/s)

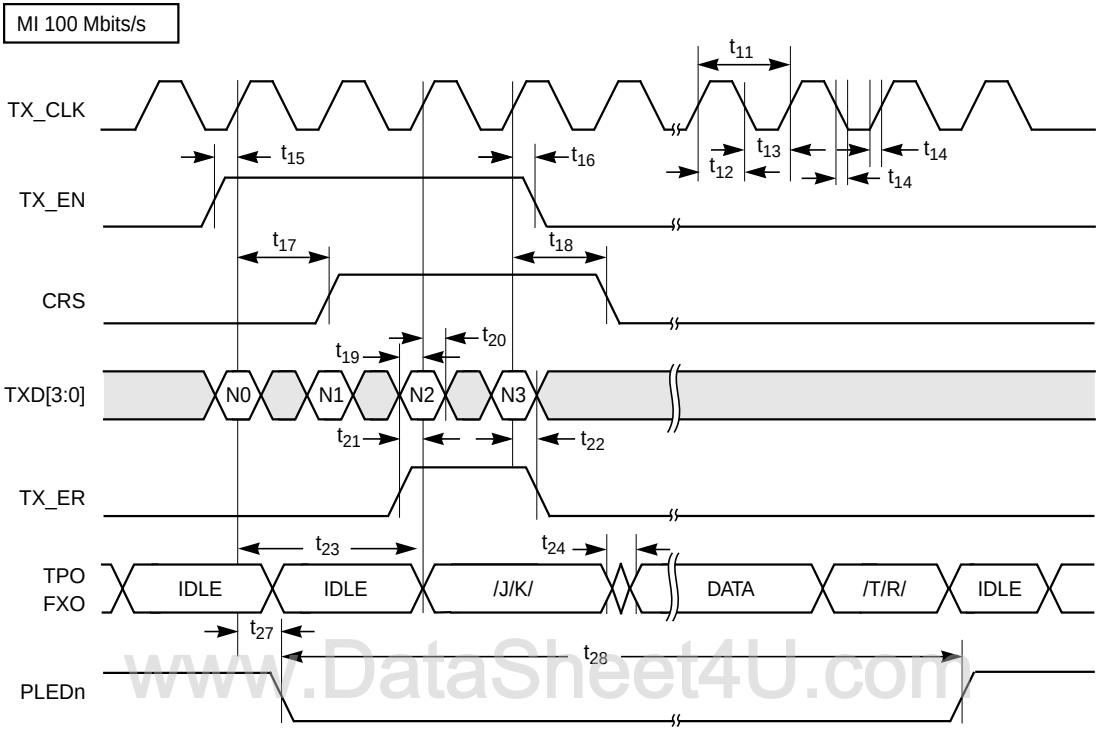
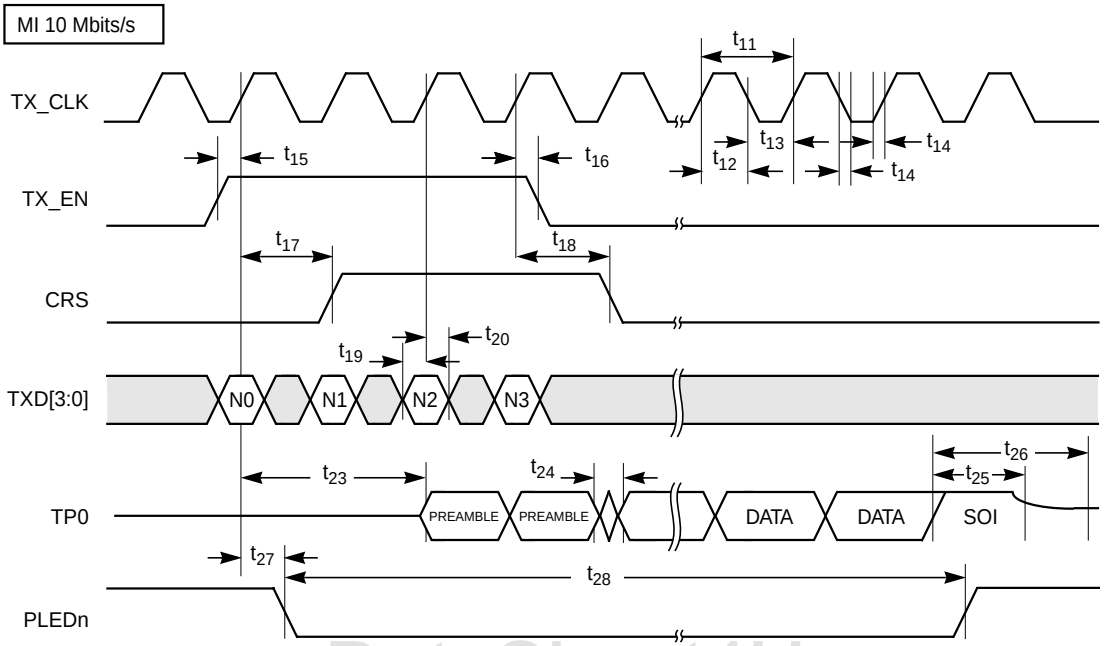


Figure 6.3 Transmit Timing (10 Mbits/s)



6.3.3 Receive Timing Characteristics

Table 6.8 shows the Receive AC timing parameters. See Figure 6.4 through Figure 6.8 for the receive timing diagrams.

Table 6.8 Receive Timing

Sym	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t31	Start of Packet to CRS Assert Delay			200	ns	100 Mbits/s, MII
				700	ns	10 Mbits/s
t32	End of Packet to CRS Deassert Delay	130		240	ns	100 Mbits/s, MII
				600	ns	10 Mbits/s. relative to start of SOI pulse
t33	Start of Packet to RX_DV Assert Delay			240	ns	100 Mbits/s
				3600	ns	10 Mbits/s
t34	End of Packet to RX_DV Deassert Delay			280	ns	100 Mbits/s
				1000	ns	10 Mbits/s. relative to start of SOI pulse
t37	RX_CLK to RX_DV, RXD, RX_ER Delay	–8		8	ns	100 Mbits/s
		–80		80	ns	10 Mbits/s
t38	RX_CLK High Time	18	20	22	ns	100 Mbits/s
		180	200	600	ns	10 Mbits/s
t39	RX_CLK Low Time	18	20	22	ns	100 Mbits/s
		180	200	600	ns	10 Mbits/s
t40	SOI Pulse Minimum Width Required for Idle Detection	125		200	ns	10 Mbits/s measure TPI± from last zero cross to 0.3 V point.

Table 6.8 Receive Timing (Cont.)

Sym	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t41	Receive Input Jitter			±3.0	ns pk – pk	100 Mbits/s
				±13.5	ns pk -pk	10 Mbits/s
t43	PLEDn Delay Time			25	ms	PLEDn Programmed for Activity
t44	PLEDn Pulse Width	80		105	ms	PLEDn Programmed for Activity
t45	RX_CLK, RXD, CRC, RX_DV, RX_ER Output Rise and Fall Times			10	ns	
t46	RX_EN Deassert to Rcv MII Output HI-Z Delay			40	ns	
t47	RX_EN Assert to Rcv MII Output Active Delay			40	ns	

Figure 6.4 Receive Timing, Start of Packet (100 Mbits/s)

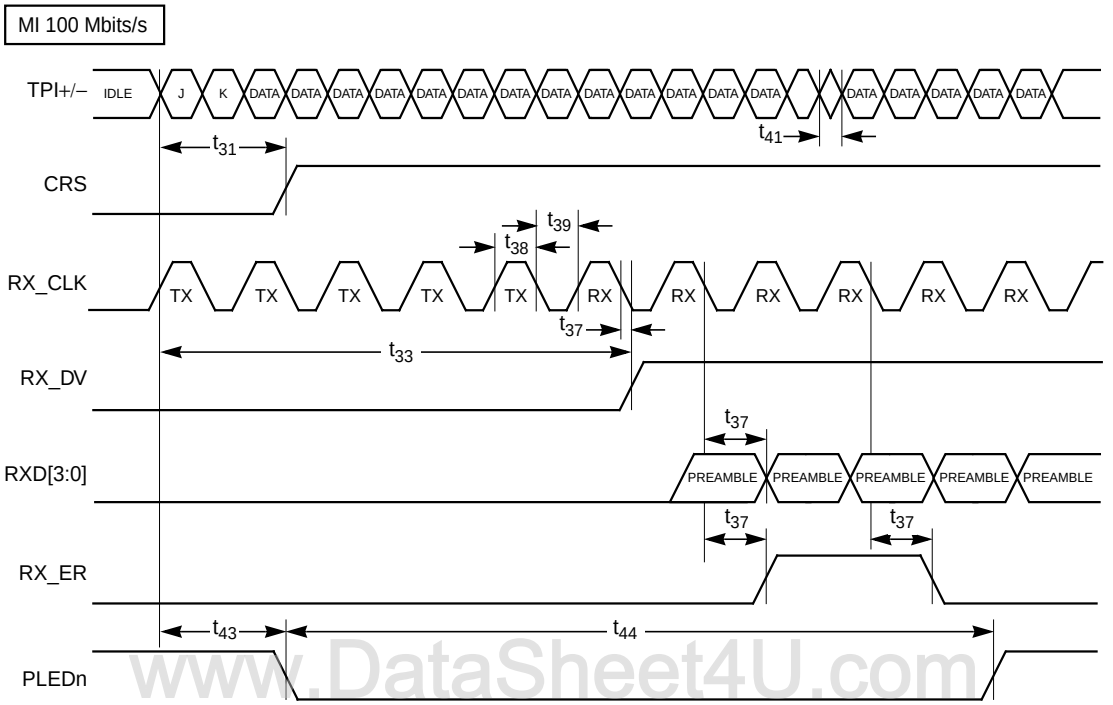


Figure 6.5 Receive Timing, End of Packet (100 Mbits/s)

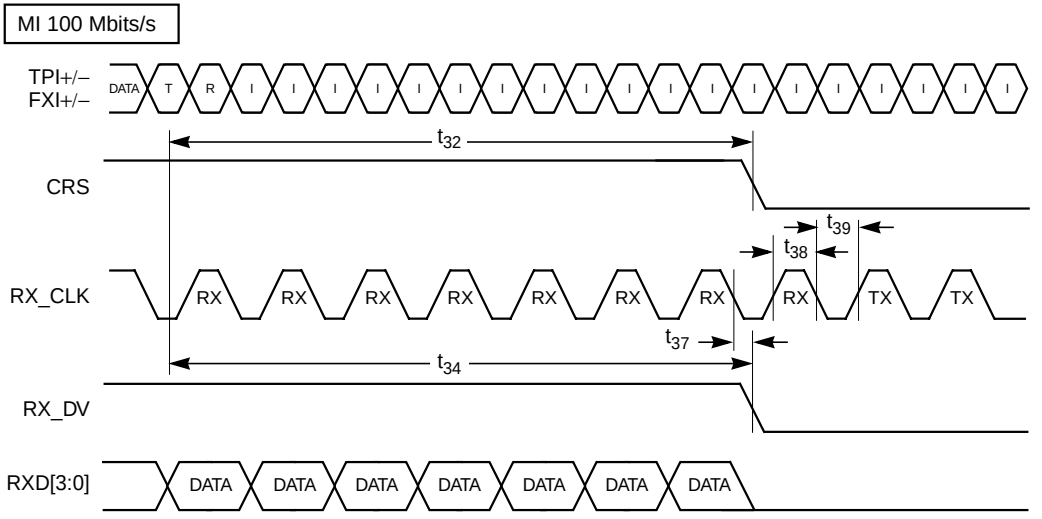


Figure 6.6 Receive Timing, Start of Packet (10 Mbits/s)

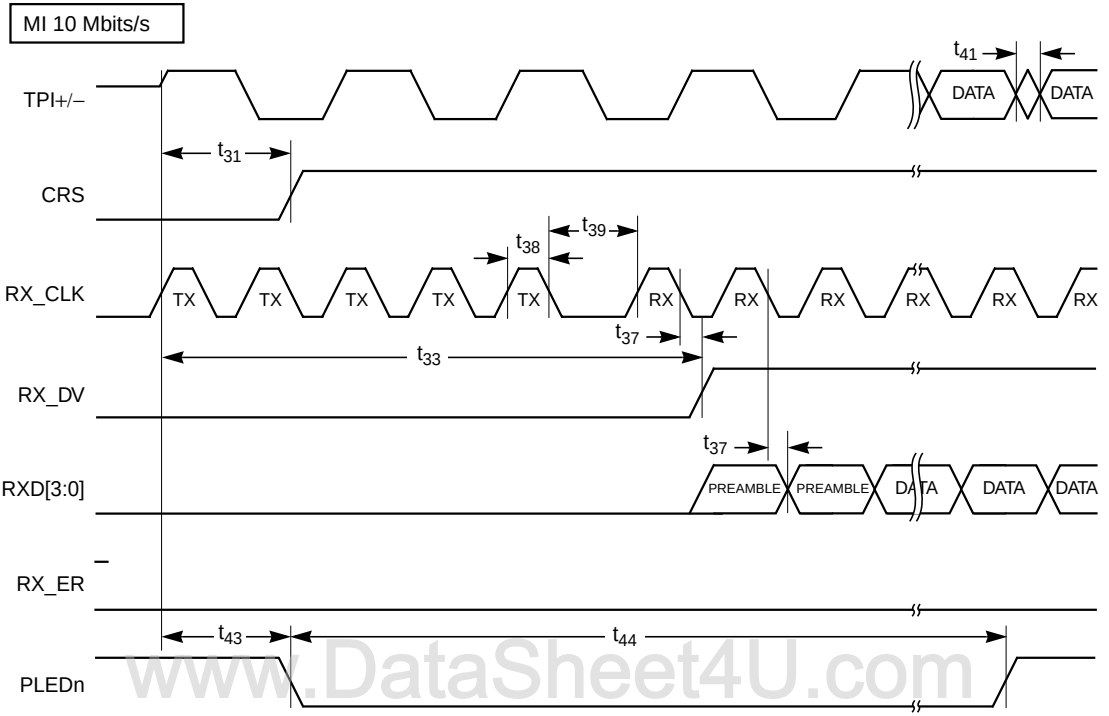


Figure 6.7 Receive Timing, End of Packet (10 Mbits/s)

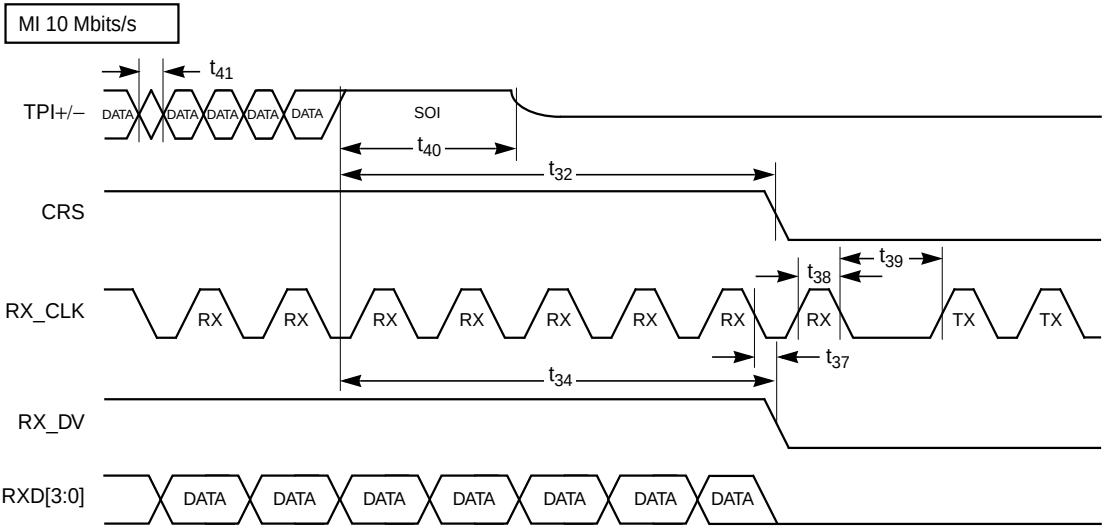
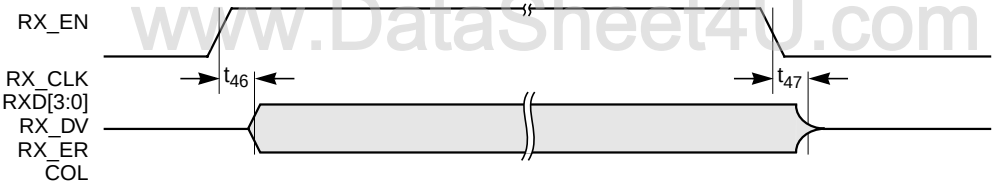


Figure 6.8 RX_EN Timing



6.3.4 Collision and JAM Timing Characteristics

Table 6.9 shows the Collision and JAM timing parameters. See Figure 6.9 through Figure 6.13 for the associated timing diagrams.

Table 6.9 Collision and Jam Timing

Sym	Parameter	Limit				Conditions
		Min	Typ	Max	Unit	
t51	Rcv Packet Start to COL Assert Time			200	ns	100 Mbits/s
				700	ns	10 Mbits/s
t52	Rcv Packet Stop to COL Deassert Time	130		240	ns	100 Mbits/s
				300	ns	10 Mbits/s
t53	Xmt Packet Start to COL Assert Time			200	ns	100 Mbits/s
				700	ns	10 Mbits/s
t54	Xmt Packet Stop to COL Deassert Time			240	ns	100 Mbits/s
				300	ns	10 Mbits/s
t55	PLEDn Delay Time			25	ms	PLEDn Programmed for Collision
t56	PLEDn Pulse Width	80		105	ms	PLEDn Programmed for Collision
t57	Collision Test Assert Time			5120	ns	
t58	Collision Test Deassert Time			40	ns	
t59[1]	CRS Assert to Transmit JAM Packet Start During JAM			300	ns	100 Mbits/s
				800	ns	10 Mbits/s
t60[1]	COL Rise and Fall Time			10	ns	

1. Timing not shown

Figure 6.9 Collision Timing, Receive (100 Mbits/s)

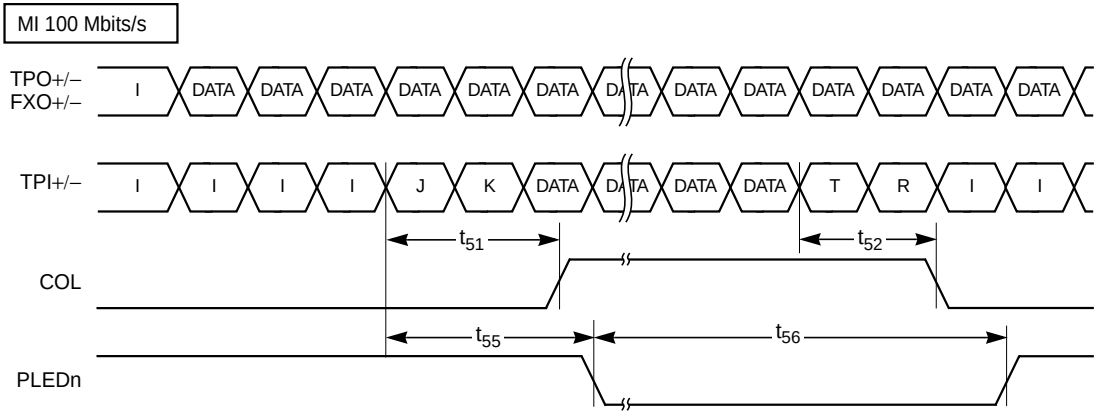


Figure 6.10 Collision Timing, Receive (10 Mbits/s)

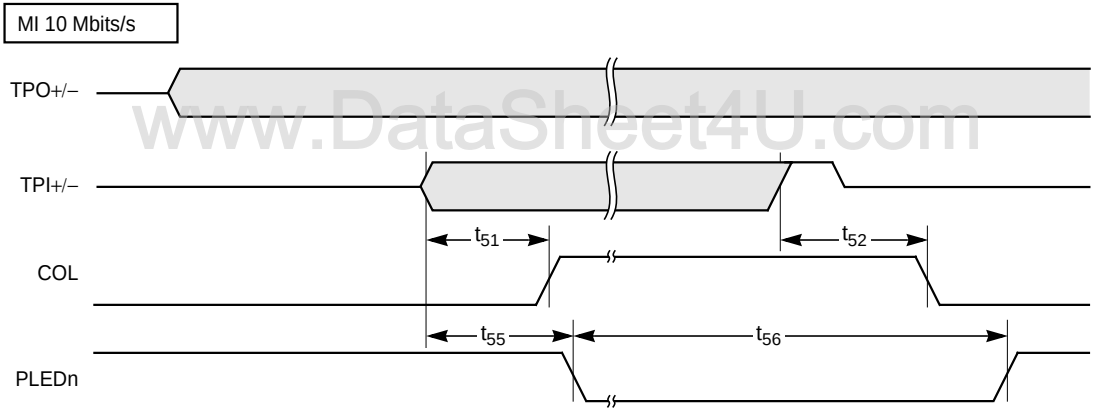


Figure 6.11 Collision Timing, Transmit (100 Mbits/s)

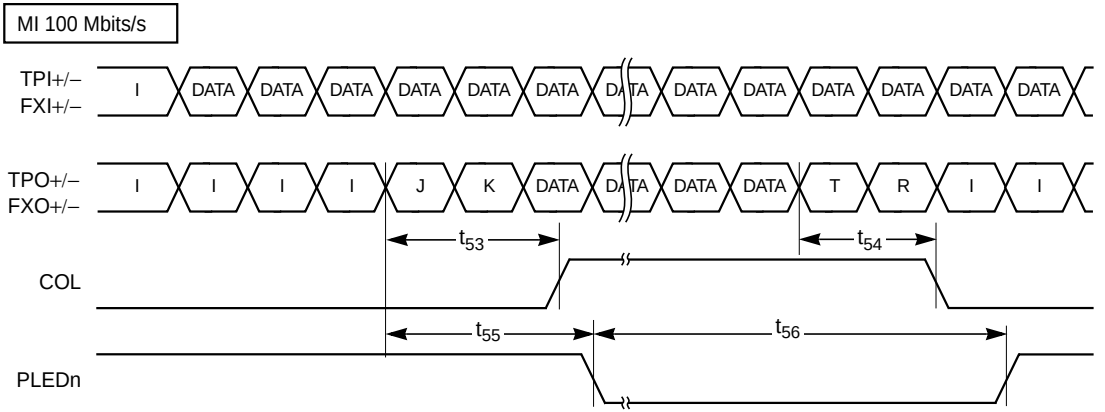


Figure 6.12 Collision Timing, Transmit (10 Mbits/s)

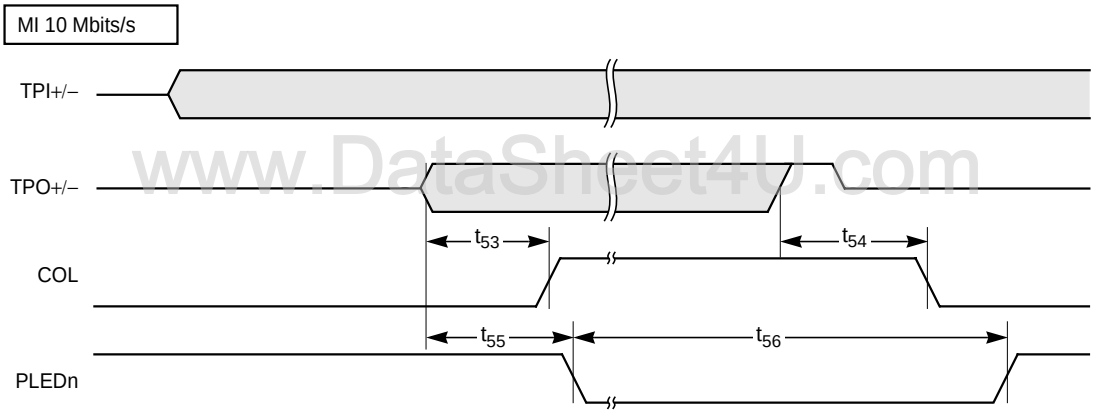
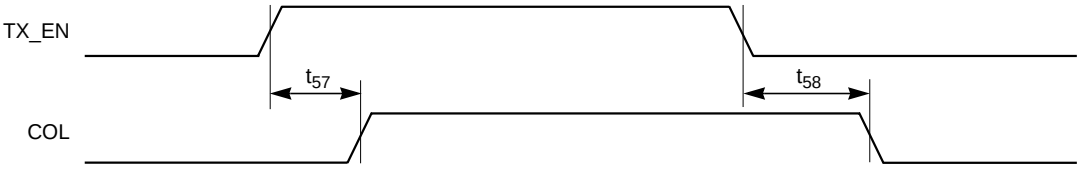


Figure 6.13 Collision Test Timing



6.3.5 Link Pulse Timing Characteristics

Table 6.10 shows the Link Pulse AC timing parameters. See Figure 6.14 and Figure 6.15 for the Link Pulse timing diagrams.

Table 6.10 Link Pulse Timing

Sym	Parameter	Limit			Unit	Condition
		Min	Typ	Max		
t61	NLP Transmit Link Pulse Width	See Figure 2.7			ns	
t62	NLP Transmit Link Pulse Period	8		24	ms	
t63	NLP Receive Link Pulse Width Required for Detection	50			ns	
t64	NLP Receive Link Pulse Minimum Period Required for Detection	6		7	ms	link_test_min
t65	NLP Receive Link Pulse Maximum Period Required for Detection	50		150	ms	link_test_max
t66	NLP Receive Link Pulses Required to Exit Link Fail State	3	3	3	Link Pulses	lc_max
t67	FLP Transmit Link Pulse Width	100		150	ns	
t68	FLP Transmit Clock Pulse to Data Pulse Period	55.5	62.5	69.5	ms	interval_timer
t69	FLP Transmit Clock Pulse to Clock Pulse Period	111	125	139	ms	
t70	FLP Transmit Link Pulse Burst Period	8		22	ms	transmit_link_burst_timer
t71	FLP Receive Link Pulse Width Required for Detection	50			ns	
t72	FLP Receive Link Pulse Minimum Period Required for Clock Pulse Detection	5		25	ms	flp_test_min_timer

Table 6.10 Link Pulse Timing (Cont.)

Sym	Parameter	Limit			Unit	Condition
		Min	Typ	Max		
t73	FLP Receive Link Pulse Maximum Period Required For Clock Pulse Detection	165		185	ms	flp_test_max_timer
t74	FLP Receive Link Pulse Minimum Period Required For Data Pulse Detection	15		47	ms	data_detect_min_ timer
t75	FLP Receive Link Pulse Maximum Period Required For Data Pulse Detection	78		100	ms	data_detect_max_ timer
t76	FLP Receive Link Pulses Required To Detect Valid FLP Burst	17		17	Link Pulses	
t77	FLP Receive Link Pulse Burst Minimum Period Required For Detection	5		7	ms	nlp_test_min_timer
t78	FLP Receive Link Pulse Burst Maximum Period Required For Detection	50		150	ms	nlp_test_max_ timer
t79	FLP Receive Link Pulses Bursts Required To Detect AutoNegotiation Capability	3	3	3	Link Pulse	
t80	FLP Receive Acknowledge Fail Period	1200		1500	ms	
t81	FLP Transmit Renegotiate Link Fail Period	1200		1500	ms	break_link_timer
t82	NLP Receive Link Pulse Maximum Period Required For Detection After FLP Negotiation Has Completed	750		1000	ms	link_fail_inhibit_ timer

Table 6.10 Link Pulse Timing (Cont.)

Sym	Parameter	Limit			Unit	Condition
		Min	Typ	Max		
t73	FLP Receive Link Pulse Maximum Period Required For Clock Pulse Detection	165		185	ms	flp_test_max_timer
t74	FLP Receive Link Pulse Minimum Period Required For Data Pulse Detection	15		47	ms	data_detect_min_ timer
t75	FLP Receive Link Pulse Maximum Period Required For Data Pulse Detection	78		100	ms	data_detect_max_ timer
t76	FLP Receive Link Pulses Required To Detect Valid FLP Burst	17		17	Link Pulses	
t77	FLP Receive Link Pulse Burst Minimum Period Required For Detection	5		7	ms	nlp_test_min_timer
t78	FLP Receive Link Pulse Burst Maximum Period Required For Detection	50		150	ms	nlp_test_max_ timer
t79	FLP Receive Link Pulses Bursts Required To Detect AutoNegotiation Capability	3	3	3	Link Pulse	
t80	FLP Receive Acknowledge Fail Period	1200		1500	ms	
t81	FLP Transmit Renegotiate Link Fail Period	1200		1500	ms	break_link_timer
t82	NLP Receive Link Pulse Maximum Period Required For Detection After FLP Negotiation Has Completed	750		1000	ms	link_fail_inhibit_ timer

Table 6.10 Link Pulse Timing (Cont.)

Sym	Parameter	Limit			Unit	Condition
		Min	Typ	Max		
t73	FLP Receive Link Pulse Maximum Period Required For Clock Pulse Detection	165		185	ms	flp_test_max_timer
t74	FLP Receive Link Pulse Minimum Period Required For Data Pulse Detection	15		47	ms	data_detect_min_ timer
t75	FLP Receive Link Pulse Maximum Period Required For Data Pulse Detection	78		100	ms	data_detect_max_ timer
t76	FLP Receive Link Pulses Required To Detect Valid FLP Burst	17		17	Link Pulses	
t77	FLP Receive Link Pulse Burst Minimum Period Required For Detection	5		7	ms	nlp_test_min_timer
t78	FLP Receive Link Pulse Burst Maximum Period Required For Detection	50		150	ms	nlp_test_max_ timer
t79	FLP Receive Link Pulses Bursts Required To Detect AutoNegotiation Capability	3	3	3	Link Pulse	
t80	FLP Receive Acknowledge Fail Period	1200		1500	ms	
t81	FLP Transmit Renegotiate Link Fail Period	1200		1500	ms	break_link_timer
t82	NLP Receive Link Pulse Maximum Period Required For Detection After FLP Negotiation Has Completed	750		1000	ms	link_fail_inhibit_ timer

Figure 6.14 NLP Link Pulse Timing

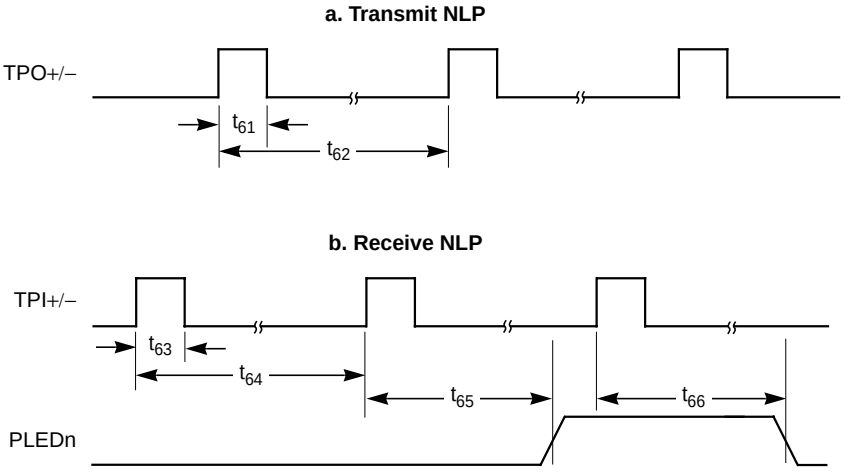
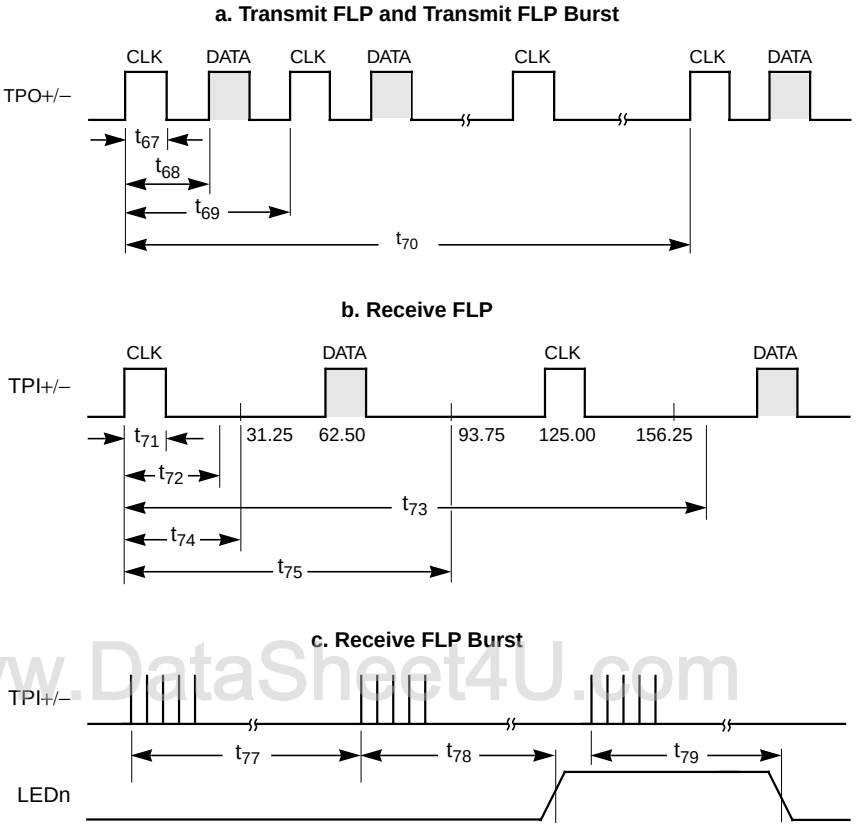


Figure 6.15 FLP Link Pulse Timing



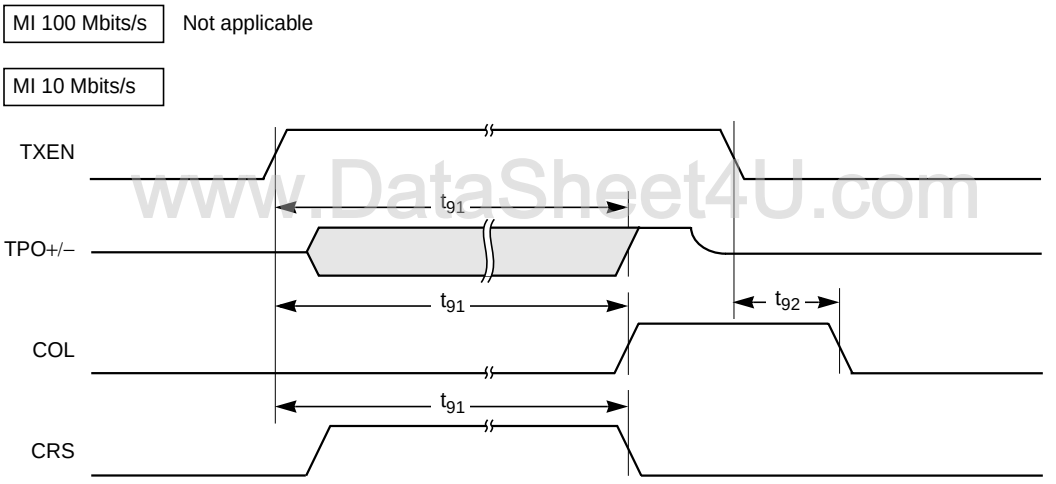
6.3.6 Jabber Timing Characteristics

Table 6.11 shows the Jabber AC timing parameters. See Figure 6.16 for the Jabber timing diagram.

Table 6.11 Jabber Timing

Sym	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t91	Jabber Activation Delay Time	50		100	ms	10 Mbits/s
t92	Jabber Deactivation Delay Time	250		750	ms	10 Mbits/s

Figure 6.16 Jabber Timing



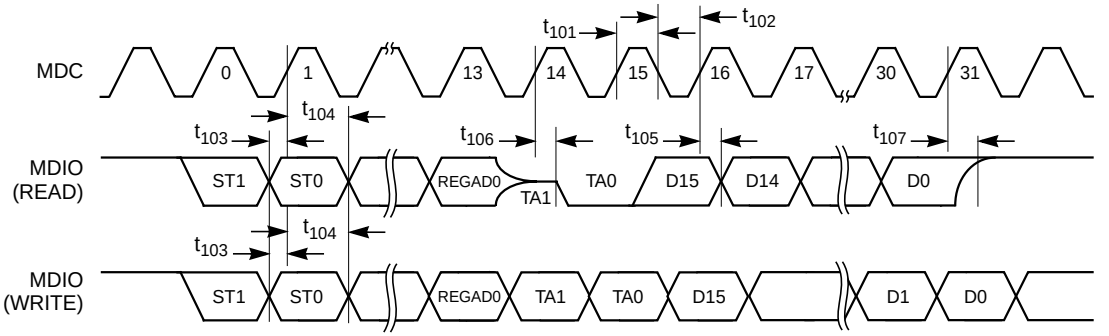
6.3.7 MI Serial Port Timing Characteristics

Table 6.12 shows the MI Serial Port AC timing parameters. See Figure 6.17 for the associated timing diagram.

Table 6.12 MI Serial Port Timing

Sym	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t101	MDC High Time	20			ns	
t102	MDC Low Time	20			ns	
t103	MDIO Setup Time	10			ns	Write Bits
t104	MDIO Hold Time	10			ns	Write Bits
t105	MDC To MDIO Delay			20	ns	Read Bits
t106	MDIO Hi-Z To Active Delay			20	ns	Write-Read Bit Transition
t107	MDIO Active To HI-Z Delay			20	ns	Read-Write Bit Transition
t108	Frame Delimiter (Idle)	32			Clocks	Number of consecutive MDC clocks with MDIO = 1

Figure 6.17 MI Serial Port Timing



6.4 Pinouts and Package Drawings

This section contains the alphabetical and numerical pin listings for the L80227 as well as its pinouts and package drawing.

6.4.1 L80227 Pinouts

Table 6.13 and Table 6.14 contain the list of L80227 signals. The first table lists the signals by category and the second lists them by pin number.

Table 6.13 L80227 Pin List (by Signal Category)

Pin Name	Pin Number	Description
Media Interface		
REXT	50	Transmit Current Set
TPI -	59	Twisted Pair Receive Input, Negative
TPI+	58	Twisted Pair Receive Input, Positive
TPO -	55	Twisted Pair Transmit Output, Negative
TPO+	54	Twisted Pair Transmit Output, Positive
Controller Interface		
CRS	13	Carrier Sense Output
OSCIN	42	Clock Oscillator Input
RX_CLK	26	Receive Clock Output
RX_DV	14	Receive Data Valid Output
RX_EN	27	Receive Enable Input
RX_ER	18	Receive Error Output
RXD0	22	Receive Data Output
RXD1	21	Receive Data Output
RXD2	20	Receive Data Output
RXD3	19	Receive Data Output
TX_CLK	34	Transmit Clock Output
TX_EN	40	Transmit Enable Input
TX_ER	39	Transmit Error Input

Table 6.13 L80227 Pin List (by Signal Category) (Cont.)

Pin Name	Pin Number	Description
TXD0	35	Transmit Data Input
TXD1	36	Transmit Data Input
TXD2	37	Transmit Data Input
TXD3	38	Transmit Data Input
Management Interface (MI)		
MDC	10	Management Interface (MI) Clock Input
MDA4n	9	Management Interface Address Input
MDIO	11	Management Interface (MI) Data Input/Output
PLED0n/MDA0n	61	Programmable LED Output/Management Interface Address Input
PLED1n/MDA1n	62	Programmable LED Output/Management Interface Address Input
PLED2n/MDA2n	3	Programmable LED Output/Management Interface Address Input
PLED3n/MDA3n	4	Programmable LED Output/Management Interface Address Input
LEDs		
PLED4n	2	Transmit LED Output
PLED5n	63	Receive LED Output
Miscellaneous		
ANEG	30	AutoNegotiation Control Input
COL	12	Collision Output
DPLX	29	Full/Half-Duplex Select Input
SPEED	28	Speed Select Input
NC	1	No Connect
NC	5	No Connect
NC	15	No Connect
NC	16	No Connect
NC	17	No Connect
NC	24	No Connect
NC	33	No Connect
NC	43	No Connect

Table 6.13 L80227 Pin List (by Signal Category) (Cont.)

Pin Name	Pin Number	Description
NC	45	No Connect
NC	46	No Connect
NC	47	No Connect
NC	48	No Connect
NC	49	No Connect
NC	51	No Connect
NC	64	No Connect
RESETn	44	Reset Input
Power		
$V_{DD}1$	56	Positive Supply. 3.3 V ±5% Volts
$V_{DD}2$	57	Positive Supply. 3.3 V ±5% Volts
$V_{DD}3$	7	Positive Supply. 3.3 V ±5% Volts
$V_{DD}4$	8	Positive Supply. 3.3 V ±5% Volts
$V_{DD}5$	25	Positive Supply. 3.3 V ±5% Volts
$V_{DD}6$	32	Positive Supply. 3.3 V ±5% Volts
Ground		
GND1	52	Ground
GND2	60	Ground
GND3	6	Ground
GND4	41	Ground
GND5	23	Ground
GND6	31	Ground
GND7	53	Ground

Table 6.14 L80227 Pin List (by Pin Number)

Pin Number	Pin Name	Description
1	NC	No Connect
2	PLED4n	Transmit LED Output
3	PLED2n/MDA2n	Programmable LED Output/Management Interface Address Input
4	PLED3n/MDA3n	Programmable LED Output/Management Interface Address Input
5	NC	No Connect
6	GND3	Ground
7	$V_{DD}3$	Positive Supply. 3.3 V ± 5% Volts
8	$V_{DD}4$	Positive Supply. 3.3 V ± 5% Volts
9	MDA4n	Management Interface Address Input
10	MDC	Management Interface (MI) Clock Input
11	MDIO	Management Interface (MI) Data Input/Output
12	COL	Collision Output
13	CRS	Carrier Sense Output
14	RX_DV	Receive Data Valid Output
15	NC	No Connect
16	NC	No Connect
17	NC	No Connect
18	RX_ER	Receive Error Output
19	RXD3	Receive Data Output
20	RXD2	Receive Data Output
21	RXD1	Receive Data Output
22	RXD0	Receive Data Output
23	GND5	Ground
24	NC	No Connect

Table 6.14 L80227 Pin List (by Pin Number) (Cont.)

Pin Number	Pin Name	Description
25	$V_{DD}5$	Positive Supply. 3.3 V ± 5% Volts
26	RX_CLK	Receive Clock Output
27	RX_EN	Receive Enable Input
28	SPEED	Speed Select Input
29	DPLX	Full/Half-Duplex Select Input
30	ANEG	AutoNegotiation Control Input
31	GND6	Ground 0 Volts
32	$V_{DD}6$	Positive Supply. 3.3 V ± 5% Volts
33	NC	No Connect
34	TX_CLK	Transmit Clock Output
35	TXD0	Transmit Data Input
36	TXD1	Transmit Data Input
37	TXD2	Transmit Data Input
38	TXD3	Transmit Data Input
39	TX_ER	Transmit Error Input
40	TX_EN	Transmit Enable Input
41	GND4	Ground
42	OSCIN	Clock Oscillator Input
43	NC	No Connect
44	RESETn	Reset Input
45	NC	No Connect
46	NC	No Connect
47	NC	No Connect
48	NC	No Connect
49	NC	No Connect

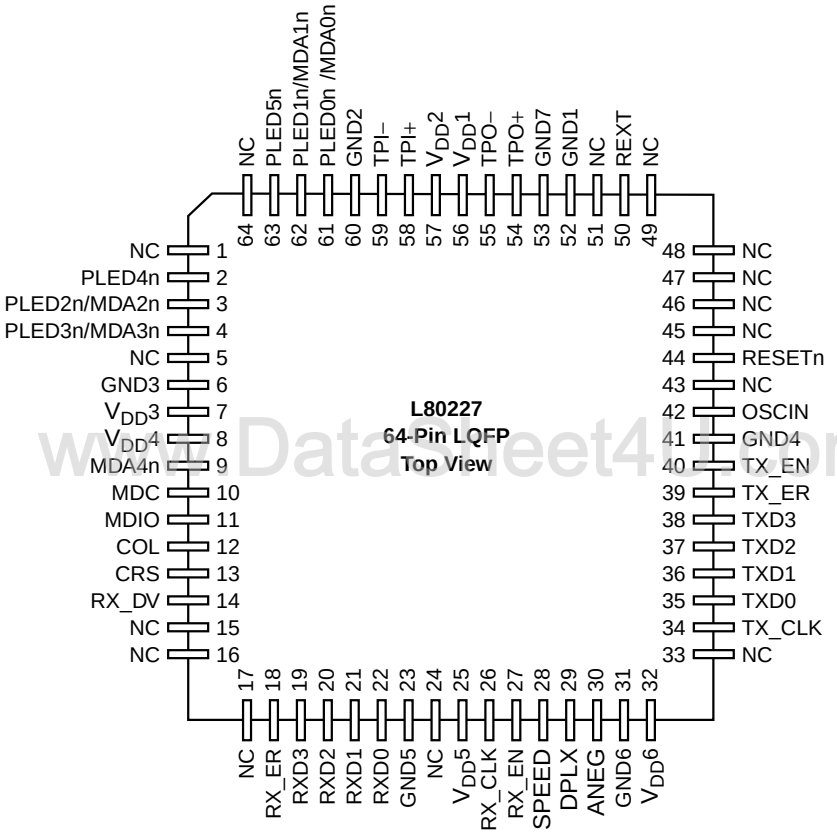
Table 6.14 L80227 Pin List (by Pin Number) (Cont.)

Pin Number	Pin Name	Description
50	REXT	Transmit Current Set
51	NC	No Connect
52	GND1	Ground
53	GND7	Ground
54	TPO+	Twisted Pair Transmit Output, Positive
55	TPO -	Twisted Pair Transmit Output, Negative
56	$V_{DD}1$	Positive Supply. 3.3 V ± 5% Volts
57	$V_{DD}2$	Positive Supply. 3.3 V ± 5% Volts
58	TPI+	Twisted Pair Receive Input, Positive
59	TPI -	Twisted Pair Receive Input, Negative
60	GND2	Ground
61	PLED0n/MDA0n	Programmable LED Output/Management Interface Address Input
62	PLED1n/MDA1n	Programmable LED Output/Management Interface Address Input
63	PLED5n	Receive LED Output
64	NC	No Connect

6.4.2 L80227 Pin Layout

Figure 6.18 shows the pin layout for the L80227 package.

Figure 6.18 L80227 64-Pin LQFP, Top View

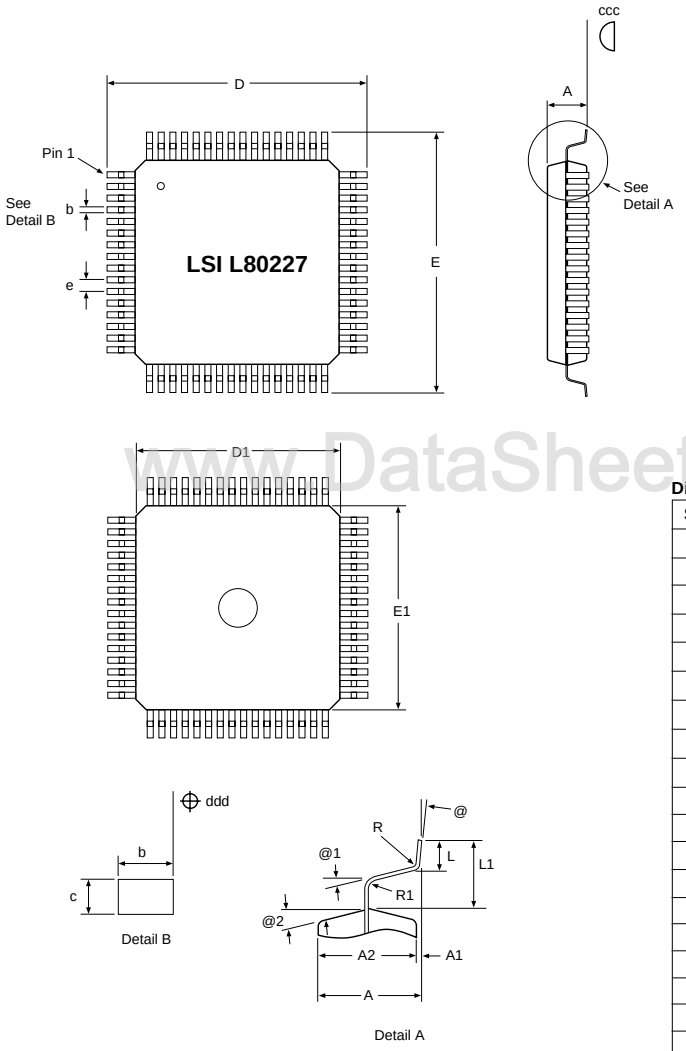


1. *NC* pins are not connected.

6.5 Mechanical Drawing

This section contains the mechanical drawing for the L80227 64-pin LQFP package.

Figure 6.19 64-Pin LQFP Package Drawing



Dimension Table

Symbol	Dimensions
b	0.17 - 0.27
e	0.50 Basic
ccc	Max. 0.08
ddd	Max. 0.08
D	11.85 - 12.15
E	11.85 - 12.15
L	0.45 - 0.75
L1	1.0 Ref
R	0.08 - 0.20
R1	Min. 0.08
A	Max. 1.60
A1	0.05 - 0.15
A2	1.292 - 1.508
c	0.09 - 0.20
D1	9.90 - 10.10
E1	9.90 - 10.10
@	0° - 7°
@1	Min. 0°
@2	12°

Notes
1. **All dimensions are in millimeters.**
2. **Dimensions do not include mold flash. Maximum allowable flash is 0.25.**
3. **All leads are coplanar to a tolerance of 0.08 (ccc). Bent leads to a tolerance of 0.08 (ddd).**

Appendix A
Application Information

This appendix contains application information for the device. It contains the following sections:

A.1 Example Schematics

A typical example schematic of the L80227 used in an network interface adapter card application is shown in Figure A.1; a typical switching port application is shown in Figure A.2; and an external PHY application is shown in Figure A.3.

Figure A.1 Typical Network Interface Adapter Card Schematic Using the L80227

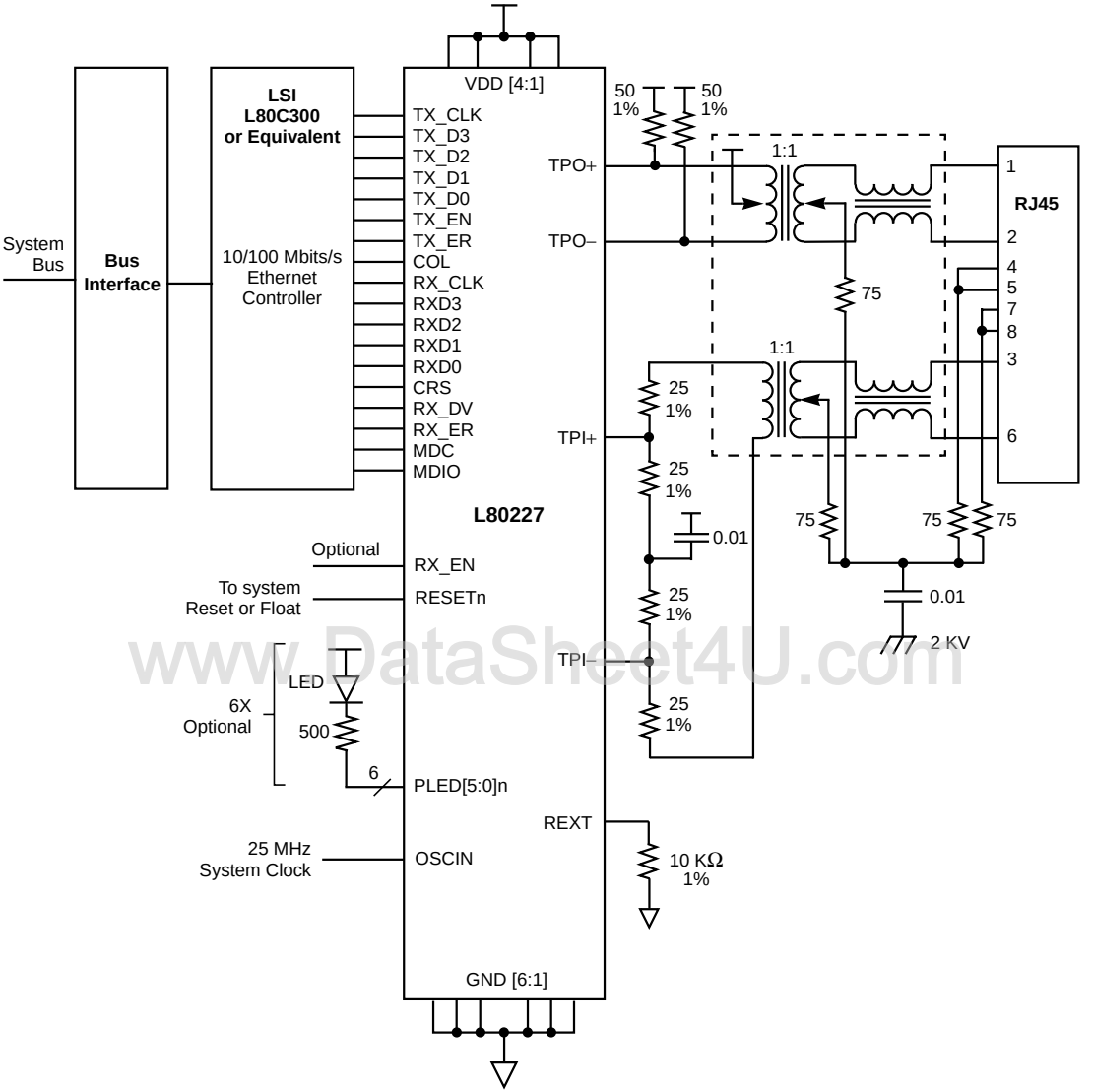


Figure A.2 Typical Switching Port Schematic Using L80227

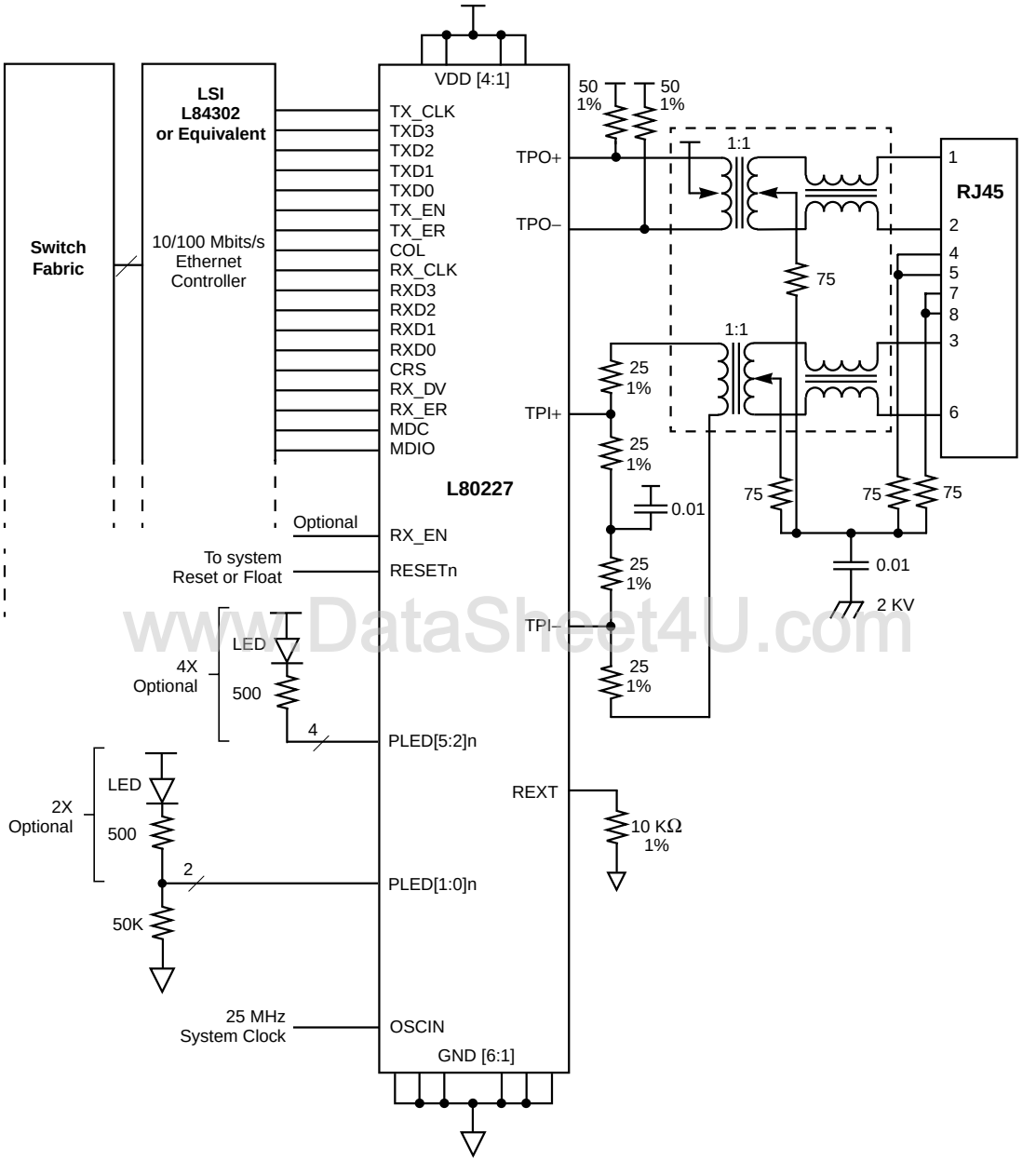
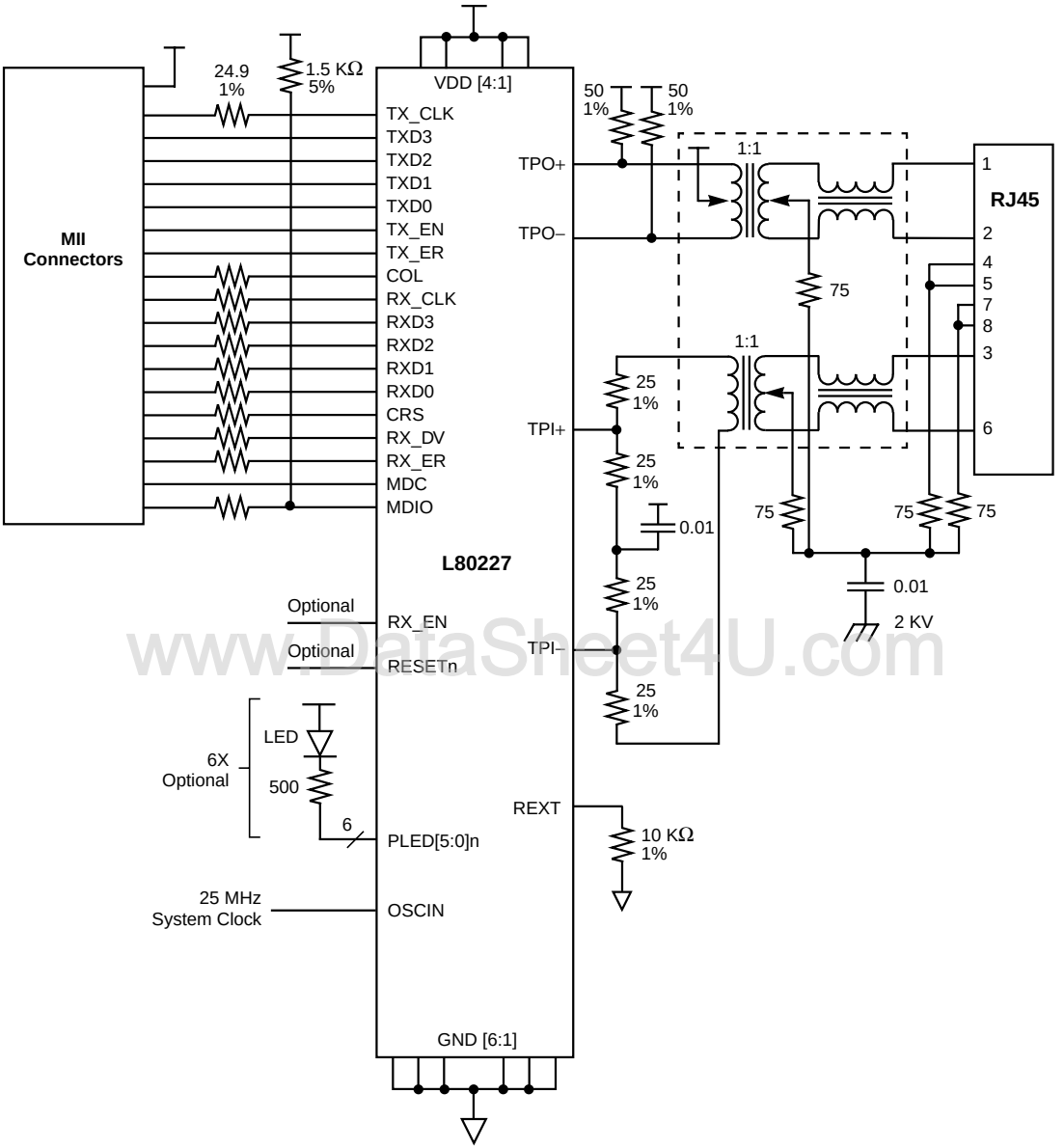


Figure A.3 Typical External PHY Schematic Using L80227



A.2 TP Transmit Interface

The interface between the TP outputs on TPO± and the twisted pair cable is typically transformer coupled and terminated with the two resistors as shown in Figure A.1 through Figure A.3.

The transformer for the transmitter should have a winding ratio of 1:1 with a center tap on the primary winding tied to V_{DD}, as shown in Figure A.1 through Figure A.3. The specifications for the transformer are shown in Table A.1. Sources for the transformer are listed in Table A.2.

Table A.1 TP Transformer Specification

Parameter	Specification	
	Transmit	Receive
Turns Ratio	1:1 CT	1:1
Inductance, (HMin)	350	350
Leakage Inductance, (H)	0.05–0.15	0.0–0.2
Capacitance (pF Max)	15	15
DC Resistance (Ω Max)	0.4	0.4

Table A.2 TP Transformer Sources[1]

Vendor	Part Number
PULSE	H1089, H1102
BEL	S558-5999-J9, 558-5999-46
HALO	TG22-3506ND TG110-S050N2
PCA	EPF8017GH
MIDCOM	$mod2_{TM}$ technology 0510[2]

1. H1089, S558-5999-46, EPF8017GH and TG22-3506ND are pin compatible. Please contact the transformer vendor for additional information.
2. RJ-45 connector with integrated magnetics and LEDs

The transmit output must be terminated with two external termination resistors to meet the output impedance and return loss requirements of

IEEE 802.3. These two external resistors must be connected between V_{DD} and each of the TPO± outputs. Their value should be chosen to provide the correct termination impedance when looking back through the transformer from the twisted-pair cable, as shown in Figure A.1 through Figure A.3. The value of these two external termination resistors depends on the type of cable the device drives.

To minimize common-mode output noise and to aid in meeting radiated emissions requirements, it may be necessary to add a common-mode choke on the transmit outputs as well as add common-mode bundle termination. The qualified transformers mentioned in Table A.2 all contain common-mode chokes along with the transformers on both the transmit and receive sides, as shown in Figure A.1 through Figure A.3. common-mode bundle termination may be needed and can be achieved when the unused pairs in the RJ45 connector are connected to chassis ground through 75 ohm resistors and a 0.01 µF capacitor, as shown in Figure A.1 through Figure A.3.

To minimize noise pickup into the transmit path in a system or on a PCB, the loading on TPO± should be minimized, and both outputs should always be loaded equally.

A.3 TP Receive Interface

Receive data is typically transformer coupled into the receive inputs on TPI± and terminated with external resistors as shown in Figure A.1 through Figure A.3.

The transformer for the receiver should have a winding ratio of 1:1, as shown in Figure A.1 through Figure A.3. The specifications for this transformer are shown in Table A.1 and sources for the transformer are listed in Table A.2.

The receive input must be terminated with the correct termination impedance to meet the input impedance and return loss requirements of IEEE 802.3. In addition, the receive TP inputs must be attenuated. Both the termination and attenuation is accomplished with four external resistors in series across the TPI± inputs, as shown in Figure A.1 through Figure A.3. Each resistor should be 25% of the total series resistance, and the total series resistance should be equal to the characteristic impedance of the cable (100 ohm for UTP). It is also recommended that

a 0.01 Fcapacitor be placed between the center of the series resistor string and V_{DD} to provide an AC ground for attenuating common-mode signal at the input. This capacitor is also shown in Figure A.1 through Figure A.3.

To minimize common-mode input noise and to aid in meeting susceptibility requirements, it may be necessary to add a common-mode choke on the receive input as well as add common-mode bundle termination. The qualified transformers mentioned in Table A.2 all contain common-mode chokes along with the transformers on both the transmit and receive sides, as shown in Figure A.1 through Figure A.3. common-mode bundle termination may be needed and can be achieved when the receive secondary center tap and the unused pairs in the RJ45 connector are connected to chassis ground through 75-ohm resistors and a 0.01 Fcapacitor, as shown in Figure A.1 through Figure A.3.

To minimize noise pickup into the receive path in a system or on a PCB, loading on TPI+/– should be minimized and both inputs should be loaded equally.

A.4 TP Transmit Output Current Set

The TPO± output current level is set with an external resistor connected between the REXT pin and GND. This output current is determined from the following equation, where R is the value of REXT:

$$I_{out} = (10K/R) \quad I_{ref}$$

Where

Ir_{ef} = 40 mA (100 Mbits/s, UTP)

= 32.6 mA (100 Mbits/s, STP)

= 100 mA (10 Mbits/s, UTP)

= 81.6 mA (10 Mbits/s, STP)

REXT should typically be a 10 kΩ 1% resistor to meet IEEE 802.3 specified levels. Once REXT is set for the 100 Mbits/s and UTP modes as shown by the equation above, I_{ref} is then automatically changed inside

the device when the 10 Mbits/s mode or UTP120/STP150 modes are selected.

Keep REXT as close to the REXT and GND pins as possible to reduce noise pickup into the transmitter.

Because the TP output is a current source, capacitive and inductive loading can reduce the output voltage from the ideal level. Thus, in actual application, it might be necessary to adjust the value of the output current to compensate for external loading. One way to adjust the TP output level is to change the value of the external resistor connected to REXT.

A.5 Transmitter Droop

The IEEE 802.3 specification has a transmit output droop requirement for 100BASE-TX. Because the L80227 TP output is a current source, it has no perceptible droop by itself. However, the inductance of the transformer added to the device transmitter output as shown in Figure A.1 through Figure A.3 causes droop to appear at the transmit interface to the TP wire. If the transformer connected to the L80227 outputs meets the requirements of Table A.1, the transmit interface to the TP cable then meets the IEEE 802.3 droop requirements.

A.6 MII Controller Interface

The MII controller interface allows the L80227 to connect to any external Ethernet controller without any glue logic, provided the external Ethernet controller has an MII interface that complies with IEEE 802.3, as shown in Figure A.1 through Figure A.3.

A.6.1 Clocks

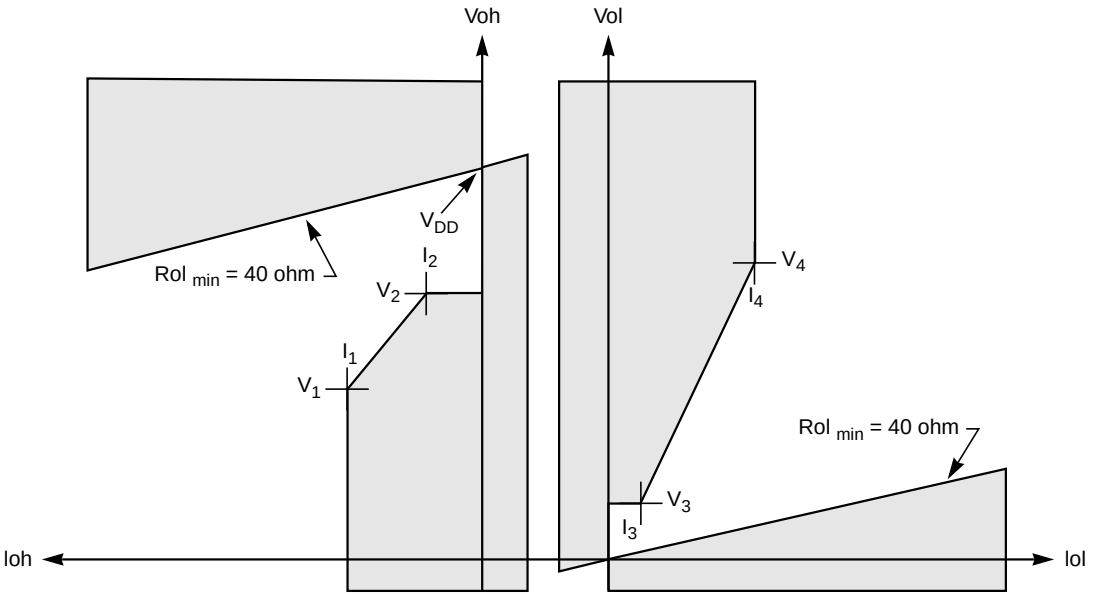
Standard Ethernet controllers with an MII use TX_CLK to clock data in on TXD[3:0]. TX_CLK is specified in IEEE 802.3 and on the L80227 to be an output. If a nonstandard controller or other digital device is used to interface to the L80227, there might be a need to clock TXD[3:0] into the L80227 on the edges of an external master clock. The master clock, in this case, would be an input to the L80227. To do this, use OSCIN as

the master clock input. Because OSCIN generates TX_CLK inside the L80227, data on TXD[3:0] can be clocked into the L80227 on edges of output clock TX_CLK or input clock OSCIN. In the case where OSCIN is used as the input clock, a crystal is no longer needed on OSCIN, and TX_CLK can be left open or used for some other purpose.

A.6.2 Output Drive

The digital outputs on the L80227 controller signals meet the MII driver characteristics specified in IEEE 802.3 and shown in Figure A.4 if external 24.9 Ω 1% termination resistors are added. These termination resistors are only needed if the outputs must drive an MII cable or other transmission line type load, such as in the external PHY application shown in Figure A.3. If the L80227 is used in embedded applications, such as adapter cards and switching hubs (see Figure A.1 and Figure A.2), these terminations resistors are not needed.

Figure A.4 MII Output Driver Characteristics



I – V	I (mA)	V (Volts)
$I_1, -V_1$	–20	1.10
$I_2, -V_2$	–4	2.40
$I_3, -V_3$	4	0.40
$I_4, -V_4$	43	3.05

A.6.3 MII Disable

Setting the MII disable bit (MII_DIS) in the MI serial port Control register places the MII outputs in the high-impedance state and the disables the MII inputs. When this bit is set to the disable state, the TP outputs are also disabled and transmission is inhibited. The default value of this bit when the device powers up or is reset is dependent on the physical device address. If the device address latched into MDA[3:0]n at reset is 0b1111, it is assumed that the device is being used in applications where there maybe more than one device sharing the MII bus, such as in the use of external PHYs or adapter cards. In this case, the device powers up with the MII interface disabled. If the device address latched into MDA[3:0]n at reset is not 0b1111, it is assumed that the device is being used in application where it is the only device on the MII bus, such as in the use of hubs, so the device powers up with the MII interface enabled.

A.6.4 Receive Output Enable

The receive output enable pin, RX_EN, forces the receive and collision MII outputs into the high-impedance state. More specifically, when RX_EN is deasserted, the RX_CLK, RXD[3:0], RX_DV, RX_ER, and COL pins are placed in a high-impedance state.

RX_EN can be used to “wire OR” the outputs of many L80227 devices in multiport applications where only one device may be receiving at a time, such as in a repeater application. Monitoring the CRS pin from each individual port enables the repeater to assert RX_EN only to that L80227 device that is receiving data. The method reduces, by eight per device, the number of pins and PCB traces a repeater core IC requires.

A.7 Repeater Applications

A.7.1 MII Based Repeaters

Using the standard MII as the interface to the repeater core allows the L80227 to be used as the physical interface for MII based repeaters. For most repeaters, it is necessary to disable the internal CRS loopback.

For some particular types of repeaters, it may be desirable to either enable or disable AutoNegotiation, force Half-Duplex operation, and enable either 100 Mbits/s or 10 Mbits/s operation. Setting the appropriate bits in the MI serial port Control register can configure these modes.

The MII requires 16 signals between the L80227 and a repeater core. The MII signal count to a repeater core is 16 multiplied by the number of ports, which can be quite large. The signal count between the L80227 and a repeater core can be reduced by eight per device if the receive output pins are shared and the RX_EN is used to enable only that port where CRS is asserted. Refer to the Section A.6.4, “Receive Output Enable,” page A-11 for more details about RX_EN.

A.7.2 Clocks

Normally, transmit data over the MII is clocked into the L80227 with edges from the TX_CLK output clock. It may be desirable or necessary in some repeater applications to clock in the transmit data from a master

clock from the repeater core. This requires that transmit data be clocked in on edges of an input clock. The OSCIN input clock is available for clocking in data on TXD. Notice from the timing diagrams that OSCIN generates TX_CLK, and TXD data is clocked in on TX_CLK edges. This means that TXD data is also clocked in on OSCIN edges. Thus, an external clock driving the OSCIN input can also be used as the clock for TXD.

A.8 Serial Port

The L80227 uses an MI serial port to access the device registers. Any external device that has a IEEE 802.3 compliant MI interface can connect directly to the L80227 without any glue logic, as shown in Figure A.1 through Figure A.3.

As described earlier, the MI serial port consists of six signals: MDC, MDIO, and MDA[3:0]n. However, only two signals, MDC and MDIO, are needed to shift data in and out. MDA[3:0]n are not needed, but are provided for convenience only.

Note that the MDA[3:0]n addresses are inverted inside the L80227 before going to the MI serial port block. This means that the MDAn[3:0] pins would have to be pin strapped to 0b1111 externally to successfully match the MI physical address of 0b00000 on the PHYAD[4:0] bits internally. The MSB of the address is internally tied to zero.

A.8.1 Serial Port Addressing

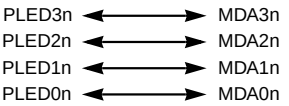
Tying the MDA[3:0]n pins to the desired value selects the device address for the MI serial port. MDA[3:0]n share the same pins as the LED outputs, respectively, as shown in Figure A.5a. At powerup or reset, the output drivers are 3-stated for an interval called the power-on reset time. During the power-on reset interval, the value on these pins is latched into the device, inverted, and used as the MI serial port address. The PLED[5:2]n outputs are open-drain with a pullup resistor and can drive LEDs tied to V_{DD}. The PLED[1:0]n outputs have both pullup and pulldown driver transistors with a pullup resistor, so the PLED[1:0]n outputs can drive LEDs tied to either V_{DD} or GND.

If an LED is to be connected on an LED output, an LED and resistor are tied to V_{DD} as shown in Figure A.4b. To set an address bit HIGH, the LED to V_{DD} connection automatically makes the latched address value a HIGH.To set an address bit LOW, a 50 KΩ resistor to GND must be added as shown in Figure A.4b.

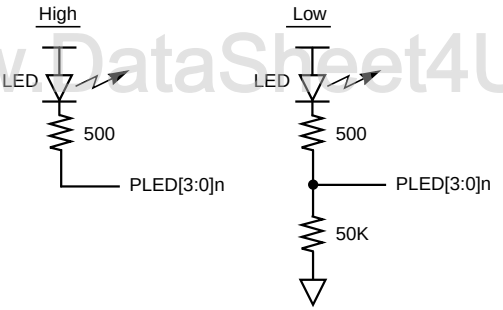
If no LEDs are needed on the LED outputs, the selection of addresses can be done as shown in Figure A.4c. To set an address bit HIGH, the pin should be tied to V_{DD}. The pin is HIGH during power-on reset time and latches in a HIGH address value. If a LOW address is desired, the LED output pins should be tied through a 50 KΩ resistor to GND.

Figure A.5 Serial Device Port Address Selection

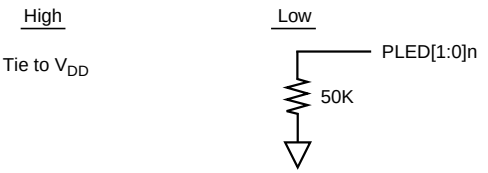
a. Output Driver/Input Address Correspondence



b. Setting Address with LEDs



c. Setting Address without LEDs

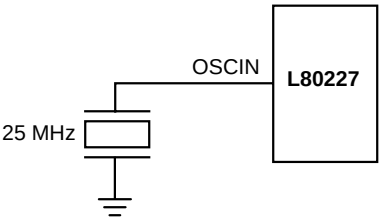


A.9 Oscillator

The L80227 requires a 25 MHz reference frequency for internal signal generation. This 25 MHz reference frequency can be generated from an external 25 MHz crystal connected between OSCIN and GND or from applying an external 25 MHz clock to OSCIN.

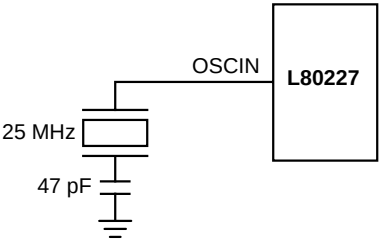
If a crystal oscillator is used, it must be a high-capacitance crystal, such as the Abracon ABLS or ABLS2, and it can be added between the OSCIN pin and GND, as shown in Figure A.6.

Figure A.6 Connecting the L80227 to a High-Capacitance Crystal



If a non high-capacitance crystal is used, a 47-pF capacitor must be added between the crystal and GND, as shown in Figure A.7.

Figure A.7 Connecting the L80227 to a Non High-Capacitance Crystal



The reason for using a 47 pF capacitor is that the resonant frequency depends on the load capacitance the crystal sees. Because the chip load capacitance is fairly high (around 30 pF), a capacitor in series with the crystal shifts the frequency back to the desired value, Adding a serial capacitor is a robust and practical approach to solving any frequency offset problem without degrading oscillator performance.

If a non high-capacitance crystal is used, it must have the characteristics shown in Table A.3, and a series capacitor must be added as shown in Figure A.7. The crystal must be placed as close as possible to the OSCIN and GND pins so that parasitics on OSCIN are kept to a minimum.

Table A.3 Non High-Capacitance Crystal Specifications

Parameter	Spec
Type	Parallel Resonant
Frequency	25 MHz ± 0.01%
Equivalent Series Resistance	40 Ω max
Load Capacitance	18 pF typical
Case Capacitance	7 pF maximum
Power Dissipation	1 mW maximum

A.10 LED Drivers

The PLED[5:0]n outputs can all drive LEDs tied to V_{DD} as shown in Figure A.1 through Figure A.3. The PLED[1:0]n outputs can drive LEDs tied to either V_{DD} or GND.

The PLED[5:0]n outputs can also drive other digital inputs, so they can also be used as digital outputs whose function can be user-defined and controlled through the MI serial port.

A.11 Power Supply Decoupling

There are nine V_{DD} pins on the L80227 and seven GND pins.

All the V_{DD} pins should be connected together as closely as possible to the device with a large V_{DD} plane. If the V_{DD} pins vary in potential by even a small amount, noise and latchup can result. The V_{DD} pins should be kept to within 50 mV of each other.

All the GND pins should also be connected together as closely as possible to the device with a large ground plane. If the GND pins vary in potential by even a small amount, noise and latchup can result. The GND pins should be kept to within 50 mV of each other.

A 0.01–0.1µF decoupling capacitor should be connected between each V_{DD}/GND set as closely as possible to the device pins, preferably within 0.5 inches. The value should be chosen based on whether the noise from V_{DD}-GND is high- or low-frequency. A conservative approach would be to use two decoupling capacitors on each V_{DD}/GND set, one 0.1 µF for low-frequency and one 0.001 Ffor high-frequency noise on the power supply.

The V_{DD} connection to the transmit transformer center tap shown in Figure A.1 through Figure A.3 has to be well decoupled to minimize common-mode noise injection from the supply into the twisted-pair cable. It is recommended that a 0.01 µF decoupling capacitor be placed between the center tap V_{DD} and the GND plane. This decoupling capacitor should be physically placed as close as possible to the transformer center tap, preferably within 0.5 inches

The PCB layout and power supply decoupling discussed above should provide sufficient decoupling to achieve the following when measured at the device:

- The resultant AC noise voltage measured across each V_{DD}/GND set should be less than 100 mV p-p
- All V_{DD} pins should be within 50 mV p-p of each other
- All GND pins should be within 50 mV p-p of each other.

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