LSI/CSI

A3800

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LS7215
LS7216

PROGRAMMABLE DIGITAL DELAY TIMER

July 2009

FEATURES:

- Programmable delay from microseconds to days
- Programmable delay controlled by 8 binary-weighted delay inputs that can be latched from a shared 8-bit bus
- On chip oscillator (RC or Crystal) or external clock time base
- Selectable prescaler for real time delay generation based on 50Hz/60Hz time base or 32,768Hz watch crystal
- Four operating modes
- Reset input for delay abort
- Low quiescent and operating current
- Direct relay drive
- +3V to +18V operation (V_{DD} - V_{SS})
- **LS7215**, **LS7216** (DIP); **LS7215-S**, **LS7216-S** (SOIC) - **See Figure 1** -

DESCRIPTION:

The **LS7215** and **LS7216** are CMOS integrated circuits for generating digitally programmable delays. The delay is controlled by 8 binary weighted inputs, WB0 - WB7, in conjunction with an applied clock or oscillator frequency. The programmed time delay manifests itself in the Delay Output ($\overline{\text{OUT}}$) as a function of the Operating Mode selected by the Mode Select inputs A and B: **One-Shot**, **Delayed Operate**, **Delayed Release** or **Dual Delay**. The time delay is initiated by a transition at the Trigger Input (TRIG).

I/O DESCRIPTION:

MODE SELECT Inputs A & B (Pins 1 & 2)
The 4 operating modes are selected by Inputs A and B according to Table 1

TABLE 1. MODE SELECTION

A	B	MODE
0	0	One-Shot (OS)
0	1	Delayed Operate (DO)
1	0	Delayed Release (DR)
1	1	Dual Delay (DD)

Each input has an internal pull-up resistor of about 500kΩ.

One-Shot Mode (OS)

A positive transition at the TRIG input causes $\overline{\text{OUT}}$ to switch low without delay and starts the delay timer. At the end of the programmed delay timeout, $\overline{\text{OUT}}$ switches high. If a delay timeout is in progress when a positive transition occurs at the TRIG input, the delay timer will be restarted. A negative transition at the TRIG input has no effect.

Delayed Operate Mode (DO)

A positive transition at the TRIG input starts the delay timer. At the end of the delay timeout, $\overline{\text{OUT}}$ switches low. A negative transition at the TRIG input causes $\overline{\text{OUT}}$ to switch high without delay. $\overline{\text{OUT}}$ is high when TRIG is low.

PIN ASSIGNMENT - TOP VIEW

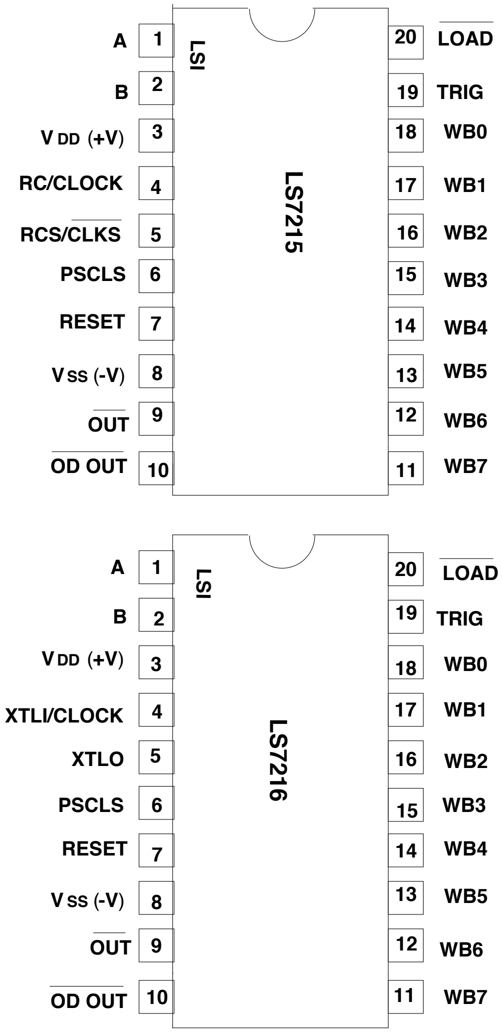


FIGURE 1

Delayed Release Mode (DR)

A negative transition at the TRIG input starts the delay timer. At the end of the delay timeout, $\overline{\text{OUT}}$ switches high. A postive transition at the TRIG input causes $\overline{\text{OUT}}$ to switch low without delay. $\overline{\text{OUT}}$ is low when TRIG is high.

Dual Delay Mode (DD)

A positive or negative transition at the TRIG input starts the delay timer. At the end of the delay timeout, $\overline{\text{OUT}}$ switches to the logic state which is the inverse of the TRIG input. If a delay timeout is in progress when a transition occurs at the TRIG input, the delay timer is restarted.

TRIGGER Input (TRIG, Pin 14)
A transition at the TRIG input causes $\overline{\text{OUT}}$ to switch with or without delay, depending on the selected mode. The TRIG input to $\overline{\text{OUT}}$ transition relation is always opposite in polarity, with the exception of One-Shot mode. (See Mode definitions above.) TRIG input has an internal pull-down resistor of about 500kΩ and is buffered by a Schmitt trigger to provide input hysteresis.

LS7215 TIME BASE Input (RC/CLOCK, Pin 4)
For **LS7215**, the basic timing signal is applied at the RC/CLOCK input. The clock can be provided from either an external source or generated by an internal oscillator by connecting an R-C network to this input. The frequency of oscillation is given by $f \approx 1/RC$. Chip-to-chip oscillation tolerance is ± 5% for a fixed value of RC.

The minimum resistance, R MIN = 4,000Ω, V_{DD} = + 3V
= 1,200Ω, V_{DD} = +10V
= 1,000Ω, V_{DD} = +18V

The external clock mode is selected by applying a logic low to the RCS/$\overline{\text{CLKS}}$ input (Pin 5); the internal oscillator mode is selected by applying a high level to the RCS/$\overline{\text{CLKS}}$ input.

LS7216 TIME BASE Input (XTLI/CLOCK, Pin 4)
For **LS7216**, the basic timing clock is applied to the XLTI/CLOCK input from either an external clock source or generated by an internal crystal oscillator by connecting a crystal between XTLI/CLOCK input and the XTLO output (Pin 5).

LS7215 TIME BASE SELECT Input (RCS/$\overline{\text{CLKS}}$, Pin 5)
For **LS7215**, the external clock operation at Pin 4 is selected by applying a logic low to the RCS/$\overline{\text{CLKS}}$ input. The internal oscillator option with RC timer at Pin 4 is selected by applying a logic high at the RCS/$\overline{\text{CLKS}}$ input. RCS/$\overline{\text{CLKS}}$ input has an internal pull-down resistor of about 500kΩ.

LS7216 TIME BASE Output (XTLO, Pin 5)
For **LS7216**, when a crystal is used for generating the time base oscillation, the crystal is connected between XTLI/CLOCK and XTLO pins.

PRESCALER SELECT Input (PSCLS, Pin 6)
The PSCLS input is a 3-state input, which selects one of three prescale factors according to Table 2.

TABLE 2. PRESCALE FACTOR SELECTION

PSCLS Input	**S (Prescale Factor)**	
Logic Level	**LS7215**	**LS7216**
Float	1	1
V_{SS}	3000	32768
V_{DD}	3600	32768 x 60

Using prescale factors of 3000 and 3600, delays in units of minutes can be produced from 50Hz and 60Hz line sources. Prescale factors of 32,768 and 32,768 x 60 can be used to generate accurate delays in units of seconds and minutes, respectively, from a 32kHz watch crystal.

TIMER RESET Input (RESET, Pin 7)
When RESET input switches high, any timeout in progress is aborted and OUT switches high without delay. With RESET high, OUT remains high. When RESET switches low with TRIG low in any mode, $\overline{\text{OUT}}$ remains high. When RESET switches low with TRIG high in Delayed Operate and Dual Delay modes, the delay timer is started and $\overline{\text{OUT}}$ switches low at the end of the delay timeout. When RESET switches low with TRIG high in Delayed Release mode, $\overline{\text{OUT}}$ switches low without delay. When RESET switches low with TRIG high in One-Shot mode, $\overline{\text{OUT}}$ remains high. RESET input has an internal pull-down resistor of about 500kΩ and is buffered by a Schmitt Trigger to provide input hysteresis.

V_{SS} (-V, Pin 8)
Supply voltage negative terminal or GND.

DELAY Output ($\overline{\text{OUT}}$, Pin 9)
Except in One-Shot mode, $\overline{\text{OUT}}$ switches with or without delay (depending on mode) in inverse relation to the logic level of the TRIG input. In One-Shot mode, a timed low level is produced at $\overline{\text{OUT}}$, in response to a positive transition of the TRIG input.

$\overline{\text{LOAD}}$ Input ($\overline{\text{LOAD}}$, Pin 20)
The $\overline{\text{LOAD}}$ input allows the weighting bits, WB0 - WB7, to be latched from a shared bus, such as a MCU IO port. When the $\overline{\text{LOAD}}$ is low, the internal weighting bits dynamically follow the data presented at the

WB0 - WB7 inputs. When the $\overline{\text{LOAD}}$ is switched high, the WB0 - WB7 data become latched, freeing up the bus to service other peripheral devices. $\overline{\text{LOAD}}$ input has an internal pull-down resistor to V_{SS}.

OPEN DRAIN DELAY Output ($\overline{\text{ODOUT}}$, Pin 10)
The ODOUT is the open drain version of the delay output which enables the chip to directly drive a relay, operating at a voltage higher than the chip supply voltage through a single NPN transistor (see Figure 10) . Functionally, the ODOUT is identical to the other delay output, $\overline{\text{OUT}}$.

WEIGHTING BIT Inputs (WB7 to WB0, Pins 11 - 18)
Inputs WB0 through WB7 are binary weighted delay bits used to program the delay according to the following relations:

One-Shot Mode: Pulse width $= \dfrac{SW}{f}$

All other Modes: Delay $= \dfrac{SW + 0.5}{f}$

Where:
S = Prescale factor (See Table 2)
f = Time base frequency at Pin 4
W = WB0 + WB1 + ... WB7

The weighting factor, W, is calculated by substituting in the equation above for W, the weighted values for all the WB inputs that are at logic high. The weighted values for the WB inputs are shown in Table 3. Each WB input has an internal pull-down resistor of about 500kΩ.

TABLE 3. BIT WEIGHTS

BITS	**VALUE**
WB0	1
WB1	2
WB2	4
WB3	8
WB4	16
WB5	32
WB6	64
WB7	128

V_{DD} (+V, Pin 3)
Supply voltage positive terminal.

ABSOLUTE MAXIMUM RATINGS: (All voltages referenced to V_{SS})

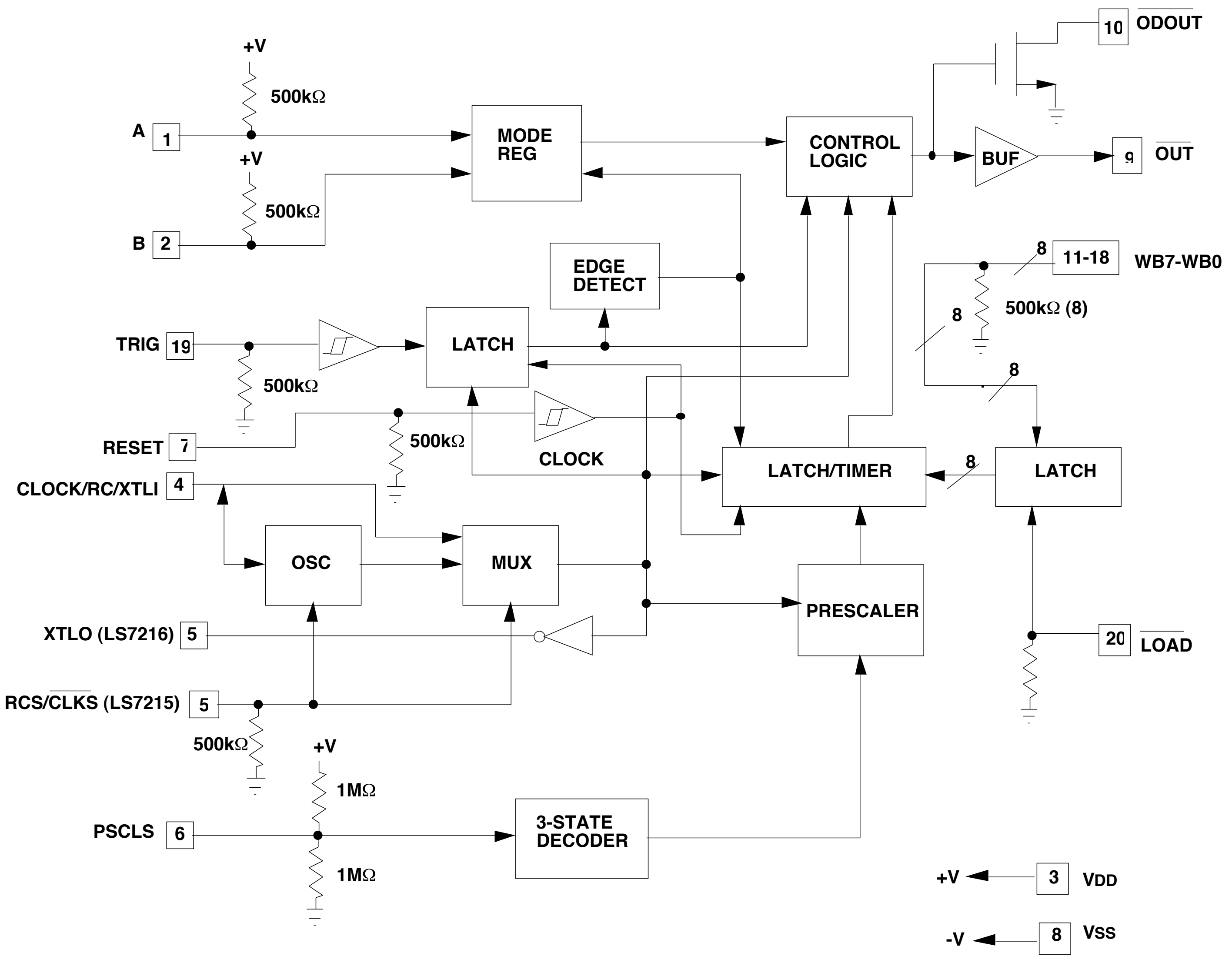
	SYMBOL	**VALUE**	**UNIT**
DC Supply Voltage	V_{DD}	+19	V
Voltage (Any Pin)	V_{IN}	V_{SS} - 0.3 to V_{DD} + 0.3	V
Operating Temperature	T_A	-20 to +85	°C
Storage Temperature	T_{STG}	-65 to +150	°C

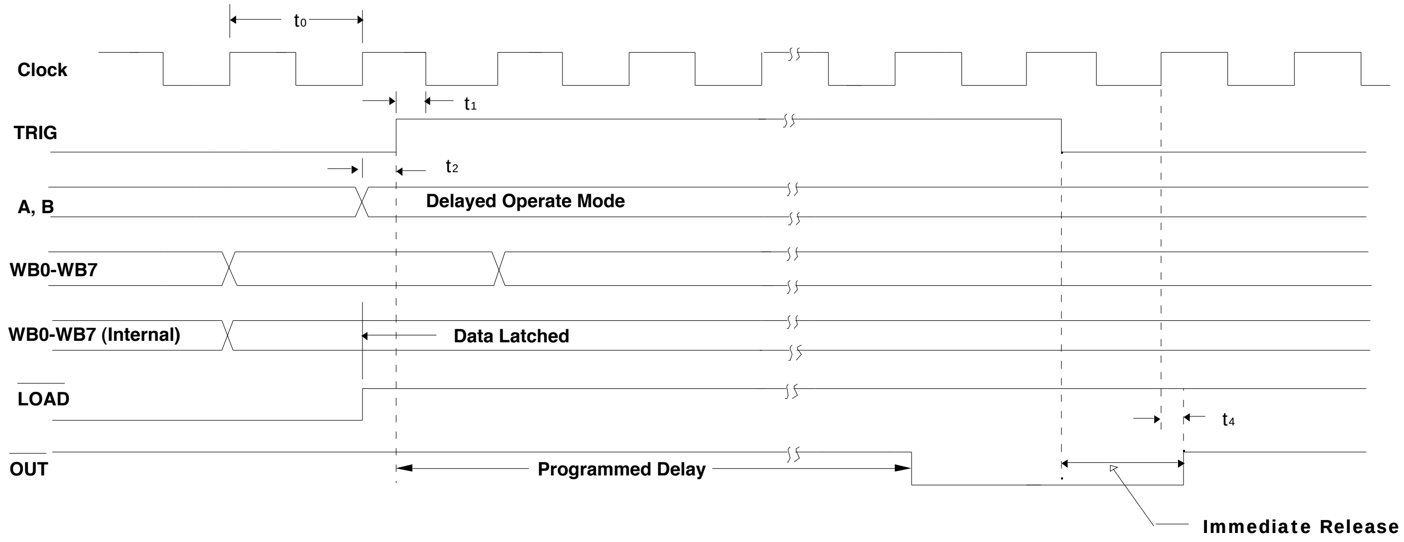
ELECTRICAL CHARACTERISTICS (Voltages referenced to Vss)

Characteristic	**SYMBOL**	**V_{DD}**	**-20°C**		**+25°C**		**+85°C**		**Unit**	**Condition**
			Min	**Max**	**Min**	**Max**	**Min**	**Max**		
Supply Voltage	V_{DD}	-	3.0	18.0	3.0	18.0	3.0	18.0	V	-
Supply Current	I_{DD}	3.0	-	66	-	55	-	44	μA	with the clock off and all inputs floating.
		10.0	-	252	-	210	-	168	μA	
		18.0	-	540	-	450	-	360	μA	
Input Voltages:										
Reset, Trigger Low	V_{TL}	3.0	-	0.8	-	0.75	-	0.7	V	-
		10.0	-	2.3	-	2.2	-	2.1	V	
		18.0	-	3.9	-	3.8	-	3.7	V	
Reset, Trigger High	V_{TH}	3.0	2.2	-	2.1	-	2.0	-	V	-
		10.0	6.1	-	6.0	-	5.9	-	V	
		18.0	9.7	-	10.5	-	11.0	-	V	
Reset, Trigger Hysteresis		3.0	0.7	-	0.7	-	0.7	-	V	-
		10.0	2.2	-	2.2	-	2.2	-	V	
		18.0	3.9	-	3.9	-	3.9	-	V	
All other inputs, Low	V_{IL}	3.0	-	1.1	-	1.1	-	1.1	V	-
		10.0	-	4.5	-	4.5	-	4.5	V	
		18.0	-	10.6	-	10.6	-	10.6	V	
All other inputs, High	V_{IH}	3.0	1.9	-	1.9	-	1.9	-	V	-
		10.0	6.5	-	6.5	-	6.5	-	V	
		18.0	13.3	-	13.3	-	13.3	-	V	
Input Currents:										
PSCLS Low	I_{PL}	3.0	-	3.2	-	2.5	-	1.9	μA	Input at V_{SS}
		10.0	-	31	-	24	-	18	μA	
		18.0	-	84	-	65	-	49	μA	
PSCLS High	I_{PH}	3.0	-	9.8	-	7.5	-	5.8	μA	Input at V_{DD}
		10.0	-	31	-	24	-	18.2	μA	
		18.0	-	85	-	65	-	49	μA	
A, B Low	I_{ML}	3.0	-	6.0	-	5.0	-	4.0	μA	Input at V_{SS}
		10.0	-	59	-	48	-	38	μA	
		18.0	-	157	-	128	-	98	μA	
A, B High	I_{MH}	-	-	100	-	100	-	200	nA	Input at V_{DD}
All other inputs, Low	I_{IL}	-	-	100	-	100	-	200	nA	Input at V_{SS}
All other inputs, High	I_{IH}	3.0	-	33	-	27	-	23	μA	Input at V_{DD}
		10.0	-	128	-	105	-	81	μA	
		18.0	-	131	-	107	-	82	μA	
Output Current:										
$\overline{OUT}$, $\overline{ODOUT}$ Sink	I_{OSNK}	3.0	13.2	-	10.1	-	7	-	mA	V_O = +0.5V
		10.0	26	-	19.7	-	15	-	mA	
		18.0	30.7	-	23.6	-	17	-	mA	
$\overline{OUT}$ Source	I_{OSRC}	3.0	4.1	-	3.2	-	2.1	-	mA	V_O = V_{DD} - 0.5V
		10.0	7.2	-	5.5	-	4.1	-	mA	
		18.0	8.2	-	6.3	-	4.6	-	mA	
$\overline{ODOUT}$ Source		-	0	-	0	-	0	-	mA	In all conditions

ELECTRICAL CHARACTERISTICS (Voltages referenced to Vss) (Con't)

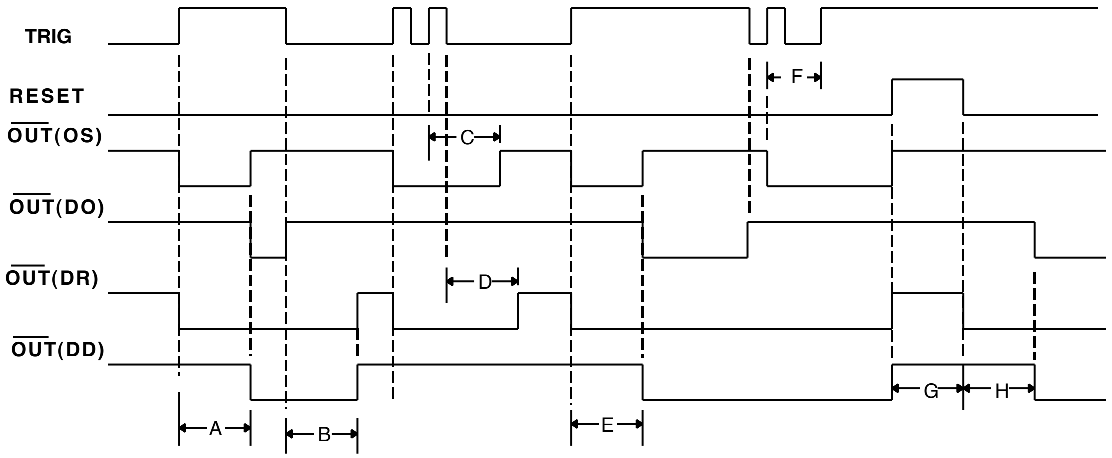
Characteristic	SYMBOL	V_{DD}	Min	Max	Min	Max	Min	Max	Unit	Condition
Switching Characteristics (See Fig. 3)										
RC Oscillator Frequency	f_{osc}	3.0	-	1.8	-	1.4	-	1.05	MHz	-
		10.0	-	4.5	-	3.4	-	2.6	MHz	
		18.0	-	8.0	-	4.0	-	3.0	MHz	
External Clock or Crystal Oscillator Frequency	f_{ext}	3.0	-	2.6	-	2.0	-	1.52	MHz	For prescale factor S = 1 or 3000 or 3600
		10.0	-	5.3	-	4.0	-	3.0	MHz	
		18.0	-	5.9	-	4.6	-	3.5	MHz	
	f_{ext}	3.0	-	7.2	-	5.5	-	4.2	MHz	S = 32768 or 32768 x 60
		10.0	-	16.0	-	12.8	-	9.7	MHz	
		18.0	-	15.9	-	12	-	9.1	MHz	
TRIG Set-Up Time	t_1	-	38	-	50	-	66	-	ns	-
A, B Set-Up Time	t_2	-	0	-	0	-	0	-	ns	-
Clock to $\overline{\text{Out}}$ Delay	t_4	3.0	-	284	-	375	-	495	ns	C_L = 50pF
		10.0	-	98	-	130	-	172	ns	
		18.0	-	87	-	115	-	152	ns	





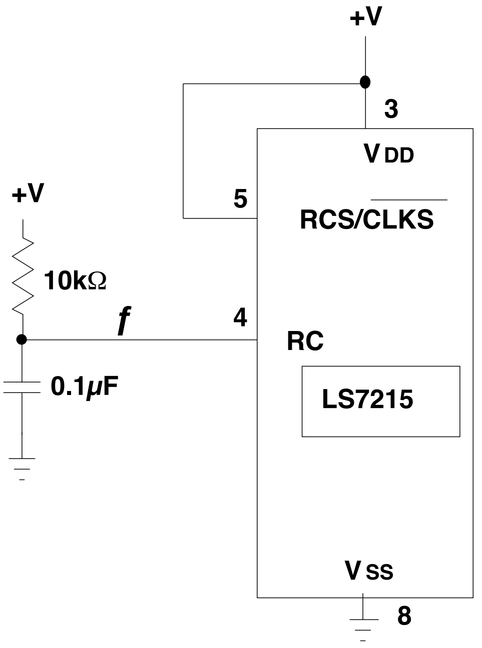
Note 1. TRIG input is clocked in by the negative edge of external clock.
Note 2. Inputs A, B are sampled only at a TRIG input transition and ignored at all other times.
Note 3. $\overline{\text{OUT}}$ is switched by the positive edge of the external clock.

FIGURE 3. INPUT/OUTPUT TIMING



A. Turn-on delay in DO and DD modes; Pulse-width in OS mode.
B. Turn-off delay in DR and DD modes.
C. Pulse-width extended by re-trigger in OS mode.
No effect in DO and DD modes because TRIG switches back low before turn-on delay has timed out.
D. Turn-off delay in DR mode.
E. Turn-on delay in DO and DD modes; pulse-width in OS mode.
F. No effect in DO, DR and DD modes because of TRIG's switching back to opposite levels.
G. Time-outs aborted and $\overline{\text{OUT}}$ forces high by RESET.
H. After the removal of RESET, $\overline{\text{OUT}}$ switches to the inverse polarity of TRIG
immediately (DR) or after the timeout (DO, DD). No effect in OS.

FIGURE 4. MODE ILLUSTRATION WITH TRIG, $\overline{\text{OUT}}$ AND RESET



$$f = \frac{1}{10 \times 10^{3} \times 0.1 \times 10^{-6}} = 1\text{kHz}$$

FIGURE 5. RC- Oscillator Connection

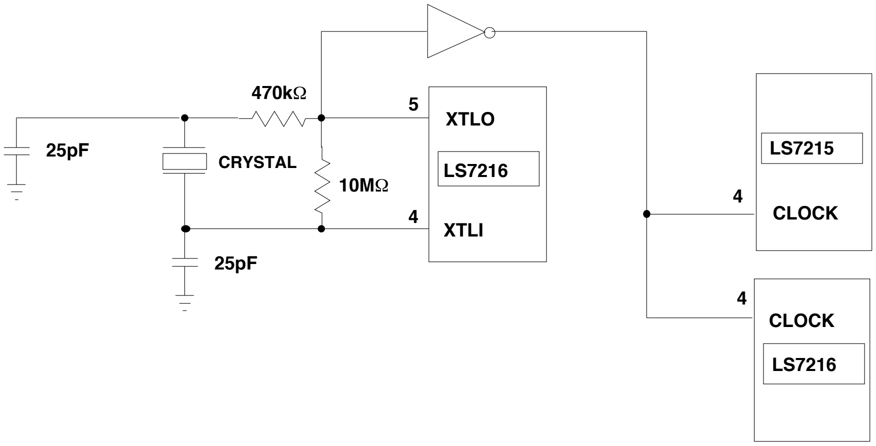


FIGURE 6. MULTI-TIMER WITH SINGLE CRYSTAL TIME-BASE

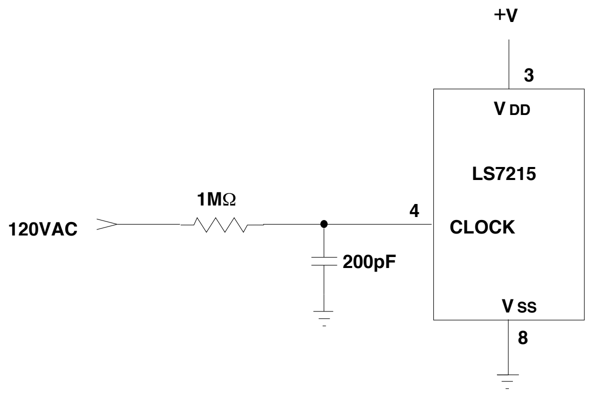
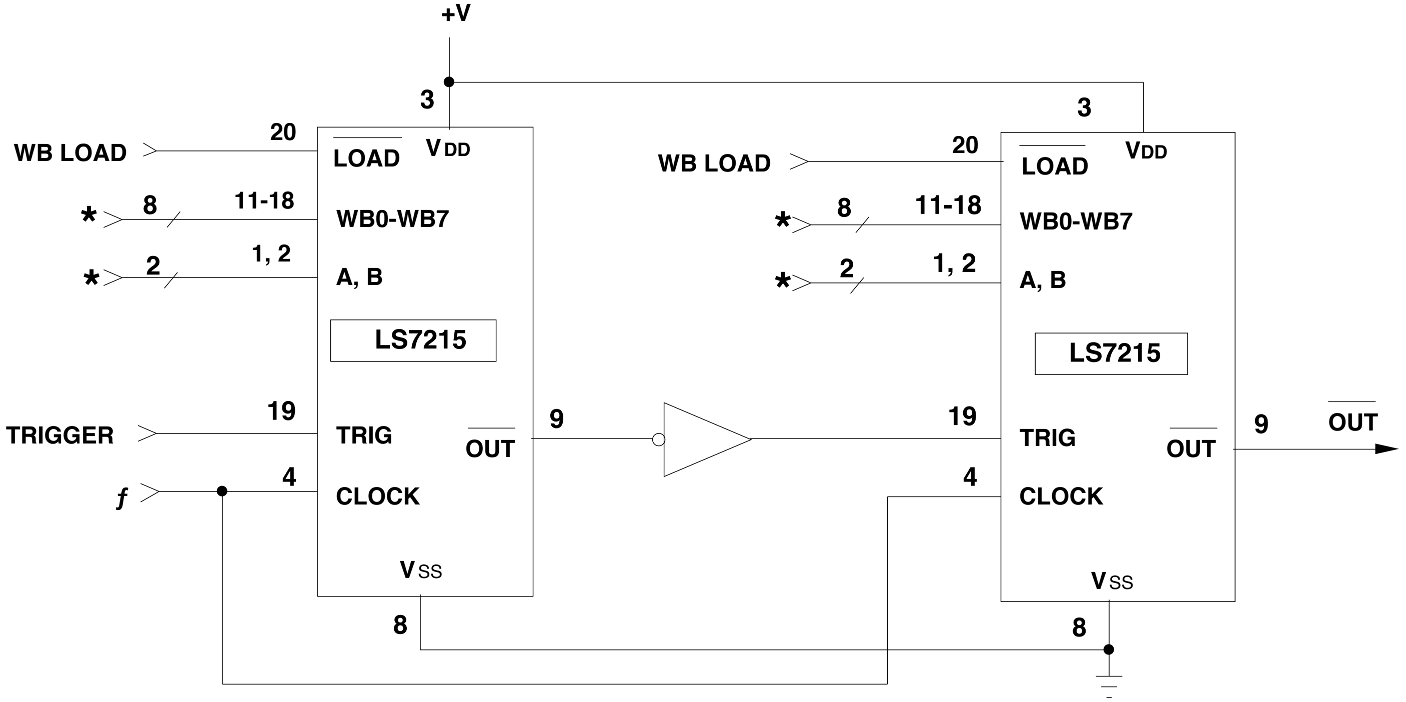
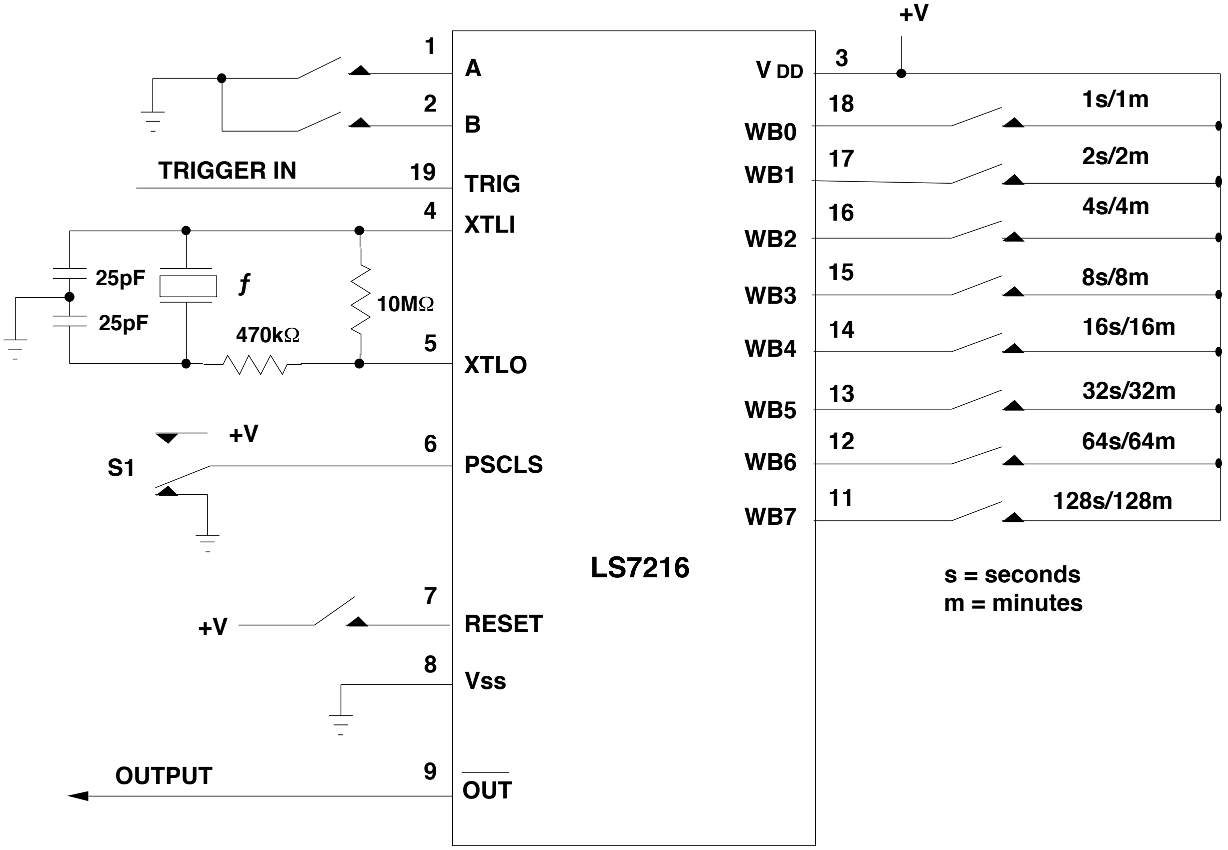


FIGURE 7. DRIVING CLOCK INPUT FROM THE AC LINE



* Connect for desired delay and mode

FIGURE 8. DELAY EXTENSION BY CASCADING



NOTE : Crystal Frequency, ƒ = 32,768Hz
Switch: S1 low: Delay increment = 1s; Maximum Delay = 255s
S1 high: Delay increment = 1m; Maximum Delay = 255m

FIGURE 9. PROGRAMMABLE ACCURATE REAL-TIME DELAY GENERATION

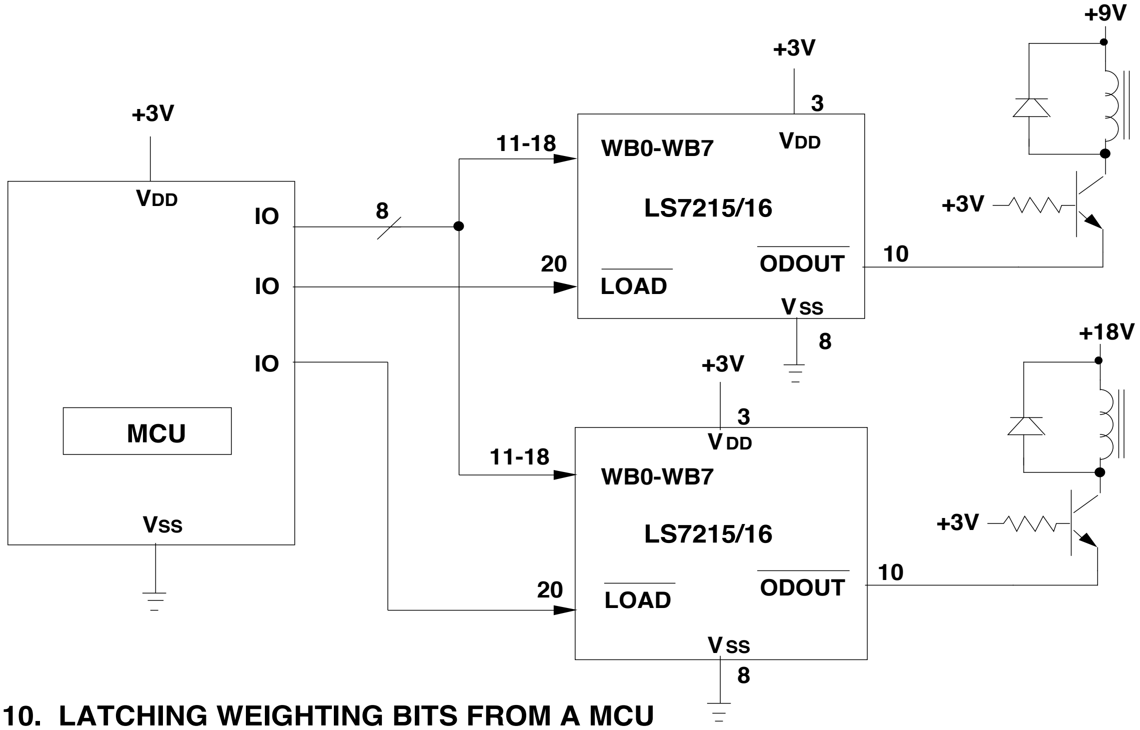
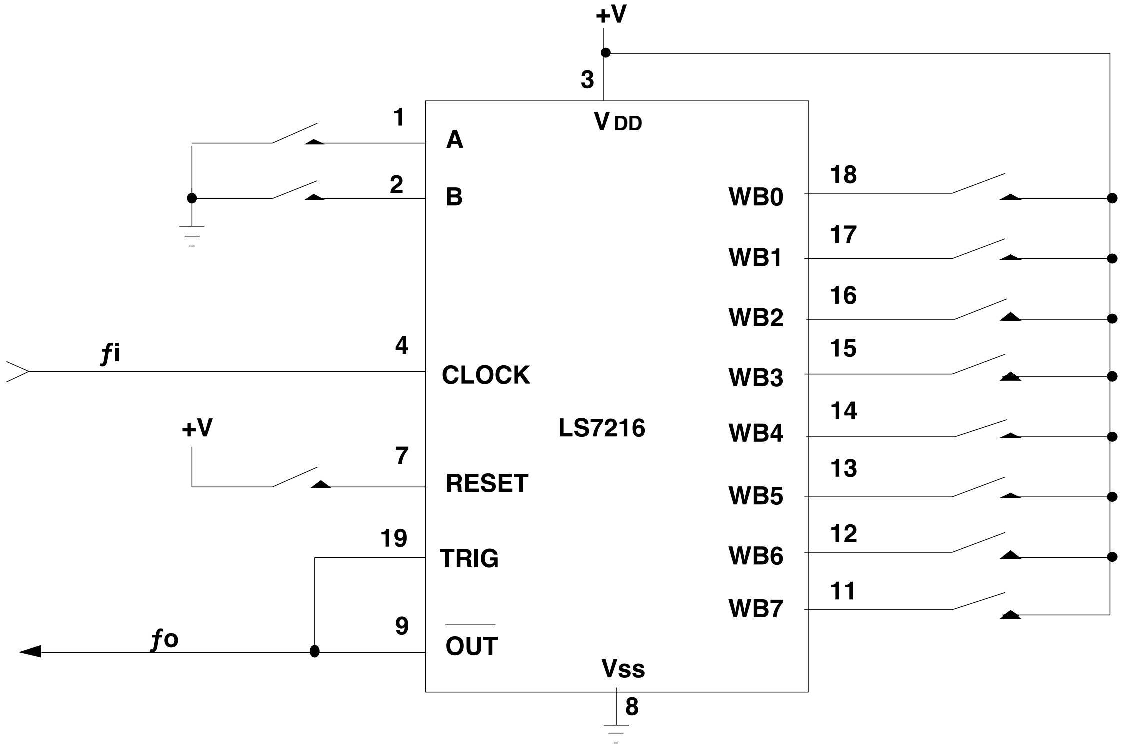


FIGURE 10. LATCHING WEIGHTING BITS FROM A MCU
(Example showing separate relay and logic supplies)



CASE 1. MODE = DO or DR; PRESCALE FACTOR, S = 1

In this setup a frequency division of the input clock, ƒi by a factor of 2 to 257, in increments of 1 can be obtained according to the equation:

$$f_o = \frac{f_i}{W + 2} \quad \text{where W (weighting factor) = 0 to 255}$$

The ƒo pulse width is non-symmetrical (non-50% duty -cycle)

CASE 2. MODE = DD; PRESCALE FACTOR, S = 1

In this setup a frequency division of the input clock, ƒi by a factor of 2 to 512, in increments of 2 can be obtained according to the equation:

$$f_o = \frac{f_i}{2\,(W + 1)} \quad \text{where W (weighting factor) = 0 to 255}$$

The ƒo pulse widths are symmetrical with 50% duty -cycle

EXAMPLES OF CASE 1 and CASE 2 FREQUENCY DIVISIONS WITH W = 2

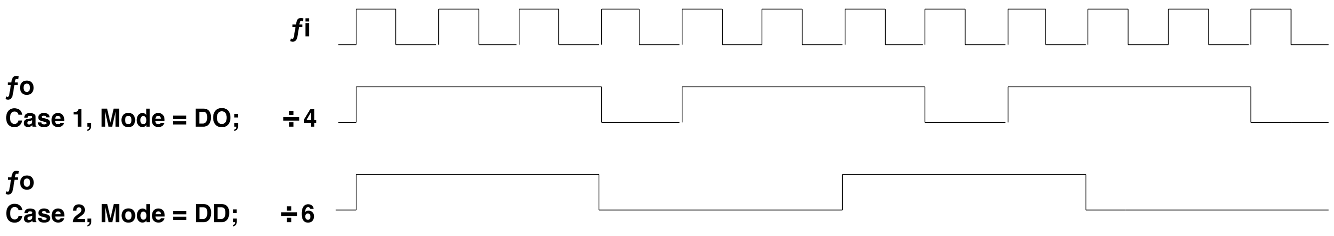


FIGURE 11. PROGRAMMABLE FREQUENCY DIVIDER