Features

- **Fulfills IEC 1036, Class 1 Accuracy Requirements**
- **Fulfills IEC 687, Class 0.5 and Class 0.2 Accuracy, with External Temperature Compensated Voltage Reference**
- **Fulfills IEC 1268, Requirements for Reactive Power**
- **Simultaneous Active, Reactive and Apparent Power and Energy Measurement**
- **Power Factor, Frequency, Voltage and Current Measurement**
- **Single- and Poly-phase Operation**
- **Three Basic Operating Modes: Stand-alone Mode, Microprocessor Mode and Multi-Channel Mode**
- **Flexible Interfacing, 8-bit Microprocessor Interface, 8-bit Status Output and Eight Impulse Outputs**
- **Calibration of Gain and Phase Error**
- **Compensation of the Non-linearity of Low Power Measurement**
- **Adjustable Starting Current and Meter Constant**
- **Measurement Bandwidth of 1000 Hz**
- **Tamper-proof Design**
- **Single +5V Supply**

Description

A two chip solution, consisting of AT73C500 and AT73C501 (or AT73C502), offers all main features required for the measurement and calculation of various power and energy quantities in static Watt-hour meters. The devices operate according to IEC1036, class 1, specification. IEC 687, class 0.5 and 0.2 requirements are fulfilled when used with external temperature compensated voltage reference.

The AT73C501 contains six, high-performance, Sigma-Delta analog-to-digital converters (ADC). The AT73C500 is an efficient digital signal processor (DSP) that supports interfacing both with the AT73C501 and with an external microprocessor. The AT73C500 can also be used with the differential input ADC, AT73C502.

With this chipset, only a minimum of discrete components is required to develop products ranging from simple domestic Watt-hour meters to sophisticated industrial meters. The chipset can be used in single-phase as well as in poly-phase systems. The AT73C500 is easy to configure. By changing the mode of the AT73C500, the device can be operated in a stand-alone environment or be used with a separate control processor. It is also possible to configure the circuit to perform the functions of three independent single phase Wh meters.

The chips support calibration of gain and phase error. All calibrations are done in the digital domain and no trimming components are needed. The calibration coefficients are either stored in an EEPROM memory or supplied by an external microprocessor.

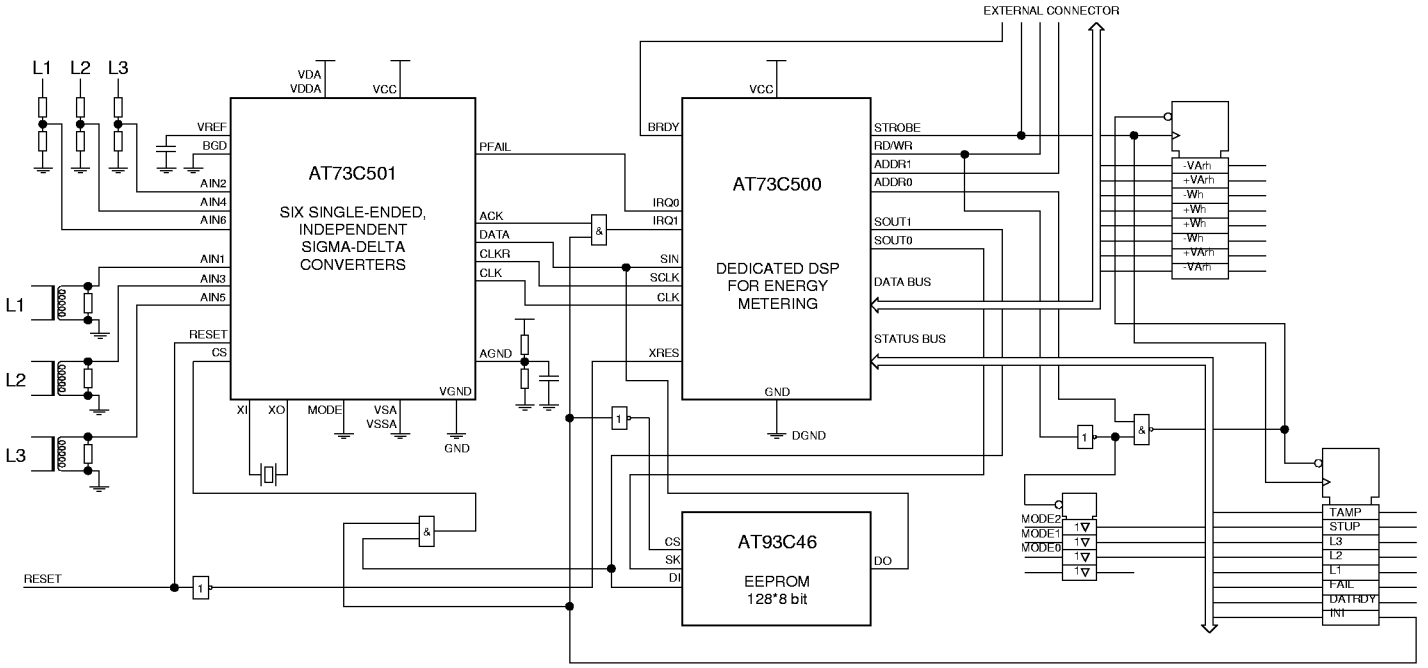
(continued)

Chipset Solution for Watt-hour Meters

AT73C500 with AT73C501 or AT73C502

Rev. 1035B–09/99

Figure 1. Block diagram of the AT73C500 chipset in stand-alone configuration



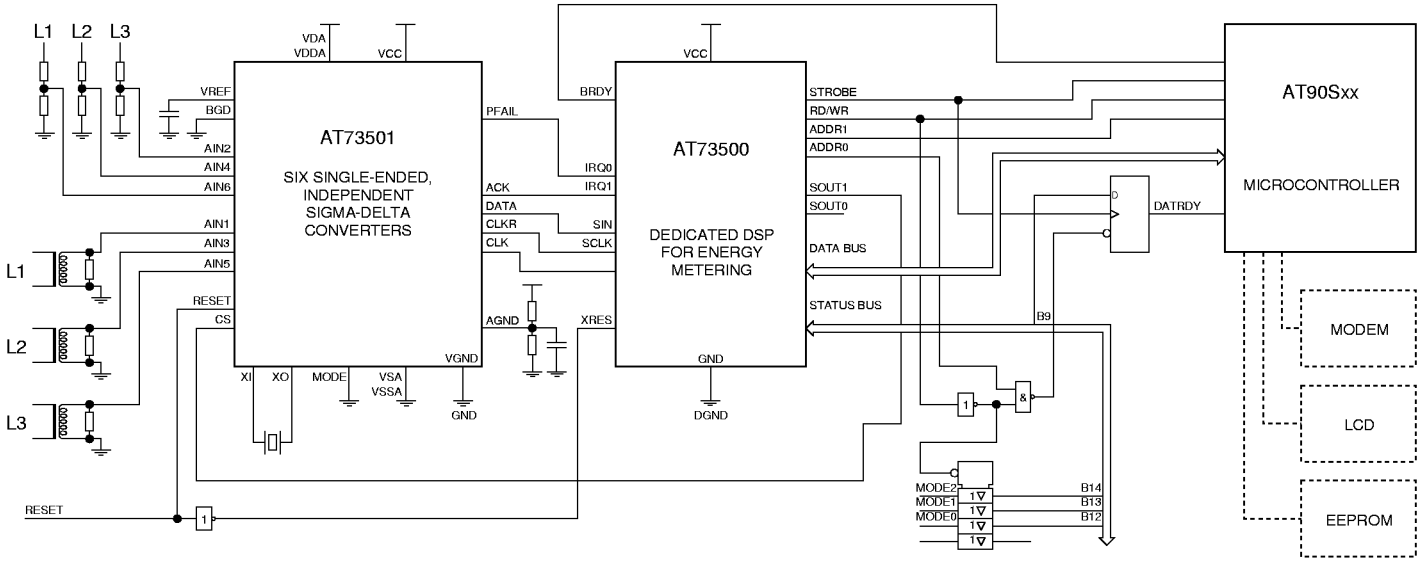
The AT73C500 is programmed to measure active, reactive and apparent phase powers. Phase factors, phase voltages, phase currents and line frequency are also measured, simultaneously. Based on the individual phase powers, total active power is determined.

The power values are calculated over one-line frequency cycle. The negative and positive results are accumulated in different registers, which allows for separate billing of imported and exported active energy. Also, the reactive results are sorted depending on whether capacitive or inductive load is applied.

Eight pulse outputs are provided. Each billing quantity (+Wh, -Wh, +VArh, -Varh) is supplied with its own meter constant output, as well as a display counter output. In multi-channel mode, AT73C500 performs the functions of three independent single phase Wh meters and three impulse outputs are available, one for each meter element.

All measurement information is available on an 8-bit microprocessor bus. The results are output in six packages, 16 bytes each. Mode and status information of the meter is also transferred with each data block.

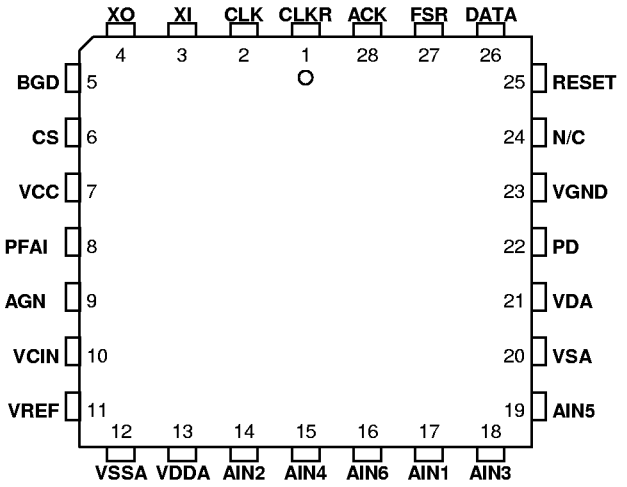
Figure 2. Block diagram of the AT73C500 chipset in microprocessor configuration



Pin Description

AT73C501 Single-ended ADC

Figure 3. PLCC-28 package pin layout



Power Supply Pins	Pin	I/O	Description
VDDA	13	PWR	Analog Supply, Positive, +5V
VSSA	12	PWR	Analog Supply, Negative, 0V
VDA	21	PWR	Analog Supply, Positive, +5V
VSA	20	PWR	Analog Supply, Negative, 0V
AGND	9	PWR	Analog Ground Reference Input
VREF	11	PWR	Reference Voltage Output/Input
VCC	7	PWR	Digital Supply, Positive, +5V
VGND	23	PWR	Digital Supply, Negative, 0V

Crystal Osc Signals	Pin	I/O	Description
XI	3	I	Crystal Oscillator Input
XO	4	O	Crystal Oscillator Output

Analog Signals	Pin	I/O	Description
AIN1	17	I	Current, Channel 1
AIN2	14	I	Voltage, Channel 1
AIN3	18	I	Current, Channel 2
AIN4	15	I	Voltage, Channel 2
AIN5	19	I	Current, Channel 3
AIN6	16	I	Voltage, Channel 3
VCIN	10	I	Input to Voltage Monitoring Block

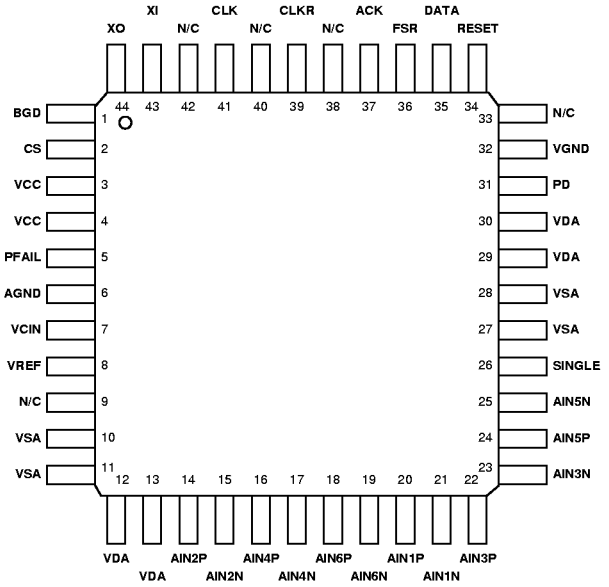
Digital Control Signals	Pin	I/O	Description
BGD	5	I	By-pass Control for Reference Voltage
CS	6	I	Chip Select Input
PD	22	I	Power Down Control for A/D Modulators
N/C	24	I	Connect to VGND
RESET	25	I	Reset Input, Active High

Status Flags	Pin	I/O	Description
PFAIL	8	O	Output of Voltage Monitoring Block

Output Bus Signals	Pin	I/O	Description
CLK	2	O	Master Clock Output
CLKR	1	O	Serial Bus Clock Output
DATA	26	O	Serial Data Output
FSR	27	O	Output Sample Frame Signal
ACK	28	O	Data Ready Acknowledge Output

AT73C502 Differential-Ended ADC

Figure 4. QFP-44 package pin layout



Power Supply Pins	Pin	I/O	Description
VDA	12, 13, 29, 30	PWR	Analog Supply, Positive, +5V
VSA	10, 11, 27, 28	PWR	Analog Supply, Negative, 0V
AGND	6	PWR	Analog Ground Reference Input
VREF	8	PWR	Reference Voltage Output/Input
VCC	3, 4	PWR	Digital Supply, Positive, +5V
VGND	32	PWR	Digital Supply, Negative, 0V

Crystal Osc Signals	Pin	I/O	Description
XI	43	I	Crystal Oscillator Input
XO	44	O	Crystal Oscillator Output

Analog Signals	Pin	I/O	Description
AIN2P	14	I	Voltage, Channel 1, Positive
AIN2N	15	I	Voltage, Channel 1, Negative
AIN4P	16	I	Voltage, Channel 2, Positive
AIN4N	17	I	Voltage, Channel 2, Negative

Analog Signals	Pin	I/O	Description
AIN6P	18	I	Voltage, Channel 3, Positive
AIN6N	19	I	Voltage, Channel 3, Negative
AIN1P	20	I	Current, Channel 1, Positive
AIN1N	21	I	Current, Channel 1, Negative
AIN3P	22	I	Current, Channel 2, Positive
AIN3N	23	I	Current, Channel 2, Negative
AIN5P	24	I	Current, Channel 3, Positive
AIN5N	25	I	Current, Channel 3, Negative
VCIN	7	I	Input to Voltage Monitoring Block
N/C	9	I	Must be left floating

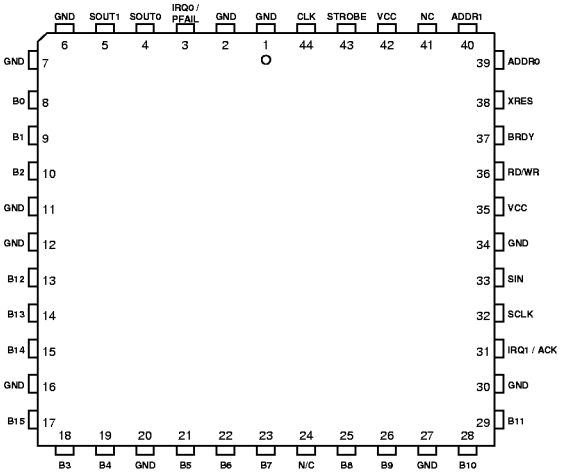
Digital Control Signals	Pin	I/O	Description
BGD	1	I	By-pass Control for Reference Voltage
CS	2	I	Chip Select Input
PD	31	I	Power Down Control for A/D Modulators
N/C	33	I	Connect to VGND
RESET	34	I	Reset Input, Active High
SINGLE	26	I	Single / Differential selector. · Low: Differential · High or n/c: Single-ended

Status Flags	Pin	I/O	Description
PFAIL	5	O	Output of Voltage Monitoring Block

Output Bus Signals	Pin	I/O	Description
CLK	41	O	Master Clock Output
CLKR	39	O	Serial Bus Clock Output
DATA	35	O	Serial Data Output
FSR	36	O	Output Sample Frame Signal
ACK	37	O	Data Ready Acknowledge Output

AT73C500 DSP

Figure 5. PLCC-44 package pin layout



Power Supply Pins	Pin	I/O	Description
VCC	35, 42	PWR	Digital Supply, Positive, +5V
GND	1, 2, 6, 7, 11, 12,16, 20, 27, 30, 34	PWR	Digital Supply, Negative, 0V

Digital Inputs	Pin	I/O	Description
CLK	44	I	Clock Input
XRES	38	I	Reset Input, active low
IRQ0	3	I	Interrupt Input, usually connected to PFAIL output of AT73C501
IRQ1	31	I	Interrupt Input, connected to ACK Output of AT73C501

Status/ Mode Bus	Pin	I/O	Description
B15	17	I/O	Status/Mode Bus, Bit7
B14	15	I/O	Status/Mode Bus, Bit6
B13	14	I/O	Status/Mode Bus, Bit5
B12	13	I/O	Status/Mode Bus, Bit4
B11	29	I/O	Status/Mode Bus, Bit3
B10	28	I/O	Status/Mode Bus, Bit2
B9	26	I/O	Status/Mode Bus, Bit1
B8	25	I/O	Status/Mode Bus, Bit0

Microprocessor Bus	Pin	I/O	Description
B7	23	I/O	µP Bus, Bit7
B6	22	I/O	µP Bus, Bit6
B5	21	I/O	µP Bus, Bit5
B4	19	I/O	µP Bus, Bit4
B3	18	I/O	µP Bus, Bit3
B2	10	I/O	µP Bus, Bit2
B1	9	I/O	µP Bus, Bit1
B0	8	I/O	µP Bus, Bit0

AT73C501 / AT73C502 and EEPROM Interface	Pin	I/O	Description
SOUT0	4	O	Serial Output, used as a clock for EEPROM
SOUT1	5	O	Serial Output, used as Chip Select (CS) for AT73C501 and as Data Input (DI) for EEPROM
SIN	33	I	Serial Data Input, data from AT73C501 or from EEPROM
SCLK	32	I	Serial Clock Input, bit clock from AT73C501

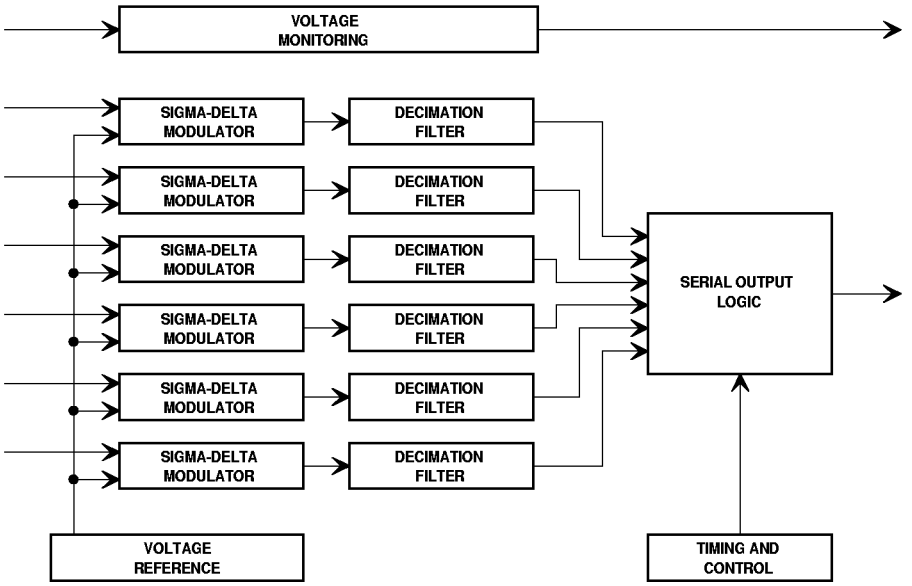
Control Signals of µP Bus and Status/Mode Bus	Pin	I/O	Description
STROBE	43	O	Strobe Output
BRDY	37	I	Microprocessor ready for I/O, Active Low
ADDR1	40	O	Address Output 1, used for µP bus
ADDR0	39	O	Address Output 0, used for Status/ Mode bus and for Impulse Outputs
RD/WR	36	O	Read/Write Signal

AT73C501 and AT73C502

The AT73C501 consists of six, 16-bit analog-to-digital converters. The converters are equipped with single-ended inputs. For differential ended applications, the AT73C502 chip is used.

The converters contain a reference voltage generator, voltage monitoring block and serial output interface. Both converters are based on high-performance, oversampling Sigma-Delta modulators and digital decimation filters.

Figure 6. Block diagram of the single-ended ADC chip, AT73C501



In a 50 Hz meter, the nominal decimated sampling rate of 3200 Hz is used. This corresponds to 64 samples per each line frequency cycle. 60 Hz meters operate with 3840 Hz sample rate. The master clock frequency of the ADC is 1024 times higher than the above frequencies, i.e. 3.2768 MHz in 50 Hz meters and 3.93216 MHz in 60 Hz systems. The default meter constant of AT73C500 energy counters is based on the above sample rates.

Other sample frequencies can be used, but the energy results have to be scaled accordingly. If higher sampling rate is selected, the meter constant will also be increased by the same ratio.

The three current inputs of AT73C501 are fed from secondary outputs of current transformers, from Hall sensors or other similar sensors. In differential-ended applications, such as with current shunt resistors, the AT73C502 ADC can be used. On both of these converters, the voltage inputs must be equipped with simple external voltage dividers.

The input voltage range of each converter is $2V_{PP}$. The characteristics of a Watt-hour meter operating, according to IEC1036 specification, are based on a certain basic current, I_B. As a default, the basic current of AT73C500 chipset is to 6.25% of the current input full scale value. This means that if a meter is designed for $I_B = 5A_{RMS}$, the full scale range of the current channels will be:

$$I_{FS} = 5\ A_{RMS} \times \frac{100}{6.25} = 80\ A_{RMS}$$

The following current transformer and voltage divider configuration is recommended for a 230V, 3-phase system, with 5A basic current:

	Voltage Inputs	Current Inputs
Converter full-scale input	$2.0V_{PP}$	$2.0V_{PP}$
Corresponding full-scale line voltage / current	$270V_{RMS}$	$80A_{RMS}$

With the above settings, the nominal pulse rate of the meter constant outputs is 1250 impulses/kWh (1250 impulses/kVArh) and the rate of four display outputs 100 impulses/kWh (100 imp/kVArh).

When used in a 5A transformer operated meter, the maximum current range can be scaled down to 8A for example. In this case, the meter constant will be ten times higher than in an 80A meter, i.e. 12500 impulses/kWh. Similarly, the starting current level will be transferred to 2mA, from 20mA.

If the nominal voltage is chosen to be 120V, the voltage divider can either have the same configuration as in the 230V meter, or it can be modified to produce $2.0V_{pp}$ with 140V phase voltage. In the latter case, the default meter constant will be roughly twice the constant of 230V meter, i.e. 2411 impulses/kWh. The meter constant can be scaled to an even number value by means of calibration.

As described above, the configuration of voltage dividers and current transformers affects to almost all parameters being metered, like energy counters and impulse outputs. A calibration coefficient is provided for the adjustment of the display pulse rates. With this coefficient, the effect of various voltage divider and current transformer configurations can be compensated. Care should be taken that the dynamic range of the A/D converters is always effectively utilized. The use of calibration coefficients is described in the next section.

Current and voltage samples of AT73C501/AT73C502 are multiplexed and transferred to AT73C500 through a serial interface. The timing of the interface is presented in the next section.

AT73C501/AT73C502 contain an internal bandgap voltage reference. When used in class 0.5 and 0.2 meters, smaller temperature drift is required. This can be achieved by bypassing the internal reference and using temperature compensated external reference instead. The reference is selected with the BGD input.

BGD	Reference
0 (V_{SS})	Internal
1 (V_{DD})	External

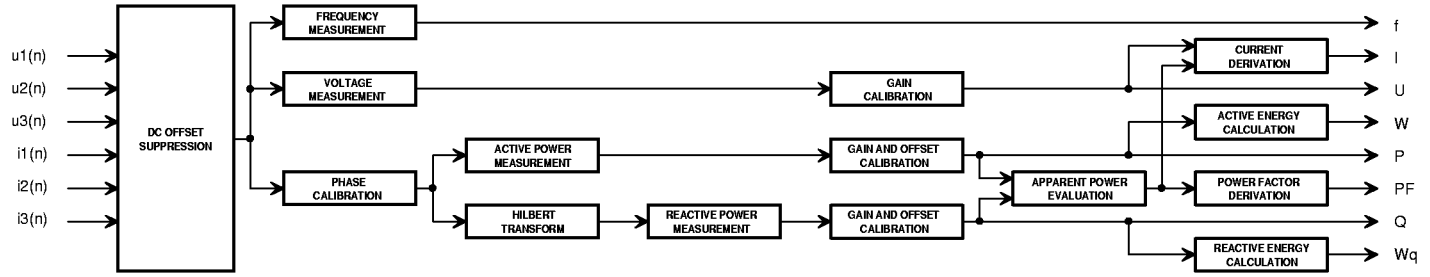
There is an integrated voltage monitoring block on the converter chip. The PFAIL output is forced high if the level of voltage supplied to V_{CIN} input drops below 4.2V. There is a hysteresis in the monitoring function and PFAIL returns low if voltage at V_{CIN} is raised back above 4.3V.

PFAIL output of AT73C501/AT73C502 can be connected to an interrupt input of AT73C500. AT73C500 detects the rising edge of PFAIL. To assure reliable power-down procedure after voltage break, the V_{CC} supply of AT73C500 must be equipped with a 470 µF or larger capacitor.

AT73C500

AT73C500 performs power and energy calculations. It also controls the interfacing to the AT73C501 (or AT73C502) and to an external microprocessor. The block diagram of the DSP is presented below.

Figure 7. Block diagram of DSP software

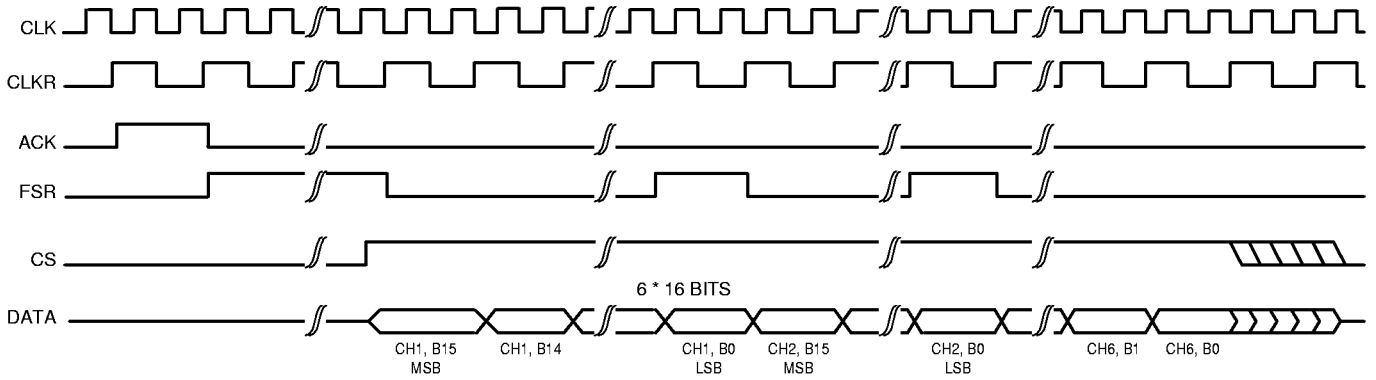


Serial Bus Interface

The timing of the serial bus interface connecting the ADC and DSP devices is presented in Figure 8. The same bus is used to read the calibration data from an external EEPROM. This operation is described in section “Loading of Calibration Coefficients” on page 19.

When the three current and three voltage samples are ready, AT73C501/AT73C502 raises the ACK output. AT73C500 detects the rising edge of ACK, and, after a few clock cycles, it is ready to read the samples through the serial bus. The transfer is initiated by CS/SOUT1 signal and the data bits are strobed in at the falling edge of CLKR/SCLK clock. Six 16-bit samples is transferred in the following sequence: I1, U1, I2, U2, I3 and U3.

Figure 8. Serial bus timing



Operating Modes of AT73C500

The AT73C500 chipset has six operating modes. The mode is selected by three mode control inputs which AT73C500 reads through a bus during the initialization procedure after a reset state. The operation of AT73C501/AT73C502 is independent of the mode selected.

In operating mode 7, the default display pulse rate is 10 impulses per kWh, instead of 100 impulses per kWh, as in other modes.

Mode Number	Mode Bit 2	Mode Bit 1	Mode Bit 0	Operating Mode	Calibration Data Storage
0	0	0	0	Not in use	
1	0	0	1	Normal operation	EEPROM
2	0	1	0	Multi-channel operation	EEPROM
3	0	1	1	Normal operation	Micro-processor
4	1	0	0	Multi-channel operation	Micro-processor
5	1	0	1	Test mode	None
6	1	1	0	Not in use	
7	1	1	1	Normal operation	EEPROM

Normal Measurement Mode

AT73C500 devices support both stand-alone and microprocessor configuration. The calibration coefficients can either be supplied by a processor or stored in an 128 x 8-bit EEPROM. The ROM is interfaced with AT73C500 via three pin serial bus. AT73C500 and the processor communicate through an 8-bit bus.

The only operational difference between stand-alone and µP mode is the way of reading calibration coefficients. This allows various combinations of these two configurations to be utilized. For example, the calibration data can be stored in an EEPROM even though the processor reads and displays the measurement results supplied by AT73C500 device.

In most cases, the use of external EEPROM gives flexibility to the meter testing and calibration, and also makes the processor interface easier to implement. Therefore, this configuration is recommended even in meters equipped with a separate microprocessor.

The same sequence of basic calculations is performed both in poly-phase and single-phase meters. This sequence consists of DC offset suppression, phase, gain and offset calibration, calculations of measurement quantities and data transfer to µP bus and pulse outputs. AT73C500 constantly monitors various tampering and fault situations, which are indicated by status bits.

After a reset state, AT73C500 goes through an initialization sequence. The device reads the operating mode and fetches the calibration coefficients and adjustment factors for output pulse rate and starting current level, either from a non-volatile memory or from a microprocessor. After that the normal measurement starts. The reset state is normally activated by power-up reset following the recovery from a voltage interruption.

Measurements and Calculations

The first operation performed by AT73C500 is digital high-pass filtering. The purpose of the filtering is to remove the DC offset of both current and voltage samples.

From offset free samples, active power is calculated phase-by-phase with simple multiplication and addition operations.

First, the current samples are multiplied by voltage samples. The multiplication results are summed over one line period and finally the sum value is divided by 64. This discrete time operation gives the average power of one 50 Hz period and the result corresponds to the following continuous time formula:

$$P = \sum_{n=0}^{N} \left(\frac{1}{T} \times \int_{0}^{T} [A_N \times U_N \times \sin\{n \times wt\} \times A_N \times I_N \times \sin\{n \times wt + \varnothing_N\} dt] \right)$$

$$= \sum_{n=0}^{N} \left(\frac{1}{2} \times A_n \times A_n \times U_n \times I_n \times \cos(\varnothing_n) \right)$$

where

T = 1/50 Hz,

n = 1, 2, 3,..., 20 (basic 50 Hz frequency and the harmonics),

A_n = frequency response of calculations.

This method of calculation does take into account the effect of harmonics.

The total power is calculated by summing the power of each line phase. Reactive power calculation is based on a similar procedure. Before multiplying the current and voltage samples AT73C500 performs a frequency independent 90 degree phase shift of the voltage signal. This is realized with a digital Hilbert transformation filter. The bandwidth of reactive power measurement is limited to 360 Hz.

Based on the active and reactive results apparent power and power factors are determined. RMS phase voltages are calculated by squaring and summing the voltage samples and finally taking a square root of the results. Current is determined by dividing apparent power result by corresponding phase voltage.

Frequency measurement is based on a comparison of the line frequency and AT73C500 sampling clock frequency. The measurement range is from 20 Hz to 350 Hz.

All measurements and calculations, except frequency measurement, are made over 10 line cycle periods. The results are updated and transferred to processor bus once in 200 ms.

Measurement Registers

For the measurement parameters 25 registers are allocated:

Register	Meaning
REG0	Phase 1, active power, P1(10T), 32-bit register;
REG1	Phase 2, active power, P2(10T), 32-bit register;
REG2	Phase 3, active power, P3(10T), 32-bit register;
REG3	Phase 1, reactive power, Q1(10T), 32-bit register;
REG4	Phase 2, reactive power, Q2(10T), 32-bit register;
REG5	Phase 3, reactive power, Q3(10T), 32-bit register;
REG6	Phase 1, apparent power, S1(10T), 16-bit register;
REG7	Phase 2, apparent power, S2(10T), 16-bit register;
REG8	Phase 3, apparent power, S3(10T), 16-bit register;
REG9	Phase 1, power factor, PF1, 16-bit register;
REG10	Phase 2, power factor, PF2, 16-bit register;
REG11	Phase 3, power factor, PF3, 16-bit register;
REG12	Active exported energy since the latest reset, +Wp, 32-bit counter;
REG13	Active imported energy since the latest reset, -Wp, 32-bit counter;
REG14	Reactive energy, inductive load, Wqind, 32-bit counter;
REG15	Reactive energy, capacitive load, Wqcap, 32-bit counter;
REG16	Number of 10T periods elapsed since the latest reset, 32-bit counter;
REG17	Frequency, f, 16-bit register;
REG18	Reserved for further use, 16-bit register;
REG19	Phase 1, voltage U1, 16-bit register;
REG20	Phase 2, voltage U2, 16-bit register;
REG21	Phase 3, voltage U3, 16-bit register;
REG22	Phase 1, current I1, 16-bit register;
REG23	Phase 2, current I2, 16-bit register;
REG24	Phase 3, current I3, 16-bit register.

The size of the registers is either 16-bit or 32-bit. IEC specifications apply to the calculations of active and reactive power and energy (REG 0-5 and REG 12-15). Other results are intended mainly for demand recording and for various diagnostic and display functions. The accuracy of those are limited due to the finite resolution.

In multi-channel mode the active energy of each three meters (phases) is stored in registers 12-14. REG15 is not in use.

The maximum value of different power registers differs, depending on the calculation formulas used. The scaling of registers is described below.

If a full scale sine signal is applied to voltage and current inputs and the voltage and current channels are exactly in the same phase, a value of 258F C2F7H will be produced in the 32-bit P1, P2 and P3 registers. The LS bit will correspond to about 34 microwatts in nominal input conditions of 270V maximum phase voltage and 80A maximum current.

If the load is fully reactive ($\pm 90°$ phase difference) and full scale signals are applied, the Q1, Q2 and Q3 register content will be 2231 594DH positive or negative, and the LSB will represent about 38 µVAr. The maximum value of the 16-bit S registers is 258EH and this value is obtained if a full scale amplitude is produced to the current and voltage inputs. LS bit of the S registers correspond to about 2.25VA power.

The following formula is used to calculate the power factor:

$$\mathrm{PF} = \mathrm{sign}(Q) \times \frac{\mathrm{abs}(P)}{\mathrm{abs}(S)}$$

The PF register contents 7FFFH represents power factor value one and the contents 0000H value zero. Negative PF values are stored correspondingly as negative binary numbers. It should be noted that the sign of power factor result indicates whether the loading is inductive (+) or capacitive (-).

The contents of frequency register (REG17) actually represents a 16-bit figure which corresponds to the duration of 50 line frequency cycles. The measurement is made by comparing the line frequency with one of the sampling clocks of AT73C500 and therefore the result depends on the crystal frequency used. With default 3.2768 MHz crystal, the resolution of time value is 1.25 ms. To get the frequency, the following calculation has to be made:

$$f = \frac{40000}{\mathrm{REG17}}\mathrm{Hz}$$

If the master clock frequency (MCLK) of AT73C500 is not nominal, the following formula gives frequency results:

$$f = \frac{40000}{\mathrm{REG17}} \times \frac{\mathrm{MCLK}}{3.2768\mathrm{MHz}}\mathrm{Hz}$$

In the default condition, value 7FFFH of register 17 corresponds to 1.22 Hz frequency, value 0320H represents 50 Hz and 0001H 40 kHz. However, in practice, the bandwidth of frequency measurement is limited to 20 Hz to 350 Hz.

The frequency measurement is locked with one of the phase voltages. If this voltage disappears, AT73C500 tries to track one of the other phases. The frequency measurement works down to about 10% level of the full scale voltage range. The harmonics content of phase voltage should be below 10%. If it is higher, erroneous frequency results may be obtained.

The voltage registers (REG19-REG21) are scaled so that full scale sinusoidal input signal at AT73C501/AT73C502 voltage channels will produce 7A8BH value into voltage registers. This means that the resolution of the registers is about 8.6 mV. Accordingly, full scale current will produce 7DA4H to current registers (REG22-REG24) providing a resolution of about 2.5 mA. In practice, the voltage can be measured down to about 25V level and current down to about 100mA.

If either voltage or current, or both, contain a considerable amount of harmonics producing a square wave type waveform, it is recommended to scale the input range so that the maximum peak-to-peak value is at least 10% below the full scale range of inputs. This is to avoid overflow in the calculations performed by AT73C500.

Energy Counters

Four 32-bit counters (REG12-REG15) measure energy consumption. In nominal situations, the counters are always incremented when 0.4Wh (0.4VArh) energy is consumed. The counters can store minimum of 1100 days consumption, provided that AT73C501/AT73C502 and AT73C500 are used with default settings.

Impulse outputs are generated from these counters. The meter constant rate represents 2 LSBs of a counter which equals 0.8 Wh (0.8 VArh) and produces 1250 impulses/kWh. (1250 impulses/kVArh). In modes 1 to 4, the display pulses are generated from 25 LSBs of a counter. This corresponds to an impulse rate of 100 impulses/kWh (100 impulses/kVArh). It is possible to adjust this rate with MCC calibration coefficient. In mode 7, 250 LSBs of the energy register is needed to generate one impulse (10 impulses/kWh).

The default values above are based on $80A_{RMS}$ full scale current, $270V_{RMS}$ full scale voltage and 3.2768 MHz clock rate.

The crystal frequency will affect the values of energy registers (REG12-REG15) and time register (REG 16). It will also change the pulse rates of the impulse outputs.

It is recommended that 50 Hz meters are operated from 3.2768 MHz crystal. In 60 Hz system, a 3.93216 MHz clock is normally used. Because the clock frequency generates a time reference for energy calculations, the content of energy registers and also the pulse rate of impulse outputs will change when crystal is changed. For example, the nominal meter constant and display pulse rate of 60 Hz meter (3.93216 MHz clock) is:

$$MC = \frac{60Hz}{50Hz} \times 1250 \frac{imp}{kWh} = 1500 \frac{imp}{kWh}$$

and

$$DP = \frac{60Hz}{50Hz} \times 100 \frac{imp}{kWh} = 120 \frac{imp}{kWh}$$

The LSB of energy registers correspond to 0.33Wh instead of 0.4Wh, as follows:

$$E_{LSB} = \frac{3.2768MHz}{3.93216MHz} \times 0.4Wh = 0.333333\ldots Wh$$

The pulse rate can be scaled to 100 imp/kWh by programming value 5 to MCC coefficient, as below:

$$IMP = (25 + MCC)\frac{1}{imp} \times E_{LSB} = 30\frac{1}{imp} \times 0.3333\ldots Wh = 10\frac{Wh}{imp}$$

which equals 100 impulses per kilowatt hour.

The following table summarizes the contents of all measurement registers.

Register	Conditions	Full Scale Output (hex)	Resolution (hex)
REG0 - REG2	U = 270V, I = 80A, PF = 1	258F C2F7	34.276 µW
REG3 - REG5	U = 270V, I = 80A, PF = 0	2231 594D	37.653 µVAr
REG6 - REG8	U = 270V, I = 80A	258E	2.2467 VA
REG9 - REG11	PF = 1 PF = -1	7FFF 8001	0.0000305 -0.0000305
REG12 - REG15	W = 1.718GWh	FFFF FFFF	0.4Wh
REG16	ΔT = 238609.3h	FFFF FFFF	0.2s
REG17	50*T = 40.959s	7FFF	1.25 ms
REG19 - 21	U = 270V	7A8B	8.6 mV
REG22 - 24	I = 80A	7DA4	2.5 mA

Output Operations

The data output by AT73C500 can be divided into three categories: data to external processor, status information and impulse outputs. AT73C500 reads mode information, and in mode 3 and 4, also calibration data via external bus. For the I/O operation, two 8-bit buses are allocated.

The same eight data lines are reserved both for the impulse outputs and for the processor interface. The separation is done with two address pins. When communicating with the microprocessor, address 1 (pin ADDR1) is activated (high). Impulses are output combined with a high level of address 0 (ADDR0). For status information separate 8-bit bus is reserved. The table below describes the use of the two buses of AT73C500.

Data bits	Bus	Address	Mode	Usage
B0 - B7	Data Bus	ADDR0	Output	Impulse Outputs
B8 - B15	Status Bus	ADDR0	Output	Status Information
B0 - B7	Data Bus	ADDR1	Input/ Output	Processor Interface
B12 - B14	Status Bus	ADDRx	Input	Mode Inputs

For status and impulse outputs, external latches are needed to store the information while buses are used for other tasks. In most cases, the data bus of AT73C500 and processor I/O bus can be connected directly with each other. The data transfer is controlled by handshake signals, ADDR1, RD/WR, STROBE and BRDY. One of the status outputs DATRDY (B9, ADDR0) can be used as an interrupt signal. Interrupt can be also generated from the handshake lines.

In most meters, only some of the I/O operations of AT73C500 are needed. If a meter contains a separate processor, status outputs of AT73C500 are typically not used since the processor will anyway track the status information supplied by AT73C500. Often only one or two of the impulse outputs are wired to the test LED or electromechanical counter.

Data Transfer to External Microprocessor

The calculation results of AT73C500 are transferred to processor via 8-bit parallel bus. During normal operation, the information transfer is divided into six packages which are written in 200ms intervals after the calculations over ten line frequency cycles have been completed. There is a time interval of one line cycle between each individual data package. The first four bytes of a package contain synchronization, mode and status information, and the rest 12 bytes are reserved for the actual measurement results. The contents of the six data packages are as follows:

Table 1. Package 0

Byte	Data	Order	Meaning
1	Sync LS	Single byte	Synchronization
2	Sync MS	Single byte	Synchronization
3	Mode	Single byte	Mode information
4	Status	Single byte	Status information
5	REG0	(LS+2) byte	Active power, phase 1
6	REG0	MS byte	Active power, phase 1
7	REG0	LS byte	Active power, phase 1
8	REG0	(LS+1) byte	Active power, phase 1
9	REG1	(LS+2) byte	Active power, phase 2
10	REG1	MS byte	Active power, phase 2
11	REG1	LS byte	Active power, phase 2
12	REG1	(LS+1) byte	Active power, phase 2
13	REG2	(LS+2) byte	Active power, phase 3
14	REG2	MS byte	Active power, phase 3
15	REG2	LS byte	Active power, phase 3
16	REG2	(LS+1) byte	Active power, phase 3

Table 2. Package 1

Byte	Data	Order	Meaning
1	Sync LS	Single byte	Synchronization
2	Sync MS	Single byte	Synchronization
3	Mode	Single byte	Mode information
4	Status	Single byte	Status information
5	REG3	(LS+2) byte	Reactive power, phase 1
6	REG3	MS byte	Reactive power, phase 1
7	REG3	LS byte	Reactive power, phase 1
8	REG3	(LS+1) byte	Reactive power, phase 1
9	REG4	(LS+2) byte	Reactive power, phase 2
10	REG4	MS byte	Reactive power, phase 2
11	REG4	LS byte	Reactive power, phase 2
12	REG4	(LS+1) byte	Reactive power, phase 2
13	REG5	(LS+2) byte	Reactive power, phase 3
14	REG5	MS byte	Reactive power, phase 3
15	REG5	LS byte	Reactive power, phase 3
16	REG5	(LS+1) byte	Reactive power, phase 3

Table 3. Package 2

Byte	Data	Order	Meaning
1	Sync LS	Single byte	Synchronization
2	Sync MS	Single byte	Synchronization
3	Mode	Single byte	Mode information
4	Status	Single byte	Status information
5	REG6	LS byte	Apparent power, phase 1
6	REG6	MS byte	Apparent power, phase 1
7	REG7	LS byte	Apparent power, phase 2
8	REG7	MS byte	Apparent power, phase 2
9	REG8	LS byte	Apparent power, phase 3
10	REG8	MS byte	Apparent power, phase 3
11	REG9	LS byte	Power factor, phase 1
12	REG9	MS byte	Power factor, phase 1
13	REG10	LS byte	Power factor, phase 2
14	REG10	MS byte	Power factor, phase 2
15	REG11	LS byte	Power factor, phase 3
16	REG11	MS byte	Power factor, phase 3

Table 4. Package 3

Byte	Data	Order	Meaning
1	Sync LS	Single byte	Synchronization
2	Sync MS	Single byte	Synchronization
3	Mode	Single byte	Mode information
4	Status	Single byte	Status information
5	REG12	(LS+2) byte	Active exported energy
6	REG12	MS byte	Active exported energy
7	REG12	LS byte	Active exported energy
8	REG12	(LS+1) byte	Active exported energy
9	REG13	(LS+2) byte	Active imported energy
10	REG13	MS byte	Active imported energy
11	REG13	LS byte	Active imported energy
12	REG13	(LS+1) byte	Active imported energy
13	REG14	(LS+2) byte	Reactive energy, inductive load
14	REG14	MS byte	Reactive energy, inductive load
15	REG14	LS byte	Reactive energy, inductive load
16	REG14	(LS+1) byte	Reactive energy, inductive load

Table 5. Package 4

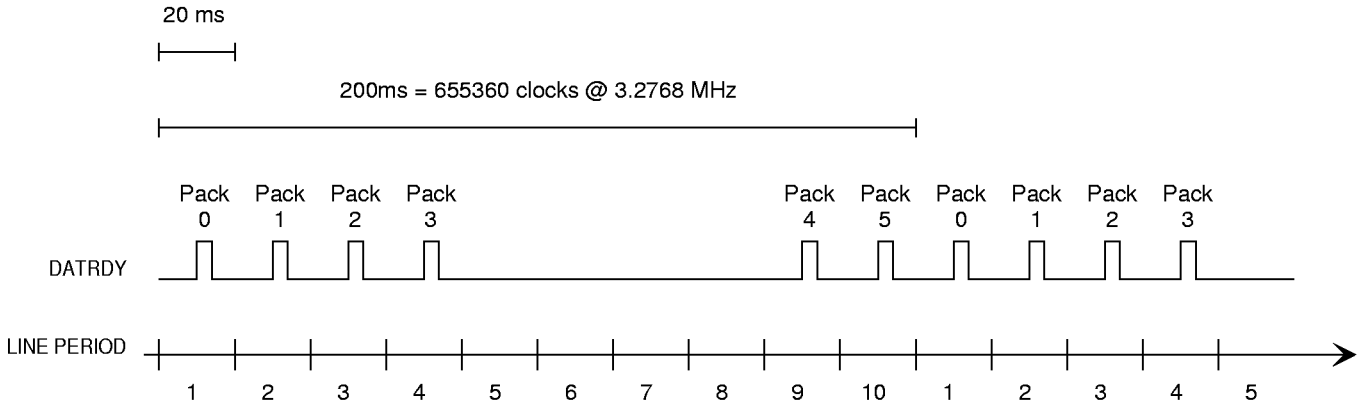
Byte	Data	Order	Meaning
1	Sync LS	Single byte	Synchronization
2	Sync MS	Single byte	Synchronization
3	Mode	Single byte	Mode information
4	Status	Single byte	Status information
5	REG15	(LS+2) byte	Reactive energy, capacitive load
6	REG15	MS byte	Reactive energy, capacitive load
7	REG15	LS byte	Reactive energy, capacitive load
8	REG15	(LS+1) byte	Reactive energy, capacitive load
9	REG16	(LS+2) byte	Counter
10	REG16	MS byte	Counter
11	REG16	LS byte	Counter
12	REG16	(LS+1) byte	Counter
13	REG17	LS byte	Frequency
14	REG17	MS byte	Frequency
15	REG18	LS byte	Reserved
16	REG18	MS byte	Reserved

Table 6. Package 5

Byte	Data	Order	Meaning
1	Sync LS	Single byte	Synchronization
2	Sync MS	Single byte	Synchronization
3	Mode	Single byte	Mode information
4	Status	Single byte	Status information
5	REG19	LS byte	Voltage, phase 1
6	REG19	MS byte	Voltage, phase 1
7	REG20	LS byte	Voltage, phase 2
8	REG20	MS byte	Voltage, phase 2
9	REG21	LS byte	Voltage, phase 3
10	REG21	MS byte	Voltage, phase 3
11	REG22	LS byte	Current, phase 1
12	REG22	MS byte	Current, phase 1
13	REG23	LS byte	Current, phase 2
14	REG23	MS byte	Current, phase 2
15	REG24	LS byte	Current, phase 3
16	REG24	MS byte	Current, phase 3

The six data packages arrive as follows:

Figure 9. Data transfer to processor in six packages



In normal mode, the Sync LS byte indicates the number of data package which will follow (value 0...5). There are also two special situations indicated by this byte. Value six of Sync LS byte means that the processor is expected to supply calibration data to AT73C500. Value seven is written by AT73C500 in case power interruption is detected and billing information needs to be transferred to microprocessor. In this case the processor knows that both packages 3 and 4 will follow one after each other as shown in Figure 10.

Content of Sync LS byte is described in the following table. Bits 3-7 of the Sync LS byte are not used.

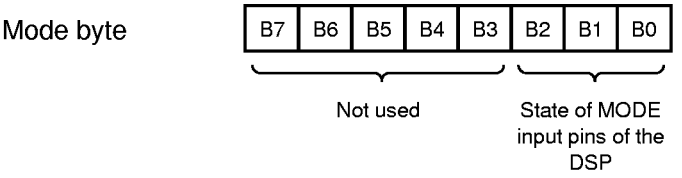
Table 7. Sync LS Byte

B7 - B3	B2	B1	B0	Data package	Mode
X X X X X	0	0	0	0	Normal operation, Data output
X X X X X	0	0	1	1	Normal operation, Data output
X X X X X	0	1	0	2	Normal operation, Data output
X X X X X	0	1	1	3	Normal operation, Data output
X X X X X	1	0	0	4	Normal operation, Data output
X X X X X	1	0	1	5	Normal operation, Data output
X X X X X	1	1	0	(none)	DSP waiting for calibration data
X X X X X	1	1	1	3 and 4	PFAIL active, billing information to be transferred

The Sync MS byte contains a unique 8-bit data, 80H. It can be used as a synchronization byte by the external controller.

The mode byte contains the following information:

Figure 10. Meaning of bits in mode byte

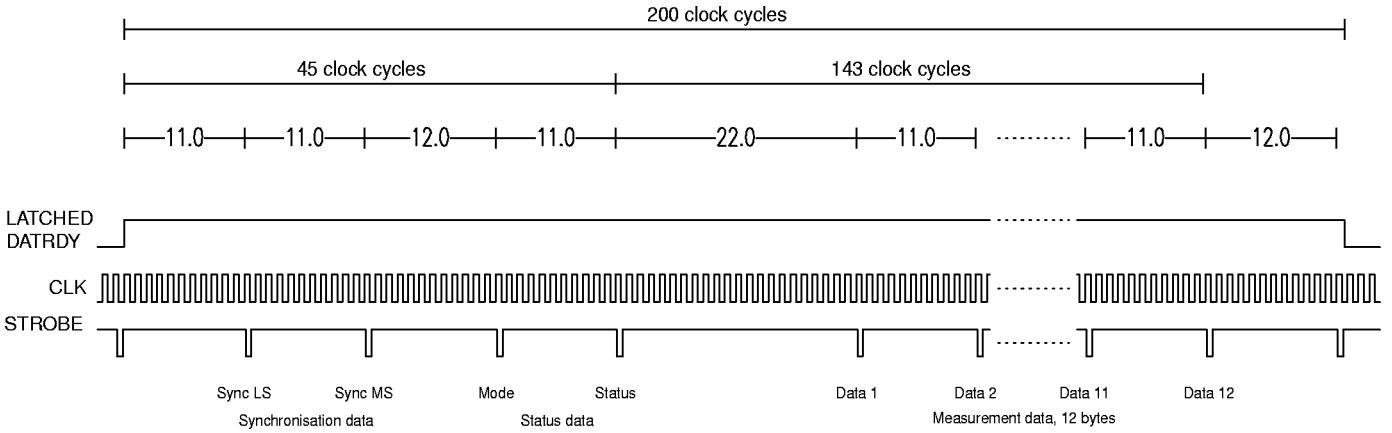


The contents of the status byte equals the content of the external Status bus as described in the section “Status Information” on page 17.

In the beginning of I/O operation, AT73C500 writes a high pulse to B9 pin of the Status bus (ADDR0). This pin can be externally latched to lengthen the pulse over the whole output operation. It can be used to generate a data ready (DATRDY) interrupt to processor.

Figure 11 shows the timing of one data package. In nominal conditions, it takes 200 clock cycles to transfer all 16 bytes. A high pulse (DATRDY) is written to bit B9 (SMBUS1) of Status bus 11 clocks before the first byte is available and low pulse 12 clocks after the last byte has been sent.

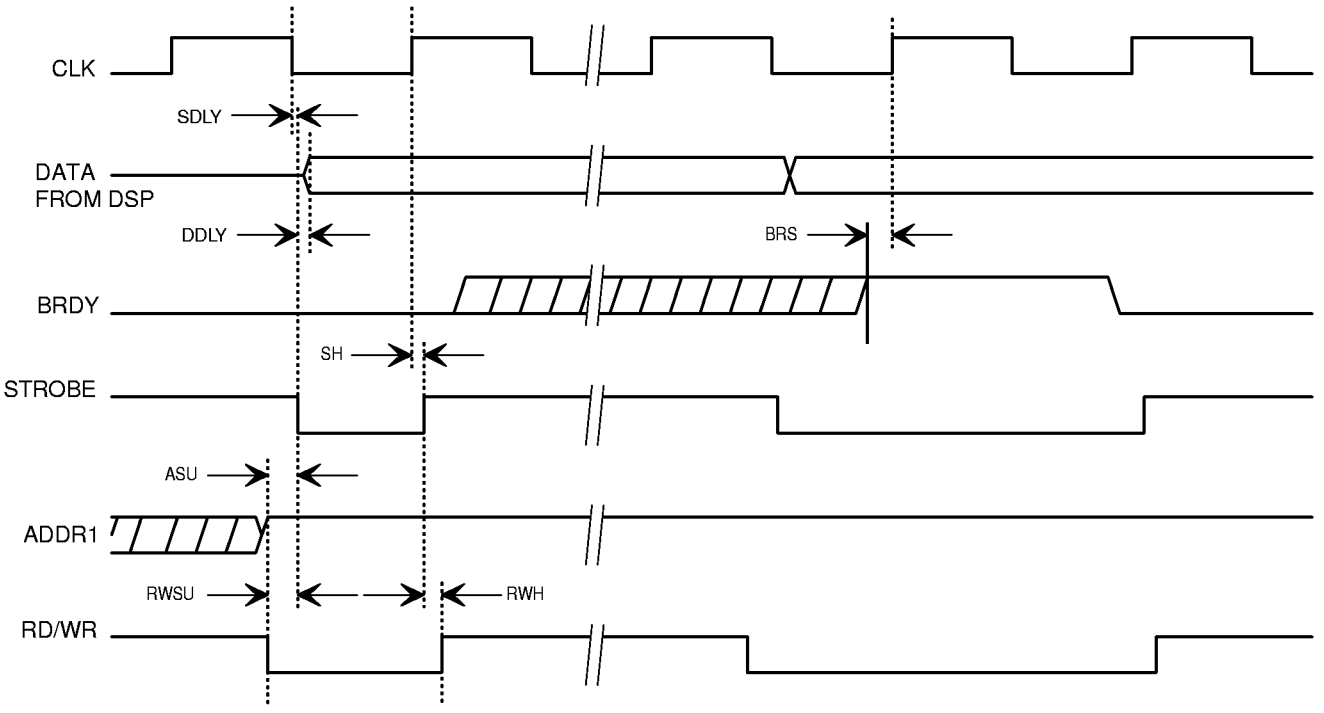
Figure 11. Contents of a data package



AT73C500 offers some time for the processor to analyze the synchronization, status and mode information before starting to supply the measurement results. The 12 measurement bytes are written on every 11th clock period.

Four handshake signals are provided, ADDR1, RD/WR, STROBE and BRDY, for interfacing with the microprocessor. ADDR1 is always taken high when AT73C500 is either writing to µP bus or reading the bus contents. When used with slow peripheral, the BRDY input of AT73C500 can be used to hold the device in write mode until the processor has finished reading the bus. However, the total length of one data package should always be less than 300 clock cycles of AT73C500. Longer I/O periods may result erroneous measurement results.

Figure 12. Handshake signals of the DSP



Following the falling edge of BRDY, the data can be strobed into the µP by the rising edge of the STROBE signal. If the microprocessor is able to read data continuously, BRDY can be kept constantly low. Also BRDY should be low whenever DATRDY is inactive allowing AT73C500 freely use its buses.

To avoid conflicts, the processor should always keep its bus in tri-state mode, unless it is used to write calibration coefficients to AT73C500.

Status Information

AT73C500 provides the following status information through the Status bus of AT73C500 (B8 - B15, ADDR0).

Status Bus Bit	Status Flag	Meaning
B15	TAMP	High: Potential event of tampering detected
B14	STUP	High: Current of all phases below starting level
B13	L3	High: Phase 1 voltage above 10% of full-scale
B12	L2	High: Phase 2 voltage above 10% of full-scale
B11	L1	High: Phase 3 voltage above 10% of full-scale
B10	FAIL	High: Operating error detected
B9	DATRDY	High: Data available on the µP bus
B8	INI	Low: AT73C500 in initialization phase, EEPROM interface in use, AT73C501 (or AT73C502) interface disabled

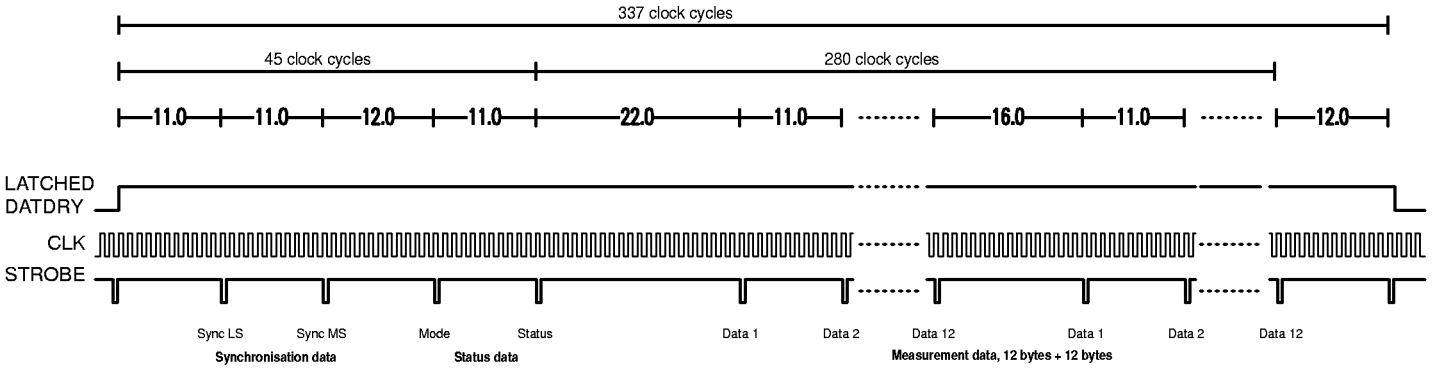
High level of Lx flags indicates that a phase voltage is above 10% level of the full scale voltage. If a voltage drop is detected, the corresponding status bit is written low. AT73C500 is continuously monitoring the voltage of each phase.

FAIL flag signifies that something abnormal has been detected. The following situations may cause a high level of FAIL: read operation of calibration coefficients is not successful, the serial bus of AT73C501 or AT73C502 is not working properly, the measurement results can't be transferred to microprocessor, AT73C500 has detected an internal failure.

If any of the calibration coefficients and corresponding back-up values do not match, AT73C500 performs two extra read operations to eliminate the possibility of a transfer error. If the error still exists after the third trial, incorrect coefficients are replaced by the default values. FAIL flag is activated indicating that a potential error has been detected. FAIL is also taken high in case it is not possible to read calibration coefficients from the µP or EEPROM, or if the processor supplies too few coefficients. In both cases, the read operation will finish in a time-out situation.

The voltage monitoring block of AT73C501/AT73C502 is used to detect voltage interruptions before the supply voltage of AT73C500 drops. High level of PFAIL output at the ADC indicates a voltage break situation. The measurement results supplied by AT73C501/AT73C502 may be erroneous, and AT73C500 and microprocessor has to be prepared for supply voltage interruption. A high level of PFAIL causes an immediate write of data packages 3 and 4 (accumulated energy information) to processor bus. The timing of this operation is presented in Figure 13. There are 16 clocks between the two 12 byte data packages but the header bytes are not repeated in the beginning of package 4.

Figure 13. Transfer of billing information to processor following a PFAIL interrupt



In case of an imminent voltage break, the microprocessor stores the energy values into a non-volatile memory. The devices can operate for a short period of time powered by an electrolytic capacitor or by battery back-up.

AT73C500 devices are taken to a soft reset state and normal operation will be recovered after the supply voltage is high again. About one line cycle is needed to start normal measurements. During this initialization phase no calculations are performed.

STUP output (active high) indicates that the current of each of the three phases is below the specified starting level and no energy is accumulated. This status flag is very useful during the calibration of a meter since immediate feedback about staring current level is provided.

TAMP flag informs about potential tampering. It is activated if one or more phase currents are zero or negative. Therefore it very effectively indicates current transformer reversal or short-circuit.

Impulse Outputs

AT73C500 provides eight impulse outputs, four meter constant outputs and four pulse outputs to drive electromechanical display counters which can register exported and imported active energy and capacitive and inductive reactive energy. These outputs use the same output lines as used for the processor interface. Impulses are combined with address 0 (ADDR0). The table below shows the impulse outputs available in modes 1 and 3. Mode 7 offers the same outputs, but the rate of the display pulses is 10imp/kWh (kVArh).

Table 8. Impulse Outputs in Operating Modes 1 and 3

Output Bit	Impulse	Output Type	Impulse Rate
B7	- VArh	Meter Constant	1250imp/kVArh
B6	+ VArh	Meter Constant	1250imp/kVArh
B5	- Wh	Meter Constant	1250imp/kWh
B4	+ Wh	Meter Constant	1250imp/kWh
B3	+ Wh	Display	100imp/kWh
B2	- Wh	Display	100imp/kWh
B1	+ VArh	Display	100imp/kVArh
B0	- VArh	Display	100imp/kVArh

An external register is needed to latch and buffer the pulses. The register can further drive both electromechanical display counters and LEDs. In modes 1 to 4, the nominal pulse rate of display outputs is 100imp/kWh or 100imp/kVArh (U_{MAX} = 270V, I_{MAX} = 80A) and meter constant outputs 1250imp/kWh (1250imp/kVArh). The length of each display pulse is 117ms when operated from 3.2678 MHz crystal. Meter constant pulse stays high for 20 ms.

If the devices are used in a 5A meter, current inputs can be scaled to 8A full scale level. In this case, the nominal impulse rates are ten times higher than the above values.

Multi-channel Mode

Modes 2 and 4 are reserved for multi-channel operation. In these modes, the chips operate like three independent single phase meters and store the calculation results in separate registers phase-by-phase (meter-by-meter). The basic sequence of operation is otherwise similar to the normal mode.

Impulse Outputs

In multichannel operation three impulse outputs are available for display counters. The absolute energy value is measured and the reversal of current flow doesn't affect to pulse rates. The FAIL signal can, however, be used to determine whether the energy being registered is positive or negative. Meter constant pulse rate corresponds to total active energy of the three single phase channels summed together as shown in the table below.

Output Bit	Impulse	Output Type	Impulse Rate
B7	Not Used	Not Used	-
B6	Not Used	Not Used	-
B5	Not Used	Not Used	-
B4	± Wh	Meter Constant Sum of all 3 channels	1250imp/kWh
B3	± Wh	Display, Channel 1	100imp/kWh
B2	± Wh	Display, Channel 3	100imp/kWh
B1	± Wh	Display, Channel 2	100imp/kVArh
B0	Not Used	Not Used	-

Test Mode

This mode can be used for initial calibration purposes or in a special meter for additional processing of sample data. In this mode, AT73C501/AT73C502 samples the six inputs normally and transfers the samples to AT73C500, which performs DC suppression and further writes the samples to 8-bit processor bus together with header bytes in the following sequence.

Byte	Contents
1	Sync LS byte
2	Sync MS byte
3	Mode Byte
4	Status Byte
5,6	I1, LS byte and MS byte
7,8	U1, LS byte and MS byte
9,10	I2, LS byte and MS byte
11,12	U2, LS byte and MS byte
13,14	I3, LS byte and MS byte
15,16	U3, LS byte and MS byte

Several input combinations can be measured to check the gain and phase error in different conditions. An interfacing computer can be programmed to calculate the calibration coefficients based on the samples supplied by AT73C500. At the end of the calibration, the coefficients have to be stored in a non-volatile memory of the meter as described in "Loading of Calibration Coefficients" on page 19.

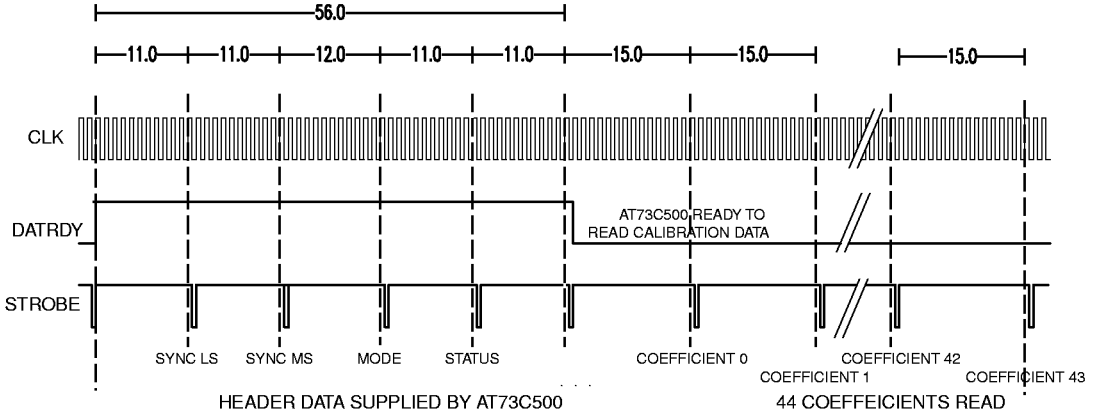
Calibration

The calibration coefficients always have to be loaded into AT73C500 registers after reset state. The coefficients are either read from an external EEPROM or supplied by a microprocessor via the 8-bit bus.

Loading of Calibration Coefficients

In modes 3 and 4, a microprocessor takes care that the coefficients are kept in a non-volatile memory during voltage break. After the voltage break, the DSP first writes the four header bytes, Sync LS, Sync MS, mode and status information on the µP bus and then starts waiting for the calibration data. The processor reads the status and mode and after that writes the coefficients on the bus. The contents of AT73C500 header bytes is described in "Data Transfer to External Microprocessor" on page 12 and "Status Information" on page 17.

Figure 14. Timing of calibration coefficient read operation



Before using the µP bus, AT73C500 writes a short pulse (DATRDY) to B9 bit of the Status bus combined with high level of address 0 (ADDR0 output). This bit can be taken directly or through an external latch to the interrupt input of the processor. After writing the status and mode bytes, AT73C500 goes to a read mode and starts waiting for calibration coefficients from the µP. Processor supplies the coefficients as 8-bit bytes one after another. The timing of this sequence is presented in Figure 14.

Nine gain calibration, six offset calibration and three phase calibration coefficients are read into the AT73C500 memory. At the same time, a scaling factor for the display pulse rate and an adjustment value for starting current is stored.

To minimize the risk of erroneous calibration values, a back-up value of each coefficient is also transferred by the microprocessor or from the ROM. The back-up value has to be written as 2's complement binary number of the actual calibration figure.

The calibration data is transferred in the following sequence:

Byte	Calibration Coefficient	Byte	Calibration Coefficient
0	PC1	1	PC1 back-up
2	PC2	3	PC2 back-up
4	PC3	5	PC3 back-up
6	MCC	7	MCC back-up
8	Not used	9	Not used
10	AGC1	11	AGC1 back-up
12	AGC2	13	AGC2 back-up
14	AGC3	15	AGC3 back-up
16	RGC1	17	RGC1 back-up
18	RGC2	19	RGC2 back-up
20	RGC3	21	RGC3 back-up
22	UGC1	23	UGC1 back-up
24	UGC2	25	UGC2 back-up
26	UGC3	27	UGC3 back-up
28	STUPC	29	STUPC back-up
30	AOF1	31	AOF1 back-up
32	AOF2	33	AOF2 back-up
34	AOF3	35	AOF3 back-up
36	ROF1	37	ROF1 back-up
38	ROF2	39	ROF2 back-up
40	ROF3	41	ROF3 back-up
42	OFFMOD	43	OFFMOD back-up

The meaning of the calibration coefficient mnemonics are as follows:

Mnemonic	Meaning
PC_N	Phase calibration factor, phase N
MCC	Display pulse adjustment factor for active and reactive energy
AGC_N	Gain calibration factor for active power and energy calculation, phase N
RGC_N	Gain calibration factor for reactive power and energy calculation, phase N
UGC_N	Gain calibration factor for phase voltage, phase N
STUPC	Starting current adjustment factor
AOF_N	Offset calibration factor for active power and energy calculation, phase N
ROF_N	Offset calibration factor for reactive power and energy calculation, phase N
OFFMOD	Controls the use of offset factors

AT73C500 provides four handshaking signals, ADDR1, RD/WR, STROBE and BRDY, for interfacing with the microprocessor. Microprocessor can use the BRDY input of AT73C500 to extend the read and write cycles. AT73C500 stays in the read or write mode as long as BRDY is high. BRDY is sampled at the rising edge of AT73C500 master clock. As soon as BRDY goes low, the read/write cycle of AT73C500 will end at the first rising edge of CLK clock. During read operation data is latched into AT73C500 register on the rising edge of the STROBE signal following the low level of BRDY. A more detailed description about the handshake signals is presented in section "Data Transfer to External Microprocessor" on page 12.

Fifteen idle cycles are inserted by AT73C500 between the read operation of each calibration byte. This allows the processor to prepare the next coefficient for transfer or to raise the BRDY signal in case it is not ready to write the following byte. If the data is available, BRDY can be kept constantly low. Microprocessor has to always supply all 44 calibration bytes even though some of those may be zero and don't affect to measurement results.

If AT73C500 detects an error when comparing the calibration data and corresponding back-up values, it writes the DATRDY bit high and after that the header bytes on processor bus indicating that it is still in initialization routine and wishes to get the calibration data to be transported once again. If the error still exists after the third trial, AT73C500 notifies the situation by a FAIL status bit and starts normal operation, discarding potentially incorrect calibration coefficients.

If AT73C500 is programmed to mode 1 or 2, the coefficients are stored in an EEPROM of type AT93C46. The ROM has to support communication through a three pin serial I/O port. The serial ROM interface uses the same port, which also connects AT73C500 to AT73C501/AT73C502 sample output. During the initialization phase, the ADC interface has to be disabled. This can be done by B8 bit of AT73C500 Status bus (ADDR0). The output has to be latched by an external flip-flop to keep the state over the whole initialization period. The same output can be used as Chip Select input for the EEPROM. AT73C500 reads, checks and stores automatically all 44 calibration coefficients. After that, B8 bit of Status byte is written low and normal measurement can start. If the EEPROM contains erroneous data and one or more coefficients don't match with their back-up values, the same procedure is followed as in the processor mode.

Gain Calibration

Gain calibration is used to compensate the accumulated magnitude error of voltage dividers, current transformers and A/D converters. There is a separate 8-bit gain calibration coefficient for each phase, and for active and reactive energy measurement. A similar formula is also used to calibrate the phase voltage values, only the calibration range is different, 20% for power and 8% for voltage. These calibrations will automatically correct the gain error of other measurement parameters.

The following calculations are done to get the calibrated results. For active power:

$$P_N = P_N \times \left(1 + 0.2 \times \frac{AGC_N}{128}\right)$$

where PN is the active power of phase N and AGC_N is the gain calibration factor of that phase. The valid range for AGC_N is -128 to +127. Similarly, for reactive power:

$$Q_N = Q_N \times \left(1 + 0.2 \times \frac{RGC_N}{128}\right)$$

where QN is the reactive power of phase N and RGC_N is the gain calibration coefficient for that phase. RGC_N valid range is -128 to +127.

Gain calibration performed on voltage measurements are:

$$U_N = U_N \times \left(1 + 0.08 \times \frac{UGC_N}{128}\right)$$

where UN is the line voltage of phase N and UGC_N is the corresponding gain calibration coefficient, ranging from -128 to +127.

Apparent power and current are automatically gain adjusted to match the calibrated settings of active power, reactive power and voltage.

Offset Calibration

The low current response of current sensors is often more or less non-linear. The error caused by this non-linearity can be compensated by a small offset factor which is added in power results. Offset calibration is done for active and reactive power, separately for each phase. The following formulas are used:

$$P_N \equiv P_N + \frac{AOF_N}{128} \times 0.004157 \times \text{sign}(P_N) \times P_{FS}$$

and

$$Q_N = Q_N + \frac{ROF_N}{128} \times 0.00457 \times \text{sign}(Q_N) \times Q_{FS}$$

where P_N and Q_N are the active and reactive power for phase N, AOF_N and ROF_N are the respective offset calibration coefficients and P_{FS} and Q_{FS} are the corresponding full

scale values of the powers. The nominal full-scale values are:

$$P_{FS} = 270V \times 80A = 21.6kW$$

$$Q_{FS} = 270V \times 80A = 21.6VAr$$

The valid range for the offset calibration factors is -128 to +127.

The scale of offset calibration for active and reactive power is different, 89W versus 98VAr in nominal conditions of 270V maximum phase voltage and 80A maximum phase current. Typically, a small offset factor of a few watts is enough to compensate the non-linearity of current sensing. It should be noted that offset calibration will also affect the starting current level of a meter. If the full scale current or voltage is changed to a non-default value, the range for offset calibration will be scaled accordingly.

The same offset value is used independent of phase angle. However, as default (OFFMOD=0), the sign of power is taken into account in the calculations so that positive offset factor will always increase the absolute power value and negative coefficient will decrease absolute results. This guarantees that current sensor non-linearity is corrected in the same way even though the current flow is reversed.

It is possible to change this default condition by programming value one to OFFMOD coefficient. In this case, offset coefficient will be always added to power result without checking the sign of the power. Positive coefficient will increase the absolute value of positive power results and decrease the absolute value of negative result.

Phase Calibration

The phase difference between voltage and current channel is compensated with three 8-bit phase calibration figures. The displacement is usually due to the phase shift in current transformers. Based on the calibration values, the DSP interpolates new current samples with sample instants coinciding with the corresponding voltage samples. The following formula is used to determine the phase offset to be used in the interpolation. One 8-bit phase calibration value is stored for each of the three phases.

$$PO_N = \frac{PC_N}{128} \times 5.625°$$

where PO_N is the sample phase offset of channel N, measured as phase(U) - phase (I). The allowed range for phase calibration factor, PC_N, is -128 to +127.

Starting Current Adjustment

The meter IC is designed to fulfill IEC 1036, class 1 specification. This specification is based on a certain basic current, I_b. As a default, AT73C500 operates with 5A basic current. The chipset has a preprogrammed starting current level of

$$I_{SU} = \frac{1}{4000} \times I_{FS}$$

where I_{FS} is the full scale current of the meter, i.e. 80A in nominal conditions. The default startup current corresponds to 0.4% of the 5A I_b, assuming that the full-scale range is 80A. When the phase current is below the starting level, the calculated cycle power results are replaced by zeros and no energy is accumulated.

It is possible to adjust the start-up level in the range of 0.2 to 10 compared with the nominal value. This is performed with a special calibration factor. The following formula is used to determine the current:

$$I_{SU} = \frac{1}{4000} \times I_{FS} \times (1 + 0.2 \times STUPC)$$

where STUPC is the starting current calibration factor, allowed to vary in range -4 to +45, only. Care should be taken that the STUPC is correctly programmed and is not beyond -4 to 45 range. Also, it should be noted that low starting thresholds may force the device to a level where accuracy is restricted due to a finite resolution of converters and mathematics.

Adjustment of Display Pulse Rate

An 8-bit byte is provided for adjustment of the impulse rate of display pulses. This coefficient will only affect the display pulse rate of active and reactive energy but not to the meter constant rate. The content of all measurement registers will remain unchanged.

The impulse rate can be scaled in the range of 1 to 6 compared to the nominal value. In default conditions (U_{max} = 270V, I_{max} = 80A) the LSB of energy registers REG12-15 (See “Status Information” on page 17.) corresponds to 0.4Wh. This means that accumulated 25 LSBs of energy will generate one pulse to the display pulse output (25 x 0.4Wh/impulse = 10 Wh/impulse = 100 impulses/kWh).

By using MCC calibration coefficient, the nominal figure 25 can be changed in the range of 25 to 152. MCC may range from 0 to 127, only. The following formulas are used to calculate the impulse rate.

$$IMP = (25 + MCC) \times E_{LSB}$$

and

$$PR = \frac{1000}{(25 + MCC) \times E_{LSB}}$$

where ELSB is the energy value of one LSB in the energy register, 0.4Wh in default conditions. When the meter is operated in non-standard conditions, the energy LSB may be recalculated as:

$$E_{LSB} = \frac{3.2768MHz}{f} \times \frac{U_{FS} \times I_{FS}}{270V \times 80A} \times 0.4Wh$$

where f is the clock frequency used, and U_{FS} and I_{FS} are the full-scale values of voltage and current.

In case the meter is used with a non-default voltage divider or current sensor, MCC factor is a convenient way to readjust the impulse rate.

Example

The meter is to be configured for use in 120V networks, with a maximum line voltage of 140V. The display pulse rate is required to remain at 100imp/kWh. To start off, the front end of the meter must be configured for the new line voltage. The voltage dividers must be configured to produce an input signal of 0.707V at the input of the ADC at maximum line voltage. At nominal meter settings, the voltage divider ratio is 270V:0.707V, in this case it must be 140V:0.707V.

Note that adjusting the line voltage of the meter will render the formatting of most calculation registers to alternative settings. For example, the meter constant pulse rate will change as follows:

$$MC = \frac{270V \times 80A}{U_{FS} \times I_{FS}} \times \frac{f}{3.2768MHz} \times 1250 \frac{imp}{kWh}$$

In our case of a meter for 120V networks, the new meter constant pulse rate would be:

$$MC = \frac{270V}{140V} \times 1250 \frac{imp}{kWh} = 2410.714\ldots \frac{imp}{kWh}$$

To make the meter constant pulse rate to an even number, for example 2500, we may choose to either re-scale the line voltage or scale the maximum line current. 2500 impulses per kilowatt hour is gained by either setting the maximum line voltage to:

$$U_{FS} = \frac{270V}{2500 \frac{imp}{kWh}} \times 1250 \frac{imp}{kWh} = 135V$$

or by retaining the line voltage at 140V and scaling the maximum line current to:

$$I_{FS} = \frac{270V \times 80A}{140V \times 2500 \frac{imp}{kWh}} \times 1250 \frac{imp}{kWh} = 77.143\ldots A$$

Regardless of which parameter (or both) is chosen, the scaling process is a simple matter of gain calibration. If, for example, the line voltage is chosen to be rescaled to 135V, this is realized with a resistor divider of half the nominal, and finetuning using the voltage gain coefficients. Also, all values resulting from voltage calculation, such as the data transferred via energy registers, should be normalized with respect to the new voltage setting.

Going back to the calibration of the display pulse rate, the new LSB value of energy registers is:

$$E_{LSB} = \frac{140V}{270V} \times 0.4Wh = 0.20741\ldots Wh$$

To maintain the display pulse rate at 100, the MCC calibration coefficient must be programmed as:

$$MCC = \frac{1000}{PR \times E_{LSB}} - 25 = \frac{1000}{100 \frac{imp}{kWh} \times 0.20741Wh} - 25 = 23.216\ldots \approx 23$$

The energy value of each display counter impulse is thereafter:

$$IMP = (25 + 23) \frac{1}{imp} \times \frac{140V}{270V} \times 0.4Wh \approx 10.0 \frac{Wh}{imp}$$

In mode 7, the default display pulse rate is 10 impulses/kWh(kVArh) instead of 100 impulses/kWh. This is convenient for meters where only one decimal digit wants to be shown. This default rate can also calibrated and the calibration formulas are:

$$IMP = (250 + MCC) \times E_{LSB}$$

and

$$PR = \frac{1000}{(250 + MCC) \times E_{LSB}}$$

Master Clock

The master clock of AT73C500 is generated by a crystal oscillator with crystal connected between pins XI and XO of AT73C501/AT73C502. Master clock can also be fed to the XI input from a separate clock source. The system clock rate of AT73C500 is the same as the clock of AT73C501/AT73C502 and is fed to the CLK input of the device from the CLK output of AT73C501/AT73C502.

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit
Supply Voltage V_{CC}, V_{DA}, V_{DDA}	4.75		5.25	V
Input Voltage, Digital	-0.3		V_{DD} +0.3	V
Input Voltage, Analog	-0.3		V_{DA} +0.3	V
Input Voltage, CI and VI inputs	1.25		3.75	V
Ambient Operating Temp.	-25		+70	C
Storage Temperature	-65		+150	C

Calibration Characteristics

Parameter	Min	Typ	Max	Units
Gain Calibration				
Calibration Range ±		20		%
Calibration Resolution		0.16		%
Phase Calibration				
Calibration Range ±		5.625		degree
Calibration Resolution		0.044		degree
Offset Calibration, Active Power				
Calibration Range		89.8		W
Calibration Resolution		0.7015		W
Range,% of Full Scale Phase Power		0.4157		%
Offset Calibration, Reactive Power				
Calibration Range		98.7		VAr
Calibration Resolution		0.7712		VAr
Range,% of Full Scale Phase Power		0.457		%

Measurement Accuracy

The accuracy measurements are based on the usage of the AT73C500 DSP with the single-ended ADC, AT73C501. Using the differential-ended ADC, AT73C502, improves some of the results.

Input Conditions

When specifying measurement accuracy, it is assumed that $80A_{RMS}$ phase current will produce $2V_{PP}$ full scale input voltage to current converters. The basic current, I_B, is supposed to be $5A_{RMS}$.

The nominal phase voltage, U_N, is specified to be $230V_{RMS}$ and $2V_{PP}$ full scale input is produced by $270V_{RMS}$.

Overall Accuracy, Active and Reactive Power and Energy Measurement

Overall accuracy including errors caused by A/D-conversion of current and voltage signals, calibration and calculations.

The accuracy figures are measured in nominal conditions unless otherwise indicated in the parameter field of the table below.

Parameter	Nominal Value
Nominal voltage, U_N	230V, ±1%
Full-scale voltage, U_{FS}	270V
Full-scale current, I_{FS}	80A
Base current, I_B	5A
Frequency, f	50.0 Hz, ±0.3%
Power factor, PF	1
Harmonic contents of voltage	less than 2%
Harmonic contents of current	less than 20%
Temperature, T	23°C, ±2°C
AT73C500 master clock	3.2768 MHz

The measurements are done according to IEC1036 specification. The results are averaged over a period of 10s. Before measurements, AT73C500 devices have been operational for minimum 1h.

Table 9. Measurement Bandwidth

Parameter	Min	Typ	Max	Units
General, 50 Hz line frequency				
- high limit (-3dB)	750			Hz
- low limit (-3dB)			30	Hz
Reactive Power and Energy, Voltage and Current Measurement				
- high limit	360			Hz
- low limit			40	Hz
Line Frequency				
- high limit	350			Hz
- low limit			20	Hz

Table 10. Maximum Error

Current	Voltage	Power Factor	Min	Typ	Max	Units
$0.05I_B$	U_N	1.000	-0.4		+0.4	%
$0.1I_B...I_{FS}$	U_N	1.000	-0.2		+0.2	%
$0.1I_B$	U_N	0.5 lagging	-0.4		+0.4	%
$0.2I_B...I_{FS}$	U_N	0.5 lagging	-0.4		+0.4	%
$0.1I_B$	U_N	0.8 leading	-0.4		+0.4	%
$0.2I_B...I_{FS}$	U_N	0.8 leading	-0.4		+0.4	%
$0.2I_B...I_{FS}$	U_N	0.25 lagging	-1.0		+1.0	%

Effect of Crosstalk

The error caused by crosstalk from one current input to other two current inputs when the meter is carrying a single-phase load.

Table 11. Single-phase Load Error

Current	Voltage	Power Factor	Min	Typ	Max	Units
$0.1I_B...I_{FS}$	U_N	1.000	-0.5		+0.5	%
$0.1I_B...I_{FS}$	U_N	0.5 lagging	-0.5		+0.5	%

Influence Quantities

The additional error caused by different influence quantities.

Table 12. Voltage Variation Error

Current	Voltage	Power Factor	Min	Typ	Max	Units
$0.1I_B$	$0.9U_N...$ $1.1U_N$	1.000	-0.2		+0.2	%
$0.1I_B$	$0.9U_N...$ $1.1U_N$	0.5 lagging	-0.2		+0.2	%

Table 13. Frequency Variation Error

Frequency	Current	Voltage	Power Factor	Min	Typ	Max	Units
$0.95f_N...1.05f_N$	$0.1I_B$	U_N	1.000	-0.2		+0.2	%
$0.95f_N...1.05f_N$	$0.1I_B$	U_N	0.5 lagging	-0.2		+0.2	%
$0.8f_N...5f_N$	$0.1I_B$	U_N	1.000	-5.0		+0.5	%
$0.8f_N...5f_N$	$0.1I_B$	U_N	0.5 lagging	-5.0		+0.5	%

Table 14. Harmonic Distortion Error

Current	Voltage	Min	Typ	Max	Units
40% of 5^{th} harmonic in current	10% of 5^{th} harmonic in voltage	-0.5		+0.5	%

Table 15. Reversed Phase Sequence Error

Current	Voltage	Min	Typ	Max	Units
$0.1I_B$	U_N	-0.3		+0.3	%

Table 16. Voltage Unbalance Error

Current	Voltage	Min	Typ	Max	Units
$0.1I_B$	One or two phases carry 0V	-0.4		+0.4	%

Table 17. DC Component in Current Error

Current	Voltage	Min	Typ	Max	Units
$I_{DC} = 0.1I_{FS}$	U_N	-0.5		+0.5	%

Starting Current

As default, the starting current is based on 5A basic current and 80A full scale current range.

Table 18. Starting Current

Voltage	Min	Typ	Max	Units
U_N			0.004	IB

Temperature Coefficient

Measured with the internal reference voltage source of AT73C501/AT73C502.

Table 19. Mean Temperature Coefficient

Current	Voltage	Power Factor	Min	Typ	Max	Units
$0.1I_B...I_{FS}$	U_N	1.000		0.02	0.04	%/K
$0.1I_B...I_{FS}$	U_N	0.5 lagging		0.02	0.04	%/K

Other Parameters

The accuracy of the following parameters is measured in the conditions below unless otherwise indicated in the parameter field of the table. The measurement error has been calculated based on values averaged over 1min period.

Parameter	Nominal Value
Nominal voltage, U_N	230V, ±1%
Full-scale voltage, U_{FS}	270V
Full-scale current, I_{FS}	80A
Base current, I_B	5A
Frequency, f	50.0 Hz, ±0.3%
Power factor, PF	1
Harmonic contents of voltage	0%
Harmonic contents of current	0%
Temperature, T	23C, ±2°C
AT73C500 master clock	3.2768 MHz

Table 20. Apparent Power and Energy Error

Current	Min	Typ	Max	Units
$0.05I_{FS}...I_{FS}$	-0.5		+0.5	%
$0.005I_{FS}...0.05I_{FS}$	-2.0		+2.0	%
$0.001I_{FS}...0.005I_{FS}$	-5.0		+5.0	%

The accuracy of Power Factor measurements was tested with PF values 0.5, -0.5, -1 and 1.

Table 21. Power Factor Error

Current	Min	Typ	Max	Units
$0.05I_{FS}...I_{FS}$	-0.5		+0.5	%
$0.005I_{FS}...0.05I_{FS}$	-2.5		+2.5	%

Table 22. Phase Voltage Error

Voltage	Min	Typ	Max	Units
$0.2U_{FS}...U_{FS}$	-0.5		+0.5	%

Table 23. Phase Current Error

Current	Min	Typ	Max	Units
$0.05I_{FS}...I_{FS}$	-0.5		+0.5	%
$0.005I_{FS}...0.05I_{FS}$	-2.5		+2.5	%

Table 24. Frequency Error

Frequency	Min	Typ	Max	Units
40 Hz...100 Hz	-0.5		+0.5	%

Digital Characteristics

V_{DD} = 5V, V_{DA} = 5V

Parameter	Min	Typ	Max	Units
High-Level Input Voltage	4.0			V
Low-Level Input Voltage			1.0	V
High-Level Output Voltage, I_{SOURCE} = -100 µA	4.0			V
Low-Level Output Voltage, I_{SINK} = 0.5 mA		0.4		V
Input Leakage Current	-10		10	µA

Crystal Oscillator

Parameter	Min	Typ	Max	Units
Crystal Frequency	1.0		6.0	MHz
Crystal Inaccuracy			30	ppm
Crystal Temp Coefficient (-25°C to +70°C)			30	ppm/C

AC Parameters

Parameter	Min	Typ	Max	Units
Master Clock Frequency	1.0		6.0	MHz
Clock Duty Cycle at XI pin	40		60	%

Timing of 8-bit Bus

Parameter	Parameter	Min	Typ	Max	Units
DDLY	Data Delay from Falling Edge of STROBE			25	ns
DH	Data Hold Time From Rising Edge of STROBE	5			ns
SDLY	Strobe Delay from Falling Edge of Clock	0		20	ns
SH	Strobe Hold Time From Rising Edge of Clock	3		20	ns
ASU	Addr Setup Time to Rising Edge of STROBE	10			ns
AH	Addr Hold Time From Rising Edge of STROBE	3			ns
RWSU	RD/WR Setup to Rising Edge of STROBE	10			ns
RWH	RD/WR Hold from Rising Edge of STROBE	3			ns
BRS	BRDY Set-Up Time to Rising Edge of Clock	40			ns

Power Supply Characteristics

Parameter	Parameter	Min	Typ	Max	Units
V_{DD}, V_{DA}	Supply Voltage	4.75		5.25	V
I_{DD} (AT73C501/AT73C502 + AT73C500)	Supply Current		15	22	mA
I_{DA} (ADC)	Supply Current		10	15	mA
A_{GND}	Analog Ground Voltage	2.45	2.5	2.55	V
V_{REF}-A_{GND}	Reference Voltage	1.17	1.27	1.37	V

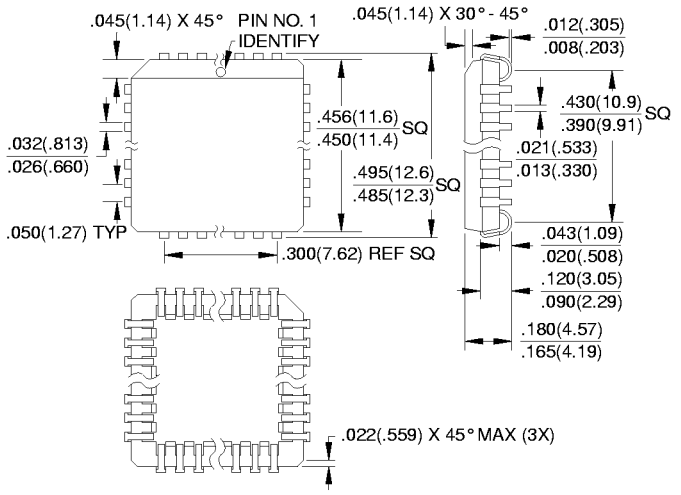
Ordering Information

Ordering Code	Package	Operation Range
AT73C500-JC	44J	Commercial (0°C to 70°C)
AT73C501-JC	28J	Commercial (0°C to 70°C)
AT73C502-QC	44Q	Commercial (0°C to 70°C)

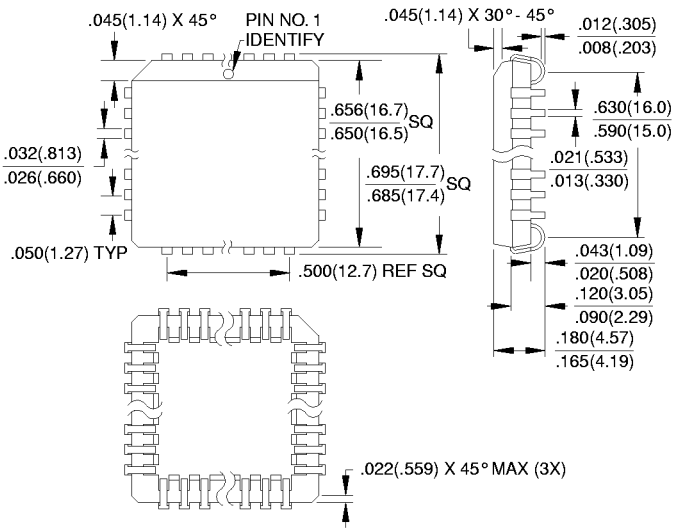
Package Type	
28J	28-lead, Plastic J-leaded Chip Carrier (PLCC)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
44Q	44-lead, Plastic Gull Wing Quad Flat Package

Packaging Information

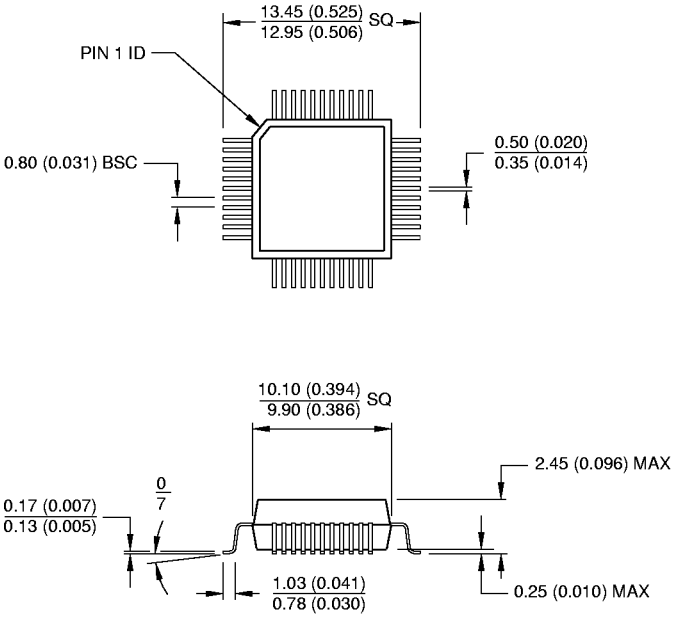
28J, 28-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AB



44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC



44Q, 44-lead, Plastic Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-022 AB



*Controlling dimension: millimeters