



5V, 1A Linear Regulator with RESET and ENABLE

Description

The CS-8121 is a 5V, 1A precision linear regulator with two microprocessor compatible control functions and protection circuitry included on chip. The composite NPN-PNP output pass transistor assures a lower dropout voltage (1.2V @ 1A) without requiring excessive supply current (4mA).

The CS-8121's two logic control functions make this regulator well suited to applications requiring microprocessor-based control at the board or module level. ENABLE controls the output stage. A high voltage (>2.9V) on the ENABLE lead turns off the regulator's pass transistor and sends the IC into Sleep mode where it draws only

250 μ A. RESET sends a RESET signal when the IC is powering up or whenever the output voltage falls out of regulation. The RESET signal is valid down to V_{OUT} = 1V.

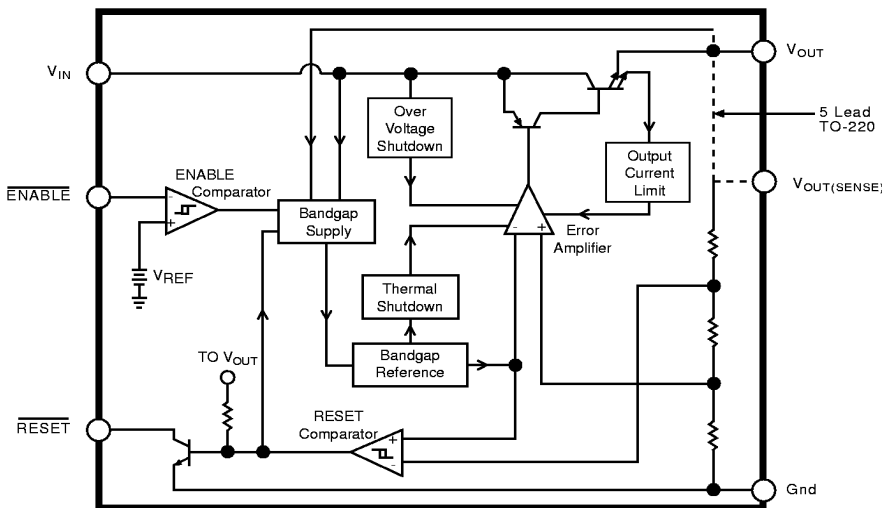
The CS-8121 design optimizes supply rejection by switching the internal bandgap reference from the supply input to the regulator output as soon as the nominal output voltage is achieved. Additional on chip filtering enhances rejection of high frequency transients on all external leads.

The CS-8121 is fault protected against short circuit, over voltage and thermal runaway conditions.

Features

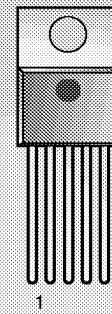
- 5V \pm 4% Output Voltage
- Low Dropout Voltage (1.2V @ 1A)
- Low Quiescent Current (4mA @ I_{OUT} = 1A)
- μ P Compatible Control Functions
RESET
ENABLE
- Low Current Sleep Mode
I_Q = 250 μ A
- Fault Protection
Thermal Shutdown
Short Circuit
60V Peak Transient Voltage

Block Diagram

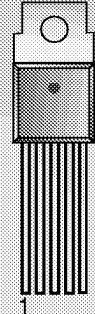


Package Options

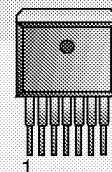
5 Lead TO-220



5 Lead TO-220 Overmolded



7 Lead D²PAK



- | | |
|---|--------------------------|
| 1 | V _{IN} |
| 2 | ENABLE |
| 3 | Gnd |
| 4 | RESET |
| 5 | V _{OUT} |
| 6 | V _{OUT} (SENSE) |
| 7 | V _{OUT} (SENSE) |



Cherry Semiconductor Corporation
2000 South County Trail
East Greenwich, Rhode Island 02818-1530
Tel: (401)885-3600 Fax (401)885-5786
email: info@cherry-semi.com

Absolute Maximum Ratings

DC Input Voltage	-0.7 to 26V
Peak Transient Voltage (46V Load Dump).....	60V
Output Current	Internally Limited
Electrostatic Discharge (Human Body Model)	2kV
Operating, Temperature	-40°C to 125°C
Junction Temperature.....	-40°C to 150°C
Storage Temperatures	-55°C to 150°C
Lead Temperature Soldering	
Wave Solder (through hole styles only)	10 sec. max, 260°C peak
Reflow (SMD styles only)	60 sec. max above 183°C, 230°C peak

Electrical Characteristics: $I_{OUT} = 5\text{mA}$, $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$, $7\text{V} \leq V_{IN} \leq 26\text{V}$, $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ unless otherwise specified

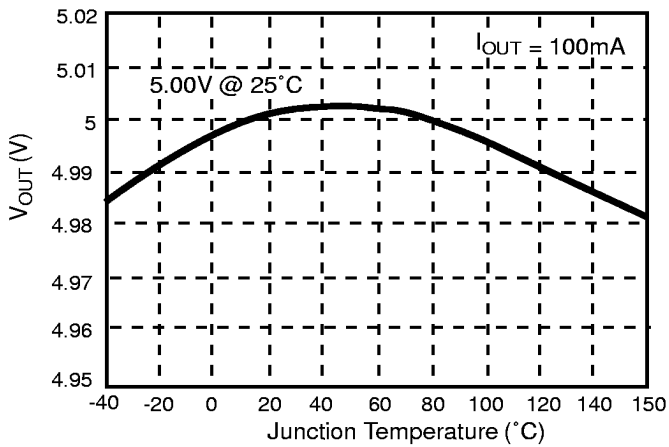
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Output Stage					
Output Voltage, V_{OUT}	$7\text{V} \leq V_{IN} \leq 26\text{V}$, $1\text{mA} \leq I_{OUT} \leq 1\text{A}$	4.8	5.0	5.2	V
Line Regulation	$7\text{V} \leq V_{IN} \leq 26\text{V}$, $I_{OUT} = 5\text{mA}$		0	50	mV
Load Regulation	$5\text{mA} \leq I_{OUT} \leq 1\text{A}$		10	70	mV
Supply Voltage Rejection	$V_{IN} = 14V_{DC} + 1V_{RMS}$ @120Hz, $I_{LOAD} = 50\Omega$	54	70		dB
Dropout Voltage	$I_{OUT} = 1\text{A}$		1.2	1.8	V
Quiescent Current	ENABLE = High, $V_{IN} = 12\text{V}$		0.25	0.65	mA
	ENABLE = Low, $I_{OUT} = 1\text{A}$		4	20	mA
■ Protection Circuits					
Short Circuit Current			1.5		A
Thermal Shutdown		150	190		$^{\circ}\text{C}$
Overvoltage Shutdown		26	40		V
■ RESET					
RESET Saturation Voltage	$1\text{V} < V_{OUT} < V_{RT(OFF)}$, 3.1k Ω pull-up to V_{OUT}		0.1	0.4	V
RESET Output Leakage Current	ENABLE = Low $V_{OUT} > V_{RT(ON)}$, $V_{RESET} = V_{OUT}$		0	25	μA
Power ON/OFF RESET Peak Output Voltage	3.1k Ω pull-up to V_{OUT}		0.7	1.0	V
RESET Threshold ON (V_{OUT} Increasing)			$V_{OUT} - 0.10$	$V_{OUT} - 0.04$	V
RESET Threshold OFF (V_{OUT} Decreasing)		4.75	$V_{OUT} - 0.14$		V
RESET Threshold Hysteresis		10	40		mV
■ ENABLE					
Input High Voltage	$7\text{V} < V_{IN} < 26\text{V}$		2.9	3.9	V
Input Low Voltage	$7\text{V} < V_{IN} < 26\text{V}$	1.1	2.1		V
Input Hysteresis	$7\text{V} < V_{IN} < 26\text{V}$	0.4	0.8	2.8	V
Input Current	$\text{Gnd} < V_{IN(HI)} < V_{OUT}$		0	± 10	μA

Package Lead Description

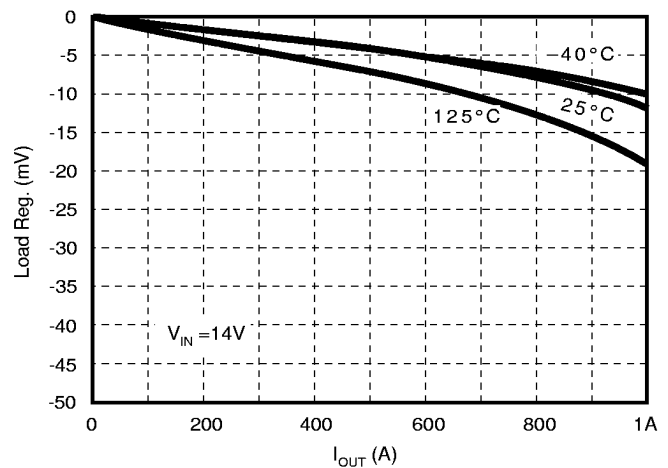
PACKAGE LEAD #		LEAD SYMBOL	FUNCTION
7 Lead D ² PAK	5 Lead TO-220 & Overmolded TO-220		
1		NC	No Connection.
2	1	V _{IN}	Supply voltage to IC, usually direct from the battery.
3	2	ENABLE	CMOS compatible logical. V _{OUT} is disabled i.e. placed in a high impedance state when ENABLE is high.
4	3	Gnd	Ground connection.
5	4	RESET	CMOS compatible output lead. RESET goes low whenever V _{OUT} falls out of regulation. The RESET delay is externally programmed.
6	5	V _{OUT}	Regulated output voltage, 5V (typ).
7		V _{OUT} (SENSE)	Remote sensing of output voltage.

Typical Performance Characteristics

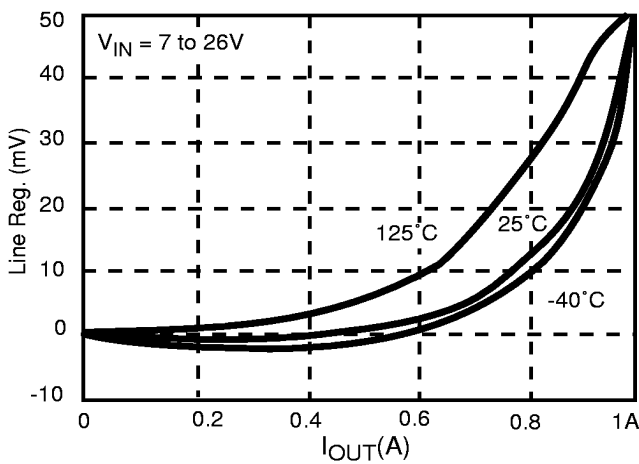
Output Voltage vs. Temperature



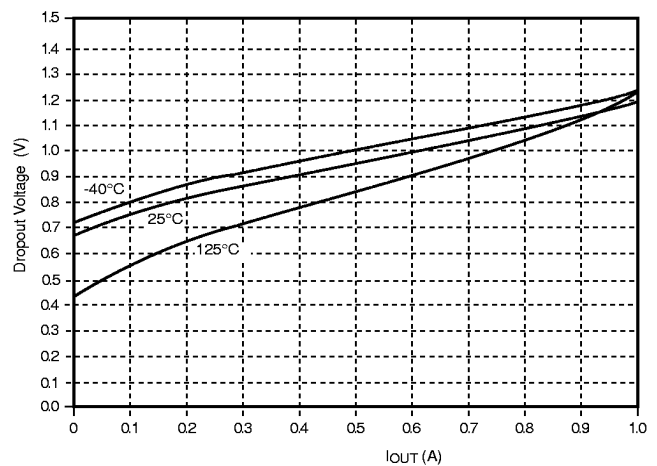
Load Regulation vs. Output Current Over Temperature



Line Regulation vs. Output Current Over Temperature

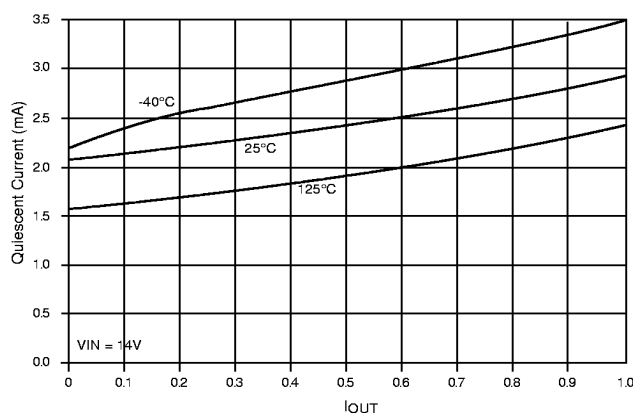


Dropout Voltage vs. Output Current Over Temperature

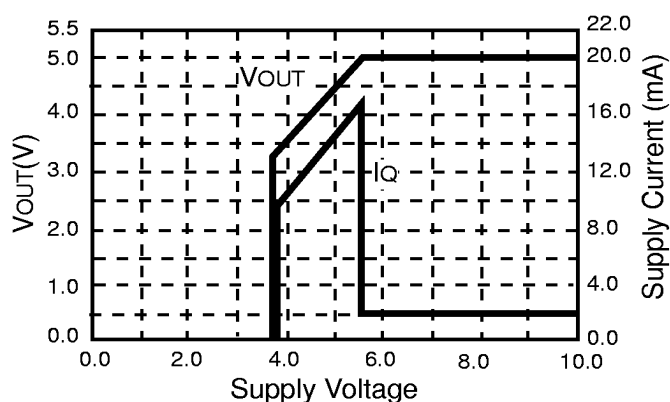


Typical Performance Characteristics: continued

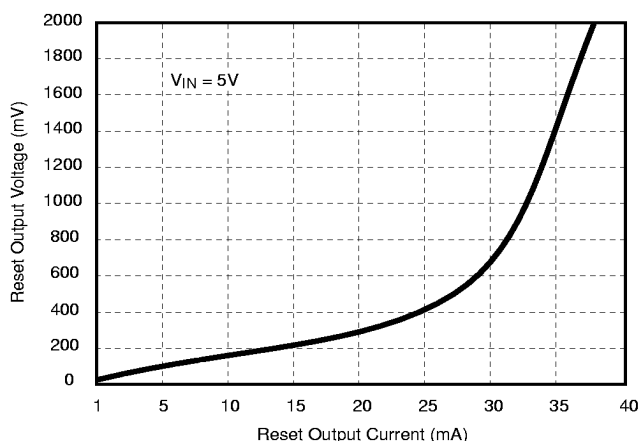
Quiescent Current vs. Output Current Over Temperature



Output Voltage and Supply Current vs. Input Voltage



RESET Output Voltage vs. Output Current



Circuit Description

Voltage Reference and Output Circuitry

Precision Voltage Reference

The regulated output voltage depends on the precision band gap voltage reference in the IC. By adding an error amplifier into the feedback loop, the output voltage is maintained within $\pm 4\%$ over temperature and supply variation.

Output Stage

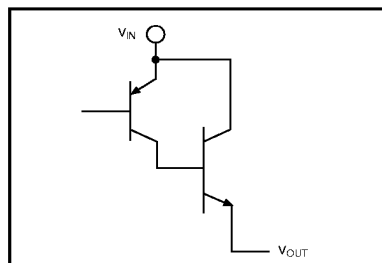


Figure 1. Composite Output Stage of the CS-8121

The composite PNP-NPN output structure (Figure 1) provides 1A (typ) of output current while maintaining a low drop out voltage (1.2V) and drawing little quiescent current (4mA).

The NPN pass device prevents deep saturation of the output stage which in turn improves the IC's efficiency by preventing excess current from being used and dissipated by the IC.

Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 2).

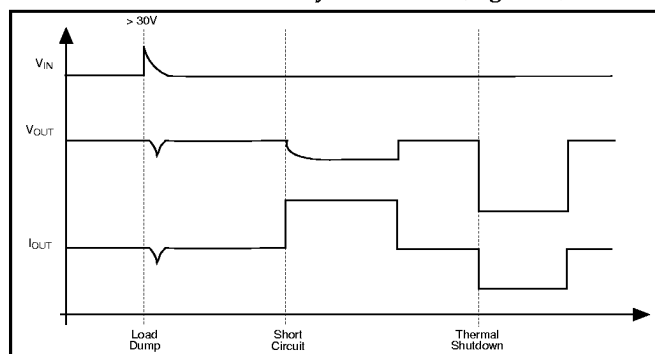


Figure 2. Typical Circuit Waveforms for Output Stage Protection.

If the input voltage rises above 30V (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.

Using an emitter sense scheme, the amount of current through the NPN pass transistor is monitored. Feedback circuitry insures that the output current never exceeds a preset limit.

Should the junction temperature of the power device exceed 180°C (typ) the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.

Regulator Control Functions

The CS-8121 contains two microprocessor compatible control functions: ENABLE and RESET (Figure 3).

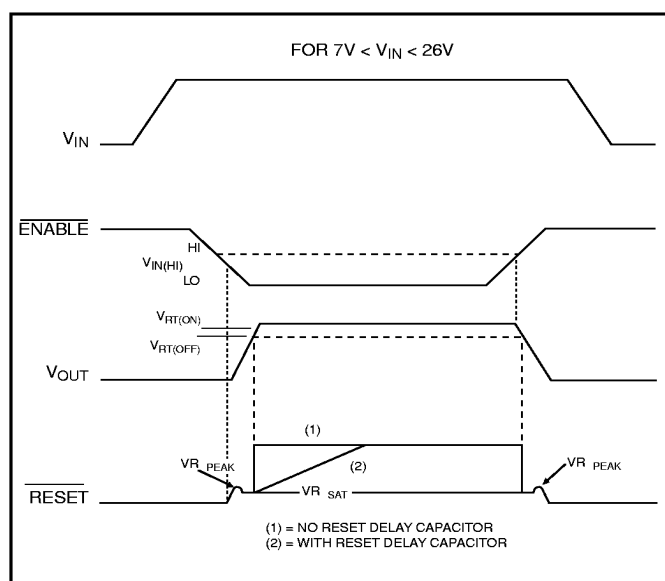


Figure 3. Circuit Waveforms for the CS-8121

ENABLE Function

The ENABLE function switches the output transistor. When the voltage on the ENABLE lead exceeds 2.9V typ, the output pass transistor turns off, leaving a high impedance facing the load. The IC will remain in Sleep mode, drawing only 250μA, until the voltage on the lead drops below 2.1V typ. Hysteresis (800mV) is built into the ENABLE function to provide good noise immunity.

RESET Function

A RESET signal (low voltage) is generated as the IC powers up ($V_{OUT} > V_{OUT} - 100\text{mV}$) or when V_{OUT} drops out of regulation ($V_{OUT} < V_{OUT} - 140\text{mV}$, typ). 40mV of hysteresis is included in the function to minimize oscillations.

The RESET output is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC, thereby guaranteeing that the RESET signal is valid for V_{OUT} as low as 1V.

An external RC network on the RESET lead (Figure 4) provides a sufficiently long delay for most microprocessor based applications. RC values can be chosen using the following formula:

$$R_{TOT} \times C_{RST} \left[\frac{-t_{Delay}}{\ln \left(\frac{V_T - V_{OUT}}{V_{RST} - V_{OUT}} \right)} \right]$$

where:

$R_{TOT} = R_{RST}$ in parallel with R_{IN} ,

$R_{IN} = \mu\text{P}$ port impedance,

$C_{RST} = \text{RESET delay capacitor,}$

$t_{Delay} = \text{desired delay time,}$

$V_{RST} = V_{SAT}$ of RESET lead (0.7V @ turn-on), and

$V_T = \mu\text{P}$ logic threshold voltage.

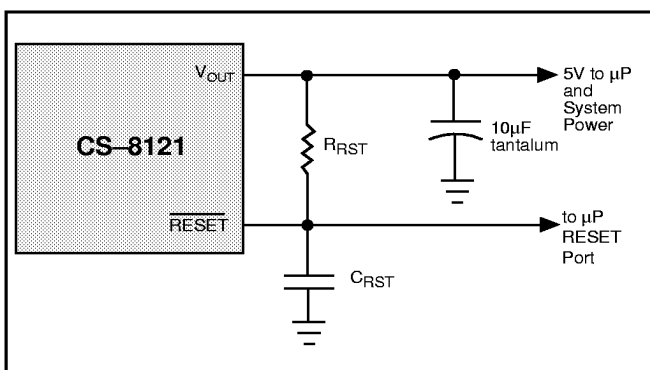


Figure 4. RC Network for RESET Delay

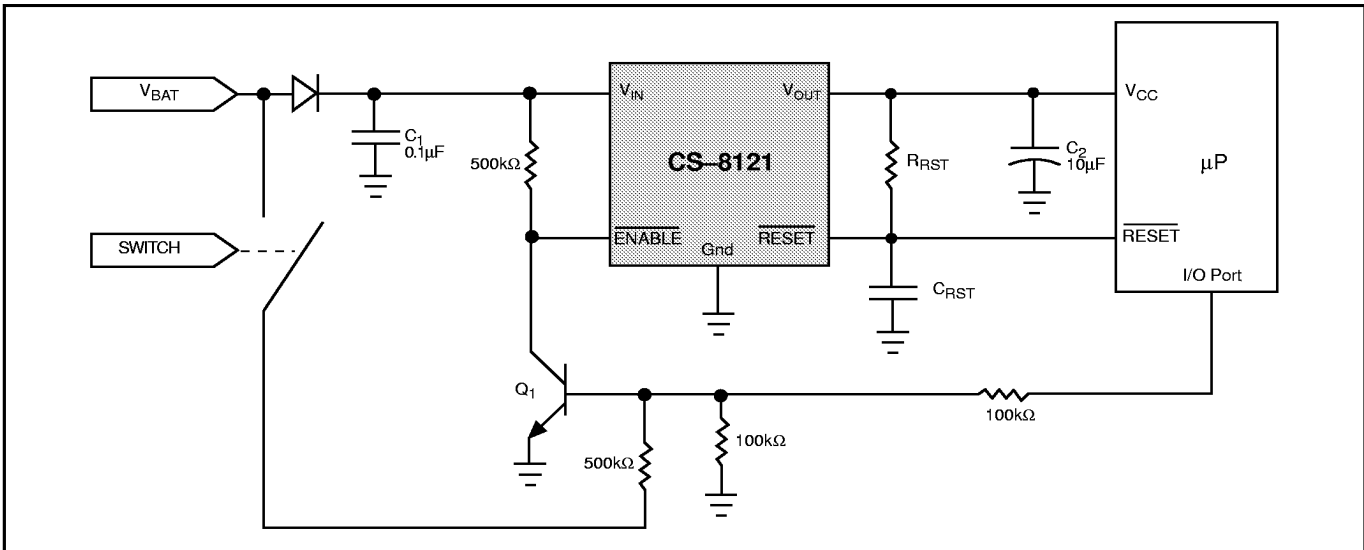


Figure 5. Microprocessor control of CS-8121 using external switching transistor Q1.

The circuit depicted in Figure 5 lets the microprocessor control its power source, the CS-8121 regulator. An I/O port on the μP and the SWITCH port are used to drive the base of Q1. When Q1 is driven into saturation, the voltage on the ENABLE lead falls below its lower threshold and the regulator's output is switched on. When the drive current is removed, the voltage on the ENABLE lead rises, the output is switched off and the IC moves into Sleep mode where it typically draws $250\mu A$.

By coupling these two controls with `ENABLE`, the system has added flexibility. Once the system is running, the state of the `SWITCH` is irrelevant as long as the I/O port continues to drive Q1. The μP can turn off its own power by withdrawing drive current, once the `SWITCH` is open. This software control at the I/O port allows the μP to finish key housekeeping functions before power is removed.

The logic options are summarized in Table 1 below

μ P I/O drive	SWITCH	ENABLE	Output
ON	Closed	LOW	ON
	Open	LOW	ON
OFF	Closed	LOW	ON
	Open	HIGH	OFF

The I/O port of the μP typically provides $50\ \mu\text{A}$ to Q1. In automotive applications the SWITCH is connected to the ignition switch.

Stability Considerations

The output or compensation capacitor C_2 helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least

expensive solution, but, if the circuit operates at low temperatures (-25°C to -40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor C_2 shown in the test and applications circuit should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for C_2 for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

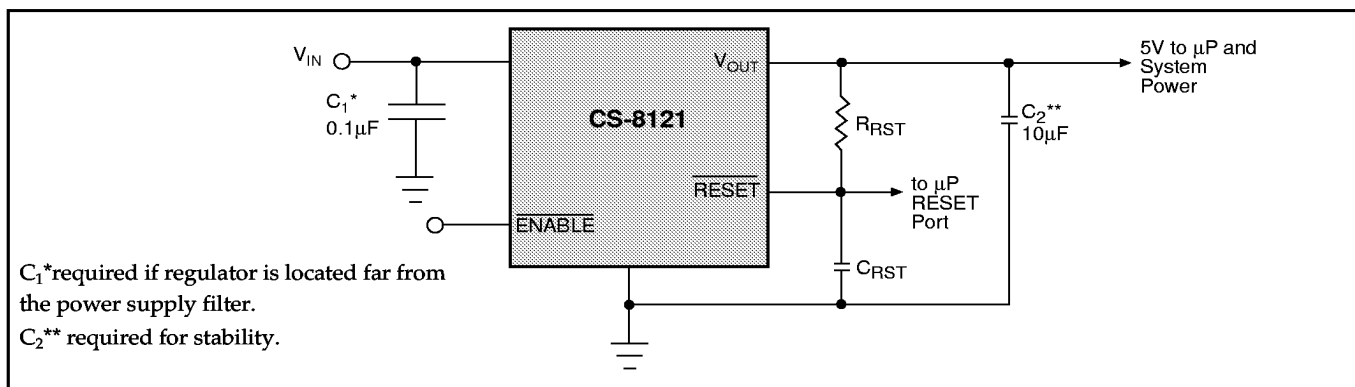


Figure 6: Test and application circuit showing output compensation.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Remove the unit from the environmental chamber and heat the IC with a heat gun. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of $\pm 20\%$ so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 7) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}]I_{OUT(max)} + V_{IN(max)}I_Q \quad (1)$$

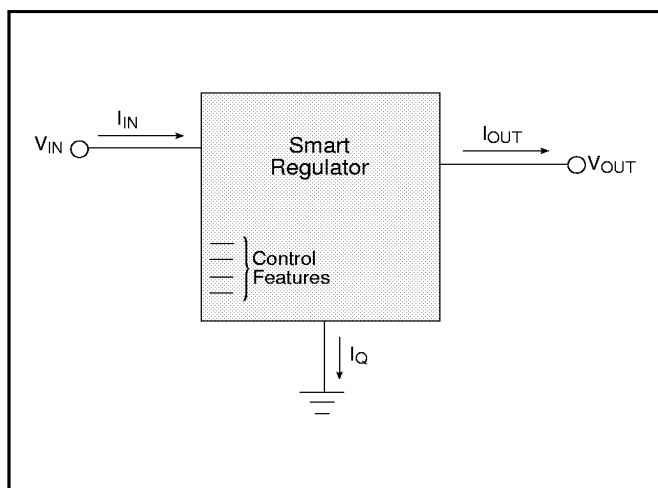


Figure 7: Single output regulator with key performance parameters labeled.

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^\circ\text{C} - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C .

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where:

$R_{\theta JC}$ = the junction-to-case thermal resistance,

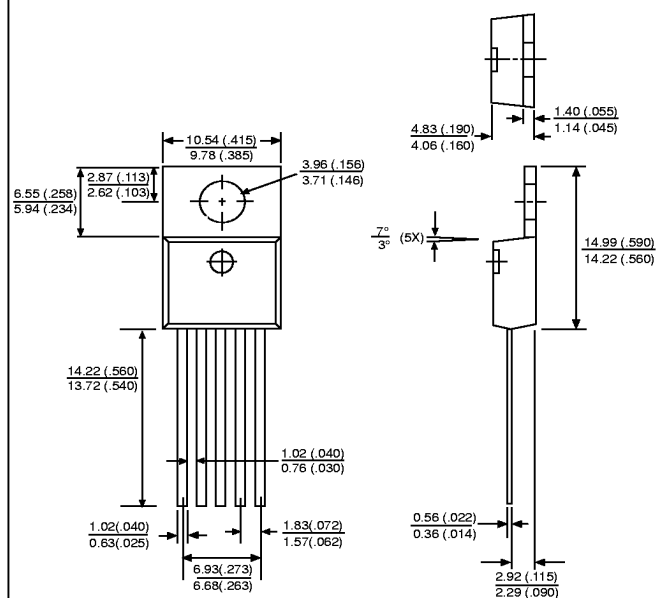
$R_{\theta CS}$ = the case-to-heatsink thermal resistance, and

$R_{\theta SA}$ = the heatsink-to-ambient thermal resistance.

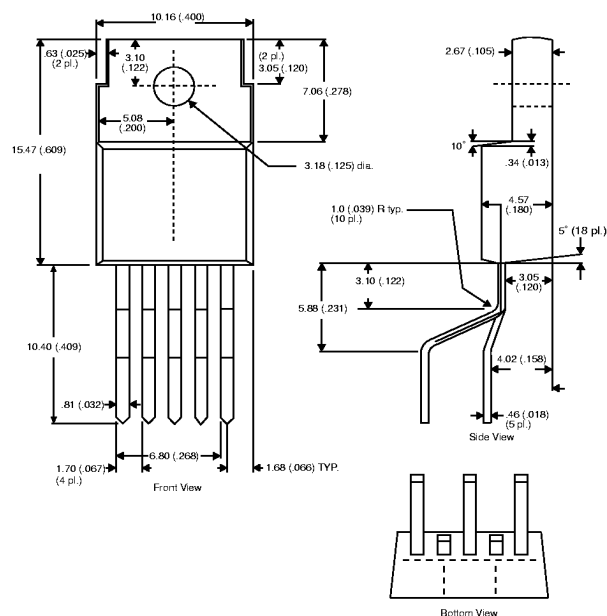
$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

PACKAGE DIMENSIONS IN mm (INCHES)

5 Lead TO-220 Straight



5 Lead TO-220 (Overmolded)



Ordering Information

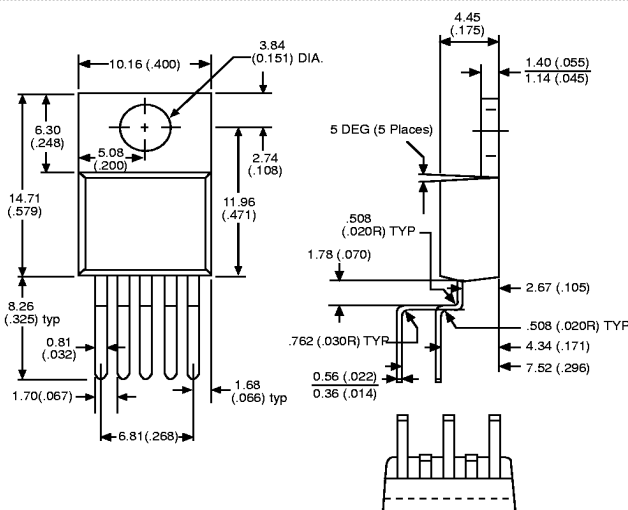
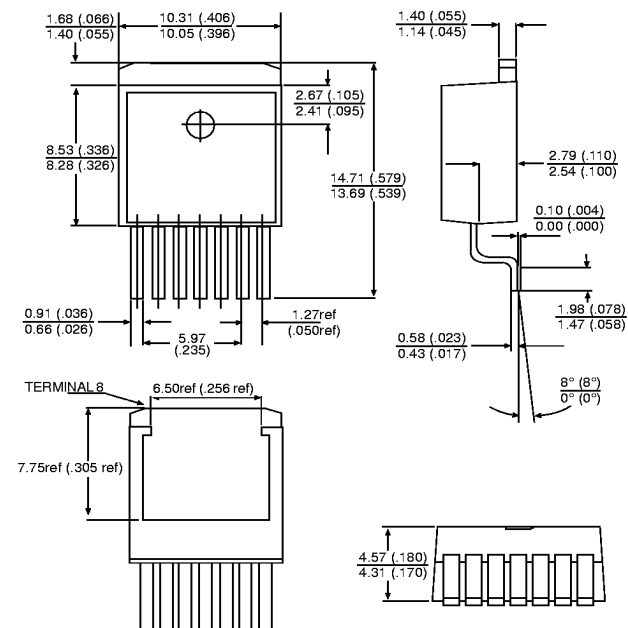
Part Number	Description
CS-8121T5	5 Lead TO-220 Straight
CS-8121TV5	5 Lead TO-220 Vertical
CS-8121TH5	5 Lead TO-220 Horizontal
CS-8121TF5	5 Lead TO-220 Overmolded
CS-8121DP7	7 Lead D ² PAK
CS-8121DPR7	7 Lead D ² PAK Tape & Reel

PACKAGE THERMAL DATA

Thermal Data	5 Lead	5 Lead	7 Lead	
	TO-220	TO-220	D ² PAK	
	(Overmold)			
R _{θJC} typ	4.0	2.5	2.5	°C/W
R _{θJA} typ	50	50	10-50*	°C/W

*Depending on thermal properties of substrate, R_{θJA} = R_{θJC} + R_{θCA}.

5 Lead TO-220 (Vertical)

7 Lead D²PAK

Cherry Semiconductor Corporation reserves the right to make changes to the specifications without notice. Please contact Cherry Semiconductor Corporation for the latest available information.