## PRODUCT DESCRIPTION

The HC3500R Gate Array (Figure 1) is a 2 nanosecond, 3854 equivalent gate density Very Large Scale Integration (VSLI) monolithic integrated circuit built using Honeywell's RICMOS (Radiation Hardened Inverse CMOS) fabrication process. The array is composed of uncommitted basic and I/O cells. The basic cell consists of 4 uncommitted n-channel and 4 uncommitted p-channel transistors. Both types of cells are heavily guard-banded and use an epitaxial layer of silicon to preclude latchup. 100% of the gates may be utilized by either autoplace or autoroute, thus giving the maximum benefits of both VLSI and proprietary design.

Designing with the HC3500R is easy and fast requiring only conventional logic design, logic simulation, and test pattern generation. The computer-aided-design and autorouting methodologies are similar to those used for printed circuit boards.

The ultra high packing density of the HC3500R results in a 200-to-1 reduction in system component count when compared with similar systems built using conventional SSI/MSI LSTTL logic functions. The user obtains a degree of optimization like that of a full custom design and the quick turnaround time of a semicustom part.

Logic functions are predefined by Honeywell and are implemented by automatically interconnecting the macrocells using two layers of metal routing. Both cell intraconnection and routing of power buses are invisible to the user. For external interface, up to 112 LSTTL compatible I/O buffers can be specified using 18 different hard macros for the I/O cells.

The design software for the HC3500R will be available on both the Daisy and Mentor graphics CAE work stations. Daisy software is currently available and release of Mentor Graphics software is scheduled for the first quarter 1986.

## FEATURES

- **Customer programmable VLSI**
- **3854 equivalent 2-input NAND gates**
- **Hardened to strategic radiation levels**
- **Single Event Upset immune**
- **Immune to Latchup**
- **Military temperature range**
  - **−55°C to 125°C**
- **Military Class S Reliability**
- **Power dissipation: 0.5 watts typical**
- **120 pin leaded-chip-carriers**

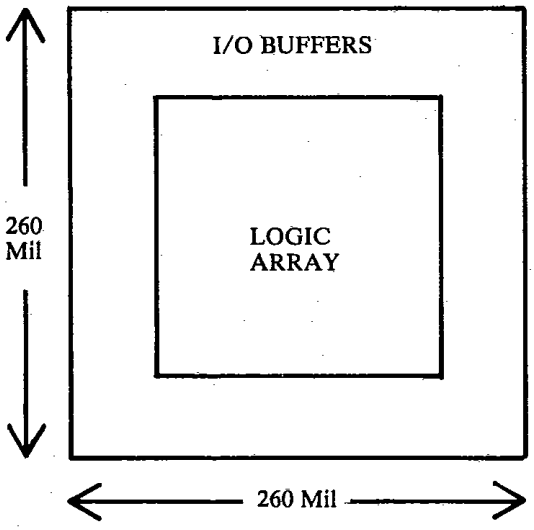



*Figure 1. Block Diagram*

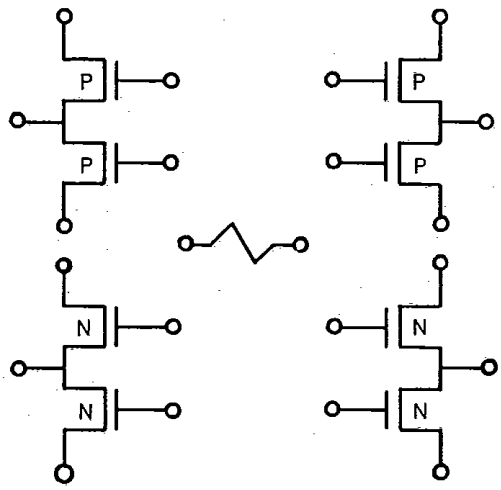



*Figure 2. RICMOS Basic Cell*

## COMPUTER-AIDED-DESIGN SYSTEM

Honeywell's Software Toolkit™ for VLSI gate array design is built around industry standard software programs. Most importantly, a standardized design language, Mentor SIM™, is available for logic simulation. This language is used hierarchically to define complex logic functions in a computer readable data base. The data is then accessed by other software programs for simulation, analysis, autorouting, and array fabrication.

In addition to Mentor SIM, the Software Toolkit contains programs for schematic entry, netlist generation, timing verification, design statistic analysis, loading/fanout analysis, media delay feedback/analysis, and test program compilation. Industry standard programs are also available for automatic placement, automatic routing, and interactive graphics editing.

Honeywell supports the Software Toolkit for customers with a variety of in-house design automation capabilities. A set of tools hosted on popular workstations provides complete schematic-through-PG tape capability in the hands of the system designer. Customers can use the Software Toolkit at Honeywell's Colorado Springs Design Center or in their own facility.

### FOR CUSTOMERS WITH MENTOR GRAPHICS ENGINEERING WORKSTATIONS

Mentor Graphics provides the following IDEA 1000™ programs as part of the Software Toolkit:

SYMED™ Mentor symbol generation package used with Honeywell-developed macrocell symbols. User may create new macrocell symbols using the macrocell library provided.

NETED™ Mentor schematic entry package used with Honeywell developed macrocells. User calls symbols from a library and interconnects them to implement his design.

SIM™ Mentor logic simulation package used with Honeywell developed macrocells. User provides input patterns to functionally debug the design.

EXPAND™ Mentor design expansion package used with Honeywell developed macrocells. Used for removing design hierarchy (nesting of macrocells) from design file prior to autoplacement.

Honeywell provides the following programs as part of the Software Toolkit:

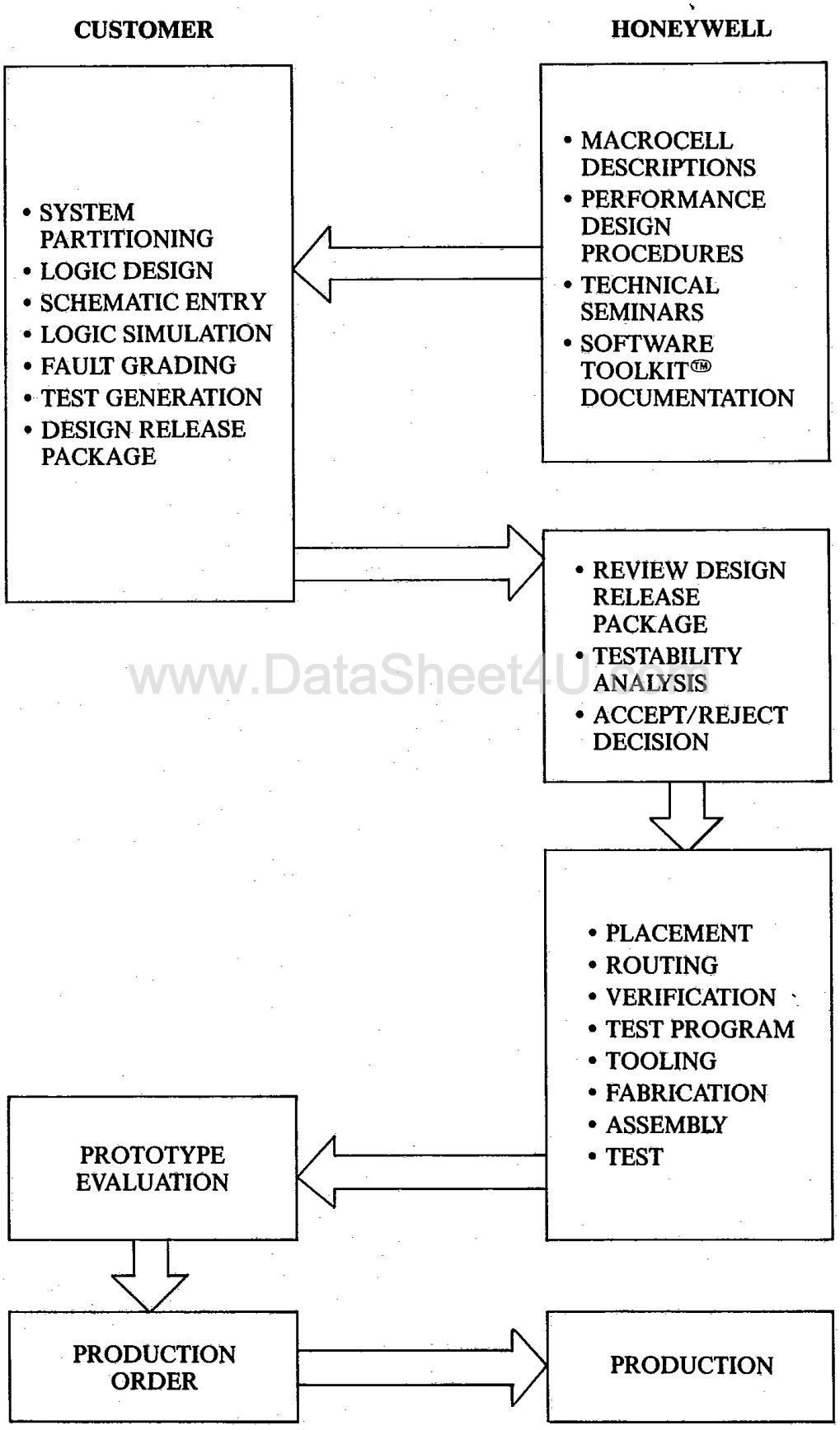
LOADS™ Honeywell developed logic rules check and load modeling program. Informs the user of illegal loading or electrical violations. Also modifies macrocell propagation delays based on junction temperature, fanout, and power supply voltage.

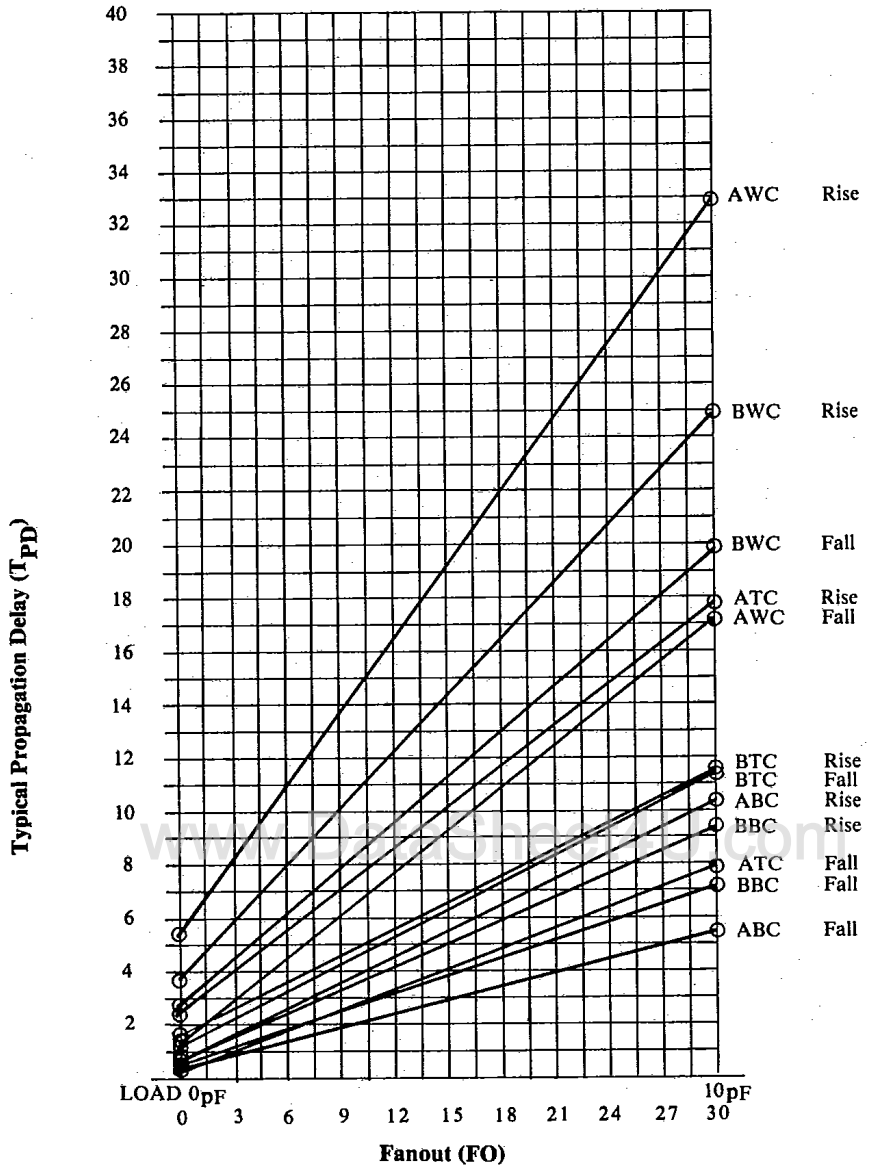
STATS™ Honeywell developed design statistics report. Lists chip power, cell count and utilization. Informs user if either cell count or I/O count exceed maximums for the specific gate array.

WIRES™ Honeywell developed wire delay calculation program. Lists all nets by line length and delay with error reporting for nets exceeding specified limits. Recomputes user design files with user specified temperature and actual wire delays.

Ask your local Honeywell sales representative for further information on the Software Toolkit.

# GATE ARRAY DEVELOPMENT FLOW






| | $V_{CC}$ V | TEMPERATURE °C | TOTAL DOSE RADS (Si) |
|---|---|---|---|
| Before Exposure, Worst Case (BWC) | +4.5 | +125 | 0 |
| After Exposure, Worst Case (AWC) | 4.5 | 125 | $10^6$ |
| Before Exposure, Typical Case (BTC) | 5.0 | 25 | 0 |
| After Exposure, Typical Case (ATC) | 5.0 | 25 | $10^6$ |
| Before Exposure, Best Case (BBC) | 5.5 | −55 | 0 |
| After Exposure, Best Case (ABC) | 5.5 | −55 | $10^6$ |

*Figure 3. Delay Times for a 2-Input NAND Gate*

## INPUT/OUTPUT CELLS

All signals within the array interface to external pads through I/O buffers located around the device perimeter.

A description plus the logic for each I/O cell are shown in Figure 4.

| INPUT/OUTPUT BUFFERS | |
|---|---|
| **DESCRIPTION:** | Tristateable Input/Output Buffer<br>TTL Input Levels |
| **DESCRIPTION:** | Tristateable Input/Output Buffer<br>CMOS Input Levels |

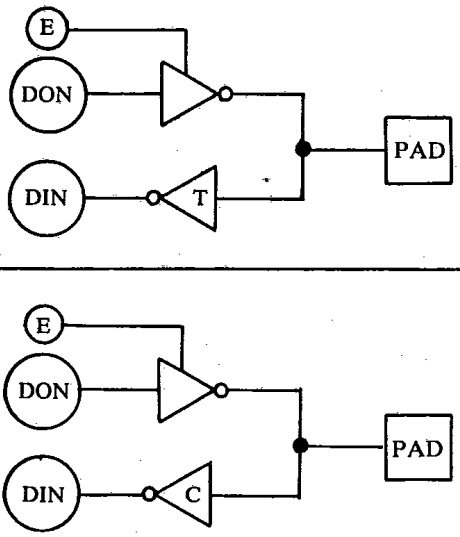



*Figure 4. I/O Cells*

**INPUT/OUTPUT BUFFERS AVAILABLE WITH:** Pullup/Pulldown Outputs
Emitter Follower Outputs
Open Collector Outputs

Input Pullup Resistors
Input Pulldown Resistors

CMOS Input Levels
TTL Input Levels

## POWER DISSIPATION

The typical power dissipation for any given implementation of the HC3500R Gate Array is given by the following equation:

Typical Power (mW) = 25m W/MHz X Average Circuit Operating Frequency.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | DESCRIPTION | MILITARY | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | NOM | MAX | |
| $V_{CC1}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $T_A$ or $T_c$ | Operating free-air temperature | −55 | | 125 | °C |
| $F_T$ | Internal flip flop toggle frequency | 30 | | | MHz |

(1) Package selection will determine the maximum input frequency. Consult Honeywell.

## ABSOLUTE MAXIMUM RATINGS (2)

| PARAMETER | DESCRIPTION | RATING | UNITS |
|---|---|---|---|
| $V_{CC1}$ | Supply voltage | +7.0 | V |
| $E_{IN}$ | Input voltage continuous | −0.5 to ($V_{CC}$ +0.5) | V |
| $I_{IN}$ | Input current continuous | −10 to +10 | mA |

| PARAMETER | DESCRIPTION | RATING | UNITS |
|---|---|---|---|
| $V_O$ | Voltage applied to three-state output in off-state | −0.5 to ($V_{CC}$ +0.5) | V |
| $T_J$ | Junction temperature | +175 | °C |



(2) Comment: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC AND AC ELECTRICAL CHARACTERISTICS—** Over full ranges of recommended operating conditions.

| PARAMETER | | | TEST CONDITIONS | MILITARY LIMITS MIN | MILITARY LIMITS TYP | MILITARY LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **CMOS GATE (Internal)** | | | | | | | |
| $t_{pdAV}$ | Average gate propagation delay | | 2 input NAND Fanout = 3 | 0.8 | 2.4 | 8.2[1] | ns |
| **INPUT BUFFERS:** | | | | | | | |
| $V_{IH}$ | Input high voltage | CMOS / TTL | | $V_{CC}-1$ / 2.0 | $V_{CC}$ | $V_{CC}$ | V |
| $V_{IL}$ | Input low voltage | CMOS / TTL | | | 0 | 1.0 / 0.8 | V |
| $I_{IN}$ | Input current | | $0 \leq V_{IN} \leq V_{CC}$ | −10 | | +10 | µA |
| FO | Fanout | CMOS / TTL | | 1 | | 11 / 22 | Unit load |
| $t_{pdLH}$ | Propagation delay, low-to-high FO = 0 | CMOS / TTL | (see figure 5a) | | | 3 / 3 | ns |
| $t_{pdHL}$ | Propagation delay, high-to-low FO = 0 | CMOS / TTL | (see figure 5a) | | | 3 / 3 | ns |
| **OUTPUT BUFFERS:** | | | | | | | |
| $V_{OL}$ | Output low voltage | | $I_{OL}$ = 8 mA | 0 | | 400 | mV |
| $V_{OH}$ | Output high voltage | | $I_{OH}$ = 8 mA | 4 | | $V_{CC}$ | V |
| $t_{tdLH}$ | Propagation delay, low-to high output | | (see figure 5b) | | | 10 | ns |
| $t_{pdHL}$ | Propagation delay, high-to-low output | | (see figure 5b) | | | 10 | ns |
| **THREE-STATE BUFFER:** | | | | | | | |
| $t_{OELQZ}$ | | | | | | 6 | ns |
| $t_{OEHQV}$ | | | | | | 5 | ns |

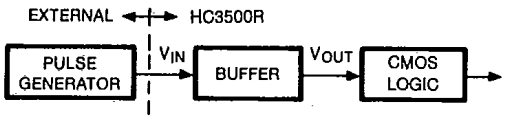
(1) After exposure to $10^6$ Rads (Si).

**RADIATION HARDNESS CHARACTERISTICS** — Over full ranges of recommended operating conditions.

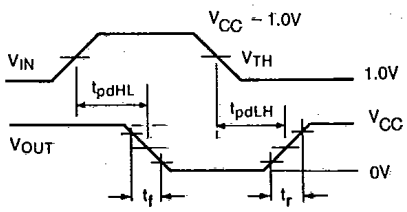
| PARAMETER | TEST CONDITIONS | MILITARY LIMITS | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **RADIATION HARDNESS** | | | | | |
| Total Dose | Nominal | $10^6$ | | | Rads (Si) |
| Dose Rate | | $10^9$ | | | Rads (Si)/sec |
| Dose Rate Survivability | 20 ns ionizing pluse | $10^{12}$ | | | Rads (Si)/sec |
| Single Event Upset | Adam's 10% worst case environment | | | $10^{-10}$ | E/Bit/Day |
| Neutron Fluence | | $3x10^{14}$ | | | $n/cm^2$ |
| Latchup[1] | | | — None — | | |

(1) Latchup has not been observed under any strategic radiation levels.

**TEST SETUP**

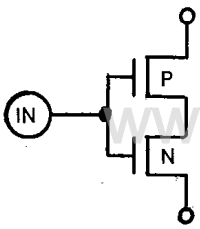



**CMOS INPUTS WAVE FORMS**

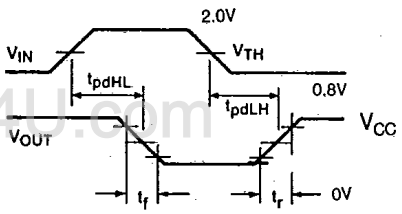



**A. INPUT BUFFER**

**EQUIVALENT CIRCUIT OF CMOS UNIT LOAD**

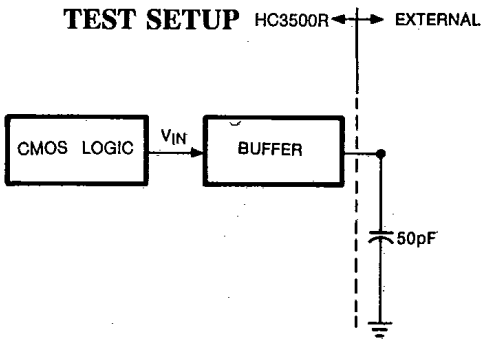



**TTL INPUTS WAVE FORMS**

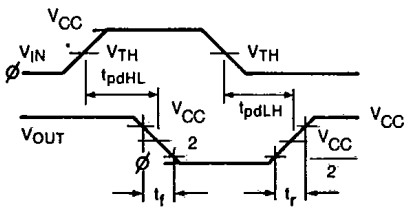



**A. INPUT BUFFER (cont.)**

**TEST SETUP**



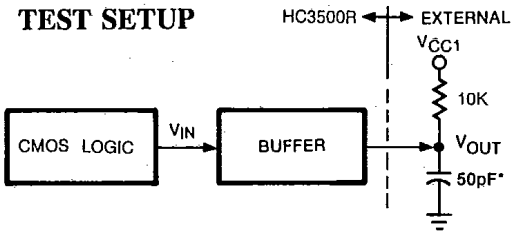

**WAVEFORMS**



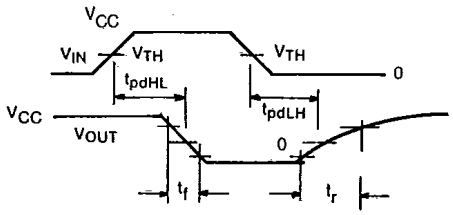

**B. ACTIVE PULLUP OUTPUT**

*Figure 5. Test Configurations*

**TEST SETUP**

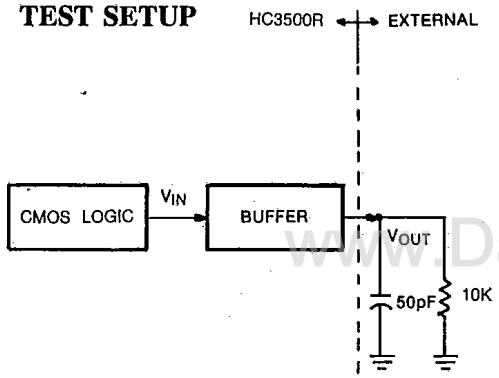



**WAVEFORMS**

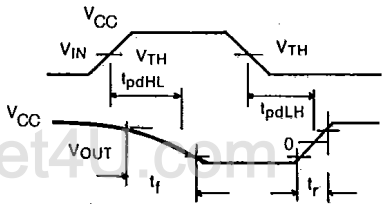



**C. OPEN COLLECTOR OUTPUT**

**TEST SETUP**



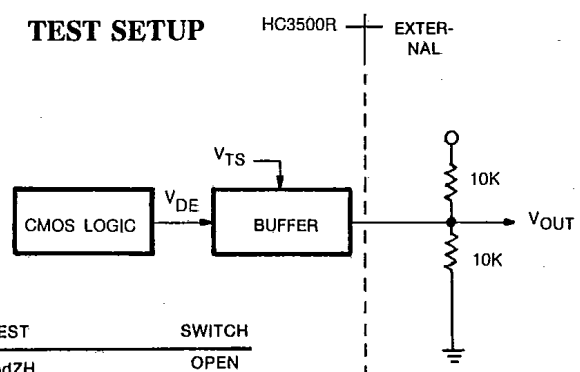

**WAVEFORMS**





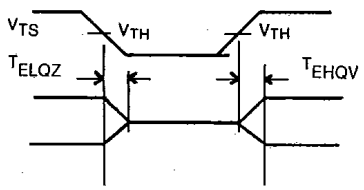

**D. EMITTER FOLLOWER OUTPUT**

**TEST SETUP**



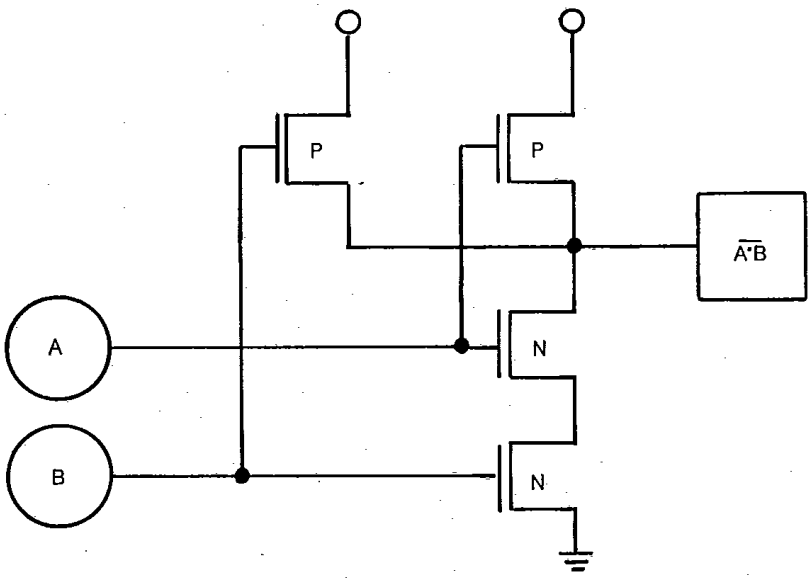

| TEST | SWITCH |
|---|---|
| $t_{pdZH}$ | OPEN |
| $t_{pdZL}$ | CLOSED |
| $t_{pdHZ}$ | OPEN |
| $t_{pdLZ}$ | CLOSED |
| $t_{pdLH}$ | OPEN |
| $t_{pdHL}$ | OPEN |

**WAVEFORMS**



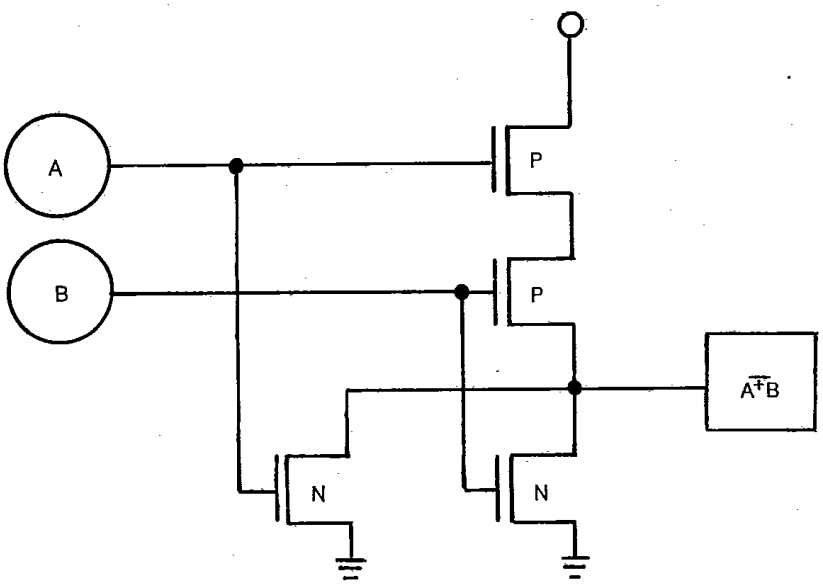

**E. THREE-STATE OUTPUT**

*Figure 5 Test Configurations (cont.)*




(A) BASIC CMOS NAND LOGIC GATE






(B) BASIC CMOS OR/NOR LOGIC GATE

*Figure 6. Basic Gates*

Honeywell