

# NDF10N62Z, NDP10N62Z

## N-Channel Power MOSFET 620 V, 0.65 Ω

### Features

- Low ON Resistance
- Low Gate Charge
- Zener Diode-protected Gate
- 100% Avalanche Tested
- These Devices are Pb-Free and RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	NDF10N62Z	NDP10N62Z	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	620 (Note 1)		V
Continuous Drain Current, R <sub>θJC</sub>	I <sub>D</sub>	10 (Note 2)		A
Continuous Drain Current, R <sub>θJC</sub> , T <sub>A</sub> = 100°C	I <sub>D</sub>	5.7 (Note 2)		A
Pulsed Drain Current, V <sub>GS</sub> @ 10 V	I <sub>DM</sub>	36 (Note 2)		A
Power Dissipation, R <sub>θJC</sub> (Note 1)	P <sub>D</sub>	36	125	W
Gate-to-Source Voltage	V <sub>GS</sub>	±30		V
Single Pulse Avalanche Energy, I <sub>D</sub> = 10 A	E <sub>AS</sub>	300		mJ
ESD (HBM) (JESD22-A114)	V <sub>esd</sub>	3900		V
RMS Isolation Voltage (t = 0.3 sec., R.H. ≤ 30%, T <sub>A</sub> = 25°C) (Figure 14)	V <sub>ISO</sub>	4500		V
Peak Diode Recovery	dv/dt	4.5 (Note 3)		V/ns
Continuous Source Current (Body Diode)	I <sub>S</sub>	10		A
Maximum Temperature for Soldering Leads	T <sub>L</sub>	260		°C
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

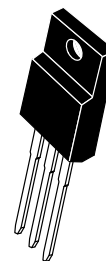
1. Surface mounted on FR4 board using 1" sq. pad size, (Cu area = 1.127 in sq [2 oz] including traces)
2. Limited by maximum junction temperature
3. I<sub>S</sub> ≤ 10 A, di/dt ≤ 200 A/μs, V<sub>DD</sub> = 80% BV<sub>DSS</sub>



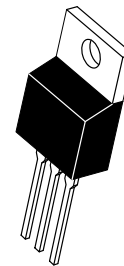
ON Semiconductor®

<http://onsemi.com>

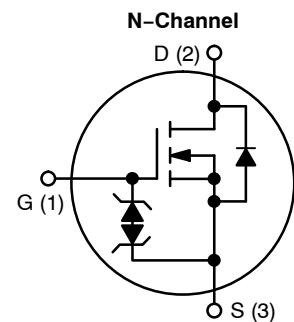
V <sub>DSS</sub>	R <sub>DS(ON)</sub> (TYP) @ 5 A
620 V	0.65 Ω



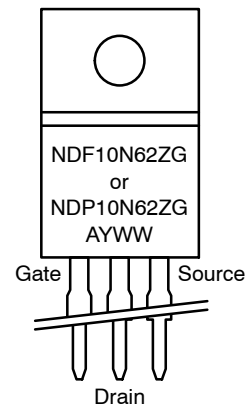
TO-220FP  
CASE 221D  
STYLE 1



TO-220AB  
CASE 221A  
STYLE 5



### MARKING DIAGRAM



- A = Location Code
- Y = Year
- WW = Work Week
- G = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping
NDF10N62ZG	TO-220FP	50 Units/Rail
NDP10N62ZG	TO-220AB	In Development

# NDF10N62Z, NDP10N62Z

## THERMAL RESISTANCE

Parameter	Symbol	NDF10N62Z	NDP10N62Z	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	3.4	1.0	°C/W
Junction-to-Ambient Steady State (Note 4)	$R_{\theta JA}$	50	50	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
----------------	-----------------	--------	-----	-----	-----	------

### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	$BV_{DSS}$	620			V
Breakdown Voltage Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D = 1\text{ mA}$	$\Delta BV_{DSS}/\Delta T_J$		0.6		V/°C
Drain-to-Source Leakage Current	$V_{DS} = 620\text{ V}, V_{GS} = 0\text{ V}$	$I_{DSS}$	25°C		1	μA
			125°C		50	
Gate-to-Source Forward Leakage	$V_{GS} = \pm 20\text{ V}$	$I_{GSS}$			±10	μA

### ON CHARACTERISTICS (Note 5)

Static Drain-to-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 5.0\text{ A}$	$R_{DS(on)}$		0.65	0.75	Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$	$V_{GS(th)}$	3.0		4.5	V
Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$	$g_{FS}$		7.9		S

### DYNAMIC CHARACTERISTICS

Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	$C_{iss}$		1425		pF
Output Capacitance		$C_{oss}$		150		
Reverse Transfer Capacitance		$C_{rss}$		35		
Total Gate Charge	$V_{DD} = 310\text{ V}, I_D = 10\text{ A},$ $V_{GS} = 10\text{ V}$	$Q_g$		47		nC
Gate-to-Source Charge		$Q_{gs}$		9.3		
Gate-to-Drain ("Miller") Charge		$Q_{gd}$		25		
Plateau Voltage		$V_{gp}$		6.4		V
Gate Resistance		$R_g$		1.5		Ω

### RESISTIVE SWITCHING CHARACTERISTICS

Turn-On Delay Time	$V_{DD} = 310\text{ V}, I_D = 10\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 5\text{ }\Omega$	$t_{d(on)}$		15		ns
Rise Time		$t_r$		31		
Turn-Off Delay Time		$t_{d(off)}$		40		
Fall Time		$t_f$		21		

### SOURCE-DRAIN DIODE CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Diode Forward Voltage	$I_S = 10\text{ A}, V_{GS} = 0\text{ V}$	$V_{SD}$			1.6	V
Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 30\text{ V}$ $I_S = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	$t_{rr}$		395		ns
Reverse Recovery Charge		$Q_{rr}$		3.0		μC

4. Insertion mounted

5. Pulse Width  $\leq 380\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

# NDF10N62Z, NDP10N62Z

## TYPICAL CHARACTERISTICS

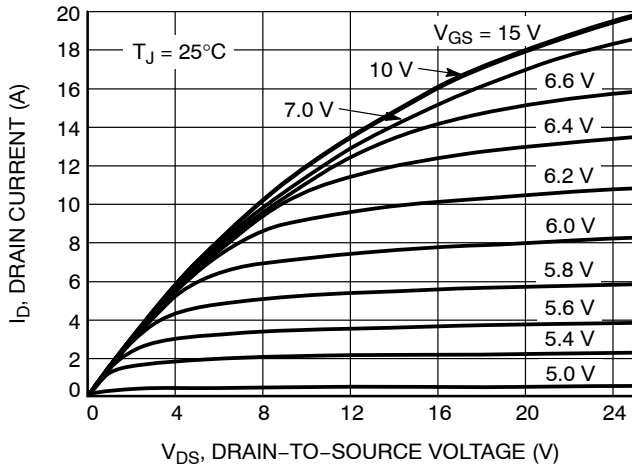


Figure 1. On-Region Characteristics

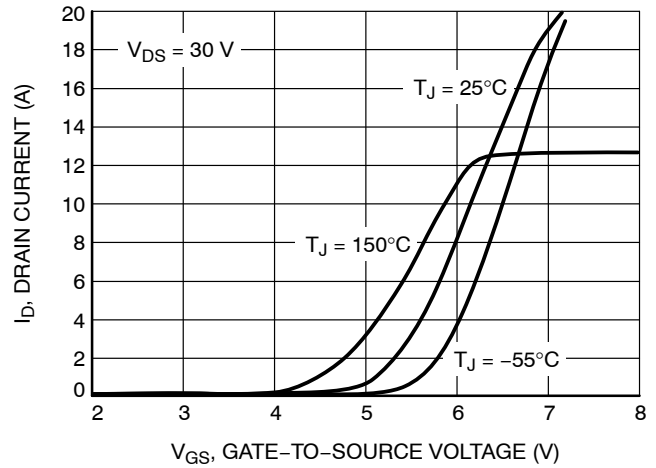


Figure 2. Transfer Characteristics

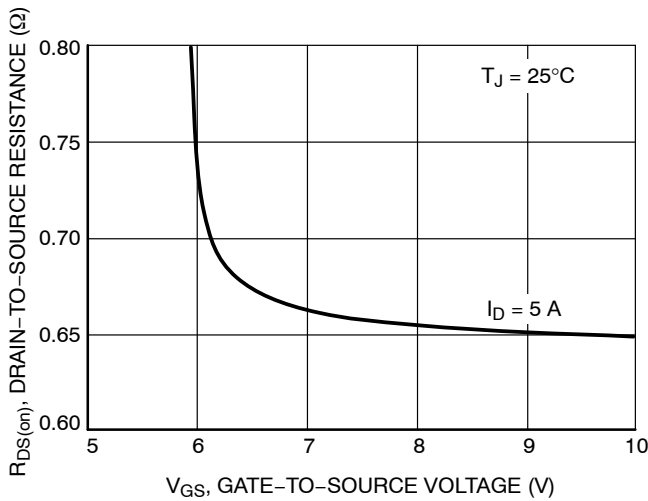


Figure 3. On-Resistance vs. Gate Voltage

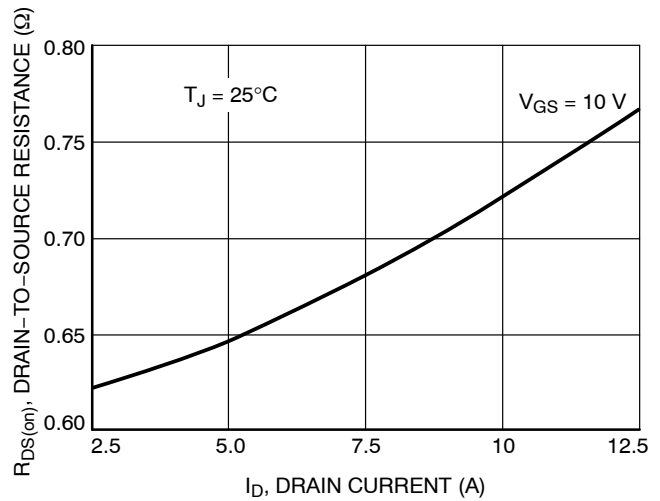


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

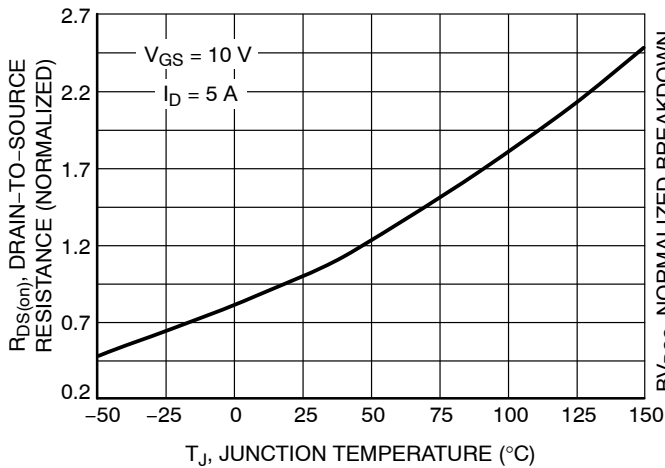


Figure 5. On-Resistance Variation with Temperature

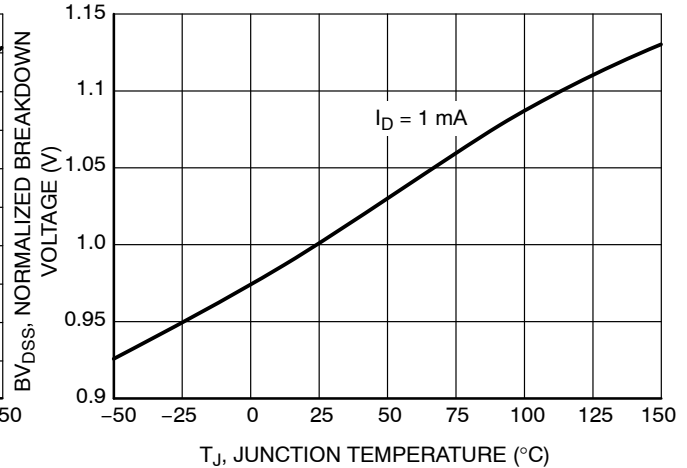
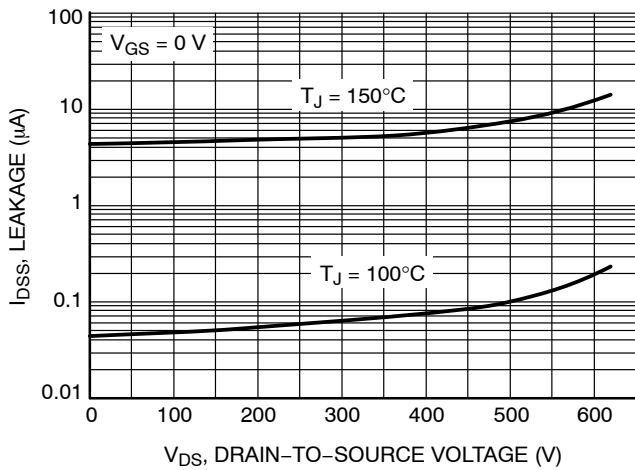


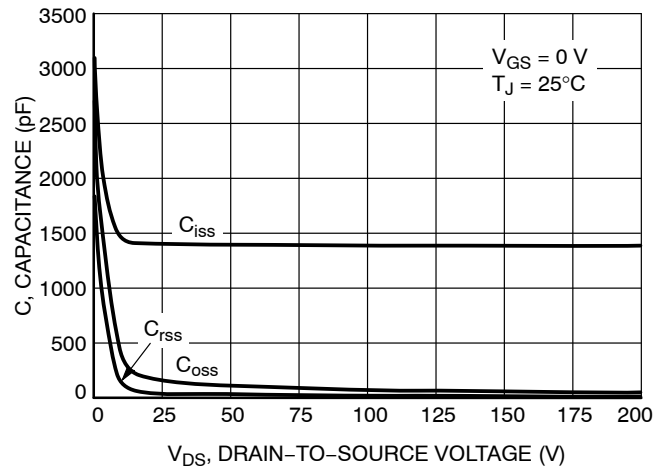
Figure 6.  $BV_{DSS}$  Variation with Temperature

# NDF10N62Z, NDP10N62Z

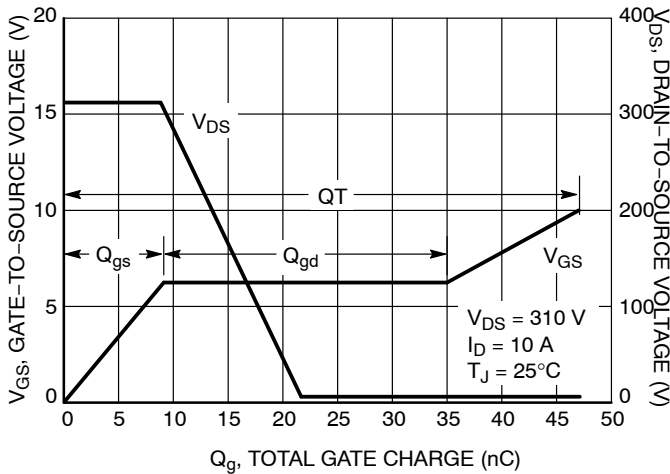
## TYPICAL CHARACTERISTICS



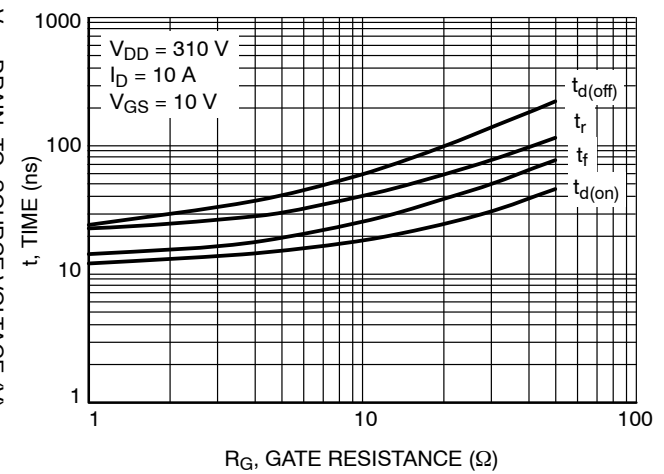
**Figure 7. Drain-to-Source Leakage Current vs. Voltage**



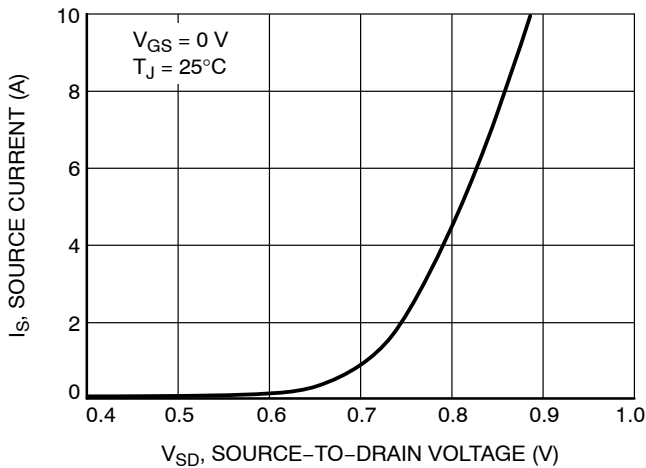
**Figure 8. Capacitance Variation**



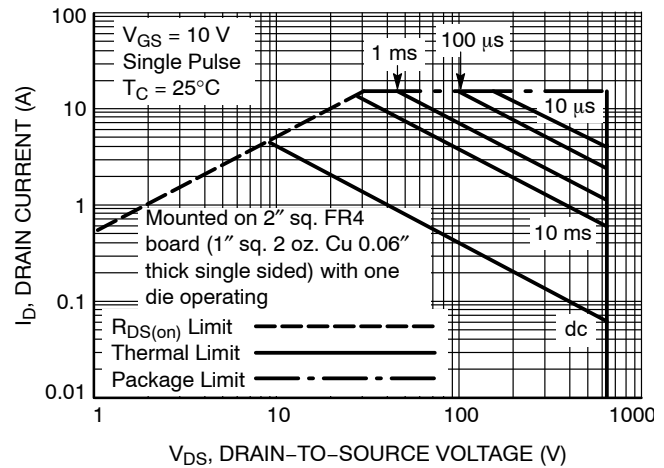
**Figure 9. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



**Figure 10. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 11. Diode Source Current vs. Forward Voltage**



**Figure 12. Maximum Rated Forward Biased Safe Operating Area for NDF10N62Z**

# NDF10N62Z, NDP10N62Z

## TYPICAL CHARACTERISTICS

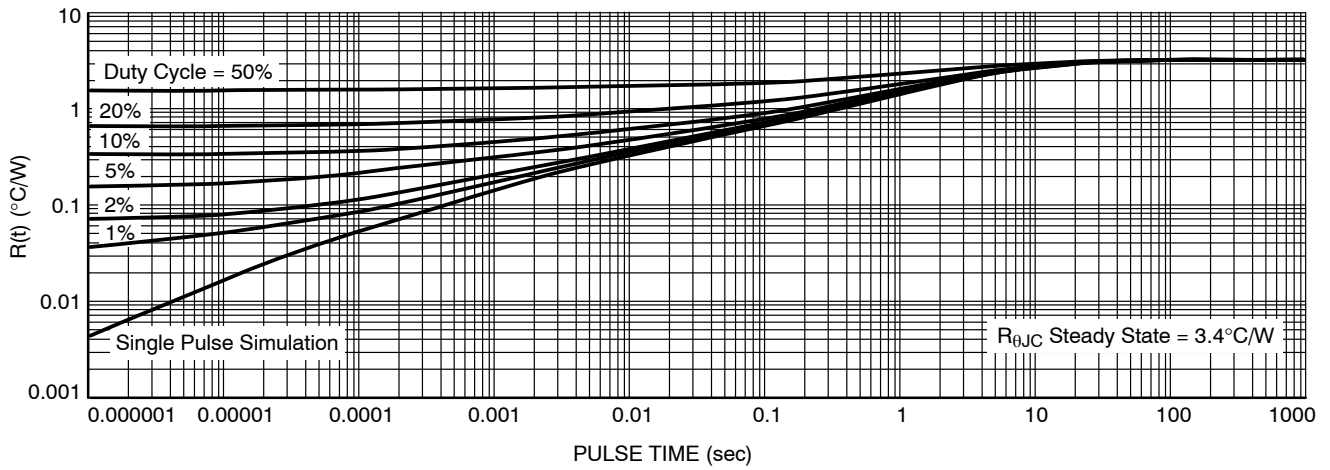


Figure 13. Thermal Impedance for NDF10N62Z

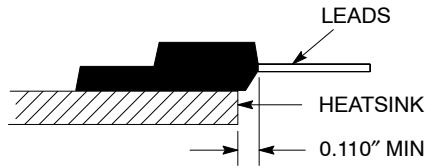


Figure 14. Isolation Test Diagram

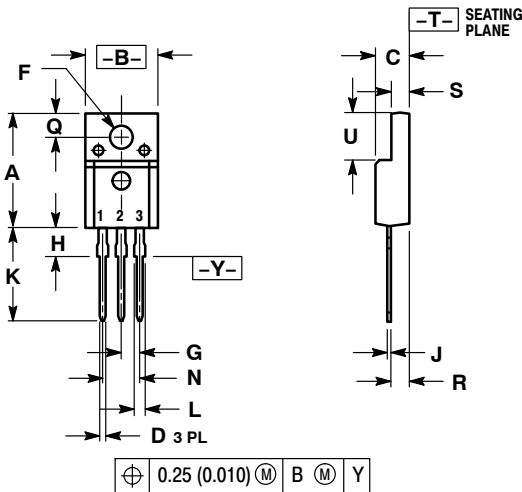
Measurement made between leads and heatsink with all leads shorted together.

\*For additional mounting information, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NDF10N62Z, NDP10N62Z

## PACKAGE DIMENSIONS

### TO-220FP CASE 221D-03 ISSUE K

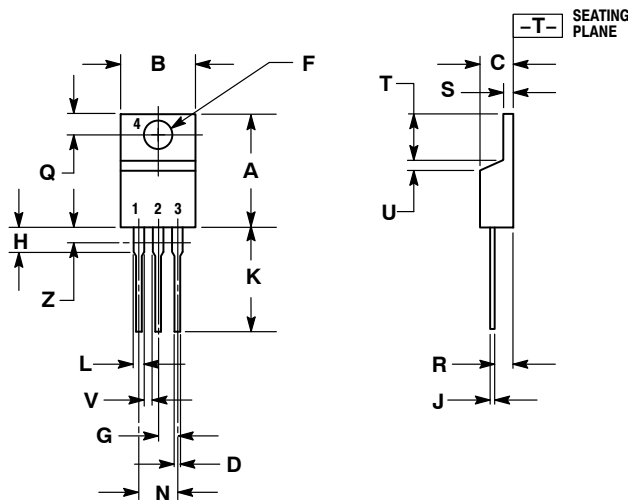


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH
  3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

- STYLE 1:
- PIN 1. GATE
  2. DRAIN
  3. SOURCE

### TO-220AB CASE 221A-09 ISSUE AE



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

- STYLE 5:
- PIN 1. GATE
  2. DRAIN
  3. SOURCE
  4. DRAIN

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative